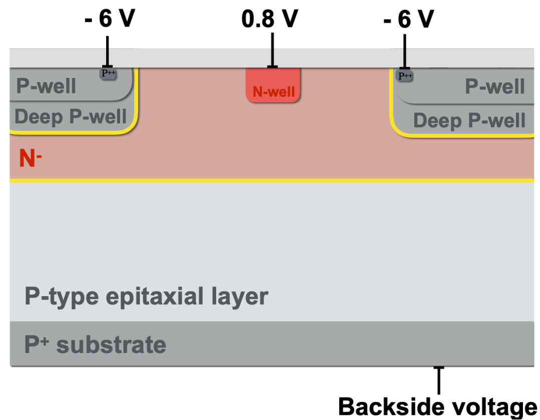
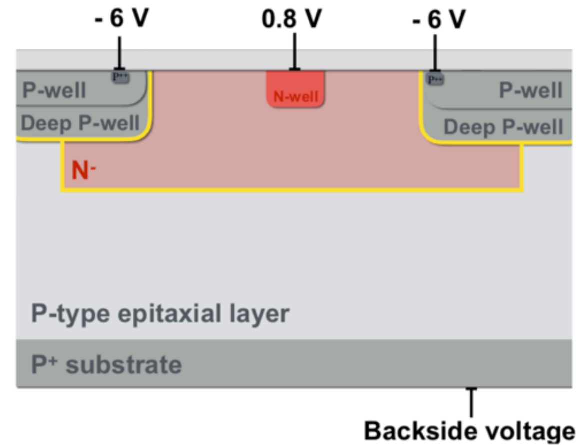
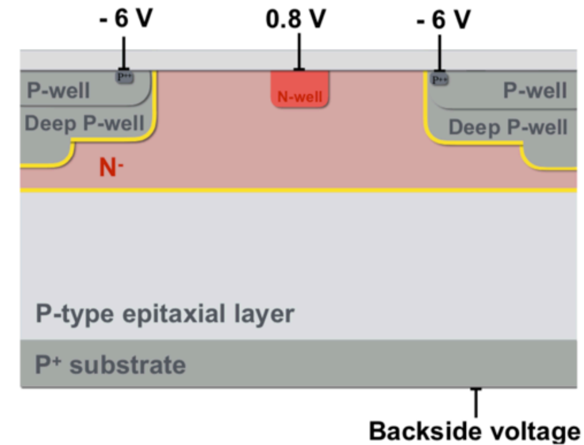
Studies for CLICTD resubmission with HR Czochralski substrate

M. Munker, 27.03.2020

Investigated technology & new pixel designs

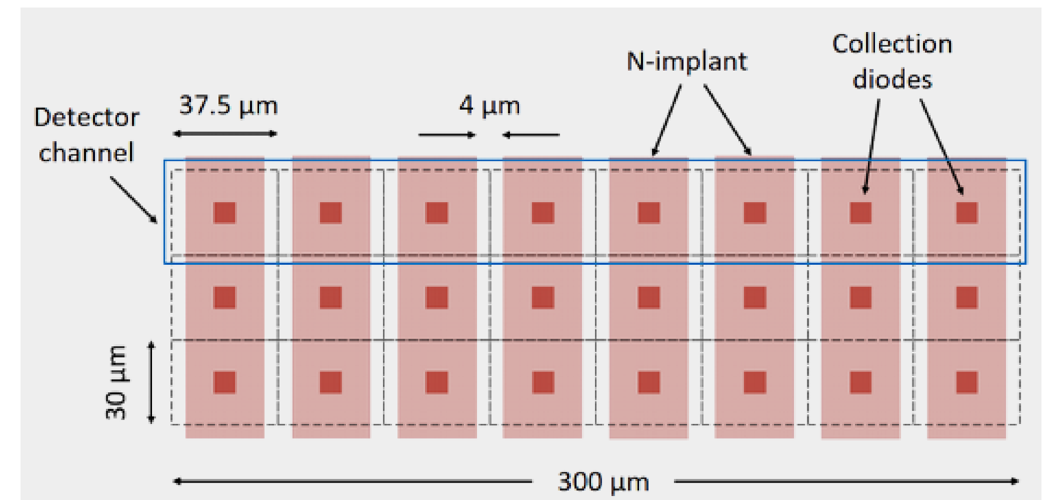






<u>CLICTD - a fully integrated small collection electrode CMOS chip for the CLIC tracker:</u>

- 180nm modified CMOS imaging process
- 30µm x 37.5µm pixel size
- Implemented on epitaxial layer of 30µm
- 8 pixels combined in common digital channel



Why to use new pixel designs for CLICTD?

Faster charge collection:

→ Impact on CLICTD measured performance limited by 10ns ToA bins

Less charge sharing:

→ Less in-channel charge sharing

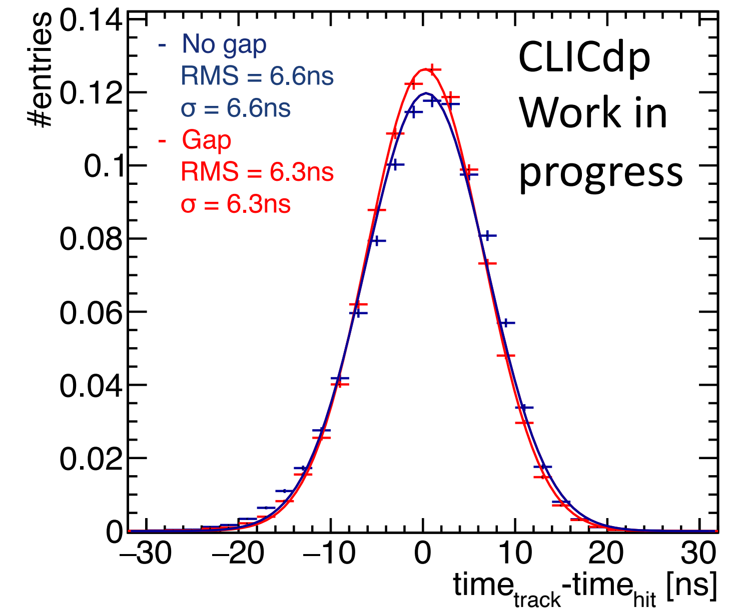
→ Beneficiary for precision with channel concept, especially at angled tracks (to be confirmed)

→ Larger seed signal:

→ Higher radiation tolerance (not relevant for CLIC)

→ Larger efficient operation window → this talk

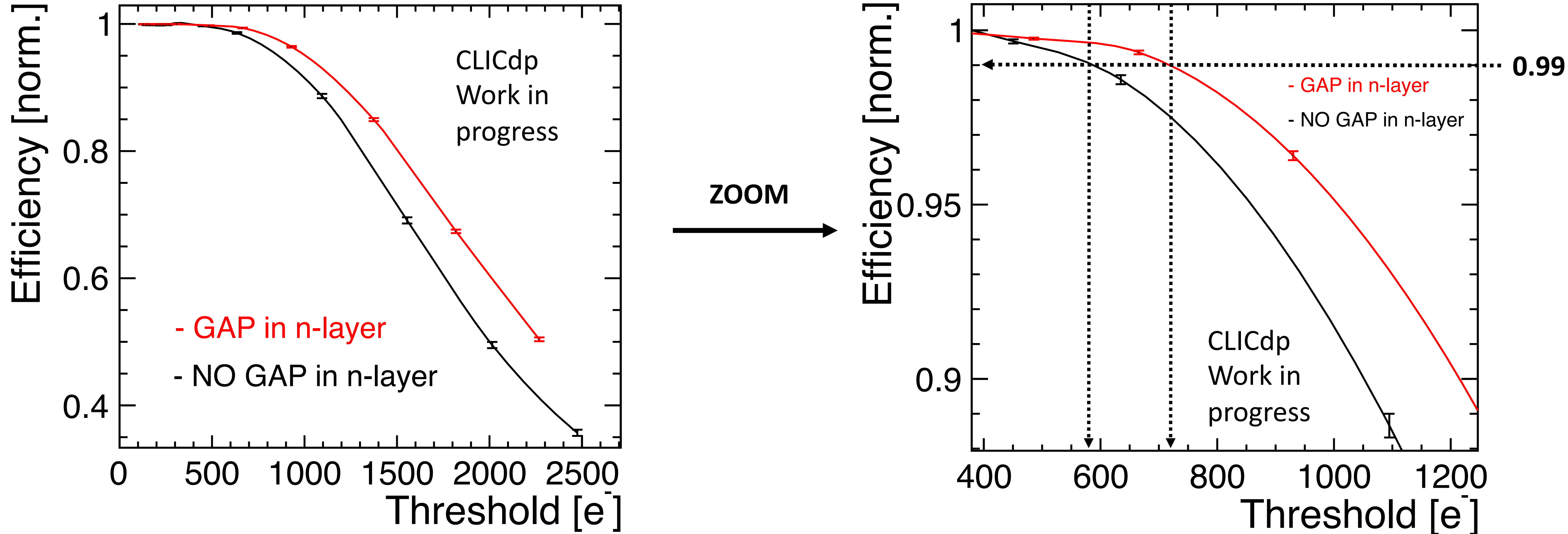
Temporal residual distribution:



→ No significant impact of new pixel design on temporal resolution due to 10ns ToA bins

Efficiency for different pixel designs

Data from December 2019 test-beam, bias p-well/substrate -6V/-6V

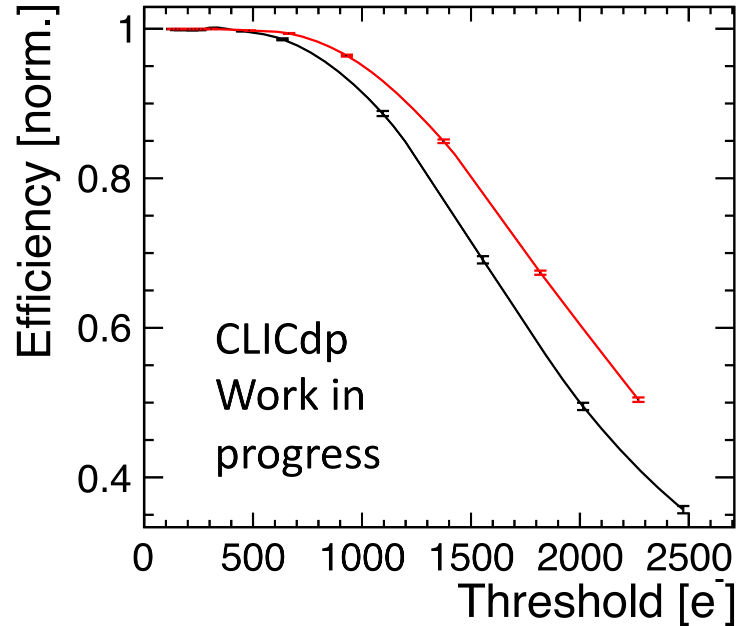


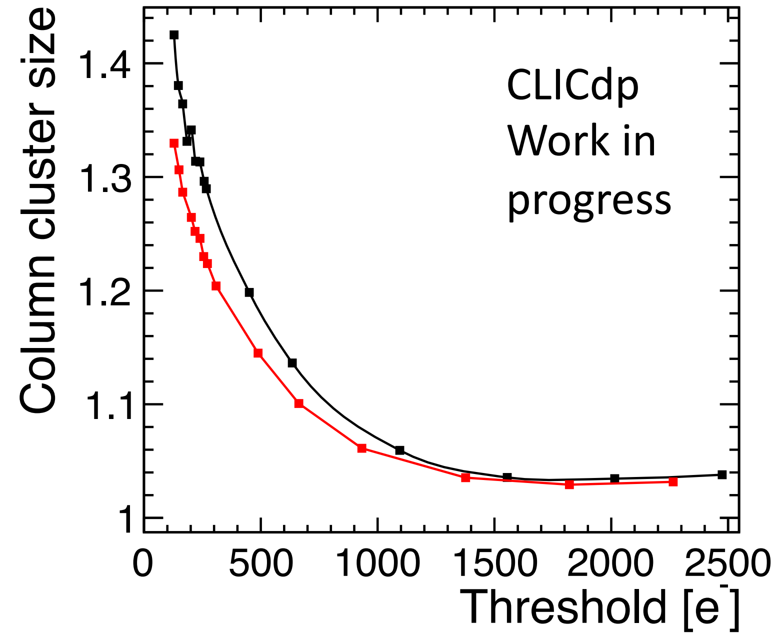
Gap in n-layer extends efficient operation window significantly to higher thresholds.

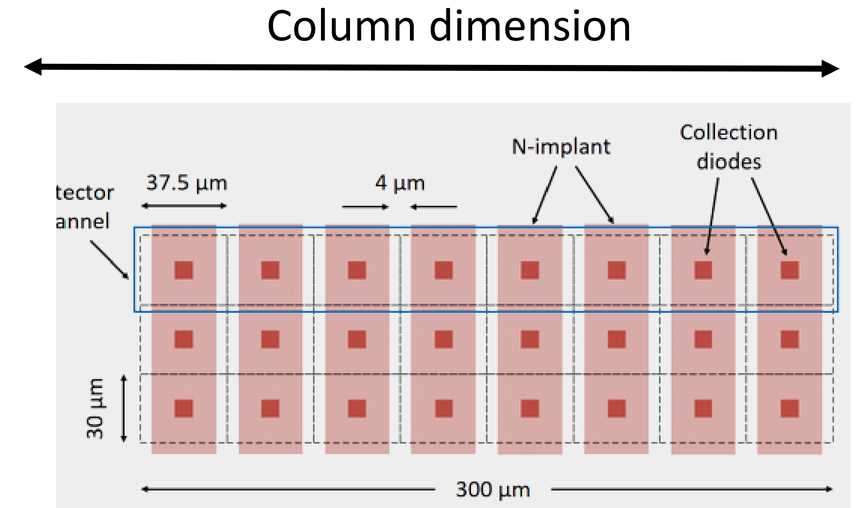
For efficiency of 0.99, the threshold range is extended by ~150e- (~25%).

Efficiency & cluster size for different pixel designs

Bias p-well/substrate -6V/-6V





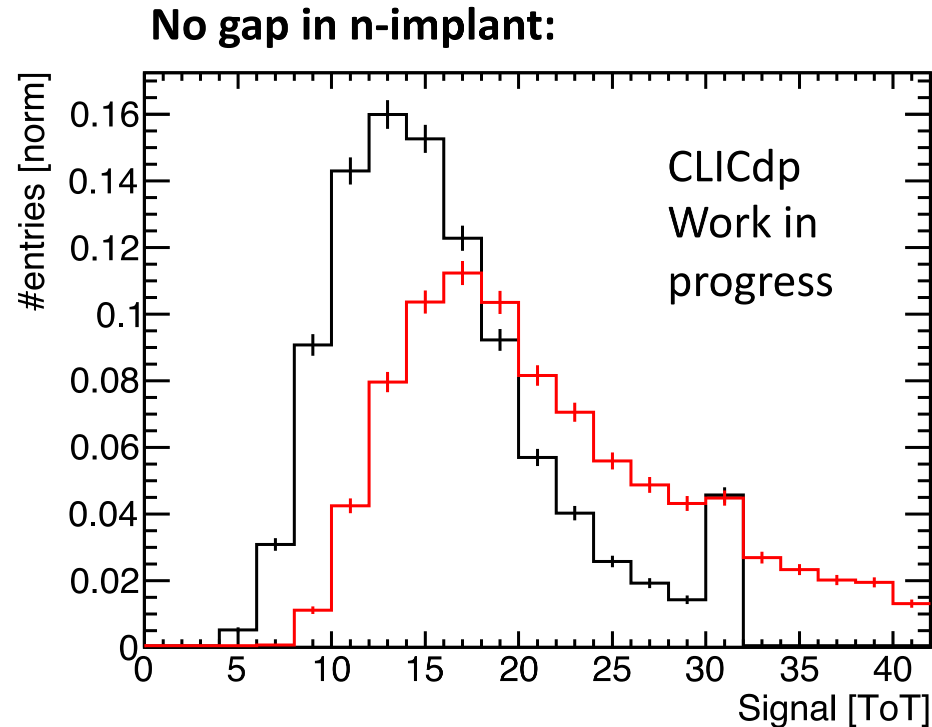


Gain in efficient operation window correlated with reduced cluster size in column dimension.

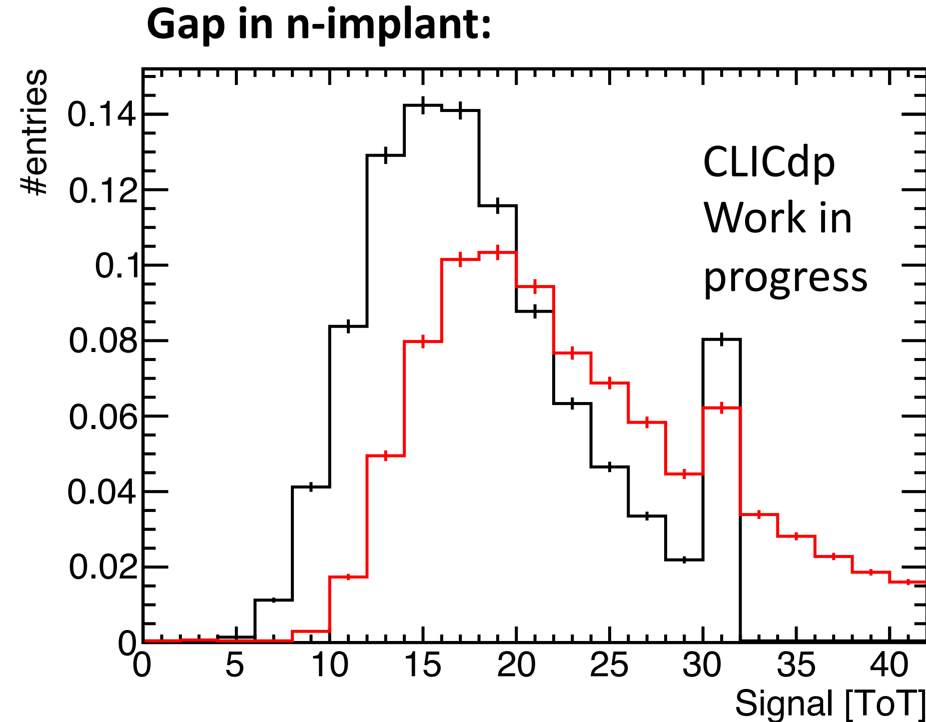
Seed & cluster signal for different pixel designs

Threshold ~150electrons, bias p-well/substrate -6V/-6V

No gap in n-implant:



Gap in n-implant:



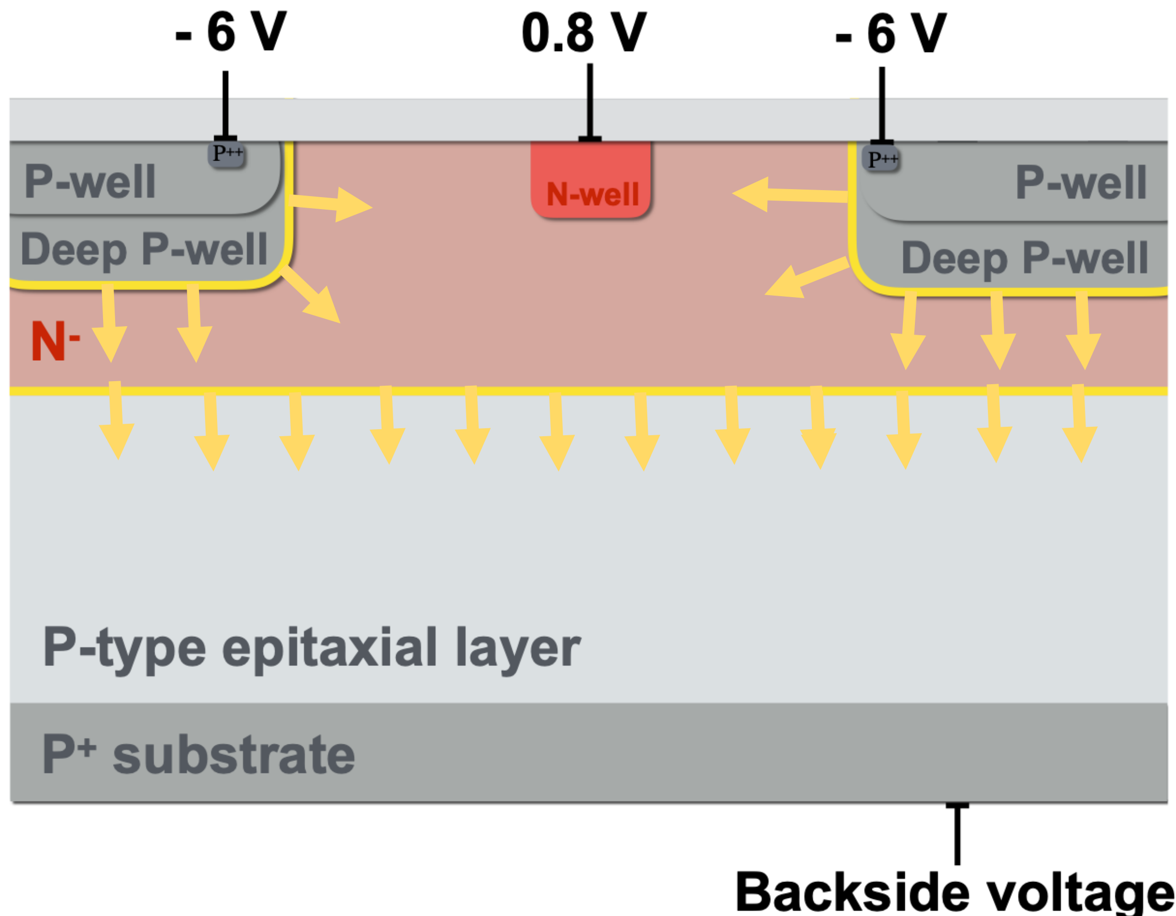
Note: no ToT calibration! → no direct comparison between seed signal distributions of different pixel designs

However: difference between seed & cluster signal corresponds to gain in efficiency due to reduced charge sharing

Cz submission – process splits for CLICTD

- Submission of MALTA on Cz wafers → thicker active layer
- Difference to CLICTD submission → higher n-implant dose (radiation hardness)

Evolvement of depleted region:



Depletion grows from junctions (yellow lines) into lower doped regions:

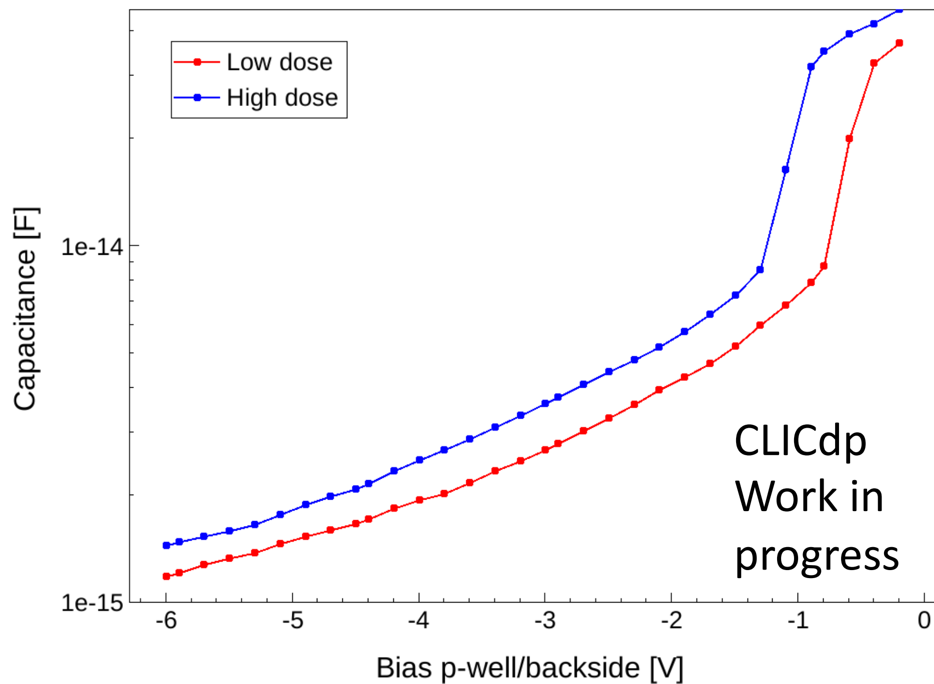
→ From p-wells, depletion grows into n-layer
→ Direct impact on depletion around collection electrode and sensor capacitance

→ From deep planar junction, depletion grows mainly in epi
→ Less impact on depletion around collection electrode and sensor capacitance (see later slides)

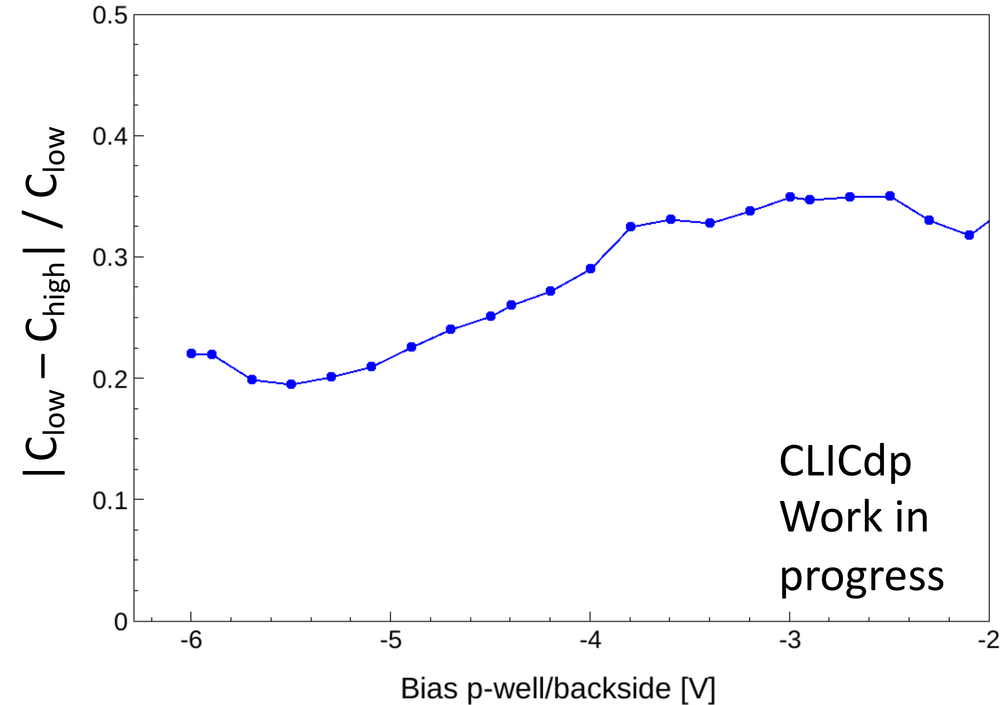
Do we want to pay for an extra split to get the lower n-implant dose?
How much does the higher n-implant dose increase the capacitance?

Capacitance simulation – CLICTD different n-implant dose

Capacitance vs. bias:



Increase of capacitance w.r.t. low dose when using high dose:



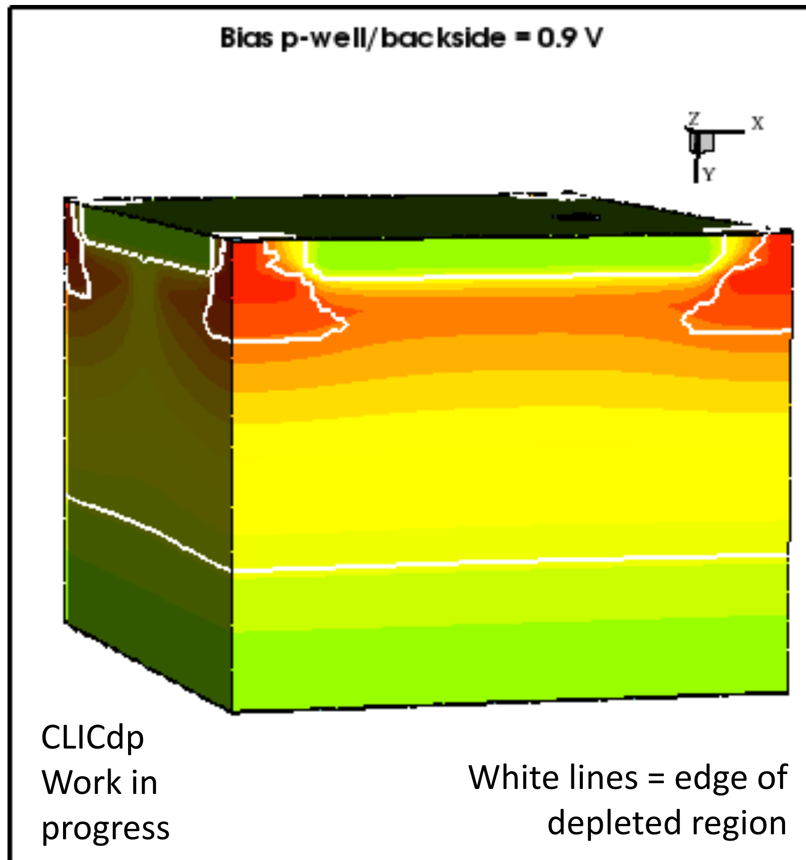
$C_{low} - C_{high} / C_{low}$ = Increase of capacitance w.r.t. low dose when using high dose

→ Capacitance increases by ~20% when using the high instead of low dose (for CLICTD design)

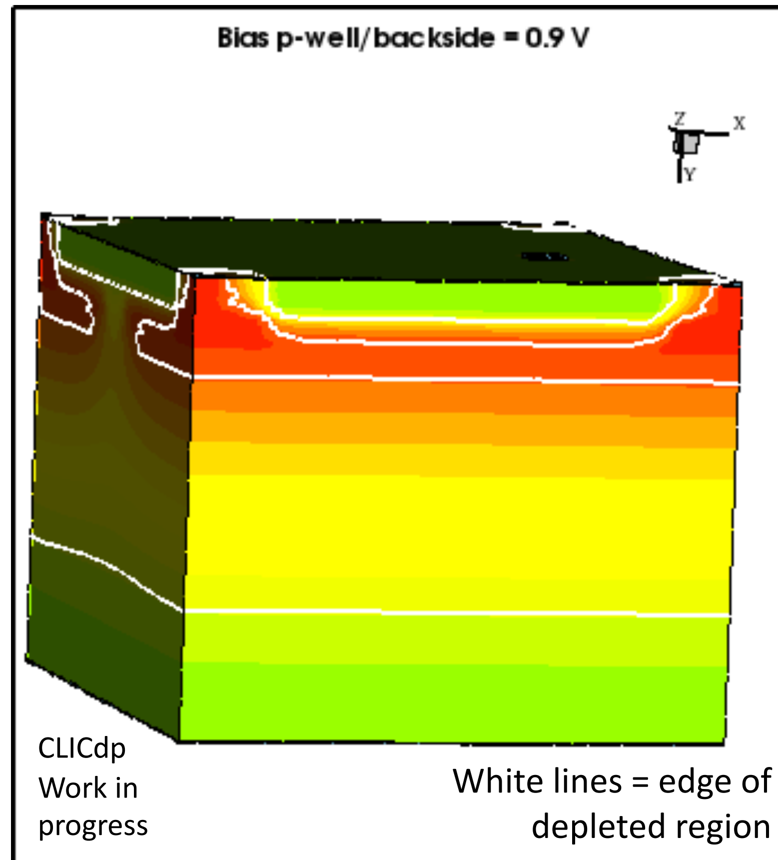
Depletion for different n-implant doses at different bias

Color scale = visualization of electrostatic potential

Low dose:



High dose:



- Different slopes due to depletion under p-wells and depletion in p-well opening
- Very low bias: gap in n-layer isolates single pixel channels
- More depletion around collection electrode for low dose

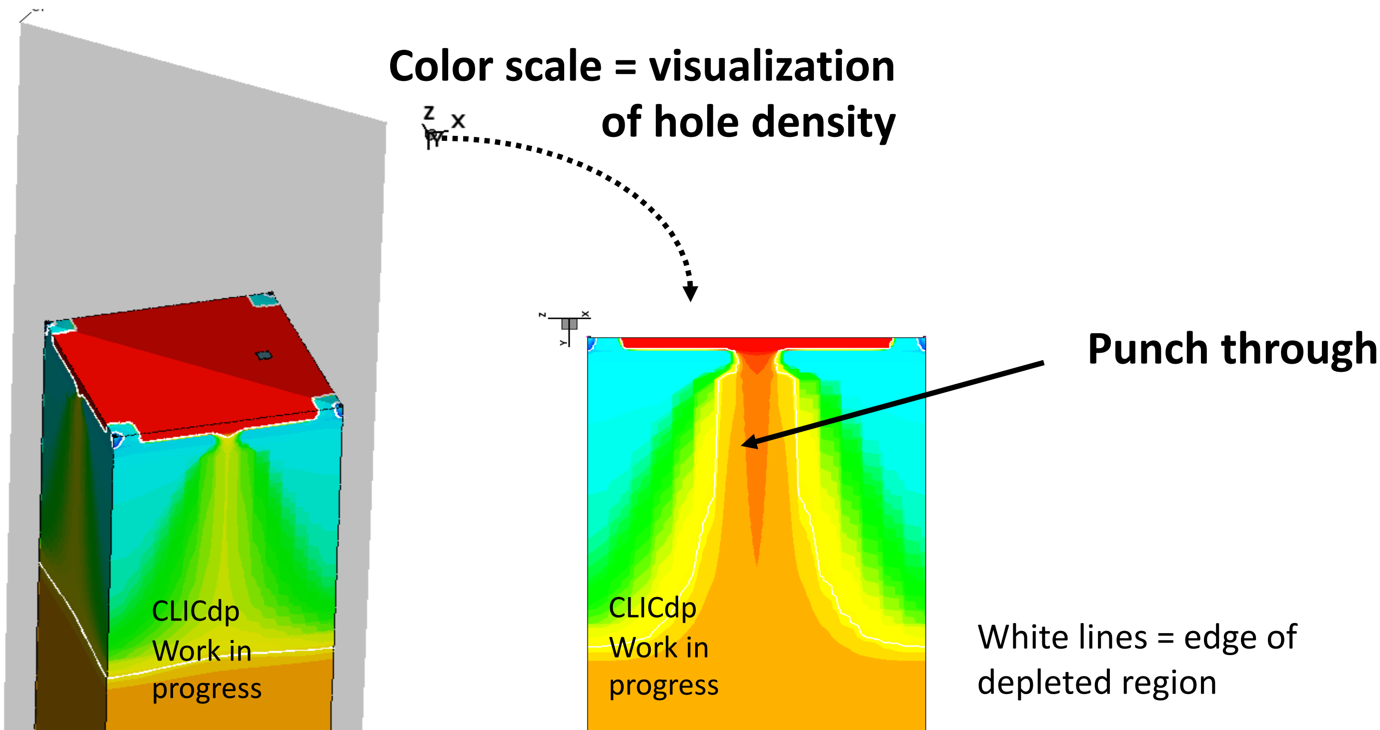
Czochralski punch-through simulations

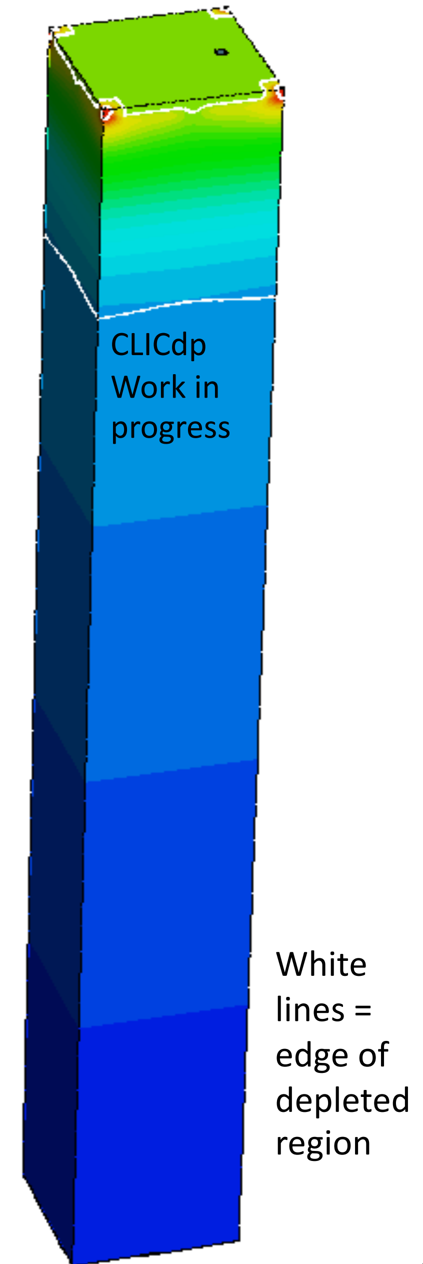
Czochralski simulation setup for MALTA design with gap in n-layer:

- Pixel size 36.5µm x 36.5µm, backside bias -20V, p-well bias -6V, no backside implantation

Punch through = current flow between p-well and backside if both are on different potential

- Czochralski: need higher backside voltage for depletion



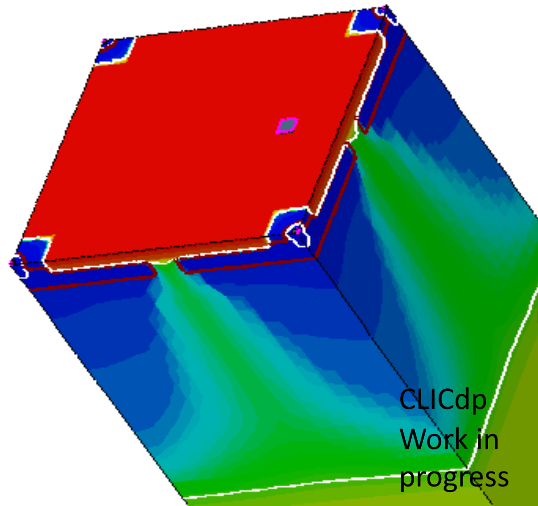


Dependence of punch through on Cz resistivity

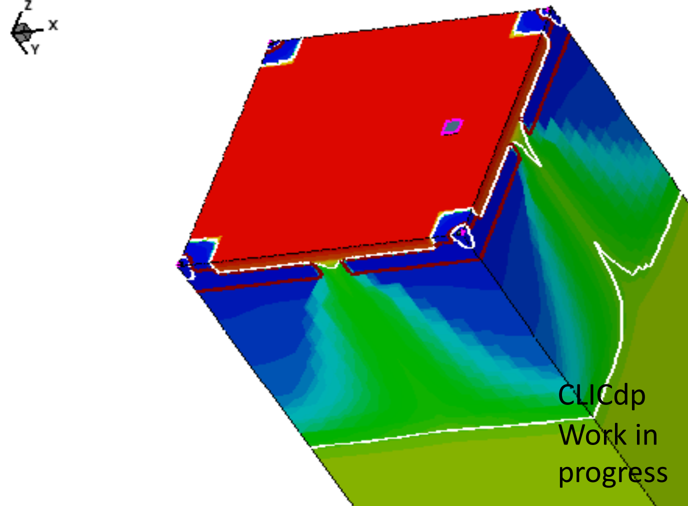
Bias p-well = -6V, bias backside = -20V, gap in n-layer

Color scale = visualization of hole density

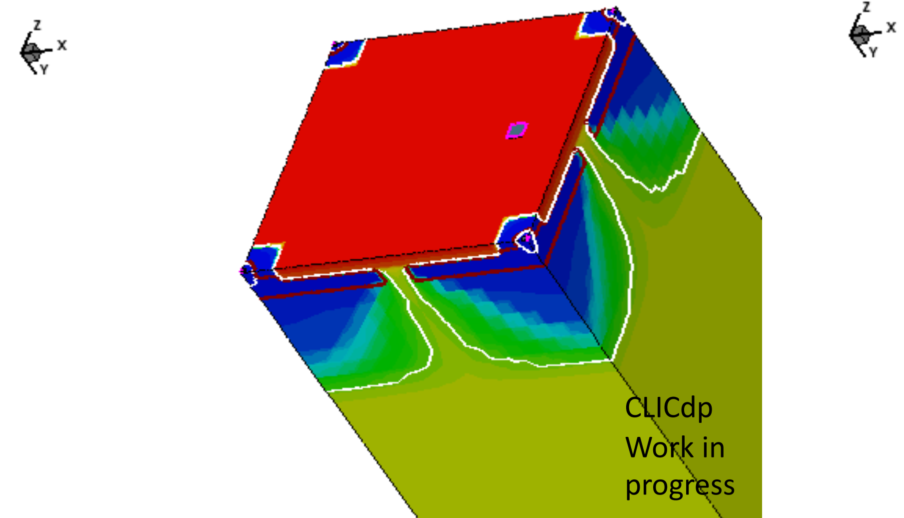
Higher Cz resistivity:



Medium Cz resistivity:



Lower Cz resistivity:



White lines = edge of depleted region

→ Strong dependence of punch through on Cz resistivity

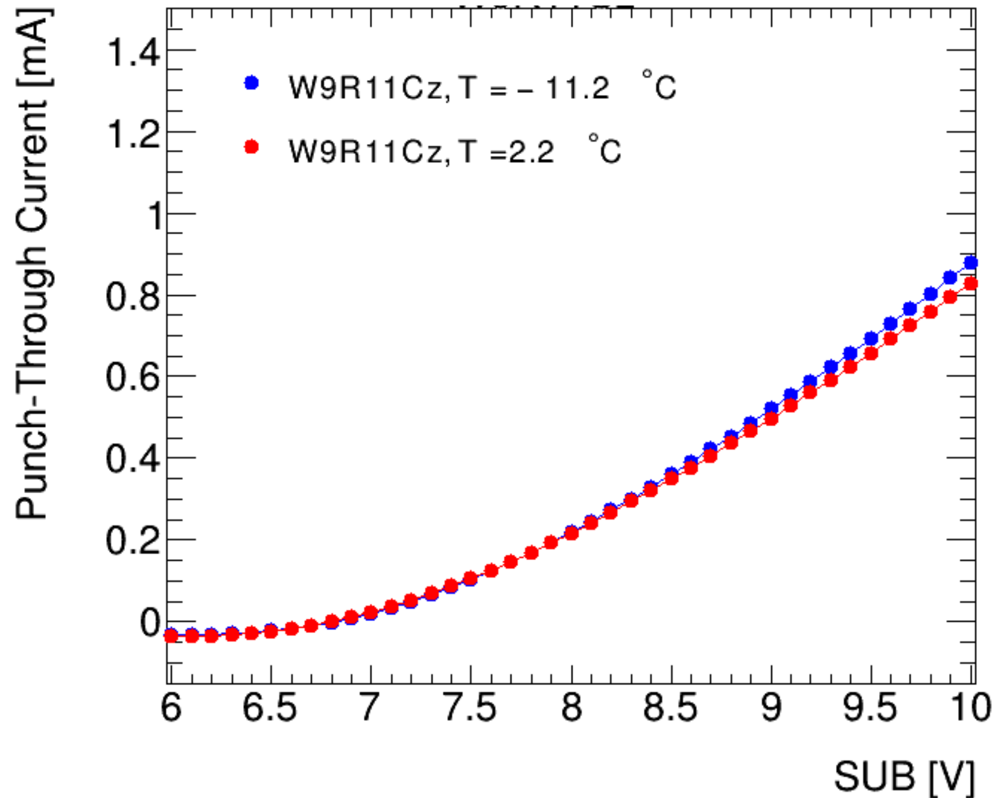
→ *Better performance of lower Cz doping level due to larger depleted region → better isolation of p-wells & larger signal*

→ Careful tuning of simulations

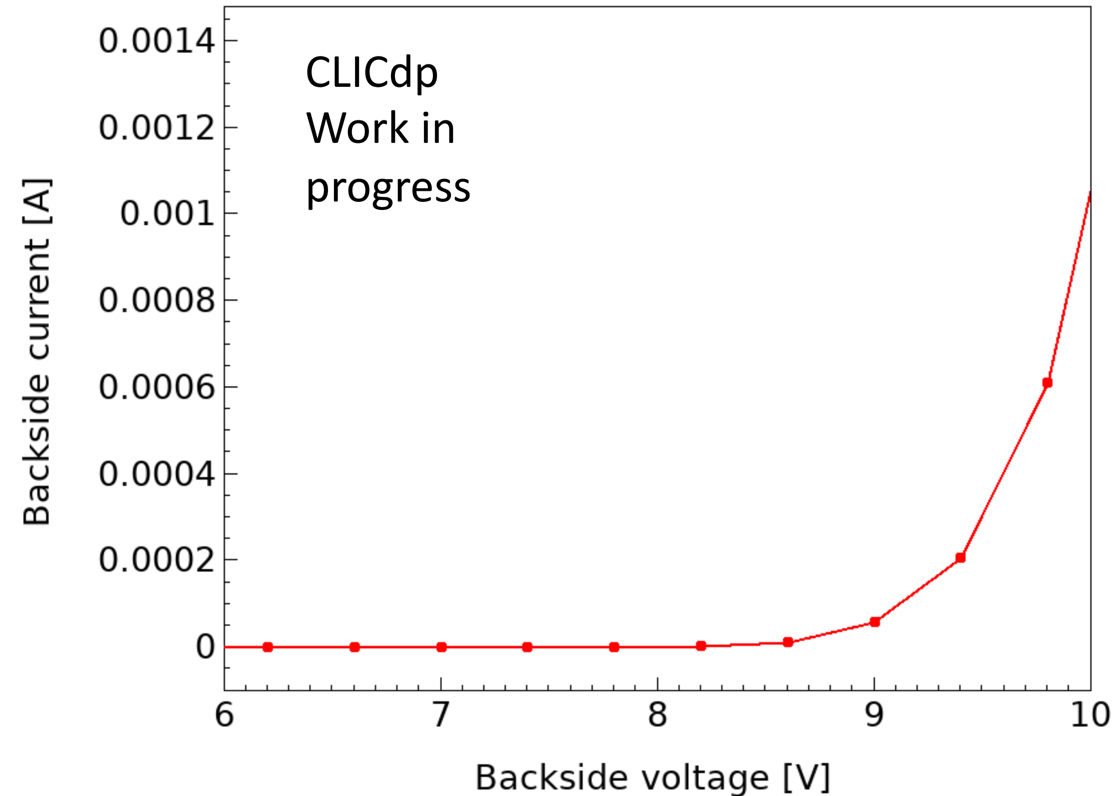
Czochralski punch-through simulations

Bias p-well = -6V, gap in n-layer

Measurements MALTA, from P. Freeman (ATLAS):



Simulations of single pixel cell scaled by MALTA matrix size, T = 2.2 degrees:



- Simulations similar order of magnitude compared to measurements
- Don’t expect perfect agreement since e.g. edge effects are not simulated
- Note: no punch through for pixel design with no gap in n-layer due to better isolation of p-wells

Summary

CLICTD test beam measurements show significant gain in efficient operation window when using gap in n-layer

CLICTD capacitance C_{CLICTD} for higher n-implant dose:

- $\mathbf{C_{CLICTD}}$ ~20% higher for higher for higher compared to lower n-implant dose:
  - **C_{CLICTD} ~ noise**
  - **C_{CLICTD} ~ 1/signal**

} Signal/noise ~ 1/ $\mathbf{C_{CLICTD}}^2$

→ *BUT: compensated by higher signal for Cz compared to epi!*

Capacitance & punch-through:

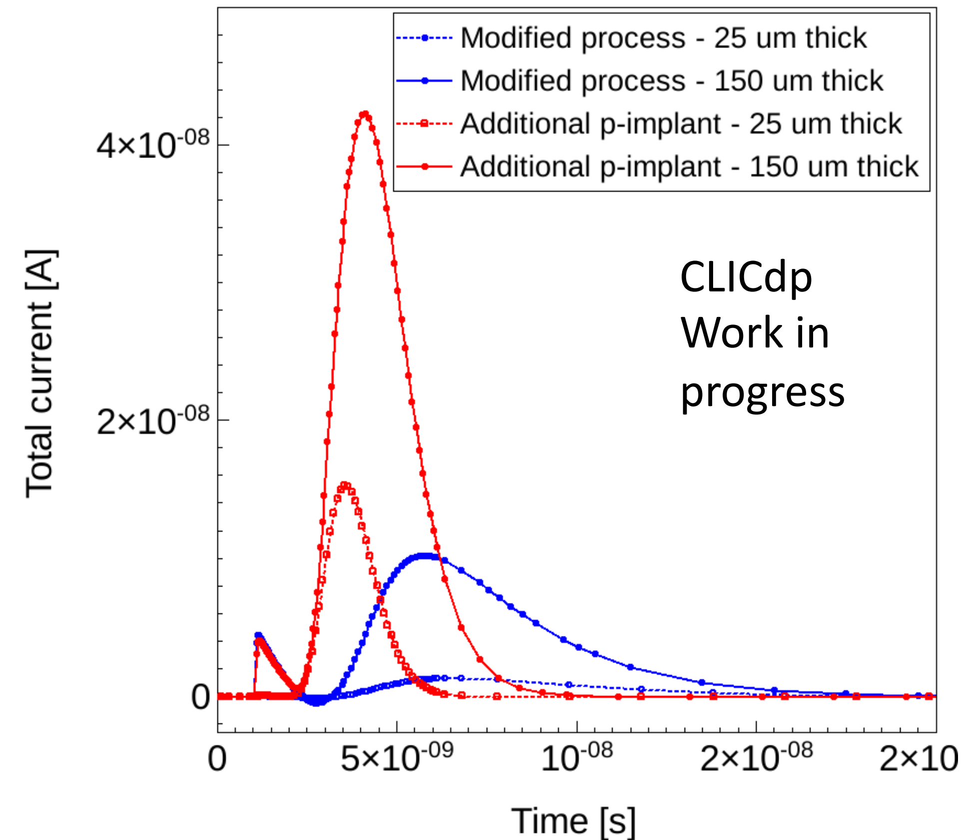
- Very relevant parameters for small collection electrode CMOS
- Only accessible with finite element simulations
- Complex dependence on other design parameters

Next steps

Transient simulation for Cz:

- What is the impact of the punch through current on the collected charge?
- What is the gain in signal when using epi instead of Cz?
- Do the process modifications still help for thick Cz sensor?

Transient simulation for different epi thickness:



BACKUP