Summary of the Progress and test campaigns on SRAM chip

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Content

• Project and design status
  • 65 nm Chip Debug
  • 28 nm SRAM design

• Experiment
  • Test performed
  • Data analysis
  • Future test
Project progress

- Project started
- 180 nm SRAM prototype
  - Tested at: RADEF, Charm, KVI, CERN NA
- 65 nm SRAM V1.0
  - Tested at: RADEF, KVI-proton, CNA-Low E, Proton, ILL-Neuton
- 65 nm SRAM V1.1
  - Planned in 2020
- 28 nm SRAM
  - Test planned: RADEF, UCL
- Dry test
65 nm SRAM design

4 Major blocks, each of them contains $512 \times 24 \times 16 = 192$K bit, total 768K bit. Controlled by digital core with SPI interface (Slave mode, CPOL=0, CPHA=0)
SRAM Chip Design

- 64K×16 bits
- 16 bit Address
- 16 bit word width
- External CLK
- SPI interface up to 50 MHz clock
- Extra power for SRAM cells to make SEU sensitivity tunable (0.4V-1.2V)
- Decoder was design to be compact rather than high speed
Malfunction

This cause that only symmetrical signals can give proper function, 1/24 of the SRAM is still accessible and have been tested.

The problem has been fixed and retyped-out on 22 Aug 2019, new chip will be ready for test in Jan 2020.
28 nm SRAM Design

- More compatible to design cells using different dimensions
- Less complex on timing control and decoder
- 1mm × 1mm 28 nm SRAM chip size (Density: 0.75Mb/mm²) has same SRAM cells as 2mm × 2mm 65 nm chip (Density: 0.18Mb/mm²)
Test Performed

- Heavy ions at RADEF 16.3MeV/u (8h)
- RADEF 52MeV proton on 65 nm SRAM (2h)
- KVI Proton test (180 MeV, 124MeV, 90 MeV, 50MeV, 0.4V and 0.6V) (6h)
- low-energy Proton at CNA (0.5 to 5.9 MeV)
- Thermal Neutrons at ILL
- Heavy ions at KVI

KVI-cart proton test  RADEF heavy ion test  CNA low-energy proton test
Data Analysis

RADEF 52MeV Proton SEU Cross Section

RADEF Heavy Ions SEU Cross Section
Future test

- Neutrons test (with/without high Z materiel coating)
- Mixed environment (composition known)
- Heavy ions
- Protons
Q&A
Data Analysis – Core Voltage

Take the SEU cross section at 1.2V as standard, normalize the curve.

- The curve $Q_c$ represent the reciprocal function ($1/Q_c$) of SRAM SEU critical charge simulated in Cadence Virtuoso.
- The curve $SNM$ represent the reciprocal function ($1/SNM$) of SRAM Static Noise Margin simulated in Cadence Virtuoso.
- The curve Proton represent test result from RADEF 52MeV proton.
- The curve Kr represent test result of 24.6MeV/(mg/cm²) Krypton irradiation. It fits the average of all heavy ion tested.
Data Analysis – Energy/LET

KVI Proton Test

RADEF Heavy ion test
Data Analysis – Threshold Voltage

CNA Low-energy proton SEU cross-section

- Table 1 illustrates no detectable difference between hvt, lvt and normal transistor cells from high-energy proton test. But the result of low energy-proton at CNA shows the SRAM is more sensitive to SEU at low threshold voltage and less sensitive at high threshold voltage.
- Table 2 is the SEU critical charge simulated in Cadence with double exponential current injection, the first 3 rows are the sizes actually implemented in the design.

<table>
<thead>
<tr>
<th>Voltage (MeV)</th>
<th>$u_{1_hvt}$</th>
<th>$u_{2_lvt}$</th>
<th>$u_3$</th>
<th>$u_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>1.65E-13</td>
<td>1.70E-13</td>
<td>1.70E-13</td>
<td>1.73E-13</td>
</tr>
<tr>
<td>0.6</td>
<td>9.12E-14</td>
<td>9.81E-14</td>
<td>8.93E-14</td>
<td>9.43E-14</td>
</tr>
<tr>
<td>0.8</td>
<td>6.03E-14</td>
<td>6.00E-14</td>
<td>6.16E-14</td>
<td>6.70E-14</td>
</tr>
<tr>
<td>1</td>
<td>4.66E-14</td>
<td>4.40E-14</td>
<td>4.48E-14</td>
<td>4.77E-14</td>
</tr>
<tr>
<td>1.2</td>
<td>3.64E-14</td>
<td>3.89E-14</td>
<td>4.02E-14</td>
<td>3.72E-14</td>
</tr>
</tbody>
</table>

Table 1. RADEF 52MeV Proton SEU Cross Section (cm²/bit)

<table>
<thead>
<tr>
<th>NMOS W/L</th>
<th>PMOS W/L</th>
<th>Qcp (fC)</th>
<th>radial</th>
<th>Qcn (fC)</th>
<th>radial</th>
</tr>
</thead>
<tbody>
<tr>
<td>230/60</td>
<td>150/60</td>
<td>1.6</td>
<td>100.0%</td>
<td>2.38</td>
<td>100.0%</td>
</tr>
<tr>
<td>230/60 hvt</td>
<td>150/60</td>
<td>1.65</td>
<td>103.1%</td>
<td>2.29</td>
<td>96.2%</td>
</tr>
<tr>
<td>230/60 lvt</td>
<td>150/60</td>
<td>1.63</td>
<td>101.9%</td>
<td>2.52</td>
<td>105.9%</td>
</tr>
<tr>
<td>230/60</td>
<td>180/60</td>
<td>1.76</td>
<td>110.0%</td>
<td>2.79</td>
<td>117.2%</td>
</tr>
<tr>
<td>275/60</td>
<td>150/60</td>
<td>1.86</td>
<td>116.3%</td>
<td>2.7</td>
<td>113.4%</td>
</tr>
</tbody>
</table>

Table 2. Cadence Critical Charge simulation result
Data Analysis – Compare to 180 nm SRAM

Both of the 65 nm and 180 nm SRAM chips were tested under RADEF heavy ion beams. The result shows that 65 nm SRAM chip has around 5 times smaller SEU cross section compared to 180 nm SRAM in overall chip.

Note:
- 180 nm SRAM has 700µm × 700µm SRAM area within a 1.5mm × 1.5mm chip, composed of 20480 bit cells.
- 65 nm SRAM chip has 4 blocks of 650µm × 600µm SRAM areas within a 2mm × 2mm chip, while 1/24 of them are accessible.