Preliminary test results on readout of a triple GEM detector using MSGCROC ASICs.

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Introduction

The goal for this work was to demonstrate performance of the MSGCROC ASIC applied to 2-D readout of a GEM detector. The demonstrator system is built around a standard 10 × 10 cm^2 triple GEM detector with double-sided readout received from CERN. The readout ASICs are mounted on the ASICs boards designed to match the connectors of the GEM detector. Each ASICs board can be equipped with up to four MSGCROC chips. The MSGCROC ASIC has been developed originally for readout of 2-D MSGC detectors dedicated for position-sensitive neutron detection [1]. A key feature of the MSGCROC demanded by application to neutron imaging is self-triggering, i.e. each signal above a given threshold triggers the readout sequence. The chip provides information on signal amplitude (energy) and on time for all events. The signal amplitudes and encoded timing information are derandomised and multiplexed in the ASICs and then transferred to the FPGA readout board equipped with Virtex4 LX60 FPGA and ADCs, which reads out all the data and send them to standard PC via optical link. A dedicated timing board generates a 256 MHz clock distributed to all MSGCROC ASICs, which is used for synchronisation of time stamping. In the report we review briefly the concept of the MSGCROC ASIC and of the readout system. Following this overview we present initial test results on energy resolution, timing performance and 2-D imaging of the demonstrator.

MSGCROC ASIC

MSGCROC is 32 channel self-triggered ASIC and provides on-chip derandomisation and sparsification of data. Reconstruction of a single event point requires timing, spatial and energy data from both (X/Y) detector planes. To extract these data from the detector signal each readout channel is split into a timing channel and an energy channel (see Fig. 1). The output from the timing channel is used to latch a 14-bit time stamp with 1 ns resolution and to enable peak detector and hold (PDH) circuit in the energy channel. The outputs from the PDH and the time stamp are stored in 4-stage FIFOs, analogue and digital one, respectively. The readout of the memories is performed via a token-ring based multiplexer [2]. The analogue data is read out via a single differential link at a rate of 32 MHz. The digital data is readout via a parallel 8-bit LVDS bus at a rate of 128 MHz. The internal programmable bias circuits, including a number of DACs, configuration and test circuits, are controlled via the I2C interface.

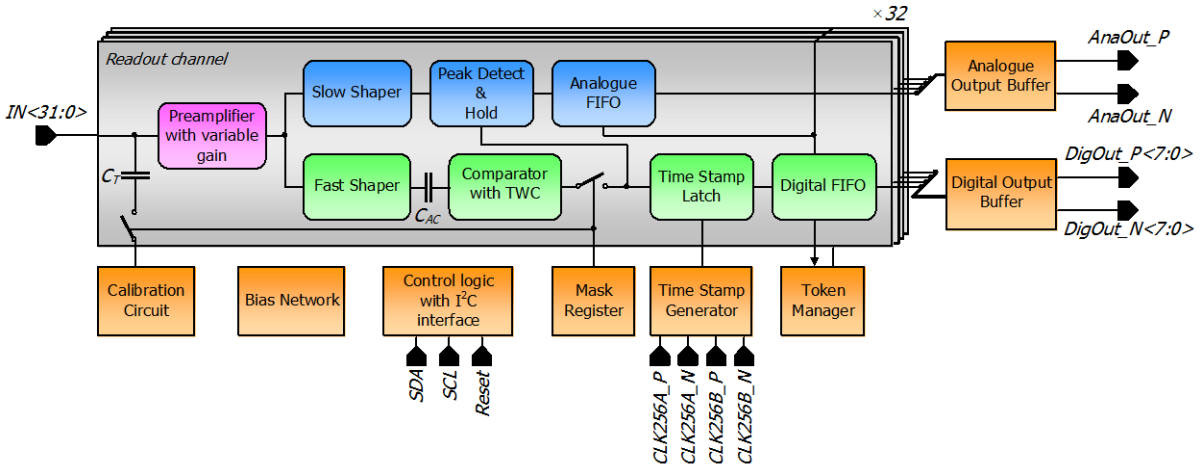


Fig. 1. Simplified architecture of the MSGCROC ASIC

Requirements

The basic requirements concerning the MSGCROC parameters are the following:

- Signal parameters to be measured: position, time, energy (amplitude).
- Hit rate per strip: up to 9×10^5 / s.
- Input signal charge: 2×10^5 e^- (32 fC) ÷ 5×10^6 e^- (800 fC) (depending on the signals generated in the detector).
- X/Y coincidence window 2 ns + (EX = EY).
- Discriminator time accuracy: time walk < 2 ns, jitter < 2 ns FWHM.
- Variable gain in a range 1 ÷ 20.
- The preamp-shaper circuits must handle both polarities of the input signal.
- The data must be buffered and derandomised on the ASIC.
- Zero suppression must be performed on the ASIC.

Preamplifier

The input stage is a transimpedance amplifier built around a folded cascade fast amplifier with a bridged-T low pass filter in the feedback loop. The preamplifier delivers fast pulses with short tails to minimize pile-ups. Variable gain is implemented in the preamplifier stage by selecting one of five feedback networks. The switchable gain factors are: ×1, ×2, ×4, ×8, and ×16 and the gain can be set depending on the gas multiplication factor of the detector to match the signal range with the liner range of the circuits following the preamplifier. The preamplifier is also equipped with a switchable inverter stage so that it delivers signals of the same polarity for either polarity of the input charge.

Every channel is equipped with a test capacitor C_T = 1 pF, connected to the input of the preamplifier, which can be used for test and calibration purposes. Specific patterns of the channels to be pulsed simultaneously can be programmed. The test pulses of required amplitudes are generated internally. The test pulse amplitudes are controlled by an internal DAC of 8-bit resolution.

Timing channel

The timing channel consists of a fast shaper (with a peaking time Tp = 25 ns) and a comparator with a Time Walk Compensation circuit (TWC). It delivers the trigger signal to the PDH circuit in the energy channel and to the time stamp latch. Thus, the detection efficiency and noise rate depend on the discrimination threshold.

Energy channel

The energy channel comprises a slow shaper (with a peaking time Tp = 85 ns) and a classical peak detector and hold circuit (PDH), which detects the peaks of incoming pulses and holds their values for a given time period triggered by the comparator in the fast timing channel. The shaping function of the slow channel is optimised taking into account the requirements concerning the noise (energy resolution), count rate, dynamic range and speed limitations of the peak detector.

Time stamp generation

The 14-bit time stamp signature is composed of a 12-bit Gray-encoded counter which provides 12 bits TS<13:2>, a toggle flip-flop, which provides TS<1> and the input clock TS<0>. The correct timing of two least significant bits, to ensure that all 14 bits are Gray encoded, is achieved by adjusting the delays appropriately through the programmable delay buffers. In this schema we can achieve 1 ns resolution for an external clock frequency of 256 MHz.

ASICs board

To connect the ASICs to the GEM detector a dedicated ASIC board has been designed and manufactured. The layout of the ASIC board is shown in Fig. 2. One ASIC board houses four MSGCROC chips so it can serve 128 strips. The MSGCROC inputs have only standard ESD protections that will be not sufficient in case of discharging in a gas detector. Therefore input protection circuits built of SMD components are implemented on the ASIC board. The schematic diagram of the input protection circuit is shown in Fig. 3.

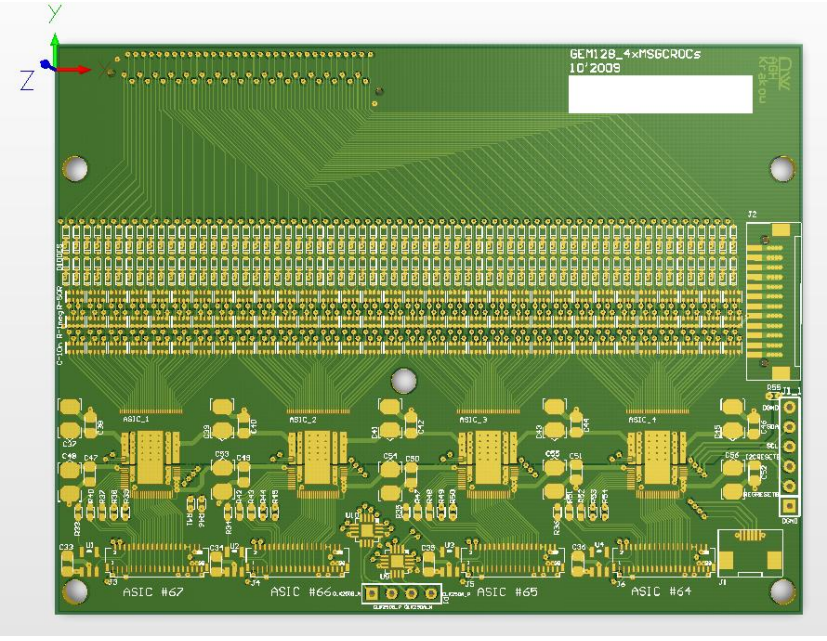


Fig. 2. ASIC board.

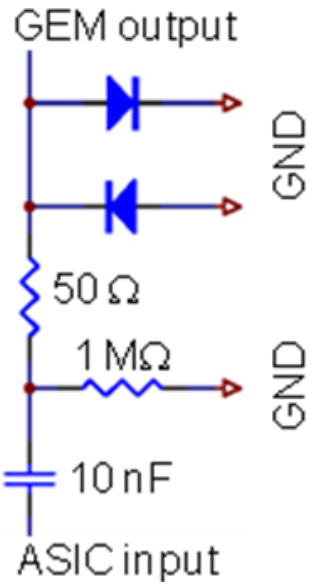


Fig. 3. Input protection circuit.

FPGA board

The block diagram of the prototype readout system is shown in Fig. 4. The system was developed by the group from FZ-Jülich in the frame of the DETNI project according to the specific requirements for readout of the MSGC neutron detectors. It is based on a Virtex-4 FPGA (XC4VLX60) and comprises four interfaces:

- I2C slow control: responsible for the ASICs' configuration and slow control.
- Host PC interface: Gigabit optical link used to transfer data to a host PC for off-line analysis.
- Frontend interface: responsible for the data transfer from the ASICs to the FPGA.
- Board-to-board: responsible for data transfer between readout modules.

Additionally, the power supply section provides power to both the onboard circuitry and the frontend modules. Analogue and digital voltages are produced using different power supplies to diminish noise. Two LDO regulators (TPS759xx) are providing separate power supply for the frontend modules' analogue and digital circuitry.

The ASICs on the frontend boards are controlled via a serial bus using the I2C protocol. This bus is accessible via a flexible printed circuit (FPC) connection from the readout board, where a parallel-to-I2C controller represents the interface to the FPGA. Thus, through adequate programming of the FPGA, access to ASICs and its registers to set values and parameters is provided.

The interface to a host PC is currently realized by the commercially available SISLINK mezzanine board, which was formerly developed in cooperation between FZ-Jülich and the company SIS. It is equipped with an on-board optical link, which allows access to the prototype readout board and a data transfer of up to 80 Mbyte/sec.

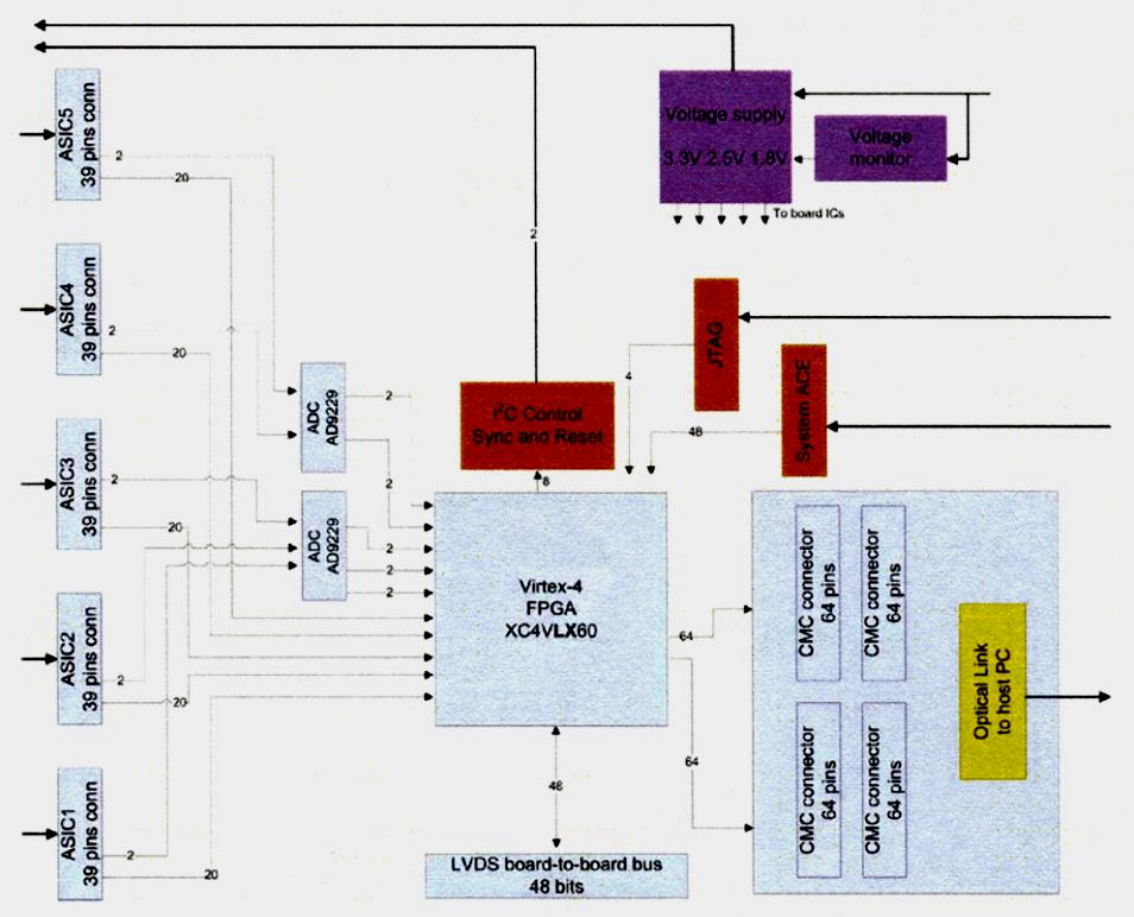


Fig. 4. Block diagram of the FPGA readout board [3].

The frontend interface of the prototype readout board is connected to each individual ASIC via a FPC connector with 0.3 mm pitch. The board comprises five such connectors so that up to five ASICs can be read out by one FPGA board. The front-end interface receives both the analogue and the digital information continuously from the ASIC FIFO buffers within 32 MHz readout cycles. The analogue signal is stabilized in the second half of each readout cycle and digitised by a quadruple ADC with quadruple serial LVDS outputs (AD9229). The coincident 32-bit digital information is four-fold multiplexed and thus delivered in four 8-bit packages clocked with 128 MHz per package. Within the FPGA the digital information is rebuilt and fed into FPGA-FIFOs together with the digitised analogue information, considering the latency introduced by the ADC [3]

Timing board

The block diagram of the clock distributions system is shown in Fig. 5. The design follows the common approach of a clock distribution system, in which all clock signals are derived from a single master clock. The master clock is a low frequency clock, generated on one of the timing boards, which can be distributed to all other timing boards. The timing boards use a frequency synthesizer and Zero-Delay-Buffers (ZDB) to multiply the master clock to 256 MHz, generate the phase shift of 90° by a programmable delay and fan out the two 256 MHz clock signals. This offers the possibility of synchronous operation of a scalable number of boards, cascaded in a tree like structure, for delivering clock signals to the ASIC boards [3]

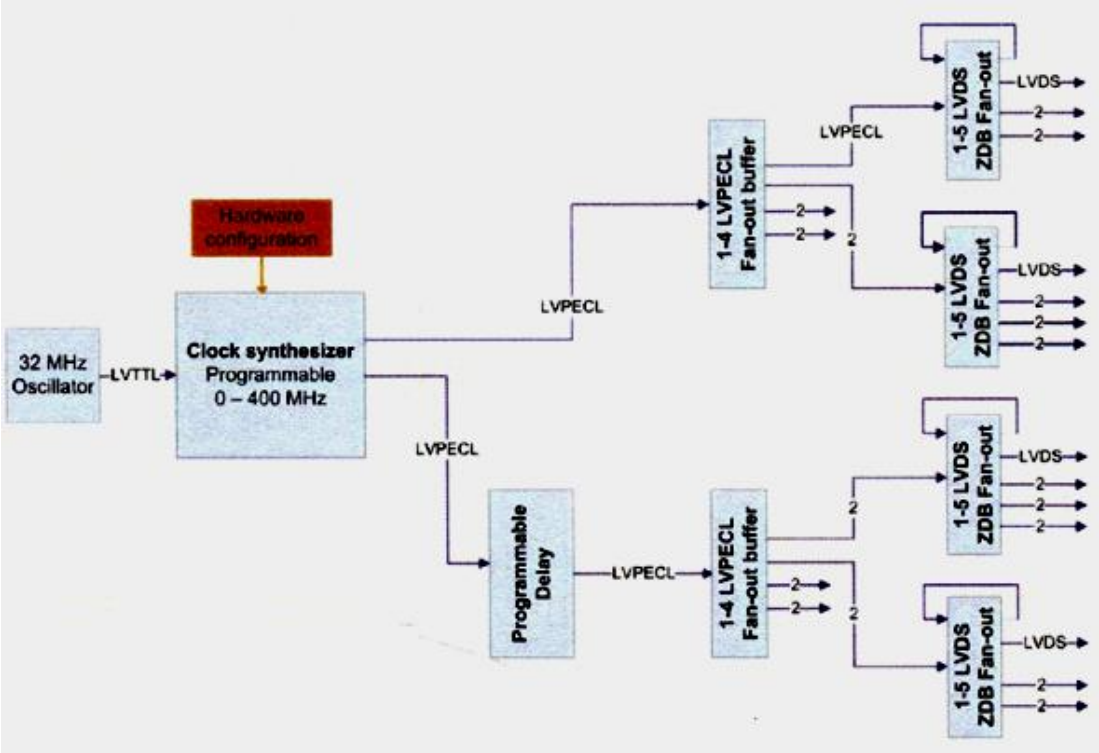


Fig. 5. Block diagram of the clock distribution system [3].

Software

The system is controlled by software packages, which perform two types of tasks:

- Configuration of the operational conditions of the ASICs (bias currents, signal polarity, gain, discriminator threshold, threshold trimming, time walk compensation, amplitudes of calibration signals, pattern of calibration signals).
- Acquisition and processing of raw data from the ASICs combined with the data from the ADC on the FPGA board, which performs digitisation of signal amplitude.

At the present stage filtering and reconstruction of events is performed by the software in the PC. It is understood that for any application of such a system to high count rate measurements it will be necessary to perform initial data processing and histogramming in the FPGA.

Test set-up

All test were done using mentioned above standard triple GEM detector, which was flushed with $ArCO_2$ 80/20 gas mixture. Two ASIC boards, each one equipped with two MSGCROC ASICs, were connected to the X and Y readout plane respectively. Thus, we were able to read out 64 X-strips and 64 Y-strips. The limitation is due to availability of single FPGA board. The measurements were performed for X-rays from the Fe-55 radioactive source.

Timing measurements

The MSGCROC ASIC stores the time stamp for each signal appearing at its inputs and this time information is a primary tool to reconstruct events in the detector by finding time coincidences between X and Y readout strips. Therefore, understanding of timing parameters of the detector and the ASIC is of primary importance. It is foreseen that, depending of the energy spectrum of the measured radiation, matching of the energy measured on X and Y strips can be used as an additional tool for reconstruction and of events. This obviously requires clustering of signals from several strips/channel, which record charges from the same event. Identification of signals belonging to the same cluster/event is performed according to timing information.

The time stamp of 1 ns resolution is generated in the MSGCROC internally. The time precision of the discriminator response is affected by the time walk and time jitter. The resulting time distribution depends on the signal amplitude distribution, on noise, and on the discriminator threshold setting. In a cluster of signals generated by a given detection event the time of the discriminator response in timing channel is measured independently for each strip/channel. Using these data we have built a time distribution of signals belonging to the same cluster. For each cluster the time stamp corresponding to the largest signal in the cluster was set as the reference zero time and the time stamps of signals on the neighbouring strips were measured with respect to that reference. Such an approach is justified by the fact that the largest signal is least affected by the time jitter.

The results for four different thresholds are shown in Figs 6—9. The discrimination threshold of the timing channel in the MSGCROC is controlled by an internal DAC (Digital-to-Analogue Converter) and is expressed in the DAC counts. The thresholds of 23, 40, 60 and 80 correspond to charges collected on single strip of 27 fC, 47 fC, 70 fC, and 94 fC, respectively. Based on cross calibration of the clustered signals in the energy channels and response of the energy channels to electronically injected input charge we have obtained a conversion factor between the collected charge and energy released in the detector volume. Thus for a given discrimination threshold we can define an equivalent energy deposition as if all charge was collected on single strip. The discrimination thresholds equal to 23, 40, 60, and 80 DAC counts, expressed in terms of this equivalent energy are 315 eV, 550 eV, 820 eV, and 1.1 keV, respectively. These are the approximate numbers valid only for specific operating conditions: gas mixture and detector bias voltage. Let us underline that we cannot cluster the signals in the timing channel so that the discrimination is applied to the single strip signals. The amplitude distribution of signals measured on single strip is obviously different compared to the distribution of clustered signals and does not correspond to the energy distribution.

The obtained time distributions are affected by time walk and time jitter. If the spread of discriminator time response was dominated by the jitter then we would expect a symmetric distribution around zero. Indeed, we see such distributions for higher threshold (Figs 8 and 9). For lower thresholds (Figs 6 and 7) we observe some asymmetry of the time distribution, which indicates for some contribution from the time walk. Obviously, for lower thresholds the distributions are wider because we discriminate then on the slow part of the leading edge of the fast shaper outputs.

In the imaging measurements without an external trigger the setting the discrimination threshold will affect not only the time resolution, detection efficiency and noise count rate, but also the spatial resolution because the discrimination threshold will define the number of strips taken for estimating the centre of gravity of each cluster. Therefore, understanding of all these parameters for a given radiation field will be important for finding a configuration resulting in the best imaging performance.

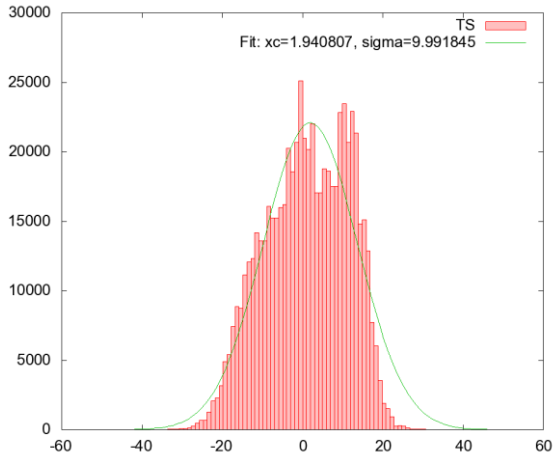


Fig. 6. Time stamp differences between hits belonging to the same event for ASIC gain 4, threshold 23, GEM voltage 3900 V.

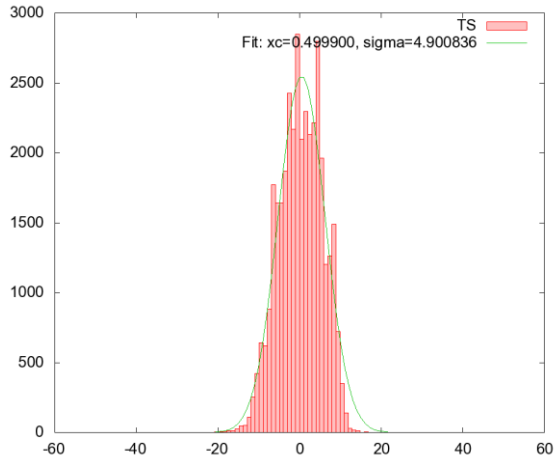


Fig. 7. Time stamp differences between hits belonging to the same event for ASIC gain 4, threshold 40, GEM voltage 3900 V.

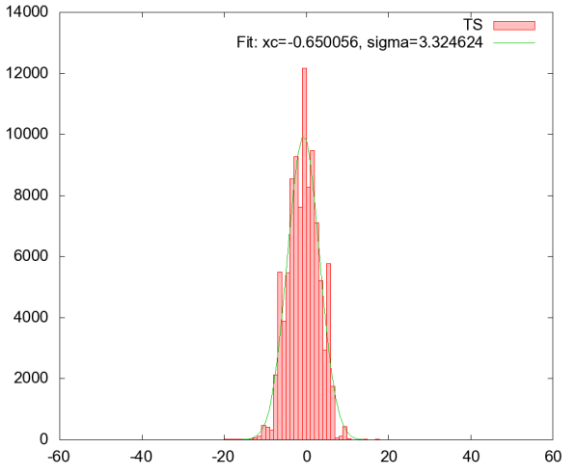


Fig. 8. Time stamp differences between hits belonging to the same event for ASIC gain 4, threshold 60, GEM voltage 3900 V.

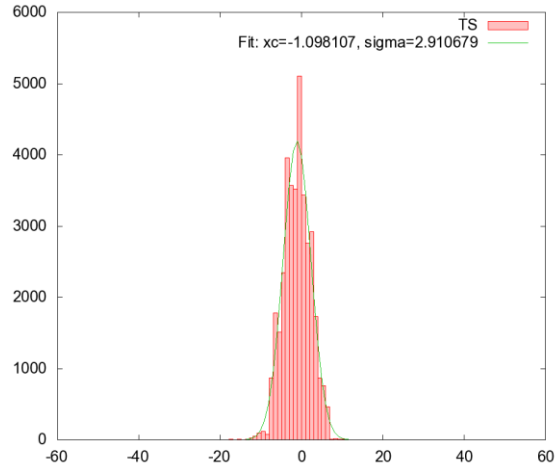


Fig. 9. Time stamp differences between hits belonging to the same event for ASIC gain 4, threshold 80, GEM voltage 3900 V.

Energy measurements

The distributions of clustered signals from the energy channels for the same discrimination thresholds as used for measurements of time distributions are shown in Figs 10-13. To determine the total energy deposited in the detector active volume one has make clustering of hits which arrived within a given time window. If the window is set too narrow small signals appearing on the channels responding with some delays with respect to the central strip of the cluster will be cut off and result lowering the estimated total charge (energy). On the other hand, if the window is set too wide one may add noise hits, which will degrade energy resolution. In the distributions shown in Figs 10-13 each cluster was defined by a time window of ± 25 ns with respect to time response of the central strip (the one with the highest signal). The energy resolution of the 5.9 keV peak is 21.5%, 25.9%, 28.9%, and 26.2%, for discrimination threshold of 23, 40, 60, and 80, respectively.

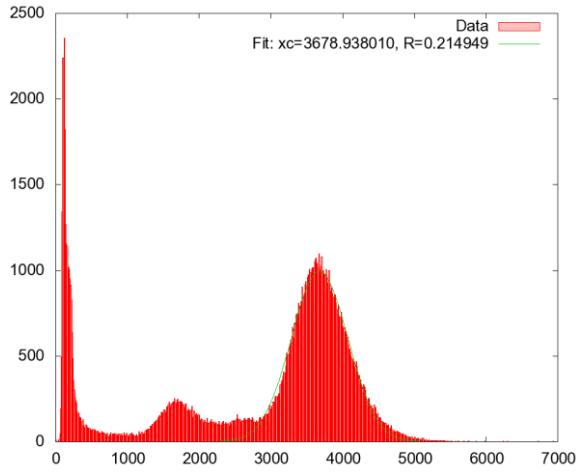


Fig. 10. Energy spectrum for ASIC gain 4, threshold 23, GEM voltage 3900 V.

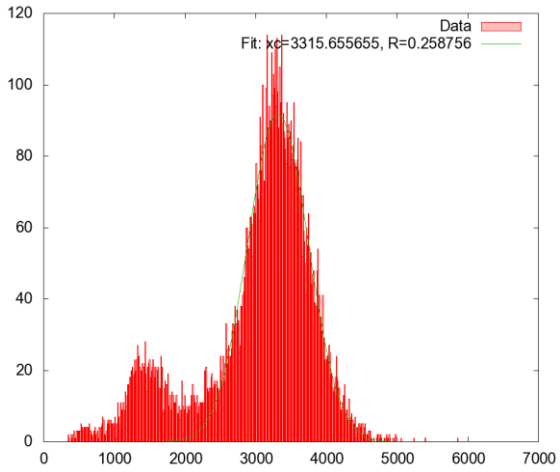


Fig. 11. Energy spectrum for ASIC gain 4, threshold 40, GEM voltage 3900 V.

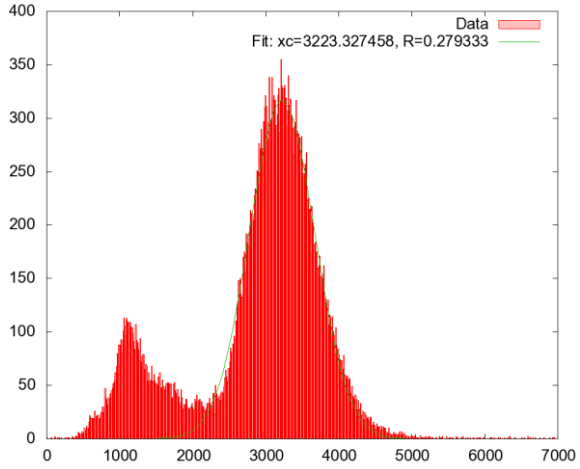


Fig. 12. Energy spectrum for ASIC gain 4, threshold 60, GEM voltage 3900 V.

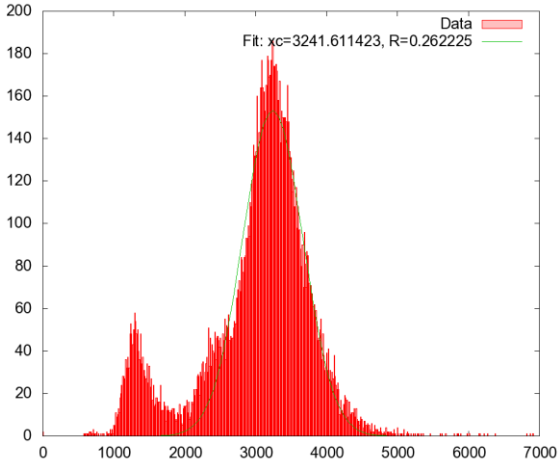
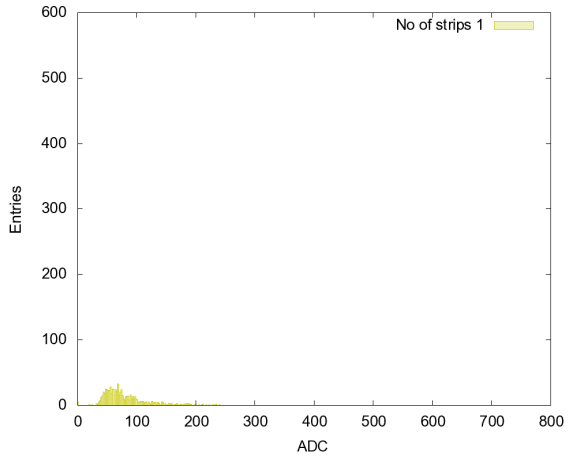
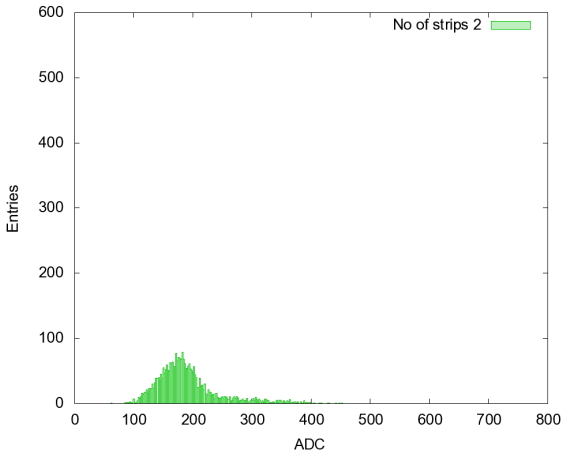


Fig. 13. Energy spectrum for ASIC gain 4, threshold 80, GEM voltage 3900 V.

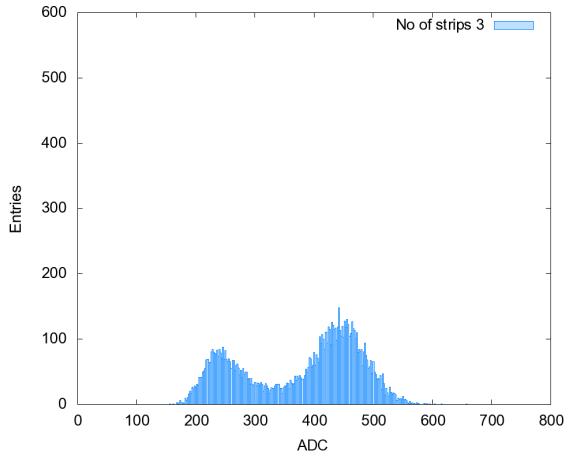
The measured distributions are composed of clusters comprising 1 to 5 strips. Figure 14 shows the relative contributions by 1-strip, 2-strip 3-strip, 4-strip, and 5-strip events to the total energy spectrum. One can see that majority of events are 3- and 4-strip clusters. The distance of 3 to 4 times the strip pitch corresponds well with the range of electrons generated by 5.9 keV photons in the detector volume.



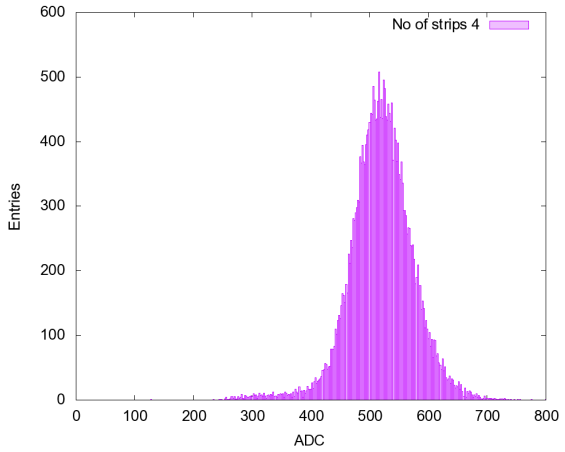
a) Amplitude distribution of 1-strip clusters.



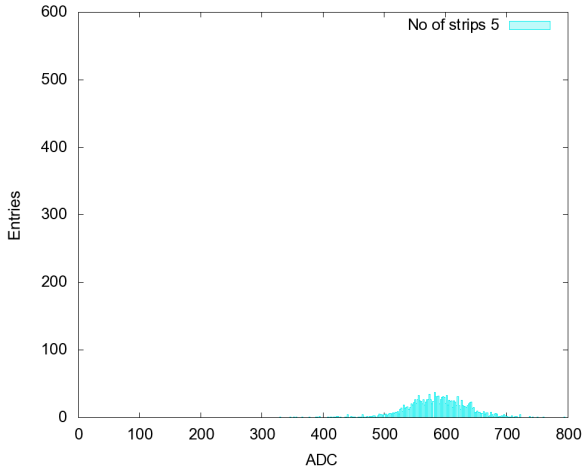
b) Amplitude distribution of 2-strip clusters.



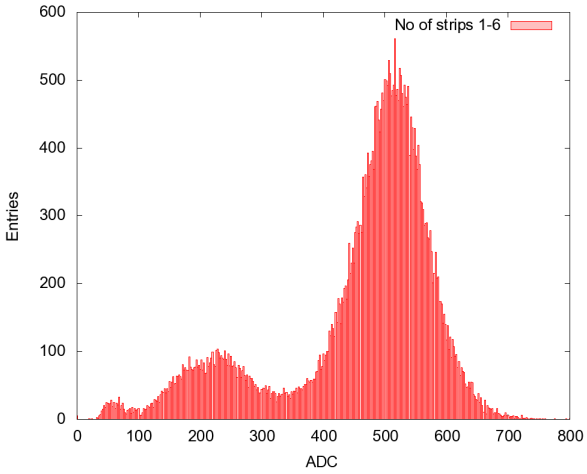
c) Amplitude distribution of 3-strip clusters.



d) Amplitude distribution of 4-strip clusters.



e) Amplitude distribution of 5-strip clusters.



f) Summary amplitude distribution comprising 1 to 5-strip clusters.

Fig. 14. Relative contributions of clusters of different size to the total energy spectrum. The units on amplitude axis are arbitrary and should not be compared with the units in Figs 10-13.

Simple 2-D imaging examples

The measurements of time and amplitude distributions described above were taken for one readout plane. In order to reconstruct X and Y position of each photon entering the detector one has to match events recorded on X and Y strips within a given time window according to their time stamps. If more than one event appear on either plane within the time window then such events are rejected. In case of a high count rate and a complex energy spectrum one can use matching of the signal amplitudes as an additional filtering tool that may improve rejection of false coincidences.

Below we show simple 2-D images obtained with 5.9 keV X-rays. The purpose of this exercise was to demonstrate that the MSGCROC ASICs are suitable for efficient readout of 2-D strip detector. The X and Y coordinates of each photon registered in the detector were defined by the coordinates of X and Y strips with the highest signals within each reconstructed event. Given the intrinsic resolution of the detector, and X-ray scattering in our set-up, calculating of the centre of gravity for each cluster does not improve the quality of the obtained images.

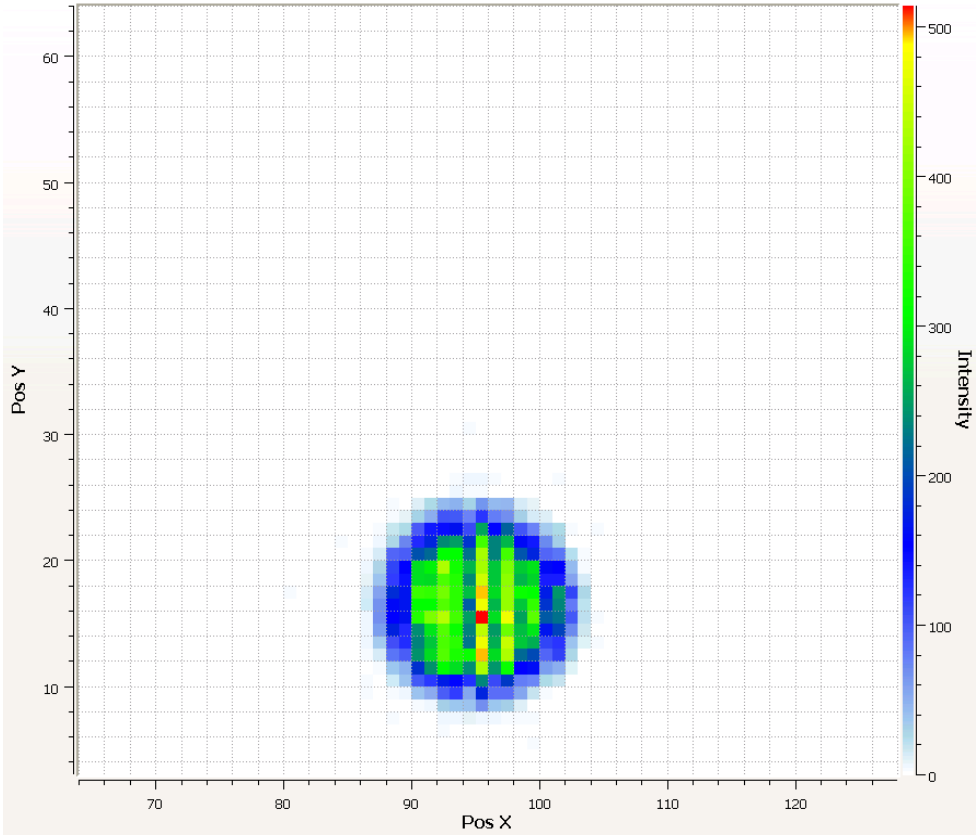


Fig. 15. Image of a barrel collimator with the inner diameter 3mm.

Other images were taken for via holes in a standard PCB. The patterns of imaged via holes, a line and a matrix, are marked in Fig. 16. The images of these patterns are shown in Figs 17 and 18, respectively.

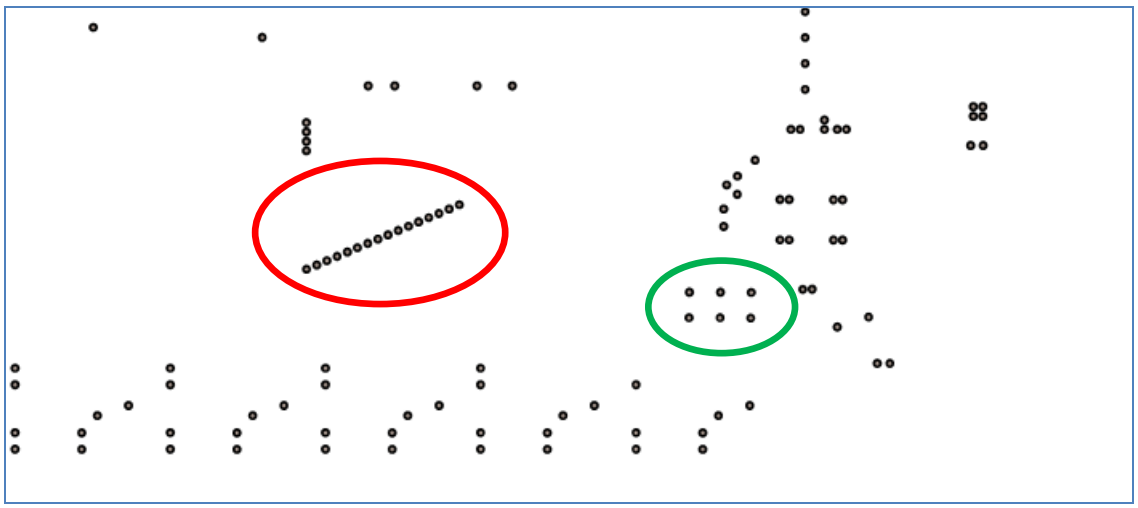


Fig. 16. Patterns of via holes in a PCB irradiated with 5.9 keV X-rays: a line of via holes of 0.3 mm diameter, a matrix of via holes spaced by 1.9 mm in vertical direction and by 2.35 mm in horizontal direction.

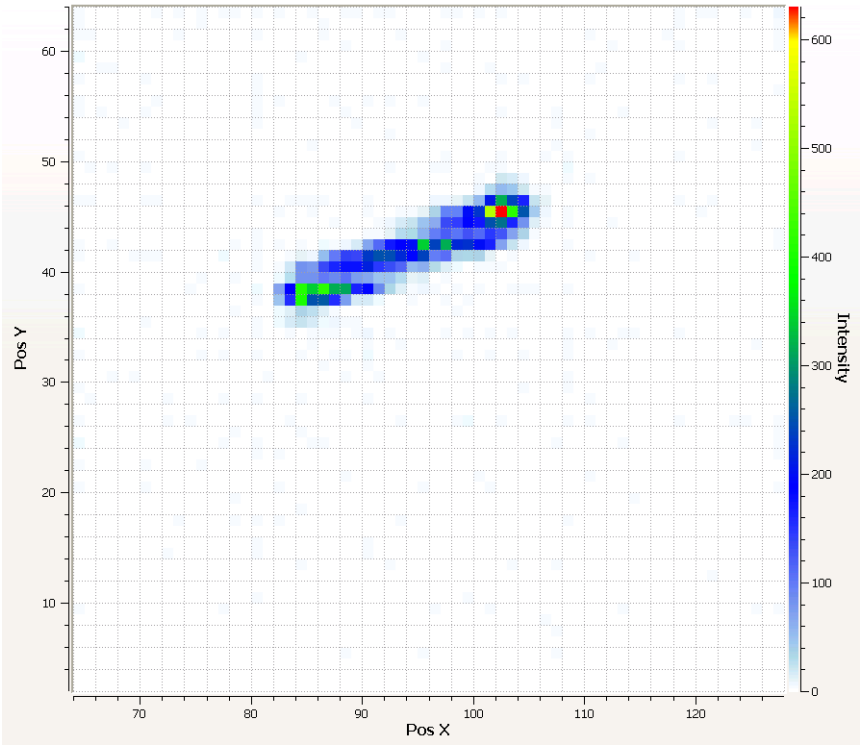


Fig. 17. Image of a line of via holes of 0.3 mm diameter.

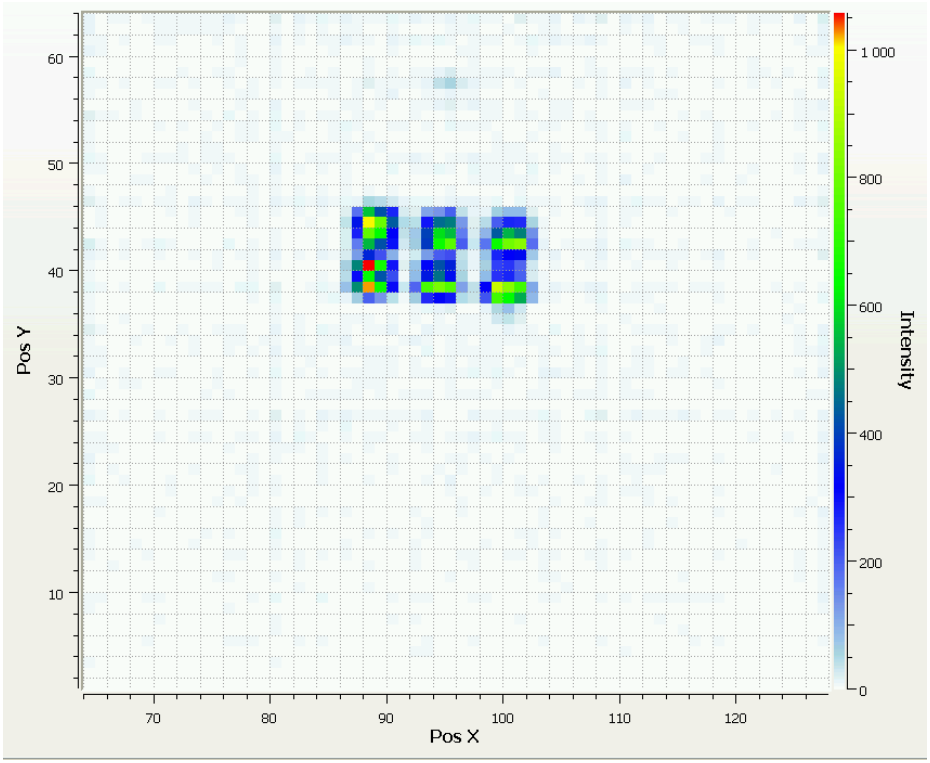


Fig. 18. Image of a matrix of via holes spaced by 1.9 mm in vertical direction and by 2.35 mm in horizontal direction.

Conclusions

We have demonstrated that the MSGCROC ASICs can be used efficiently for 2-D readout of GEM detectors. The basic parameters of the MSGCROC, dynamic range, noise, time resolution, suit well the signals delivered by the GEM detector. Furthermore, readout architecture of the MSGCROC is suitable for high count rate 2-D readout of GEM detectors without external trigger. A readout mechanism using an external trigger can be easily added in the MSGCROC architecture.

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