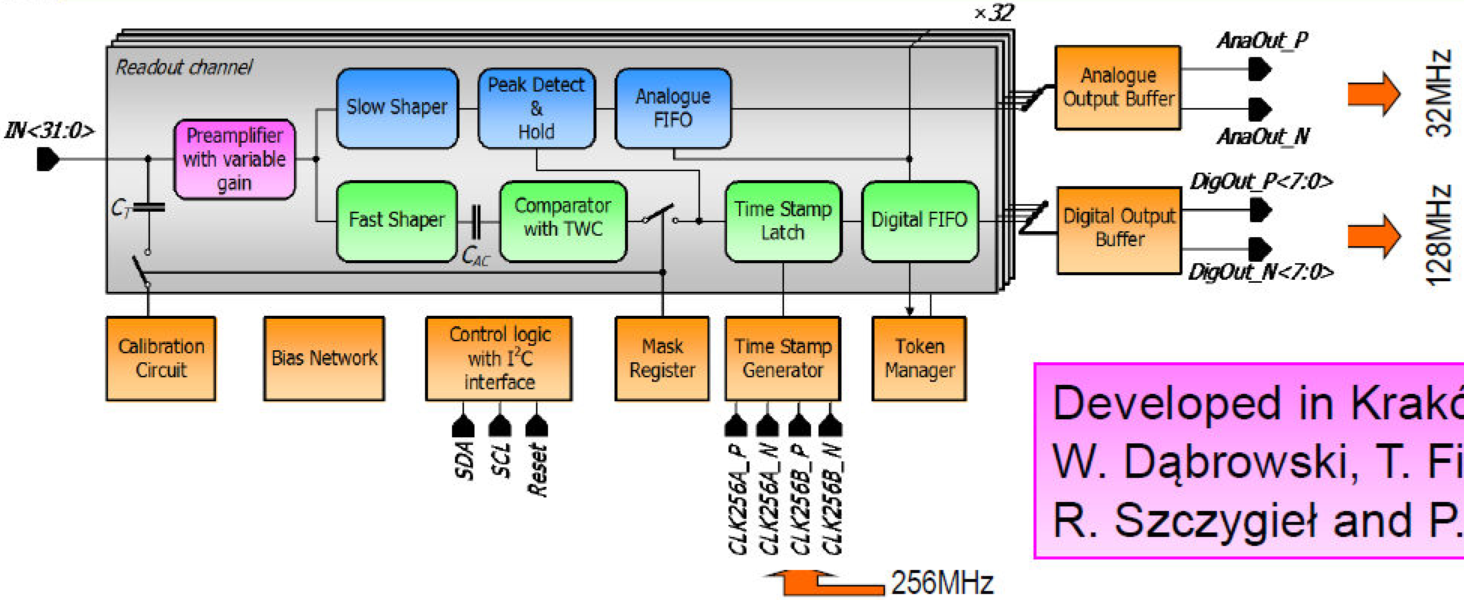
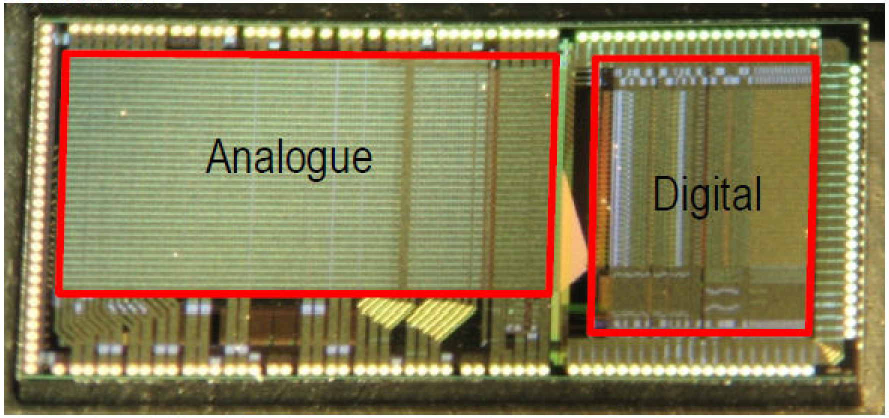
GEMROC Discussion

MSGCROC architecture



Developed in Kraków by:
W. Dąbrowski, T. Fiutowski, R. Szczygieł and P. Wiącek

3.2x6.7 mm^2



0.35 µm CMOS process from Austria Microsystems

Input device: PMOS 2368µm/0.4 µm

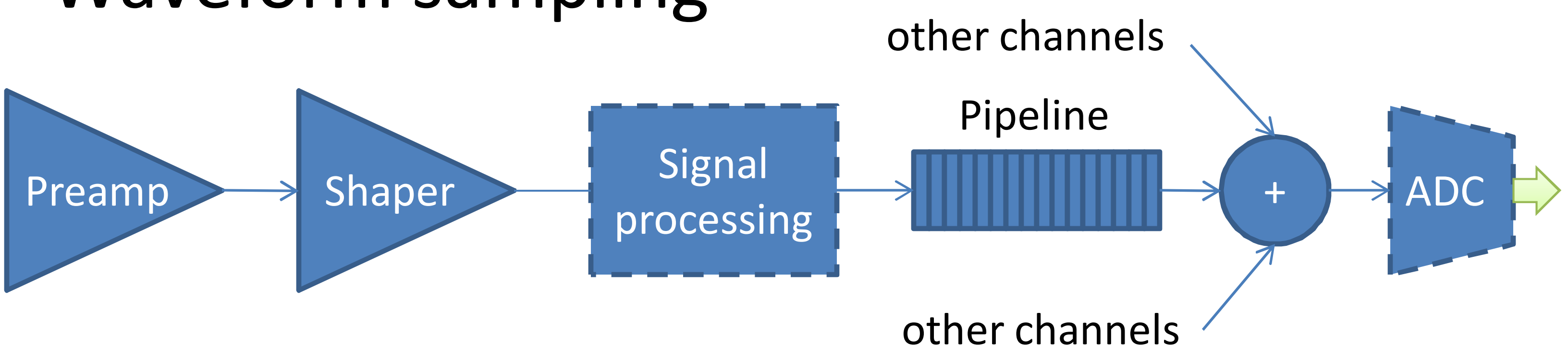
Bias current of the input transistor: 2.36mA (nominal)

Power consumption ~25 mW/channel (@ 3.3 V)

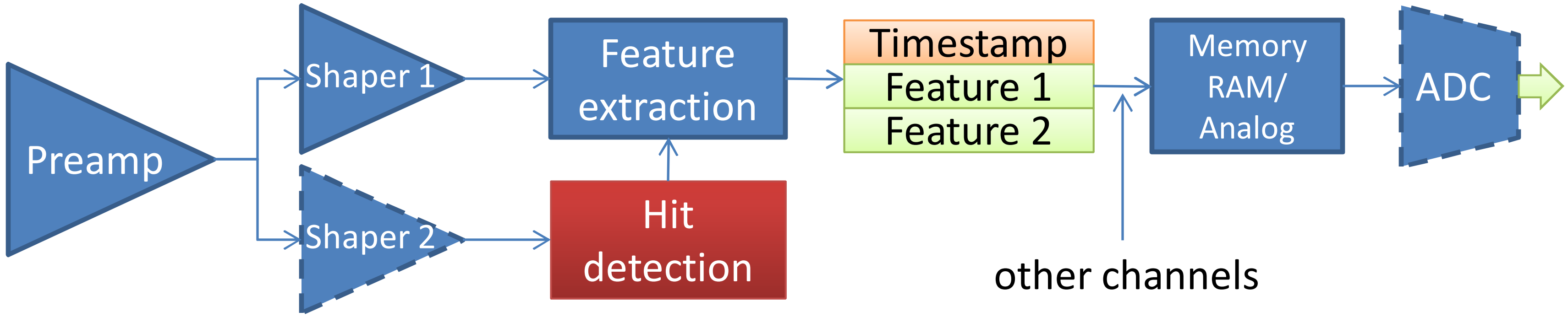
Separated analogue and digital power supply

Front-End Architecture

- Waveform sampling



- Self-triggered channel



Requirements

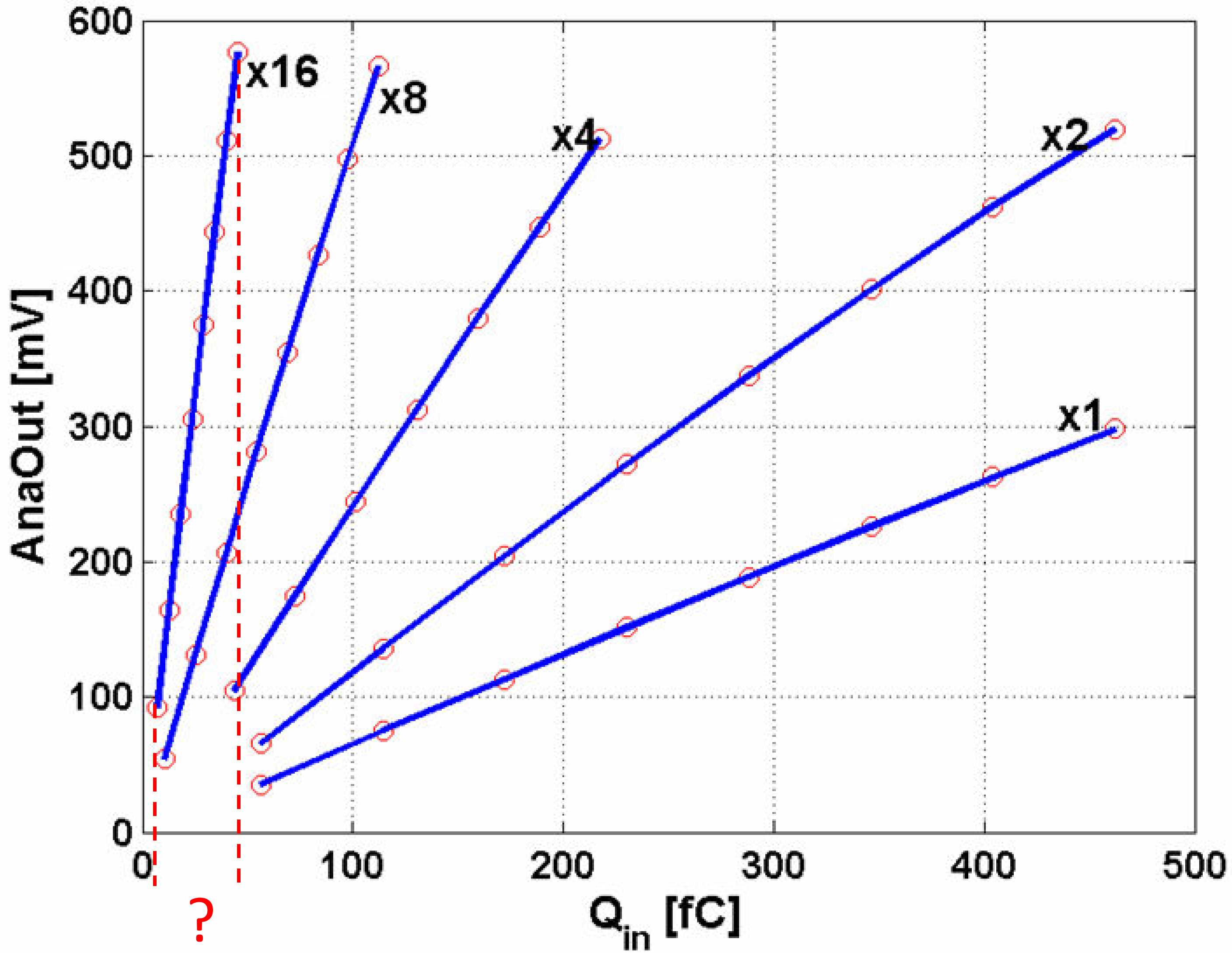
The basic requirements concerning the MSGCROC parameters are the following:

- Signal parameters to be measured: position, time, energy (amplitude).
- Hit rate per strip: up to 9×10^5 / s.
- Input signal charge: 2×10^5 e^- (32 fC) $\div$ 5×10^6 e^- (800 fC) (depending on the signals generated in the detector).
- X/Y coincidence window 2 ns + (EX = EY).
- Discriminator time accuracy: time walk < 2 ns,
- Variable gain in a range 1 $\div$ 20.
- The preamp-shaper circuits must handle both polarities of the input signal.
- The data must be buffered and derandomised on the ASIC.
- Zero suppression must be performed on the ASIC.

is this the full dynamic range or the end of scale for different gain settings?

The results for four different thresholds are shown in Figs 6—9. The discrimination threshold of the timing channel in the MSGCROC is controlled by an internal DAC (Digital-to-Analogue Converter) and is expressed in the DAC counts. The thresholds of 23, 40, 60 and 80 correspond to charges collected on single strip of 27 fC, 47 fC, 70 fC, and 94 fC, respectively. Based on cross calibration of the

what is the minimum threshold?



600
500
400
300
200
100
0
0
100
200
300
400
500
AnaOut [mV]
Q_{in} [fC]
x16
x8
x4
x2
x1
?

Noise level - simulation

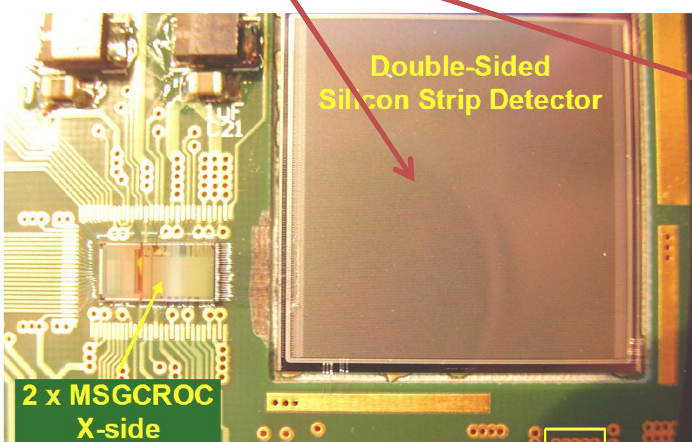
- Noise level for positive signals (33 fC) and C_D=23pF

Gain	×1	×2	×4	×8	×16
ENC_{FSH} [e^-]	4148	2248	1373	993	794
SNR_{FSH}	50	46	37	26	16
ENC_{SSH} [e^-]	3590	2164	1300	850	610
SNR_{SSH}	57	48	40	30	21

- Noise level for negative signals (33 fC) and C_D=23pF

Gain	×1	×2	×4	×8	×16
ENC_{FSH} [e^-]	5373	2815	1616	1089	857
SNR_{FSH}	38	37	32	24	15
ENC_{SSH} [e^-]	4365	2579	1485	918	625
SNR_{SSH}	47	40	35	28	21

C_D = ?



Noise - measured with Si detector

An average noise level for positive and negative signals for energy channel

Gain	ENC positive [e^-]	ENC negative [e^-]
x1	10984	10210
x2	6026	6073
x4	3458	3152
x8	1888	1579
x16	1126	837

Current Noise — detector capacitance

$$ENC^2 = i_n^{\,2} A_i \tau_S + \frac{S_w A_w (C_D + C_g)^2}{\tau_S} + S_f A_f (C_D + C_g)^2$$

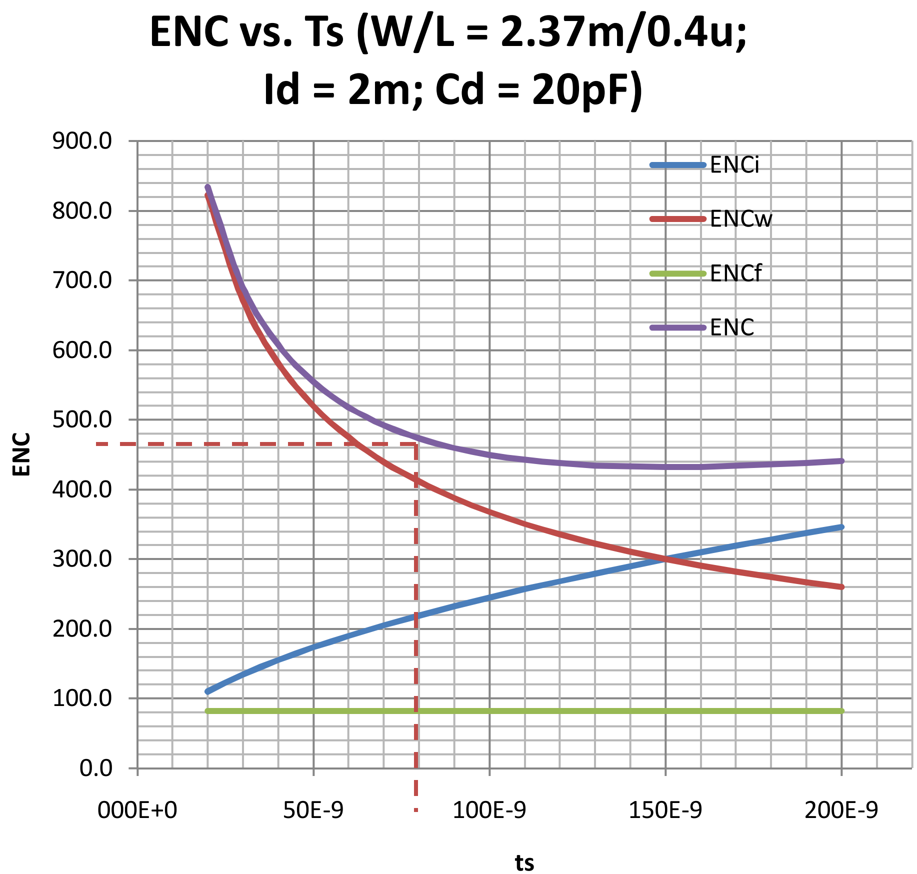
shaping time

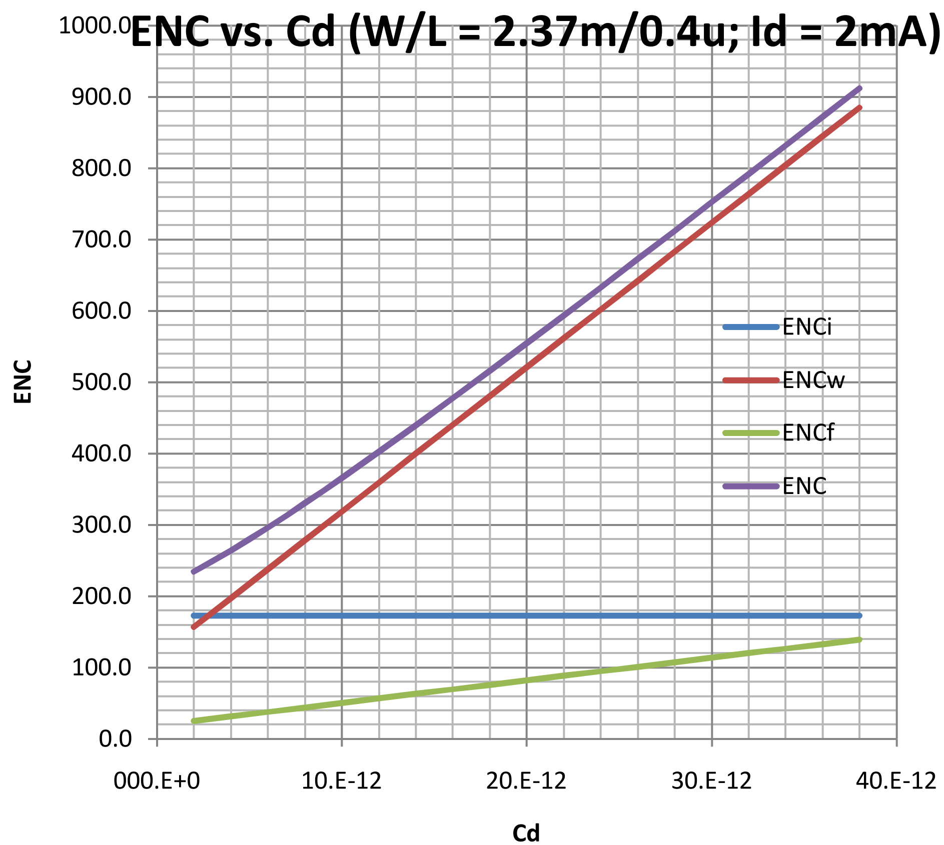
White Noise — 1/f Noise

$$S_w = \frac{8}{3}\frac{KT}{g_m}$$

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}$$

** TSMC 0.35um data from the web*





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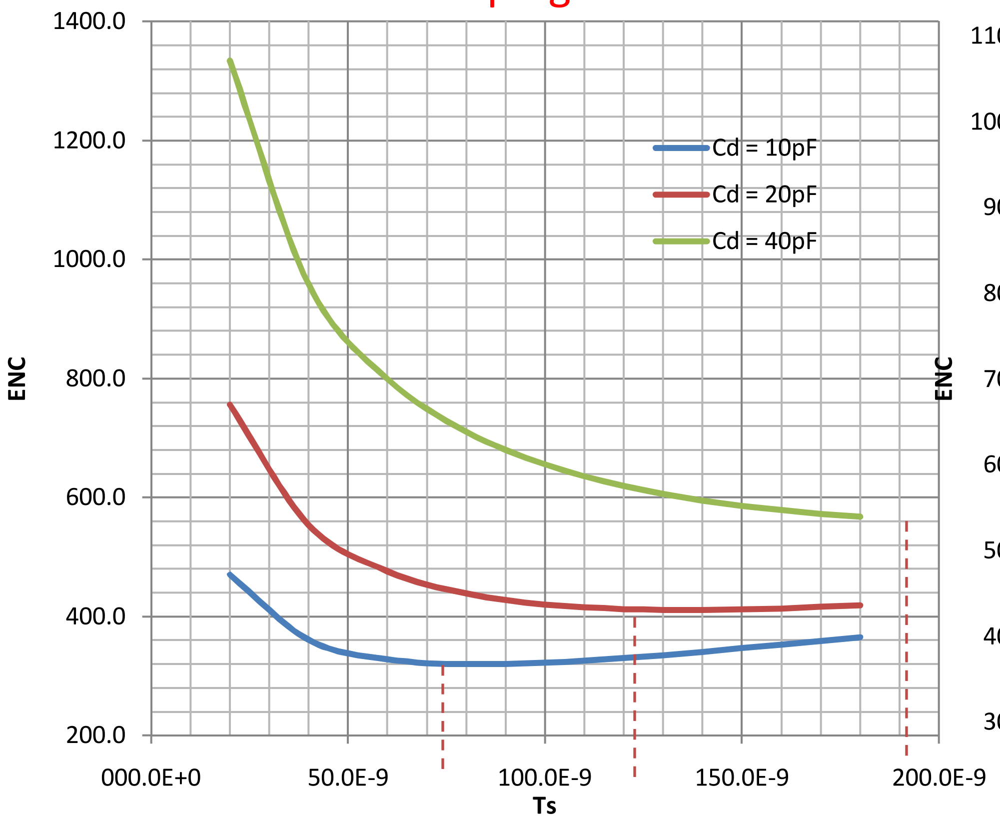
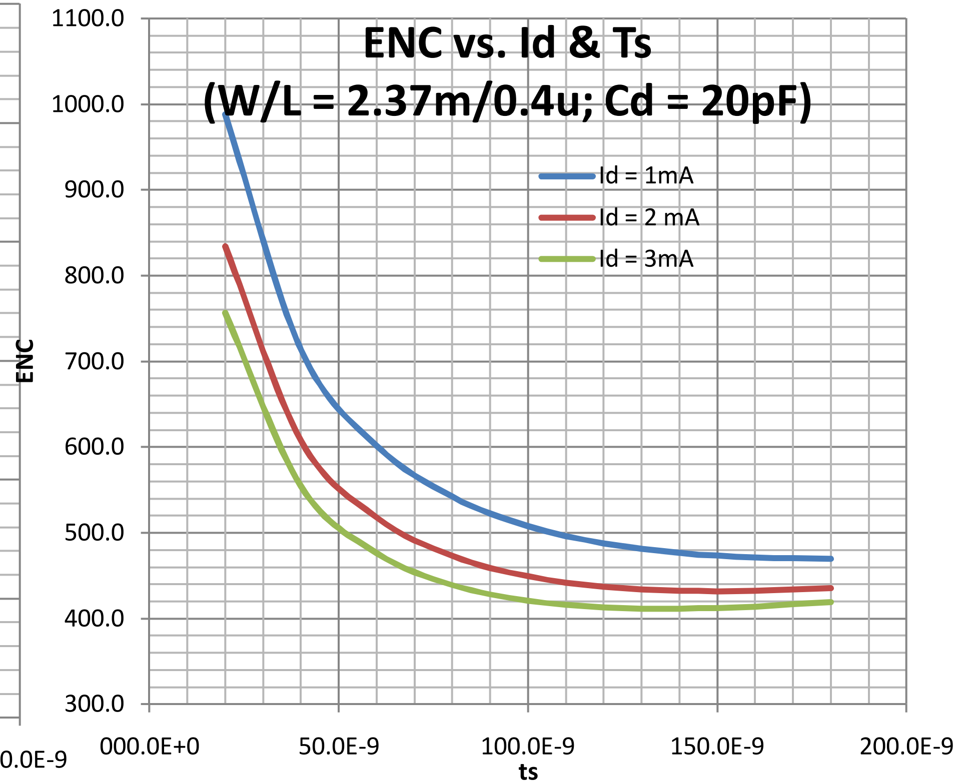
- variable shaping: 50 … 300 ns





Capacitive Matching

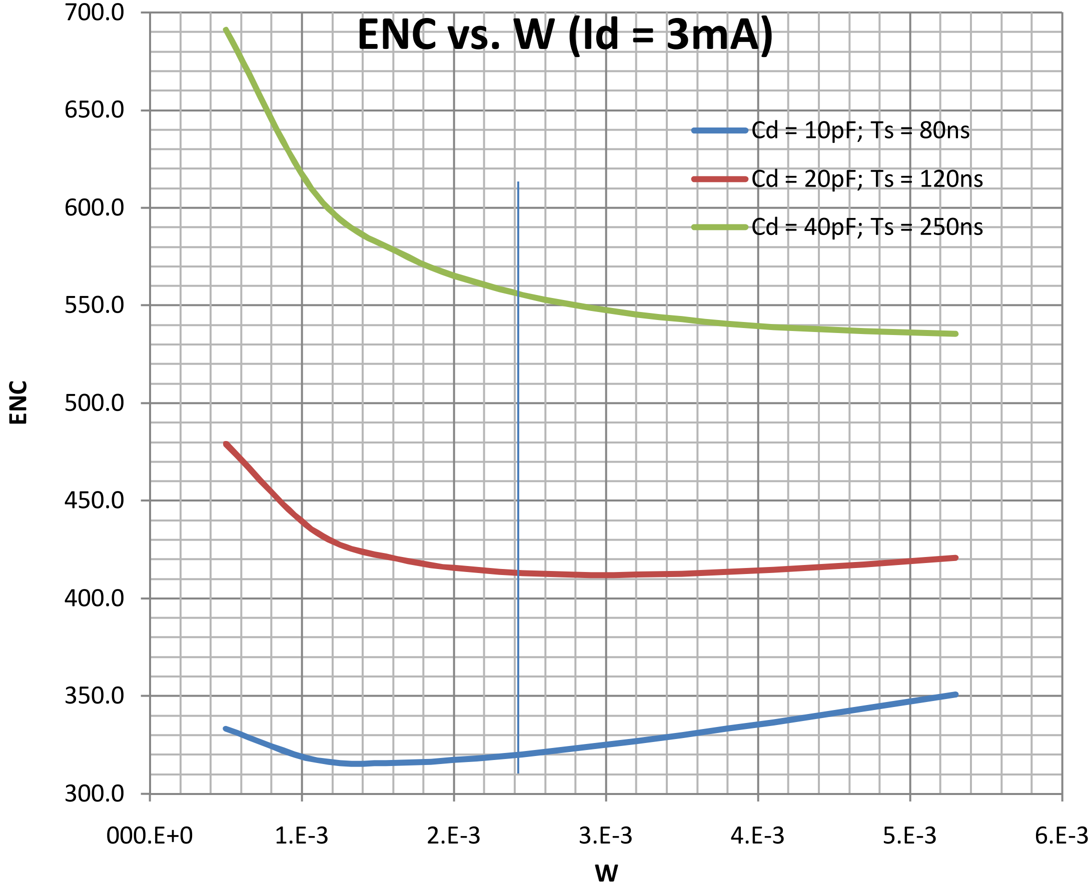
- 1/f noise dominant

$$ENC_{1/f}^{\ 2} = A_f K_f \frac{(C_D + C_g)^2}{C_g^{\ 2}} \quad \Rightarrow \quad C_g = C_D$$

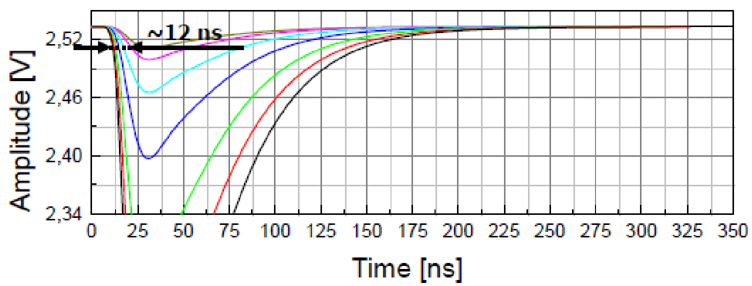
- white noise dominant

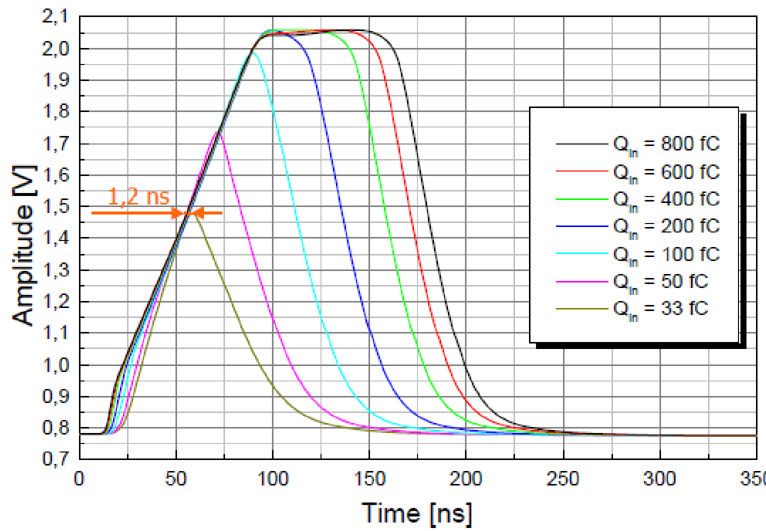
$$ENC_w^{\ 2} = \frac{8}{3} \frac{KTA_w}{\tau_S} \sqrt{\frac{L^2}{2\mu}} \frac{(C_D + C_g)^2}{\sqrt{C_g}} \quad \Rightarrow \quad C_g = C_D / 3$$

- No preamplifier can provide optimum noise performance for every detector


ENC vs. W (Id = 3mA)
Cd = 10pF; Ts = 80ns
Cd = 20pF; Ts = 120ns
Cd = 40pF; Ts = 250ns
700.0
650.0
600.0
550.0
500.0
450.0
400.0
350.0
300.0
ENC
000.E+0
1.E-3
2.E-3
3.E-3
4.E-3
5.E-3
6.E-3
W

Time Walk Compensation



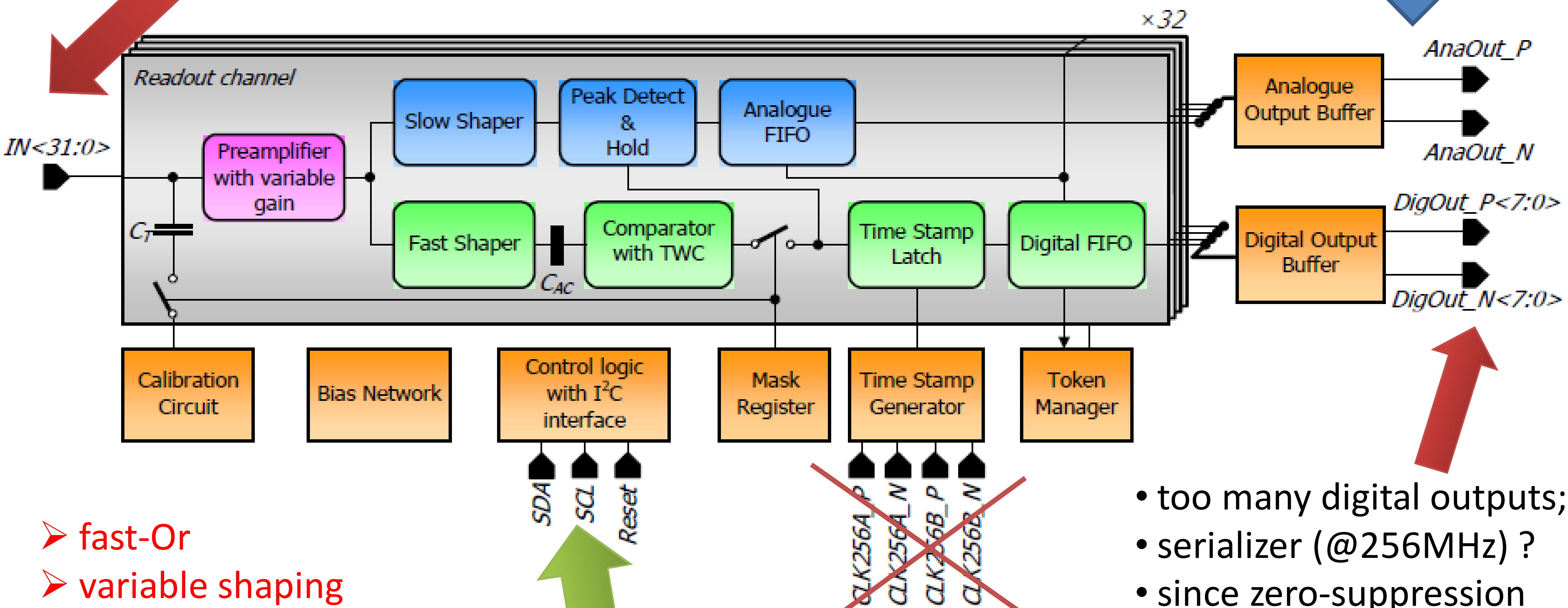


- Crossing of the same threshold level is relatively different in time for small and high signals
  - Gain x1
  - About 12 ns window
  - Compensated by TWC to 1.2 ns

How accurate is this across process variations?
Option: offline compensation using analog information ?

multiplexer for multiple chips?

32, 64, 128 channels? bonding/package?



- too many digital outputs;
- serializer (@256MHz) ?
- since zero-suppression comes natural with architecture, data bandwidth is probably low -> low speed serial

- ➢ fast-Or
- ➢ variable shaping

- ➢ reduce to minimum I/O count to DAQ
- ➢ multipurpose I/O lines (eg. trg(read) + rst + testpulse)

OK!

internal synthesizer?

Features

Chip matrix

Name	Exp	Det	#ch	Shaper (ns)	Noise	Range (fC)	Pol.	ADC	f (MHz)	P/ch. (mW)	Feat.	Tech	Rad hard
APV25	CMS	Si strip	128	50	270+38e/pF	20	both	A	40	2.7	PD, PR	0.25 CMOS	10
AFTER	T2K	TPC	72	100-2000 s-gauss	(350-1800) + (22-1.8)e/pF	19	both	A	1-50 (100)	7.5	VG,VS	0.35 CMOS	no
MSGCROC	DETNI	Gas strip	32	T: 25 E: 85	2000e @ 40pF	800	both	A,1	2ns TDC		VG, ZS	0.35 CMOS	no
Beetle	LHCb		128	25	500+50e/pF	17.5	both	A/1	40	5.2	F-OR	0.25 CMOS	40
VFAT	TOTEM		128	22	650+50e/pF	18.5 (cal)	both	1	40	4.47	F-OR	0.25 CMOS	50
NINO	ALICE	TPC	8	1	1900+165/pF	2000 th<100	both	1	async	30	BR	0.25 CMOS	no
CARIOCA	LHCb	MWPC	8	<15 @ 220pF	2000+40e/pF	250	both	1	async	46	BR	0.25 CMOS	20
PASA+ ALTRO	ALICE TPC	TPC	16	190_{fwhm} s-gauss	570e @20 pF	160	both	10	20	< 40	BC, TC, ZS	0.35,0.25 CMOS	
SVX4	CDF, D0	Si strip	128	100-360	410+45e/pF	60fC	neg	8	106 (212)	2	ZS	0.25 CMOS	20
SPIROC	ILC, T2K	SiPM	36	A:25-175 T: 10	A: 1/11pe; T:1/24pe	2000 pe	neg	8-12	100ps TDC	0.025 *pulse*	dual-gain	0.35 SiGe	no
Legend:	PD = peak detection, PR = pile-up rejection, VG = variable gain, VS = variable shaping, F-OR = fast-OR, BR = baseline restorer, BC = baseline correction, TC = tail correction, DC = data compression, ZS = zero suppression												

- ✓ fast-OR,
- ✓ variable gain,
- ✓ variable shaping,
- ✓ peak detection
- ✓ pile-up rejection,
- ✓ baseline restorer,
- ✓ baseline correction,
- ✓ tail correction,
- ✓ data compression,
- ✓ zero suppression

?