MSGCROC – an ASIC for High Count Rate Readout of Position Sensitive Microstrip Gas Chambers for Thermal Neutrons

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***Abstract*–In this paper we report on the development of an ASIC for readout of position sensitive neutron detectors based on low-pressure Micro-Strip Gas Chambers with solid composite ^{157}Gd/CsI converter. Global counting rates of 10^8 cps for a detector area of 25×25 cm^2 covered with 400×400 strips requiring 2 ns time resolution for coincidences of signals from X- and Y-strips set very demanding requirements for the ASIC performance.**

The MSGCROC ASIC employs a novel readout ASIC architecture, in which time stamps of timing signals are buffered in the digital form on channel basis. The X- and Y-signals are matched in an external FPGA-based circuitry according to their time stamps. In parallel with time measurements also signal amplitudes are measured and buffered on the chip. The signal amplitudes are used to discriminate between the signals from neutrons and from background X-rays, as well as to calculate centre of gravity for events with signals spread over 3 to 4 strips in case of MSGC detectors.

The preamplifier-shaper circuits in the MSGCROC can handle both polarities of the input signals so that it can be used for the cathode as and the anode readout. Furthermore, in other to cope with various gas amplification factors resulting in different input charges, a switchable gain stage has been implemented in the preamplifier with five relative gain steps from 1 to 20.

The readout of both buffers is performed via a token-ring based multiplexer, which ensures data sparsification and full zero suppression so that only non-zero data are transmitted to an external FPGA-based front-end board including fast ADCs. The analogue data is read out via a single differential link at a rate of 32 MHz. The digital data is read out via a parallel 8-bit LVDS bus at a rate of 128 MHz.

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I. Introduction

THE increasing intensity of neutron sources opens new research possibilities in investigations of physics and chemistry of solid-states and soft condensed matter, liquids and biological tissue [1]. However, in order to be able to exploit fully the research potential of these sources adequate detectors are required, which are suitable for 2-D imaging with high spatial resolution and can cope with high counting rates. During last two decades significant progress has been made in development of high resolution position sensitive detectors for high energy particle physics experiments and for synchrotron radiation instrumentation [2]. In comparison with the state-of-the-art detectors used in other fields the detectors employed in the neutron instruments are of rather low performance with respect to count rate and spatial resolution.

In the area of X-ray imaging and tracking detectors for particle physics experiments hybrid pixel detectors have been proven to provide excellent spatial resolution and high counting rate capability. This technology has also been demonstrated to be adequate for neutron detection after adding a proper neutron converter [3], [4]. There are, however, serious limitations when expanding this technique for large area detector. Besides pure technical issues that still need to be solved the high cost of such detectors is an important factor.

Double-sided silicon microstrip detectors in high spatial resolution applications and microstrip gas chambers offering nearly as good spatial resolution but larger areas were demonstrated only for low count rate applications so far. The application of double-sided silicon microstrip detectors to neutron detection has been demonstrated in the past too, but indeed for measuring low intensities of neutrons [5], [6]. It is worth noting that modern detectors have to be considered as highly integrated structures combining sensor technologies, like semiconductor pixel and microstrip detectors, Microstrip Gas Chambers (MSGC), Gas Electron Multipliers (GEM), and advanced microelectronics techniques. In many designs the technical challenges are transferred to the readout electronics.

Up to now the count rate limitations of two-dimensional position sensitive microstrip detectors, silicon detectors and MSGCs, have been due to the limited time resolution of the readout electronics, i.e. a minimum time window that defines the simultaneity of the signals from the two microstrip coordinates. Let us note that the intrinsic time resolution of the

detectors themselves, silicon microstrip detectors and microstrip gas chambers, is sufficiently high to increase the count rate capability of such detectors substantially, much beyond 10^4 cps per detector unit, which has been achieved so far [7]. The charge collection time in these detectors is of the order of 10 ns, which potentially offers time resolutions in a range of 1-2 ns or below for the very good signal to noise ratio achieved in the MSGC case, providing that one can use this intrinsic time resolution efficiently in the readout electronics.

In the Joint Research Activity DETNI (DETectors for Neutron Instrumentation) of the Integrated Infrastructure Initiative for Neutron Scattering and Muon Spectroscopy (NMI3) in the EU Research Framework Program FP6 we have developed an Application Specific Integrated Circuit MSGCROC for readout of two-dimensional position sensitive MSGC neutron detectors.

The detector is a low-pressure Micro-Strip Gas Chamber using solid converter technology based on ^{157}Gd combined with CsI [8]. The very demanding requirement concerning a global counting rate capability of 10^8 cps for a detector area of 25×25 cm^2 covered with 400×400 strips is about two orders of magnitude higher than reported before for 2-D strip detectors. These requirements translate to a 2 ns time resolution requirement for coincidences of signals from X- and Y-strips. Finding coincidences of raw timing signals in the matrix of 400×400 channels with such a resolution is not feasible. Therefore we have proposed and developed a novel readout ASIC architecture, in which time stamps of timing signals are buffered in digital form on channel basis. The X- and Y-signals are then matched in external FPGA-based circuitry according to their time stamps.

In the paper we present the design of the MSGCROC – a 32-channel ASIC for readout of MSGC detectors. The prototype ASIC has been manufactured in a 0.35 μm CMOS process. The basic functionality and parameterization of the ASIC have been confirmed by electrical testing using the testability functions implemented in the design. Prototype detector modules using the MSGCROC chips for readout, a double-sided silicon strip detector in one case and a prototype MSGC detector in another case, have been built and tested. The results of electrical performance tests of the prototype detector modules are presented and discussed in the paper.

II. REQUIREMENTS

The architecture and parameters of the readout electronics, including the MSGCROC ASIC, are driven by the design and requirements of the MSGC detector being developed. The detector concept and details of the detector design are described elsewhere [8]. Translating the detector parameters and requirements to the specification requirements for the MSGCROC ASIC one has to take into account the following points:

- The event rate capability should be 10^8 cps per readout plane. Given that each plane of the MSGC detector comprises 400 strips and one expects the charge to be collected on 3 to 4 strips on average for each event the expected average count rate per strip is 9×10^5 cps.
- In the MSGC detector we expect significant variation of the signal charges induced on the strips due to: (i) fluctuation of the number of secondary electrons emitted from the CsI layer, (ii) diffusion and division of avalanche charge between 3 to 4 strips, (iii) variation of the total gas amplification factor, which depends strongly on the detector bias. Taking into account all these factors we have assumed the input charge per strip to be in a range 2×10^5 e^- (32 fC) to 5×10^6 e^- (800 fC). In order to cope with the required dynamic range a stage with variable gain factor of 1 to 20 in the front-end circuit is required.
- Given the relatively large input signals from the MSGC detectors the noise may seem to be not critical as long as the total induced charge per event is considered. However, in order to achieve the required spatial resolution of the order of 100 μm for the detector strip pitch of 635 μm one has to estimate the centre of gravity for each event. This requires the signals to be measured with high signal-to-noise-ratio at 3 to 4 strips. Furthermore, low noise is required to limit the jitter of the time response. Combining all these requirements we have specified the Equivalent Noise Charge to be below 2000 e^- for a strip capacitance of up to 40 pF.
- In order to cope with the required count rate of up to 10^8 cps per detector plane the signals induced in the X- and Y-coordinate strips must be associated as simultaneous ones within a coincidence time window of 2 ns. Further improvement of the coincidence efficiency can be obtained by requesting that the energy of the clusters in the X-strip and Y-strips is equal for a given event.
- The ASIC must deliver for each strip the time and amplitude (charge) information. Thus, the front-end circuitry should be optimized with respect to time resolution as well as amplitude resolution.
- In order to achieve a 2 ns coincidence window the time response of the front-end circuit must be sufficiently fast. The corresponding parameters for the discriminator are: time walk < 2 ns and time jitter < 2 ns FWHM.
- Taking into account the timing requirements only, one would aim at fastest possible shaping in the front-end circuit. A lower limit of the shaping time is due to the duration time of the induced signals, which is in a range 5 to 10 ns in the developed MSGC detector. Another limitation on the bandwidth of the front-end circuit to be taken into account is the power dissipation, which has to be kept within a few mW per channel to be able to cool the ASICs efficiently.
- Concerning optimum signal-to-noise ratio for amplitude measurements one can follow standard optimization procedures of the shaping time constant taking into account the voltage and current noise sources at the input and the detector capacitance. However, for the expected

count rate per strip the shaping time constant has to be sufficiently short to avoid pile-up effects, which would deteriorate amplitude measurements.

- Since the signals induced in the planes with orthogonal strips are of different polarities the front-end circuit must be capable of handling both polarities in order to avoid the development and manufacturing of two different ASICs.
- Given the detector strip pitch of 635 µm it will not be practical to match the channel pitch of the ASIC to the strip pitch. Instead, a modularity of 32 channels per ASIC with the input pads of 100 µm pitch has been chosen as a practical solution.
- The time and amplitude data from 32 channels should be multiplexed and transmitted off the ASIC through a limited number of links.
- In order to adjust the bandwidth of the data links to the average count rate per ASIC instead to the maximum one the data must be buffered and derandomized in the ASIC.
- Furthermore, zero suppression must be performed in the ASIC.

III. ASIC Design

A functional block diagram of one channel of the MSGCROC ASIC is shown in Fig. 1. Since the ASIC must deliver time and energy information for each event we have used a classical approach with each readout channel split into a timing and an energy channel. The timing channel is equipped with a discriminator. The discriminator output signal is used to latch a 14-bit time stamp of 2 ns resolution and to enable the Peak Detect and Hold (PDH) circuit in the energy channel.

The signal amplitude from the PDH circuit and the time stamp are stored in an analogue and a digital derandomizing buffer respectively. Each buffer contains only four cells, which is sufficient to keep the data losses due to buffer overflows below 10% for maximum expected courting rates.

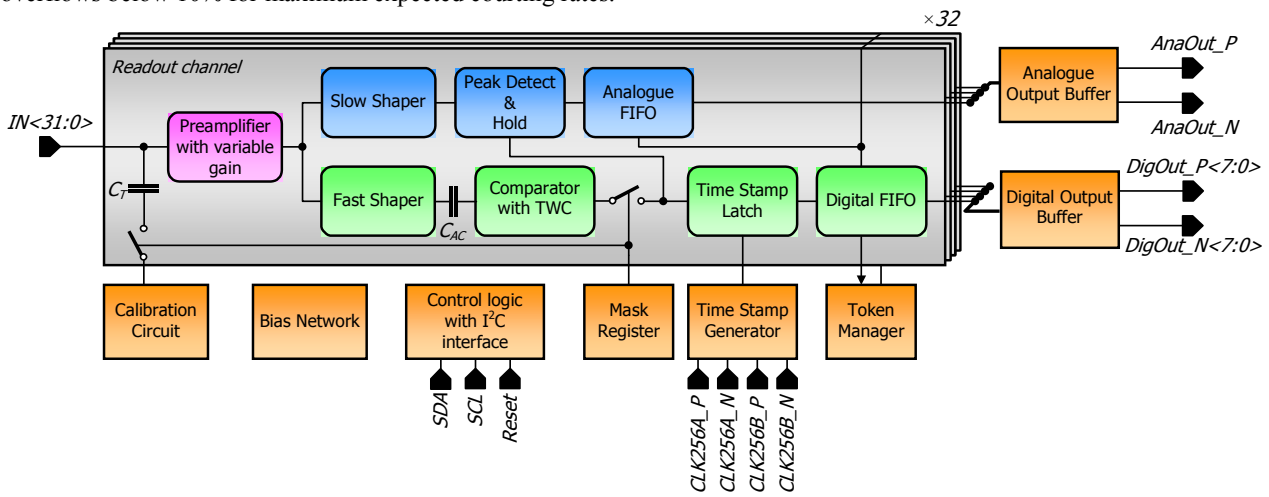

Fig. 1. A functional block diagram of the MSGCROC ASIC.

The transresitance gain for each network is set by the resistor in the feedback network while the capacitances are adjusted such that the pulse shapes are identical for all feedback networks. It is worth noting that for large gains and

The readout of each buffers is performed via a token-ring based multiplexer. In this readout scheme when the token signal moves across the channels it skips the channels with no data. Thus the effective depth of the buffer available for derandomizing the data is 32 channels times 4 cells in each channel. The analogue data is read out via a single differential link at a rate of 32 MHz. The digital data is read out via a parallel 8-bit LVDS bus at a rate of 128 MHz. The internal programmable bias circuits, including a number of DACs, configuration and test circuits are controlled via an I^2C interface.

A. Preamplifier

The input stage is a transimpedance amplifier built around a fast folded cascode amplifier with a bridged-T low pass filter in the feedback loop. The dimensions and the bias current of the input transistor have been optimized taking into the required peaking time of 25 ns and the detector capacitance of 40 pF. The short-channel noise coefficients as a function of the gate length and bias current have been evaluated earlier for test transistors manufactured in the same process as used for this design [9]. Based on these results we have selected for the input device a PMOS transistor of dimensions W = 2368 µm and L = 0.4 µm. The bias current of the input transistor is controlled by an internal DAC and can be adjusted within a range from 1 to 3 mA.

The preamplifier delivers fast pulses with short tails to minimize the pile-up effects. A schematic diagram that illustrates the implementation of the switchable gain in this stage is shown in Fig. 2. Variable gain is implemented in the preamplifier stage by selecting one of five feedback networks. The relative gain factors for the five feedback networks are: ×1, ×2, ×4, ×8, and ×16.

so large feedback resistors the time constants are affected significantly by the stray capacitances associated with the resistors as well as with the connecting traces. Therefore final adjustment of the parameters of the feedback networks has been performed running post-layout simulations taking into account parasitic capacitances extracted from the layout.

The preamplifier is also equipped with a switchable inverter stage so that it delivers signals of the same polarity for either polarity of the input charge.

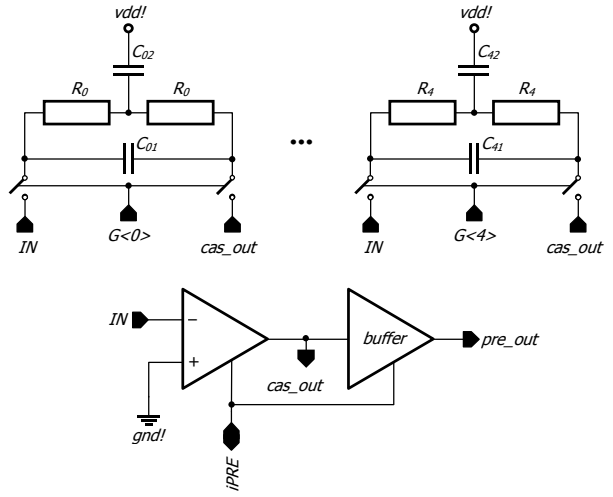

Fig. 2. Schematic diagram of the preamplifier with folded cascode core and switched bridged-T low-pass filter feedback.

B. Timing channel

The timing channel consists of a fast shaper, which delivers signals with a peaking time of 25 ns and a comparator with a Time Walk Compensation circuit (TWC). The TWC circuit is based on the concept described in [10]. The comparator delivers the timing signal and the trigger signal to the PDH circuit in the energy channel. Thus, the detection efficiency and noise rate depend on the discrimination threshold.

Since a common threshold voltage is applied to all channels, the channel-to-channel offset spread is a very critical parameter. In order to compensate possible channel-to-channel threshold offsets, each comparator is equipped with a 5-bit trimming Digital-to-Analog Converter (DAC), which allows correcting the threshold offset on the channel basis with a precision better than 1 LSB in the threshold DAC common for all channels.

The effectiveness of the trimming procedure for a threshold set to 116 fC is illustrated in Fig. 3. The trimming procedure is performed in two steps. For a given value of the calibration signal, corresponding to the target value of the threshold, a threshold scan is performed for each of the 32 values of the trimming DAC (Fig. 3, upper plot – scans for channels #0, #4, #8, #12, #16, #20, #24 and #28). On this basis trimming DACs are set to values that ensure response of all channels for chosen target value of the threshold DAC (Fig. 3, lower plot). For the eight channels shown the peak-to-peak offset spread before trimming is about 10 LSB and is reduced to 1 LSB after trimming. One can notice that best matching of the threshold is obtained for the target value. Applying the same trimming factors to other input charges results in somewhat worse matching since in addition to the offset of each channel the effective discrimination threshold is also affected by the gain of that channel, which also varies across the channels.

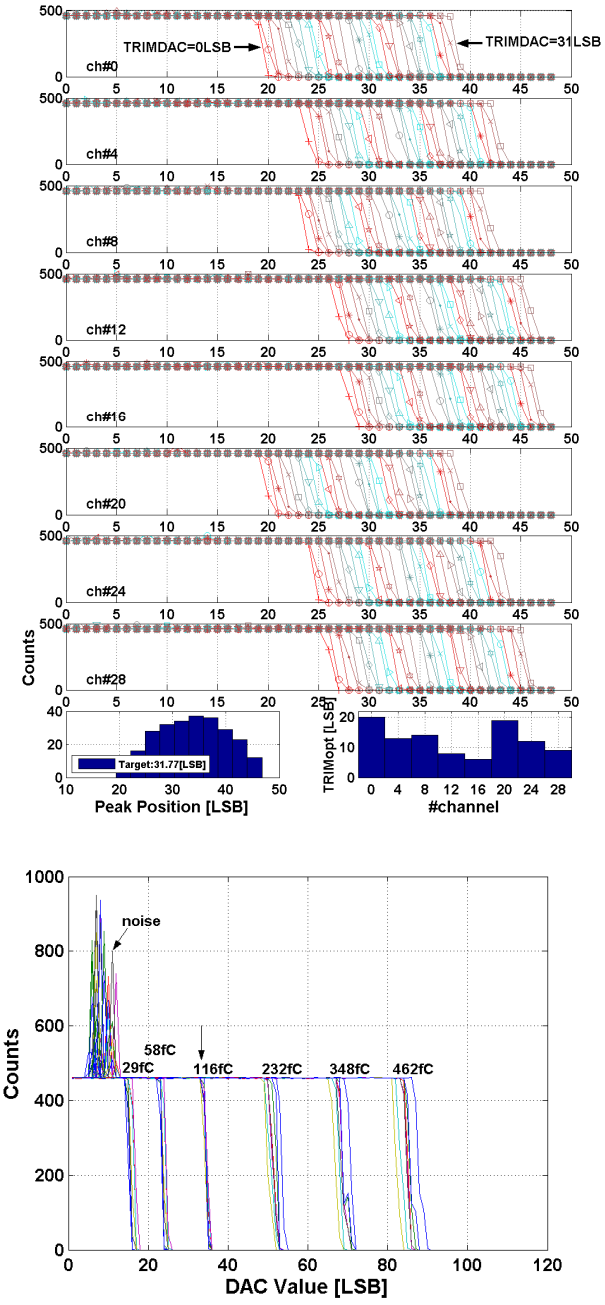

Fig. 3. Illustration of the procedure of adjusting discriminator offsets to a common value for all 32 channels.

C. Energy channel

The energy channel comprises a slow shaper (with a peaking time T_p = 85 ns) and a classical peak detector and hold circuit (PDH) [11], which detects the peaks of incoming

pulses and holds their values for a given time period triggered by the comparator in the fast timing channel. The shaping function of the slow channel is optimized taking into account the requirements concerning noise (energy resolution), count rate, dynamic range and speed limitations of the peak detector.

The response curves of the full energy channel, including the PDH circuit, analogue memory and analogue multiplexer, for different preamplifier gain settings are shown in Fig. 4. The measured relative gain factors are: ×1, ×1.7, ×3.6, ×7.8 and ×19.7. They differ slightly from the nominal values, however, the exact values of the gain factors are not critical as long as the different settings cover the full range of expected input signals.

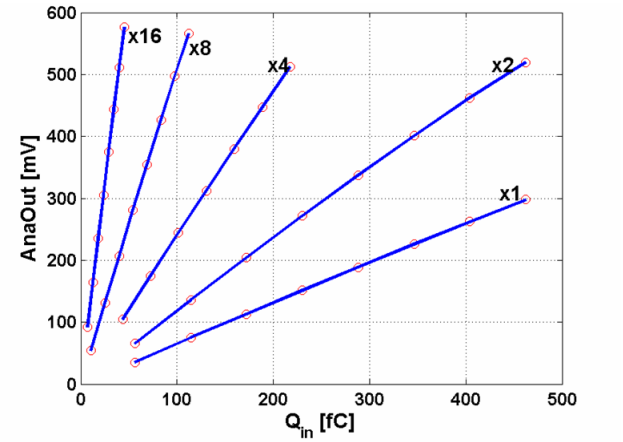

Fig. 4. Response curves of the complete energy channel for different setting of the gain.

D. Time stamp generation

The principle and the block diagram of the time stamp generation circuit are shown in Fig. 5. The 14-bit time stamp signature is composed of a 12-bit Gray-encoded counter (TS<13:2>), a toggle flip-flop (TS<1>) and the buffered input clock (TS<0>). The correct timing of bits TS<1> and TS<0> is obtained by adjusting the delays appropriately through the programmable delay buffers #0 ÷ #2. Precise adjusting of the delays is critical to ensure that all 14 bits are Gray encoded. In this scheme we can achieve 1 ns resolution at the clock frequency 256 MHz.

E. Physical design

The MSGCROC ASIC has been designed and manufactured in the 0.35um CMOS process with four metal layers and high resistivity polysilicon resistors from Austria Microsystems. The dimensions of the ASIC are 3.2×6.7 mm^2. Figure 6 shows the microphotograph of the MSGCROC.

A critical aspect of the MSGCROC design, which has been analyzed carefully at the level of physical mask design, is the cross coupling between the analogue and the digital blocks. In order to minimize the crosstalk special attention has been paid to proper isolation between the analogue and the digital parts. Separate power supply busses and bonding pads for each part have been implemented. The analogue and digital blocks are enclosed in guard rings connected to separate bonding pads. It should also be noted that in the digital part we have used standard cells with the bulk connection separated from the lower (digital) power supply.

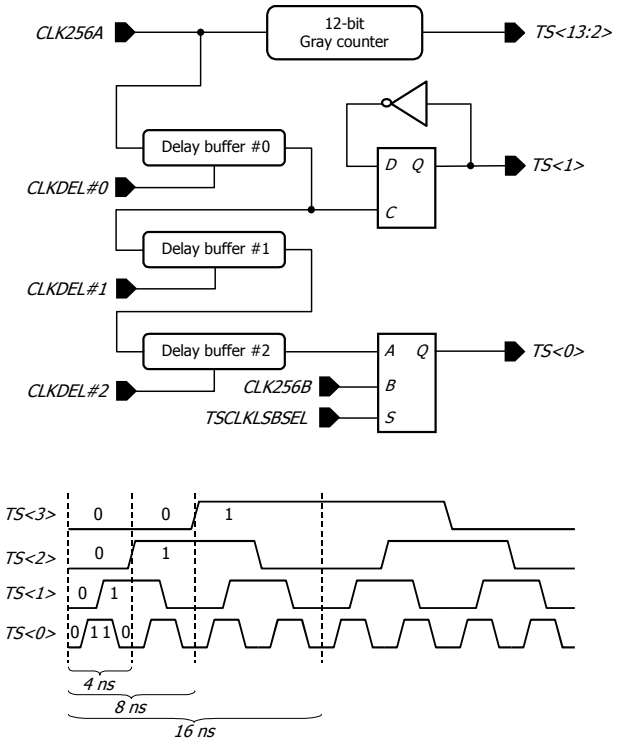

Fig. 5. Schematic diagram and illustration of principle of operation of the time stamp generation circuit.

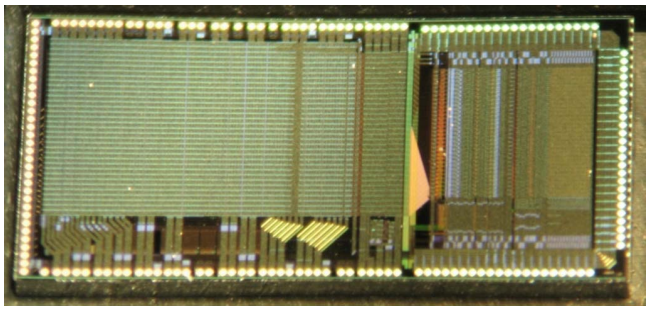

Fig. 6. Photo of the MSGCROC ASIC

IV. Measurement Results

The test bench for evaluation of the ASIC performance is based on a double-sided silicon microstrip detector of 300 µm thickness and 50 µm strip pitch. The detector and the ASICs are mounted on a PCB as shown in Fig. 7. One 32-channel MSGCROC per side is connected to the detector and every second strip of the detector is wire bonded to the ASIC because the pitch of the input pads on the ASIC is 100 µm. The ASICs are read out with a custom designed data acquisition board, which has been adapted to the structure of the output data and the readout protocol of the MSGCROC. The available data acquisition board can deliver a clock signal of 256 MHz.

The basic functionality of the prototype ASIC has been tested using electronic signals delivered by the internal calibration system. Although the MSGCROC has been designed for large input charges from the MSGC detector, setting up the highest gain (x16) in the preamplifier stage allows us to measure also lower charges from a silicon strip detector.

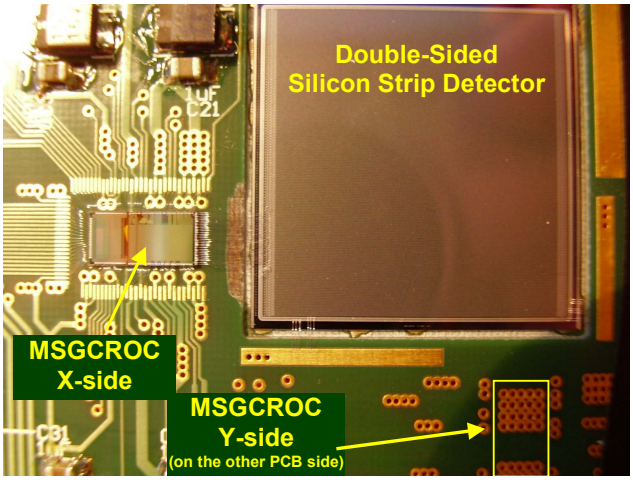

Fig. 7. MSGCROC evaluation board with a double-sided silicon strip detector.

A. Timing measurements

A histogram of time coincidences between signals from two MSGCROC ASICs connected to X and Y channels is shown in Fig. 8. As expected for the clock frequency of 256 MHz, the majority of events are confined within a single bin of 1 ns. The plot confirms that the time jitter is well below 2 ns FWHM, as expected for a relatively low input capacitance represented by the silicon strip detector. We observe some tails in the distribution, which are most likely due to errors caused in the preliminary data acquisition system used for the test by the clock skew and clock jitter.

B. Energy measurements

The single strip amplitude distributions of electrons from a ^{90}Sr source and of γ-rays from an ^{241}Am source measured with the silicon strip detector are shown in Fig. 10. The measurements have been performed in the typical operation mode of the MSGCROC. The analogue signals have been read out at the end of the entire energy channel, i.e. preamplifier, slow shaper, PDH circuit triggered by the signal from the timing channel, analogue memory and analogue output multiplexer.

For electrons one expects a Landau distribution and for γ-rays a Gaussian distribution. Let us note that the measured distributions are affected by two effects: (i) because of charge sharing between neighboring strips one would expect tails extending towards lower energies, (ii) because the measured signals are just above the noise level in the timing channels the lower parts of the distributions, especially for the γ-rays are cut off at the discrimination level.

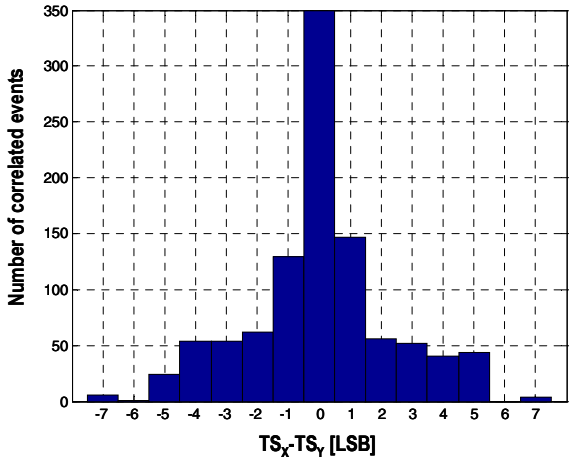

Fig. 8. The histogram of Time Stamp coincidence between X- and Y-strips demonstrates the coincidence resolution of 1 ns as expected for the clock frequency of 256 MHz.

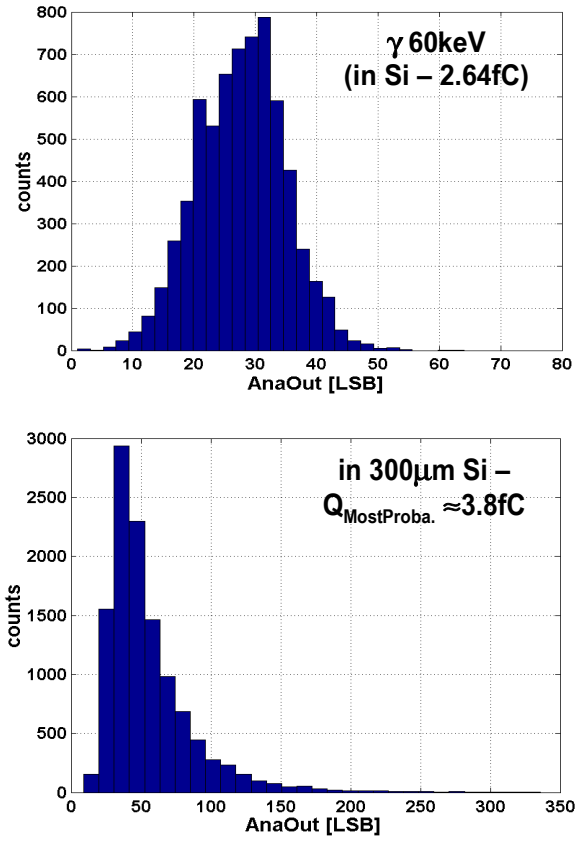

Fig. 9. Amplitude distributions of γ-rays from a ^{241}Am source (upper plot) and electrons from a ^{90}Sr source (lower plot) measured with the silicon strip detector.

C. Laser measurements

In order to demonstrate capability of 2-D imaging with the MSGCROC ASICs we have measured a laser beam using the double-sided silicon strip module. Figure 10 shows a picture obtained with a focused pulsed light beam. The wavelength of

the laser was 1060 nm. The figure shows the image of the beam obtained by taking measurements at five different threshold and finding off-line time coincidences of signals at X- and Y-strips. We see that the light spot is spread over nine pixels and no spurious hits are recorded.

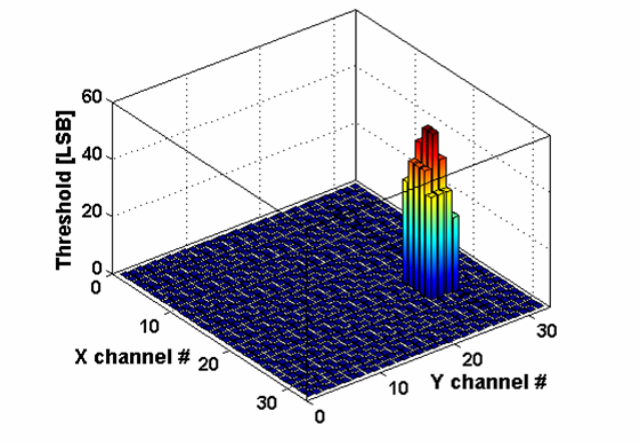

Fig. 10. A 3-D histogram of Time Stamp coincidence between X and Y strips by the five threshold values for a laser measurement.

V. Conclusions

Future high intensity pulsed neutron sources will require novel detectors with higher counting rate capability and high time and position resolution. A 32-channel MSGCROC ASIC with complete functionality required for the readout of 2-D position sensitive MSGC detectors with composite ^{157}Gd/CsI converter has been designed and manufactured. The performed electrical tests of the MSGCROC as well as the measurements performed with the test bench module based on a double-sided silicon strip detector have confirmed correct functionality of all building blocks.

The developed MSGCROC ASIC is a first experimental proof of the novel method of readout of 2-D strip detectors. Employing such a readout architecture one can overcome the major counting rate limitation of the 2-D strip detectors. This opens new possibilities of applications of either 2-D position sensitive MSGC detectors or double-sided silicon microstrip detectors to imaging with high counting rates of up to 10^8 cps per detector module. Thus, the 2-D position sensitive strip detectors can be competitive with the pixel detectors in many imaging applications. The 2-D strip detector technologies offer further advantages with respect to: large detector area of single detector module, no coverage of the sensor area with the electronic chips, simpler assembly techniques and lower cost.

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