Performance of thin planar sensors irradiated to a fluence of 10^{16} n_{eq}/cm^2 and development of a new interconnection technology for the upgrade of the ATLAS pixel system

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Munich

- Thin Planar Pixel Sensors
  - Sensor thinning technology at MPI HLL
  - Results of the first thin n-in-p sensor production
- SLID Interconnection
- Through Silicon Vias

In collaboration with Fraunhofer EMFT

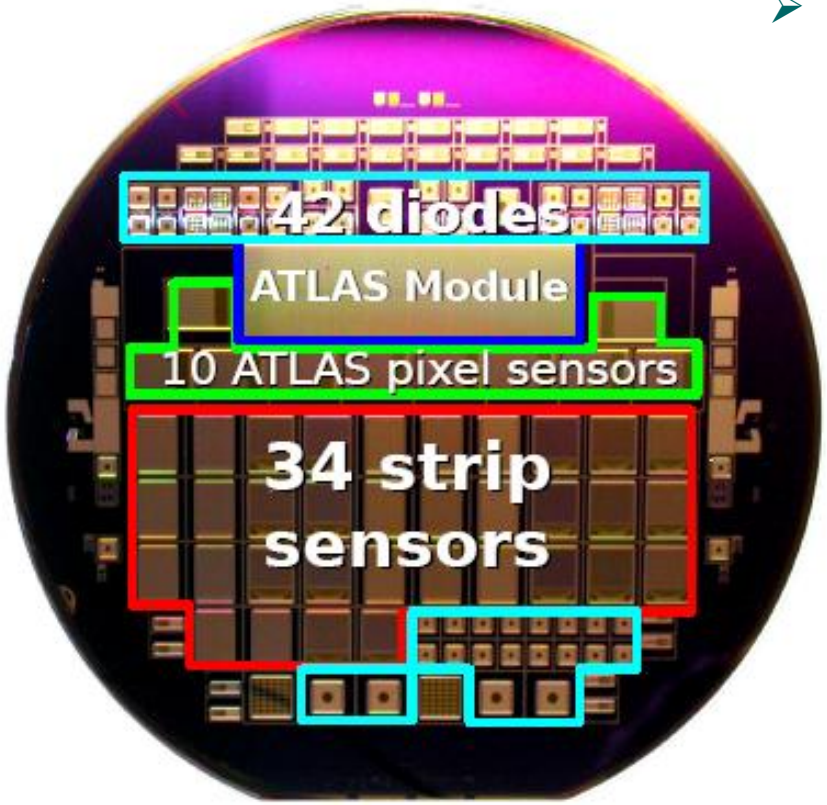
Pixel 2010 Conference, 6 – 10 September 2010, Grindelwald (CH)

Thin planar pixel sensors

First thin planar pixel production at MPP-HLL

Motivations:

- At the same voltage thin (= over depleted) detectors have a higher electric field than thick (= partially depleted) detectors → better CCE
- They contribute to keep the material budget low, which is extremely important in the inner layers to maintain a good tracking performance.

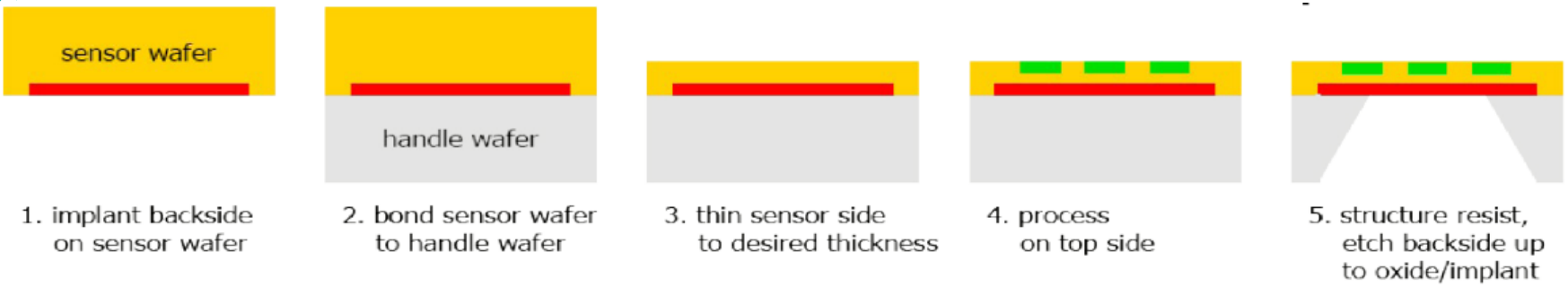


Aim: evaluate suitability as sensors for ATLAS IBL + SLHC Upgrade

Production characteristics:

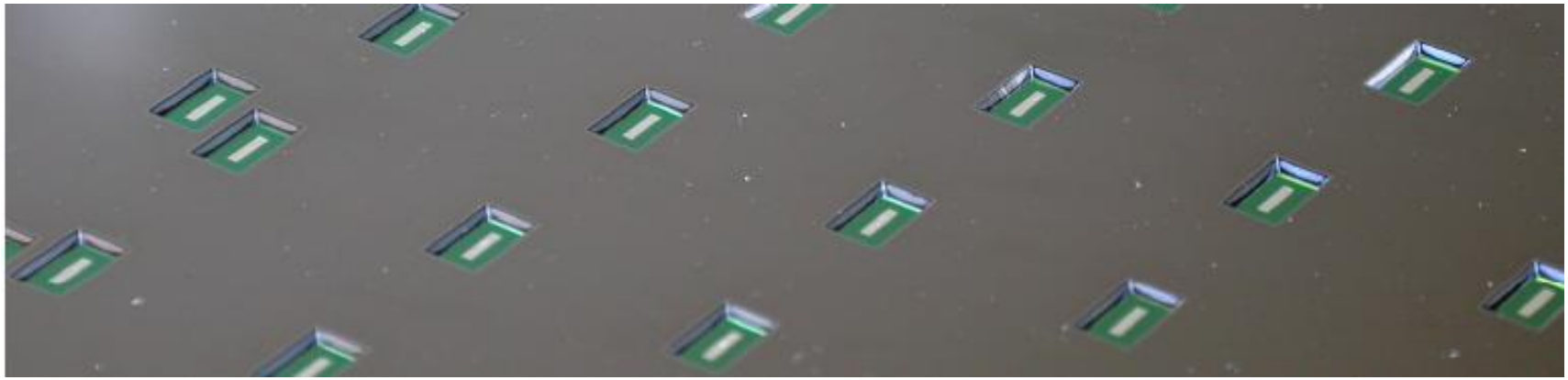
- Different bulk materials: 4 n-in-n and 8 n-in-p 6“ wafers.
- Different active thicknesses: 75µm and 150µm.
- Different isolation methods: homogenous p-spray and moderated p-spray, with two different implantation parameters each.
- Pixel sensors compatible with the ATLAS FE-I3 chip
- Various strip sensors with different isolation geometries.

Sensor thinning technology at MPP-HLL



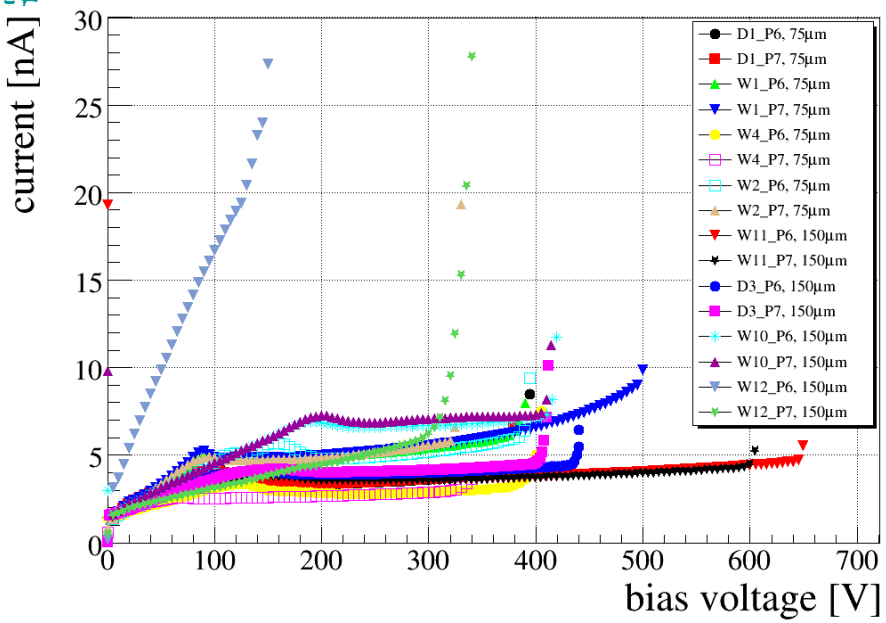
- For the n-in-p wafers the process completed up to step #4. The handle wafer will be used as a support also during the ASIC interconnection phase.

- n-in-n wafers need a window etched through the handle wafer to access the patterned p+ implantation on the backside. Dicing (still to be performed) is needed for a thorough electrical characterization.



View of the back-side of a n-in-n wafer, with the window etched through the handle wafer

Characterization of the n-in-p wafers

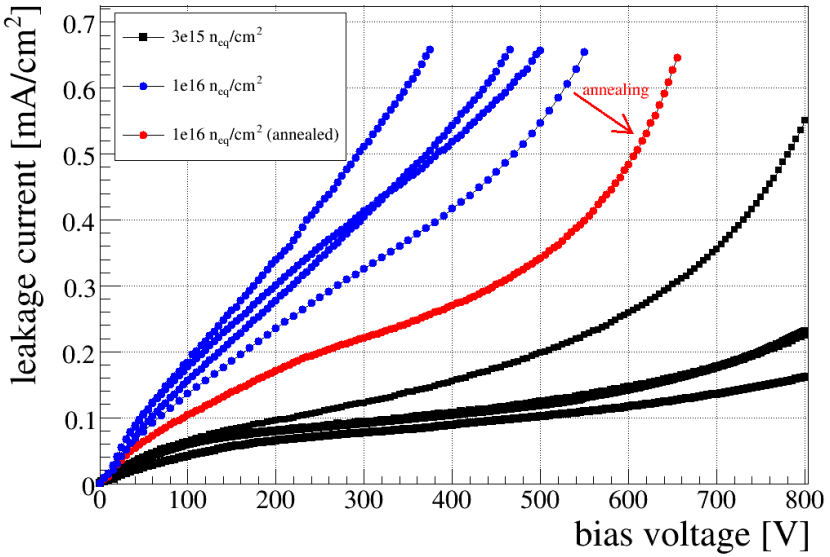


- Characterization completed:
  - Excellent device yield (79/80)
  - Low currents (~10 nA /cm^2)
  - Good breakdown behaviour (V_{bd} >>V_{fd})

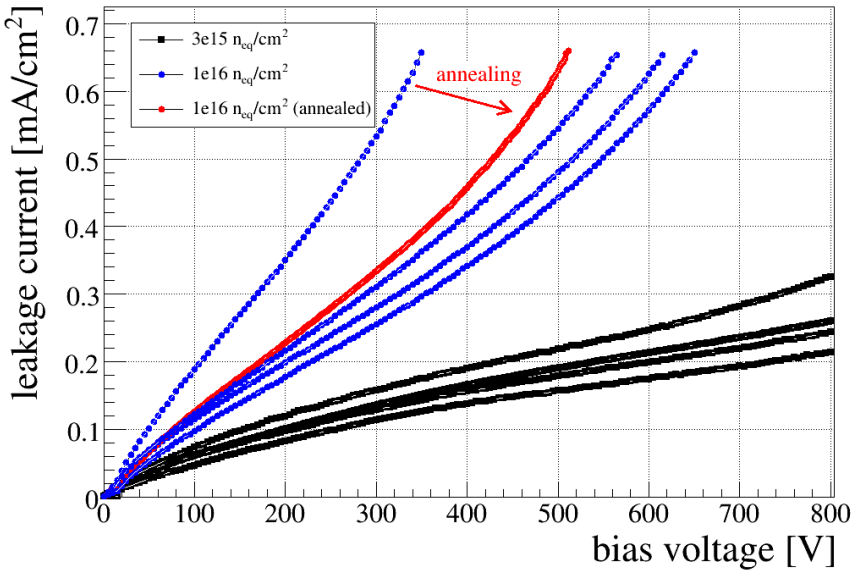
L. Andricek et al., doi:10.1016/j.nima.2010.04.087

- Diodes, micro-strips and pixels of the n-in-p wafers have been irradiated in Karlsruhe with 26 MeV protons up to a fluence of 10^{16} n_{eq}/cm^2

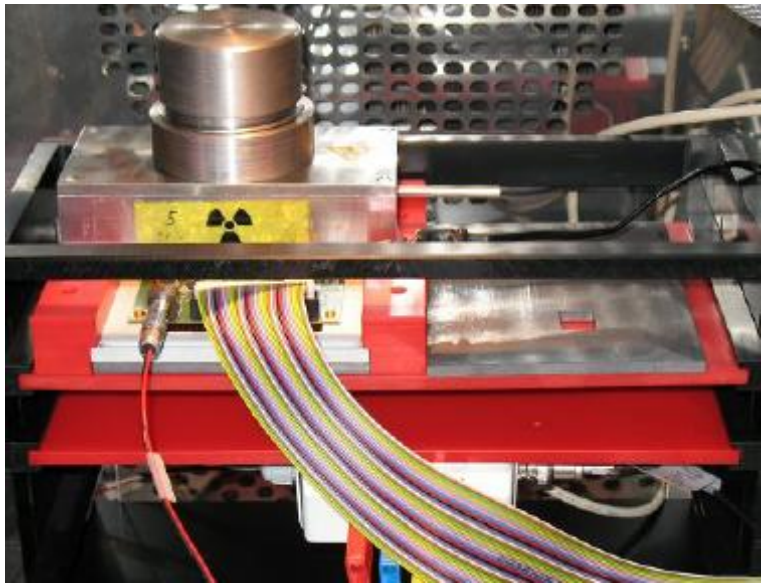
75 µm thick, IV @ T= -10°C



150 µm thick, IV @ T= -10°C



CCE Measurements (I)

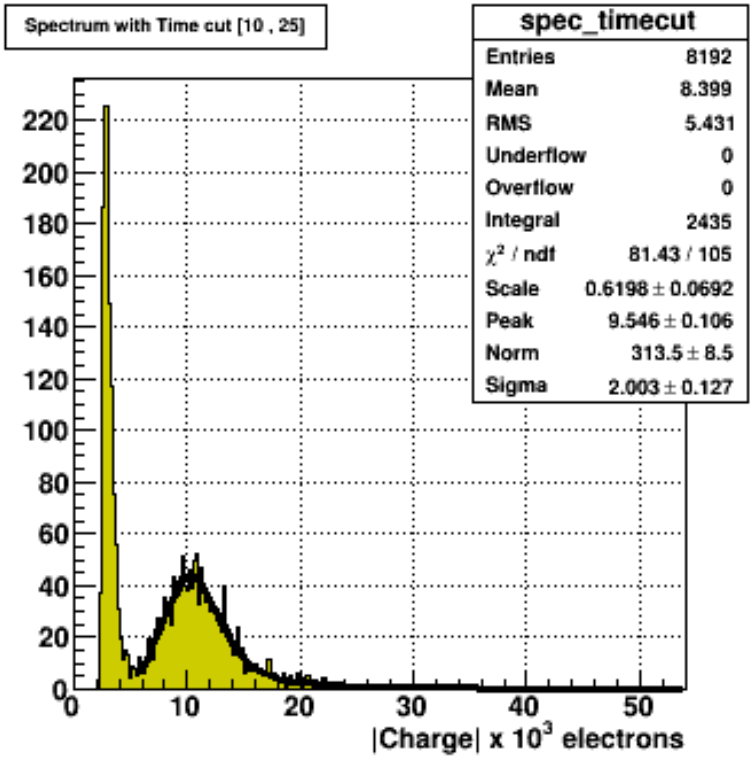


➢CCE measurements on irradiated n-in-p strips, from the same production,are on-going with the ALIBAVA system.

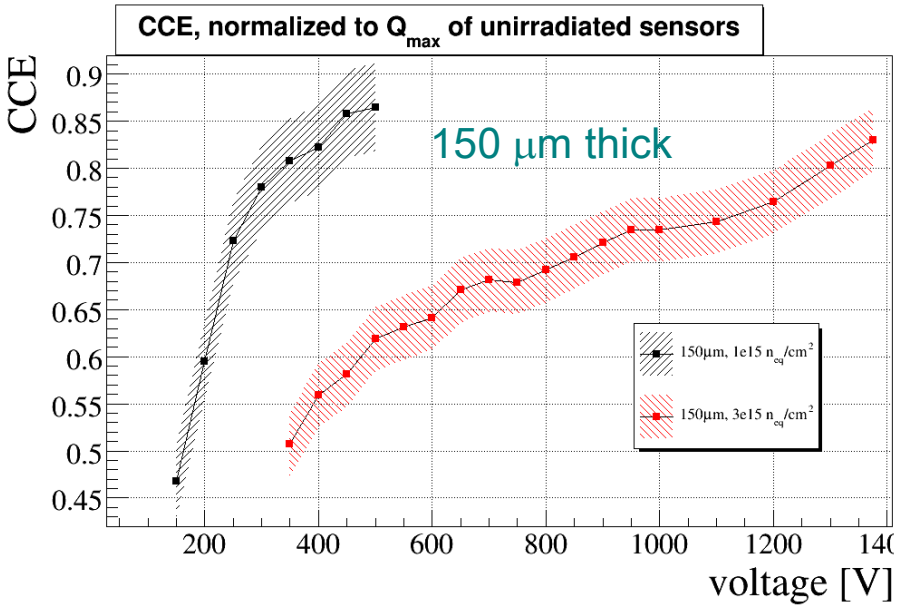
➢ The strip sensors used in these measurements have the same structure as the pixels (punch-through biasing, DC coupling) with the exception of the length (~ 7 mm)

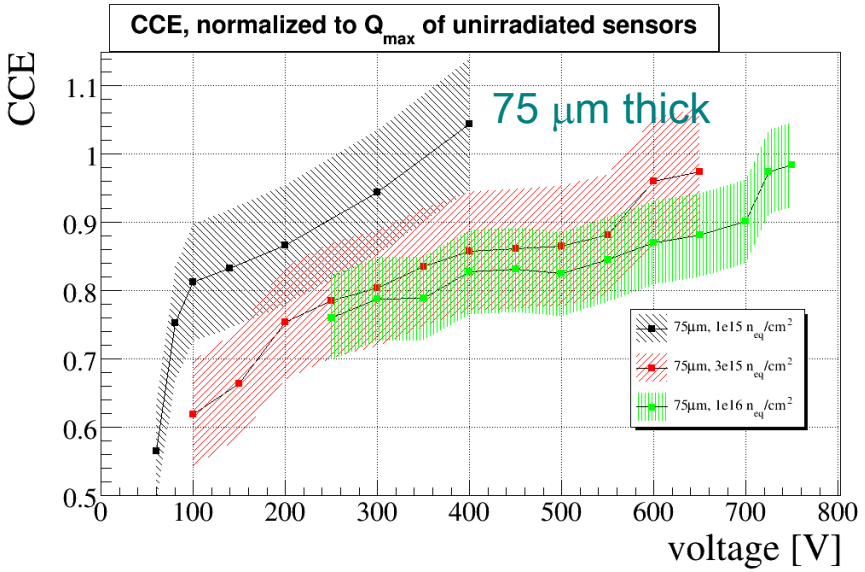
➢ CCE measurements on pixels are only possible after SLID interconnection of sensor and FE-I3 (in preparation, see next slides).

150 μm thick, Φ=3E15 n_{eq} /cm^2, V_{bias}=650 V



CCE Measurements (II)





- Measurements performed at T=-30°C for Φ=1x10^{15} n_{eq}/cm^2
  T=-(40-46)°C for Φ=(3-10)x10^{15} n_{eq}/cm^2
- The error bands correspond to 500 e^- uncertainty estimated on each measured point.
- For the 150 μm thick sensors a higher voltage is required to recover the pre-irradiation charge with respect to the 75 μm thick sensors.
- Charge multiplication can explain these CCE results, see M. Beimforde Ph.D. thesis
  http://publications.mppmu.mpg.de/2010/MPP-2010-115/FullText.pdf
- Further measurements at Φ=10^{16} n_{eq}/cm^2 are presently ongoing

Vertical integration technology

Beyond IBL: 3D Technology for the ATLAS Pixel Upgrade

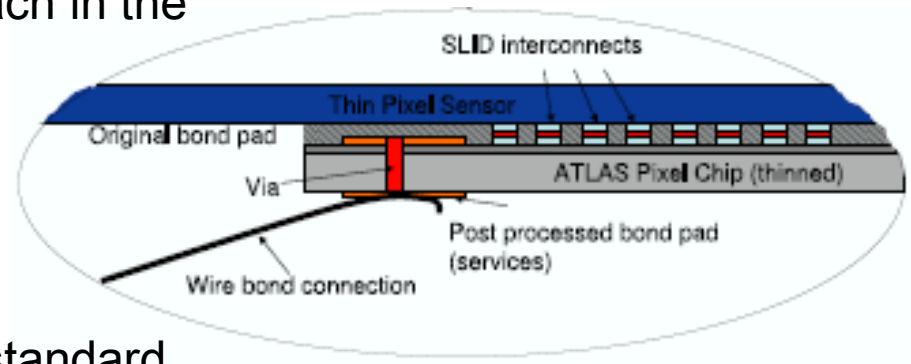
➢ The ATLAS FE-I4 chip profits from technology shrinking (250 nm → 130 nm) to achieve finer granularity (50x400 μm^2 → 50x250 μm^2).

Talk by M. Barbero,"FE-I4 Chip Development for Upgraded ATLAS Pixel Detector at LHC"

➢ Another step ahead can be provided by vertical integration technology:

- Multi-tier ASIC → functionalities splitting → further reduction in pixel size
- Thin sensors and ASIC → material budget reduction
- 4-side buttable ASIC → larger active area

➢ 3D prototypes versions of the FE-I4 chips are in production with the "Via First" approach in the MPW Chartered-Tezzaron run.

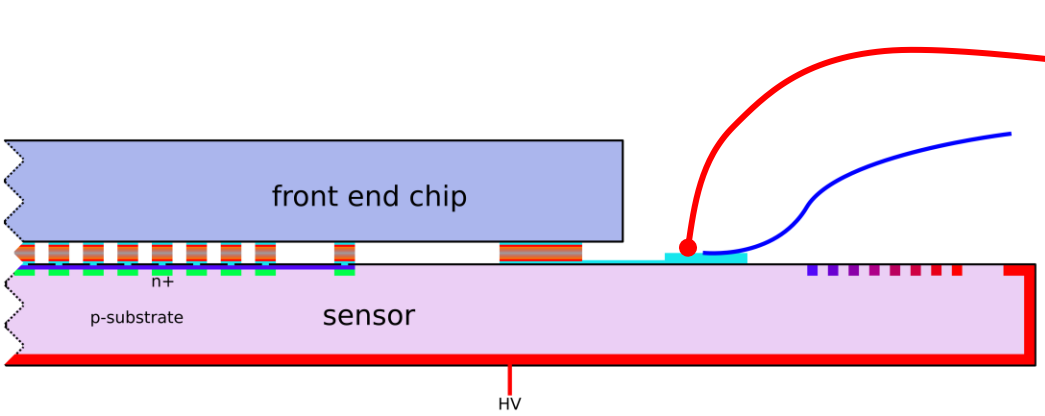


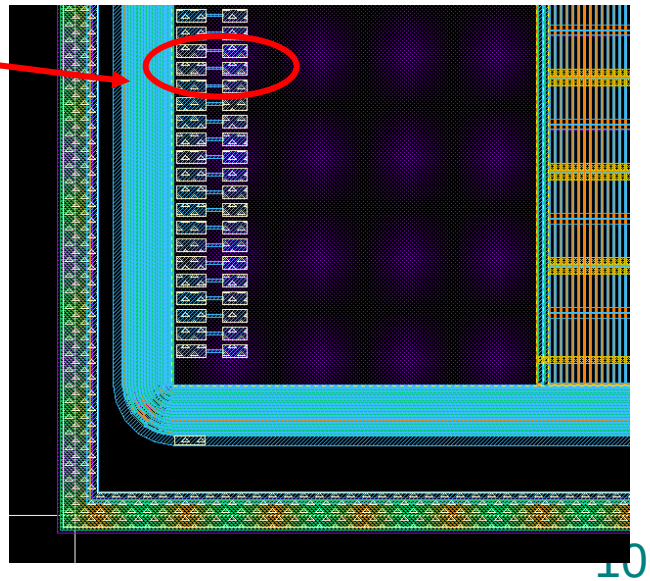
➢ MPP activity is mainly focused on:
- interconnection sensor-FE
- demonstration of post-processing of standard ASICs with "Via Last" approach

MPP 3D R&D Program: demonstrator module

- Step I:
  - FE-I3 ASIC thinned to 200 μm
  - thin sensors / ASIC interconnection using SLID
  - No TSV, integrated fan-out on sensor for service connection

- Step II:
  - TSV etched in the read-out chip on the front-side on every wire bonding pad to route signal and services to the ASIC backside
  - FE-I3 ASIC thinned to 50 μm
  - thin sensors /ASIC interconnection using SLID





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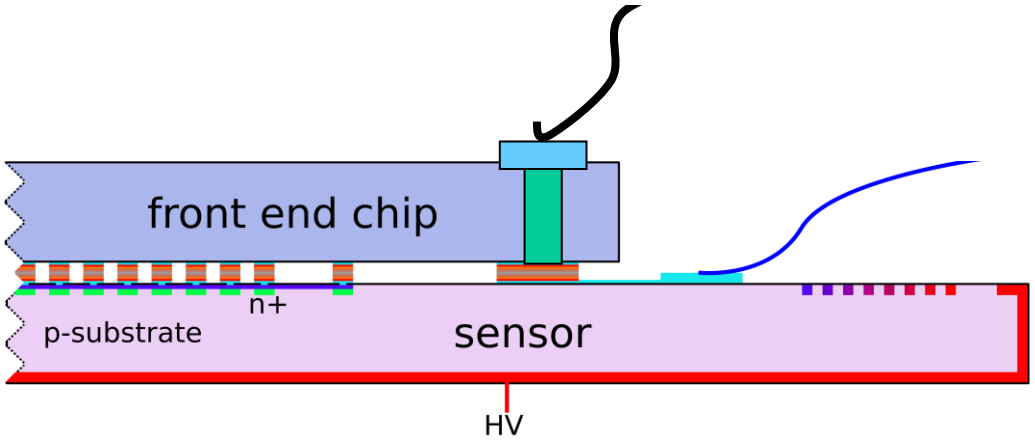
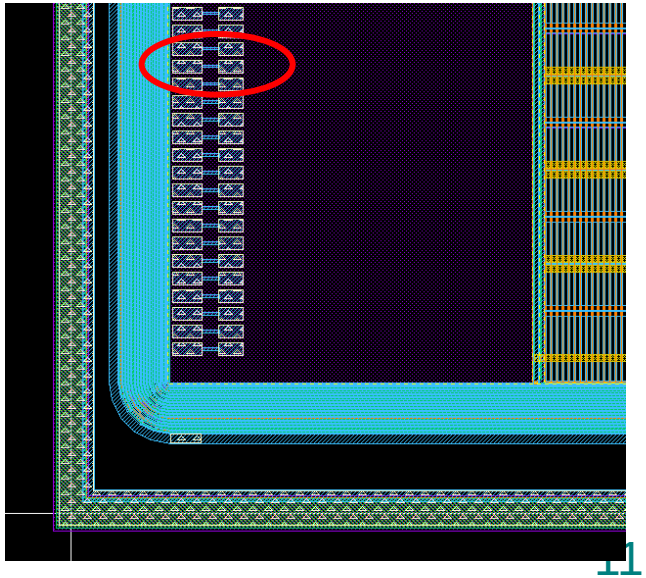
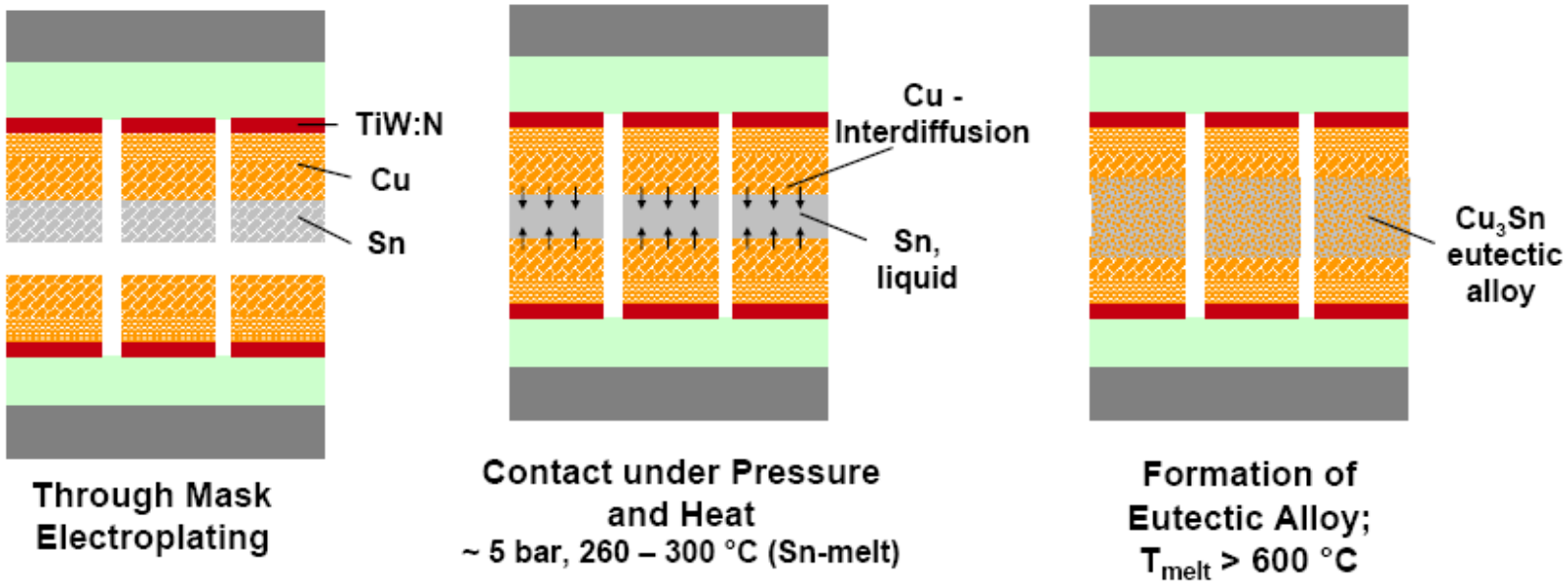




EMFT SLID Process

Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps “lower cost” (EMFT)).
- Small pitch possible (~ 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

- However: no rework possible.

Fraunhofer EMFT

EMFT SLID Process

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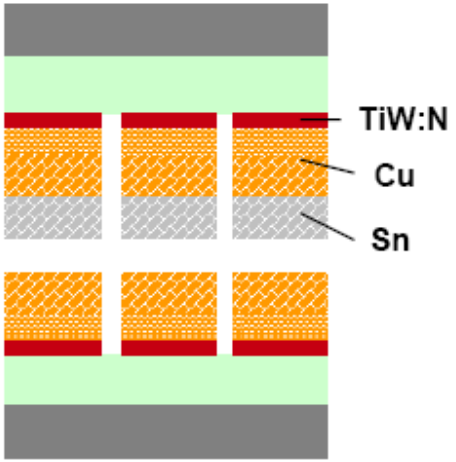
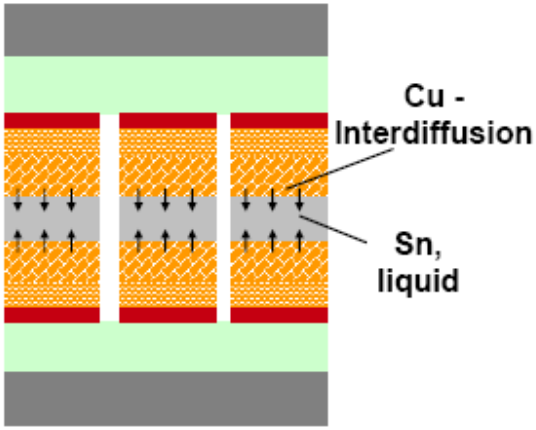
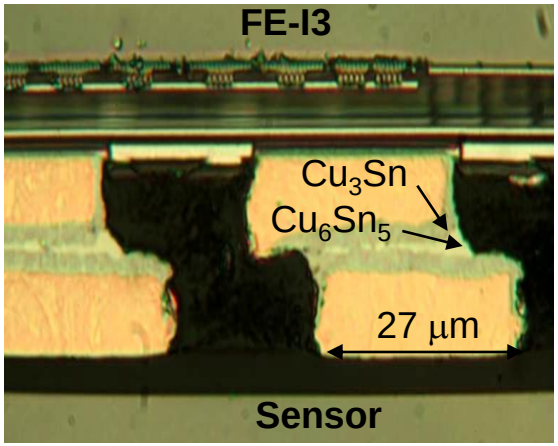


Through Mask Electroplating



Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)



Formation of Eutectic Alloy;
T_{melt} > 600 °C

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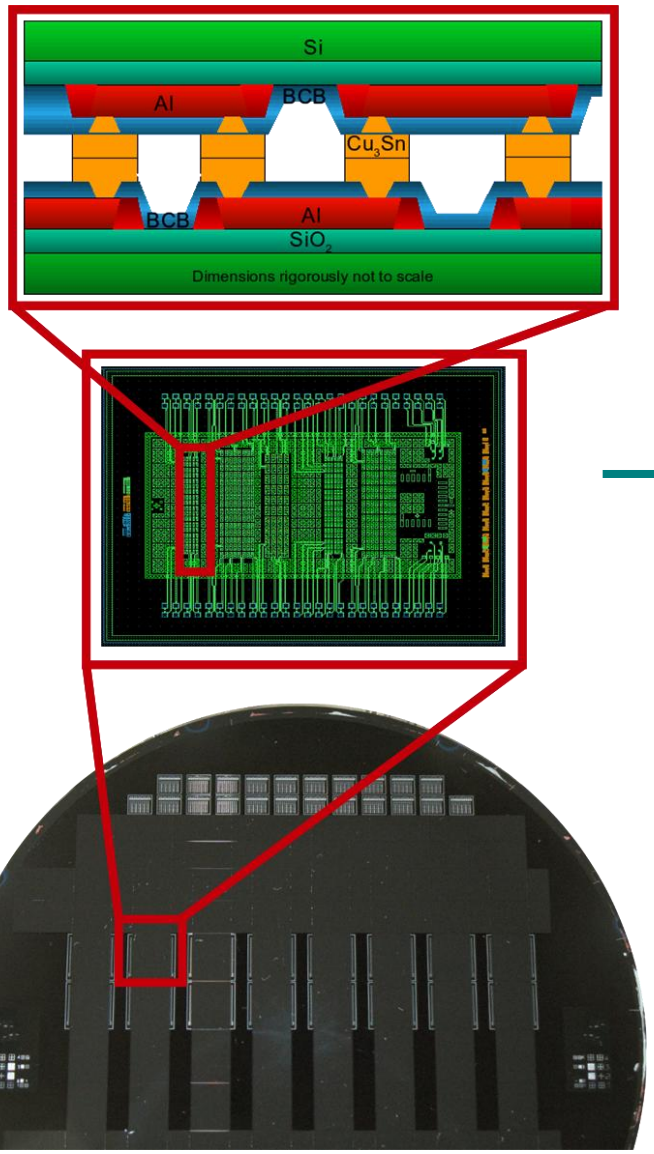
Fraunhofer EMFT

Daisy chains: wafer-to-wafer SLID



➢ SLID efficiencies measured with daisy chains structures (wafer to wafer connections):

Pad width [μm²]	Pitch [μm]	Aplanarity	SLID Inefficiency
30x30	60	0	$<1.2\times10^{-4}$
80x80	115	0	$<8.9\times10^{-4}$
80x80	100	0	$<7.8\times10^{-4}$
27x60	50,400	0	$(5\pm1)\times10^{-4}$
30x30	60	100 nm	$(10\pm4)\times10^{-4}$
30x30	60	1 μm	$(4\pm3)\times10^{-4}$

A. Macchiolo et al. “Application of a new interconnection technology for the ATLAS pixel upgrade at SLHC“

http://cdsweb.cern.ch/record/1234896/files/p216.pdf

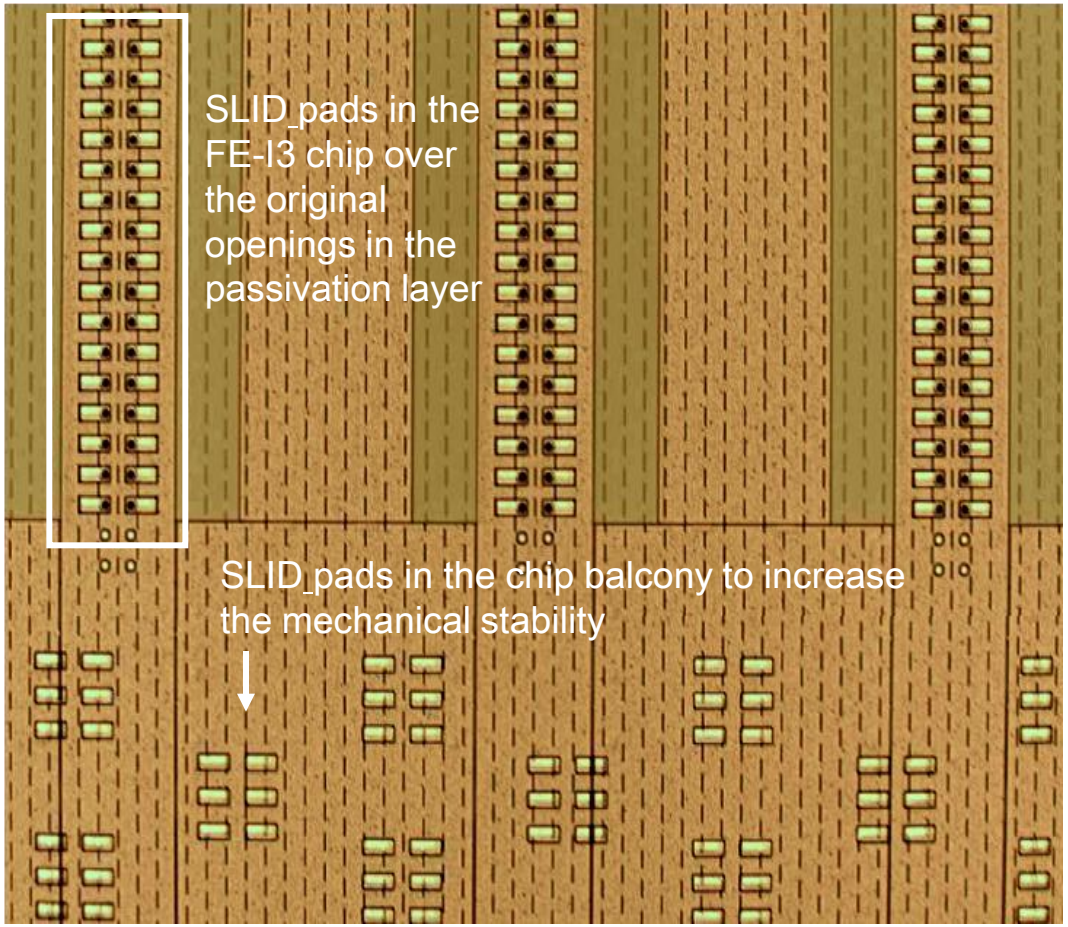
- “Chip to wafer” interconnection with the daisy chain structures resulted in a chip placement precision on the handle wafer not accurate enough (chips of different sizes, stemming from different wafers).

Interconnection of FE-I3 pixels

Sensor-ASIC interconnection is achieved with a “chip to wafer” approach:

- 4 n-in-p sensor wafers (6”) with pixels sensors FE-I3 compatible have been left undiced.
- Electroplating to create the SLID pads has been performed at the wafer level both on sensors and chips

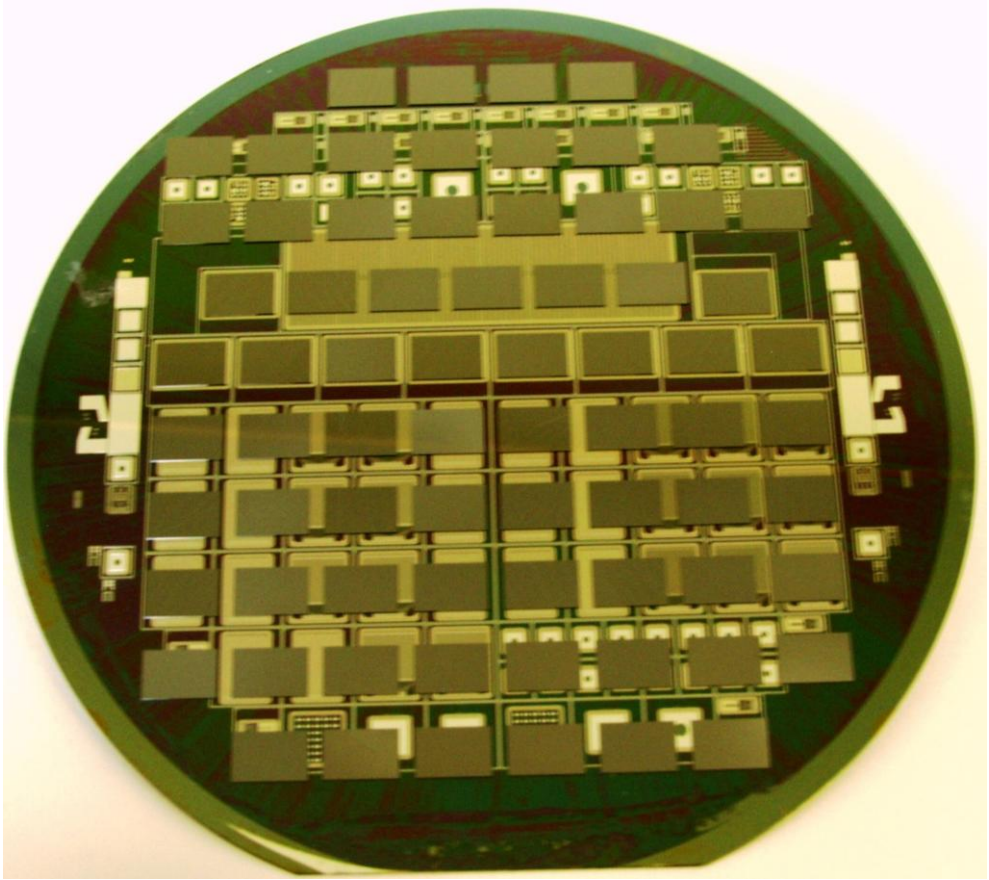
FE-I3 chips after electroplating of the SLID pads



- SLID pads of 27x60 μm^2: determination of optimal SLID pad placement and size based on results of daisy chain production.

Step I: FE-I3 interconnection without TSV

- After electroplating, FE-I3 chips are singularized and reconfigured on a 6” handle wafer. This is removed after the interconnection to the sensor wafer.
- First assembly, composed by a dummy sensor wafer and real FE-I3 chips, is ready. Used to verify the alignment precision of the chips in the handle wafer and the mechanical stability of the SLID connection
- Alignment accuracy in x and y directions of the hot chips in the handle wafer < 12 μm.
  Still some concerns about the measured tilting angle
  (α_{mean} =0.08°, one sample up to 0.34°)



Dummy sensor wafer (only Aluminum deposited) with the connected FE-I3 chips after release of the handle wafer

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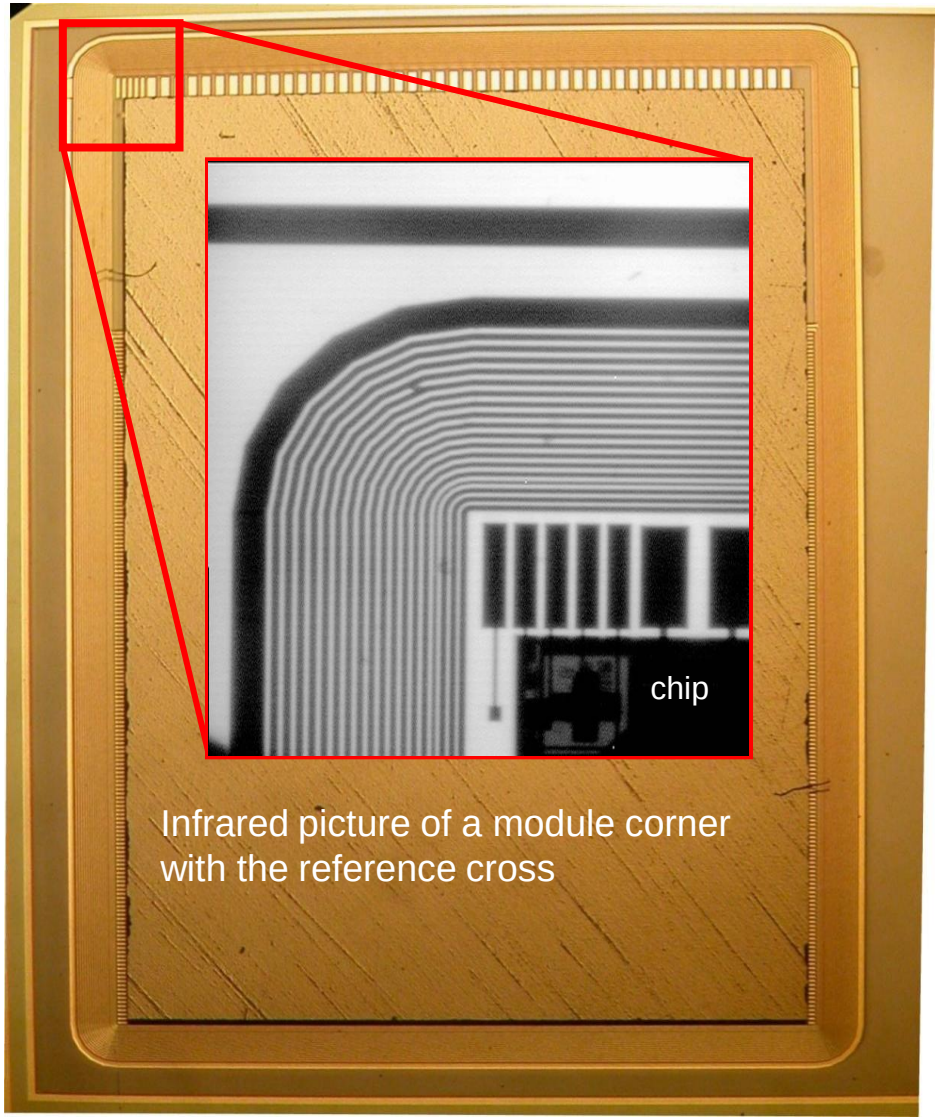
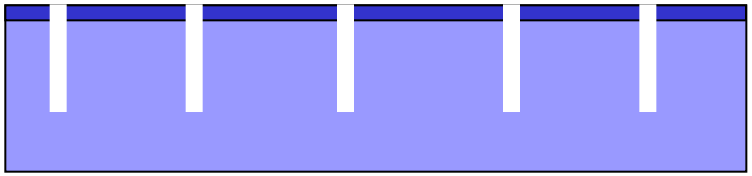


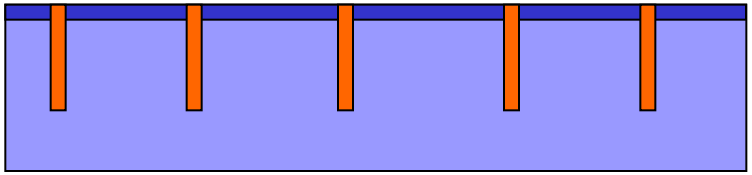
View of a pixel module composed of dummy sensor plus FE-I3 chip interconnected via SLID

Trough Silicon Vias processing

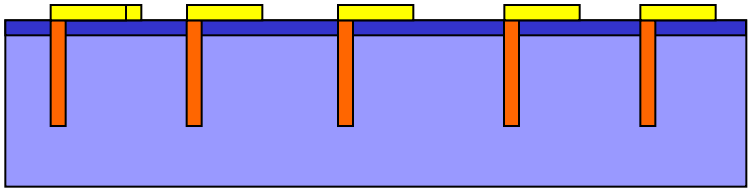
CMOS bulk



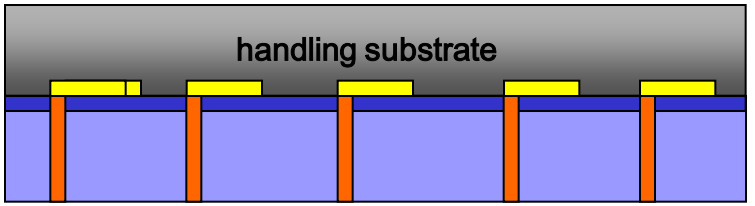
Etching (Bosch process) on FE-I3 8" wafers. 60 μm deep TSVs with lateral dimensions of 3 x 10 μm^2



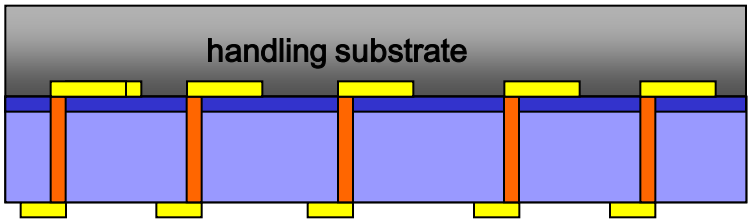
Insulation, filling with tungsten



Electroplating, metallization on the ASIC front side



Back thinning to expose the TSV, backside isolation



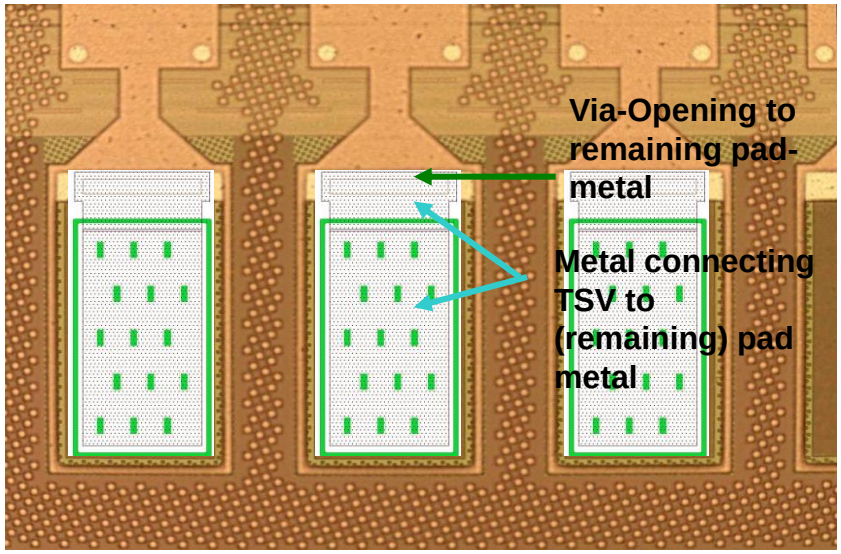
Electroplating, metallization on the ASIC back side

- Face to face connection for our project (also die up connections are possible).
- 2.5 Ohm/per via (including SLID).
- No significant impact on chip performance (test performed on MOS transistors).

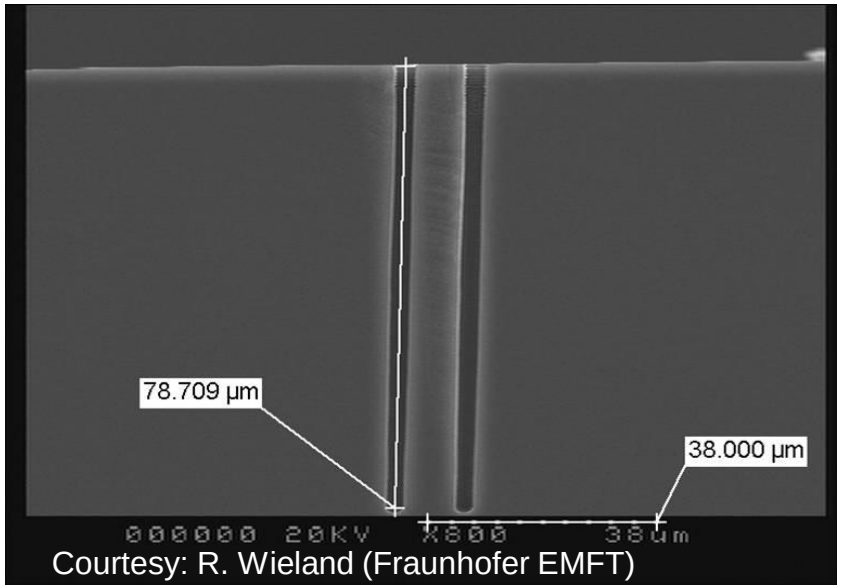
Step II: FE-I3 interconnection with TSV

➢ Etching trials and first lithographic steps for TSV on-going at EMFT on two FE-I3 wafers

- Layout of TSV structures (3.6 µm x 10.6 µm) to be placed within metal-free area of FEI3 pads
- Width of Surrounding trench: 2.6 µm



- Typical result of Deep Trench etching of vias with high aspect ratios > 20:1
- STS Pegasus equipment at Fraunhofer EMFT (lateral dimensions: 3 µm x 10 µm)



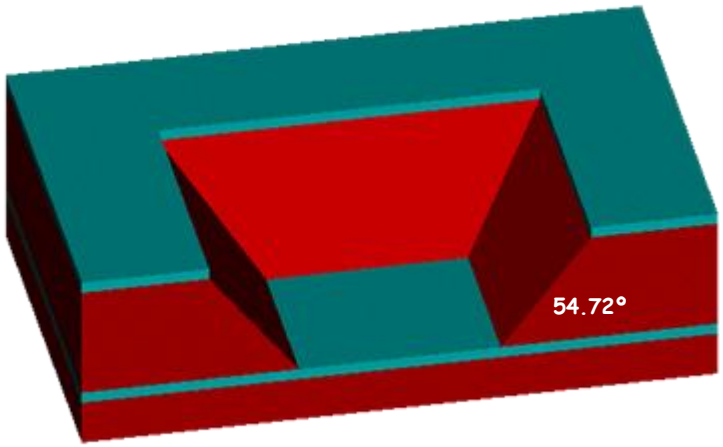
Courtesy: R. Wieland (Fraunhofer EMFT)

Summary and Outlook

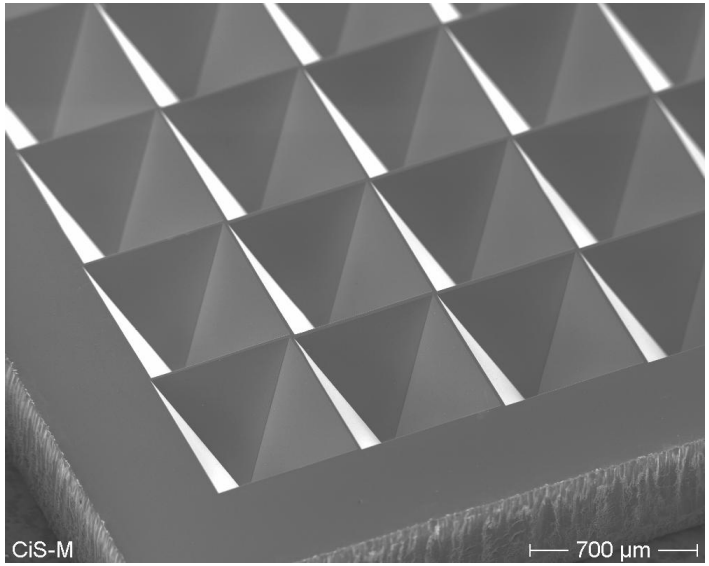
- HLL has developed a technology to produce planar sensors with an active thickness that can be freely chosen down to 50 μm
- Thin planar pixel sensors (75 μm and 150 μm thick) have been produced and tested: good performances of FE-I3 compatible pixels and promising CCE measurements after irradiation.
- A second thin n-in-p pixel production is on-going to serve as a qualification run for the ATLAS IBL project (150 μm thick, FE-I4 compatible) .
- 3D interconnection technology:
  - Wafer-to-wafer SLID feasibility demonstrated with daisy chains of ATLAS pixel geometry.
  - Interconnection of FE-I3 pixels with SLID expected to be completed in a few months.
  - TSVs etched on test FE-I3 wafer. First photolithographic steps on the hot FE-I3 wafer. Interconnection of chips with TSVs to sensors foreseen in 2011.

Back-up slides

Sensor thinning technology at MPP-HLL (II)

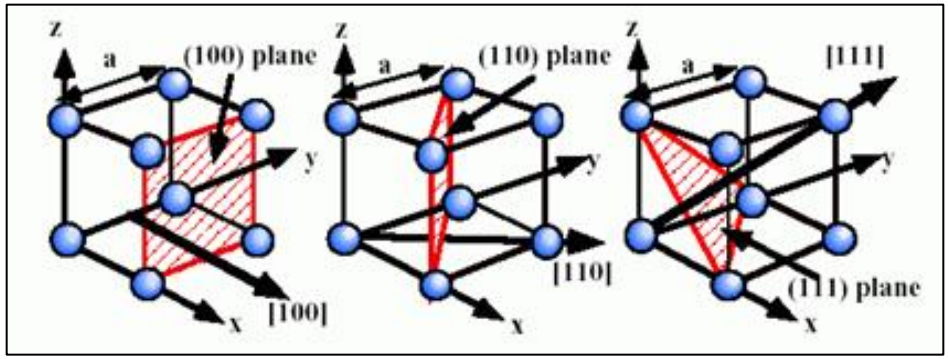


SEM picture of mechanical dummies



Etching with TetraMethyl Ammonium Hydroxide:

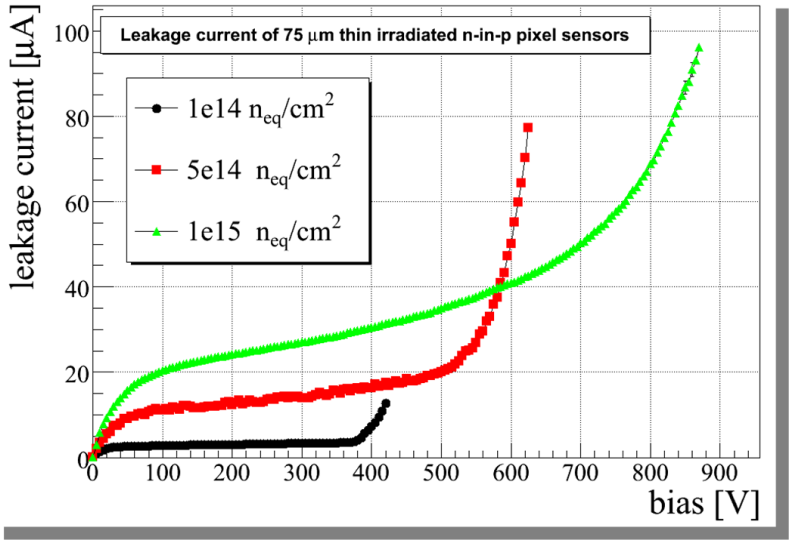
- etch rate in <100> direction larger than for higher indexed planes
- poorer selectivity to <111> (~ 30:1)
- good selectivity to oxide
- etch rate Si<100> ~ 60 µm/hr

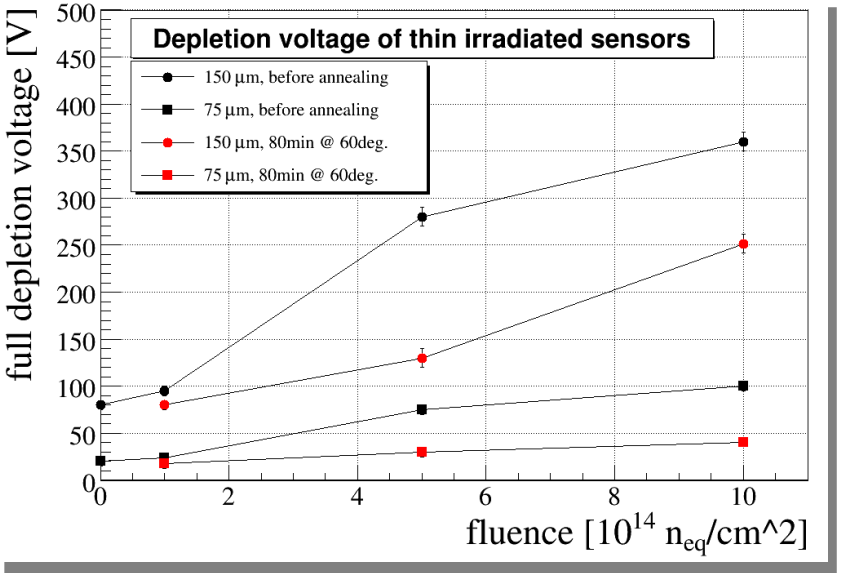


- Frames can be left on the handle wafer to offer enhanced mechanical stability to the stack composed by the sensor and the chip (it is foreseen to thin the FE-I4 chip down to a thickness of ~ 100 µm for IBL)

Post-irradiation characterization of the n-in-p wafers

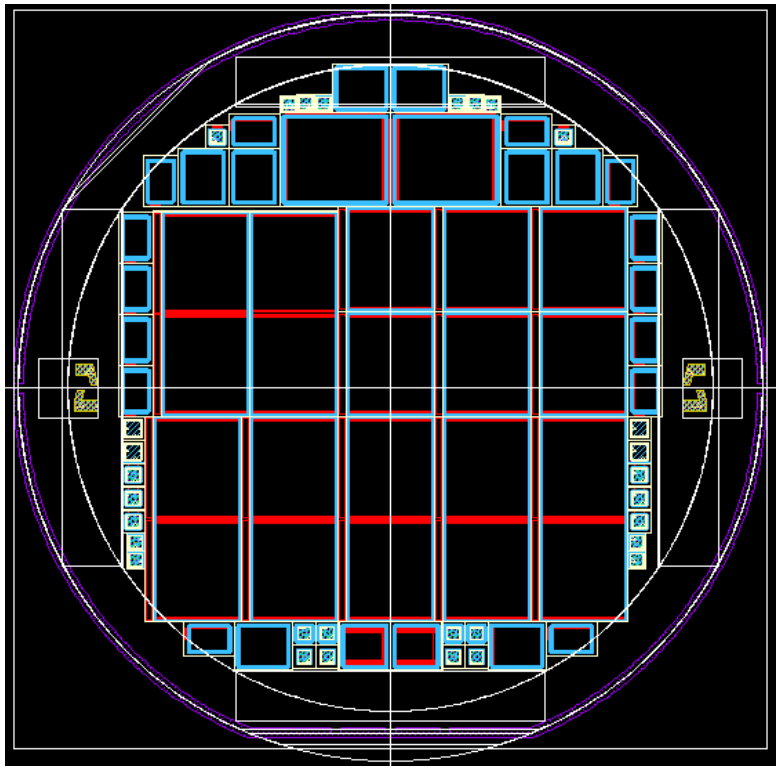
IV on irradiated p-type pixels – FE-I3 geometry





- All the structures show the expected improved breakdown behavior after irradiation with $V_{break} >> V_{depl}$

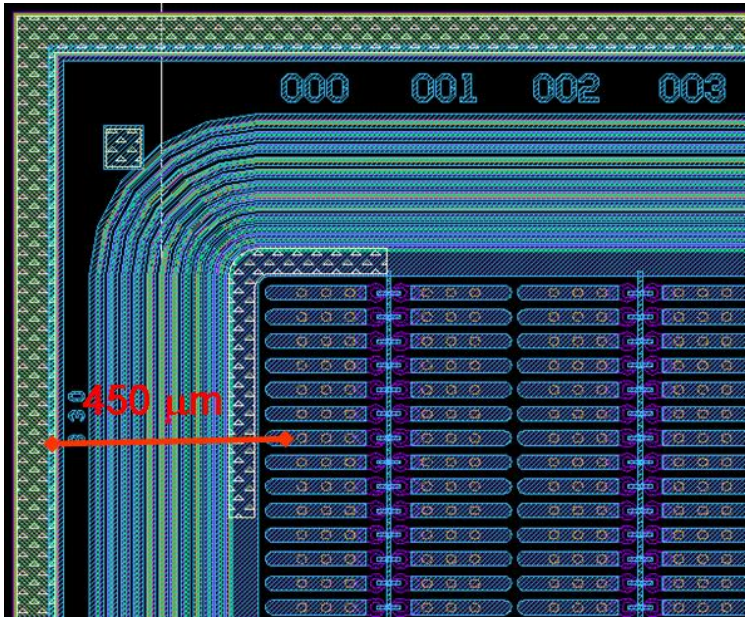
Second thin pixel production for IBL at MPP-HLL



- 6” n-in-p wafers with an active thickness of 150 μm in production at MPP-HLL
- Sensors comply with the IBL requirements: 2x1 FE-I4 geometry and inactive edge limited to 450 μm

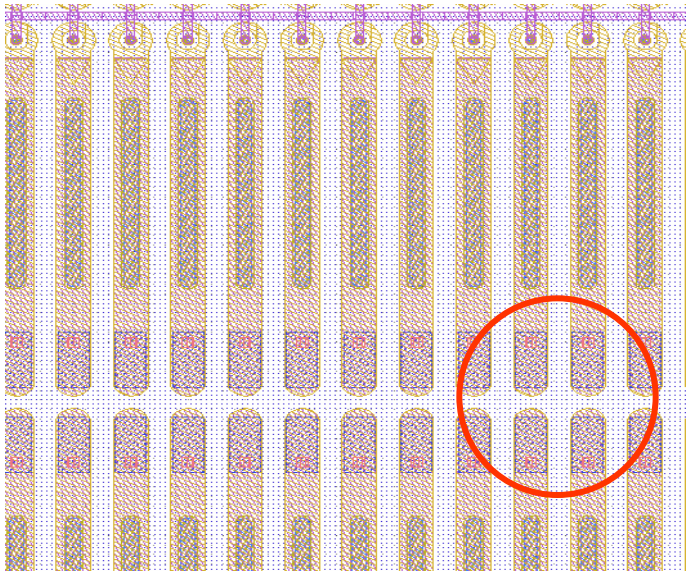
Talk by F. Huegging,“ The ATLAS Insertable B-Layer Detector (IBL)“

- To be qualified for IBL this production will be interconnected to the FE-I4 chips with standard bump-bonding at IZM-Berlin

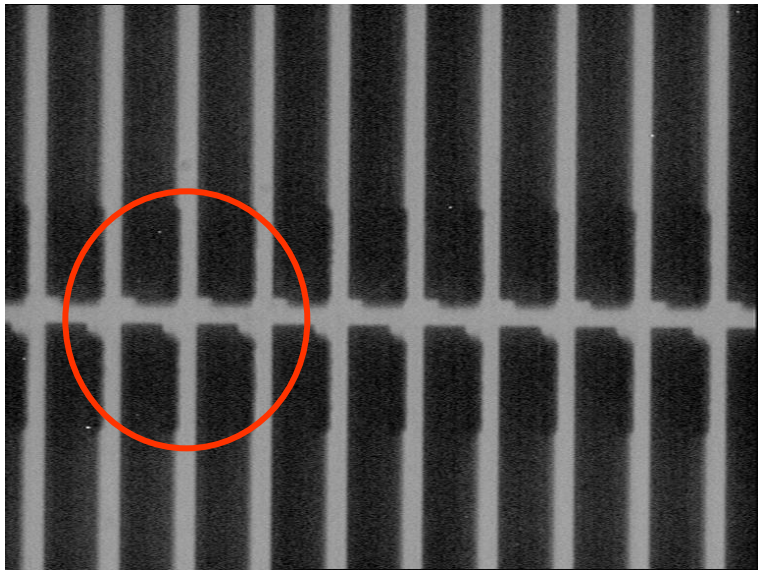


Wafer-to-wafer SLID: ATLAS pixel geometry

Pixel sensor with the pads for the SLID interconnection to the FE-I3 chip



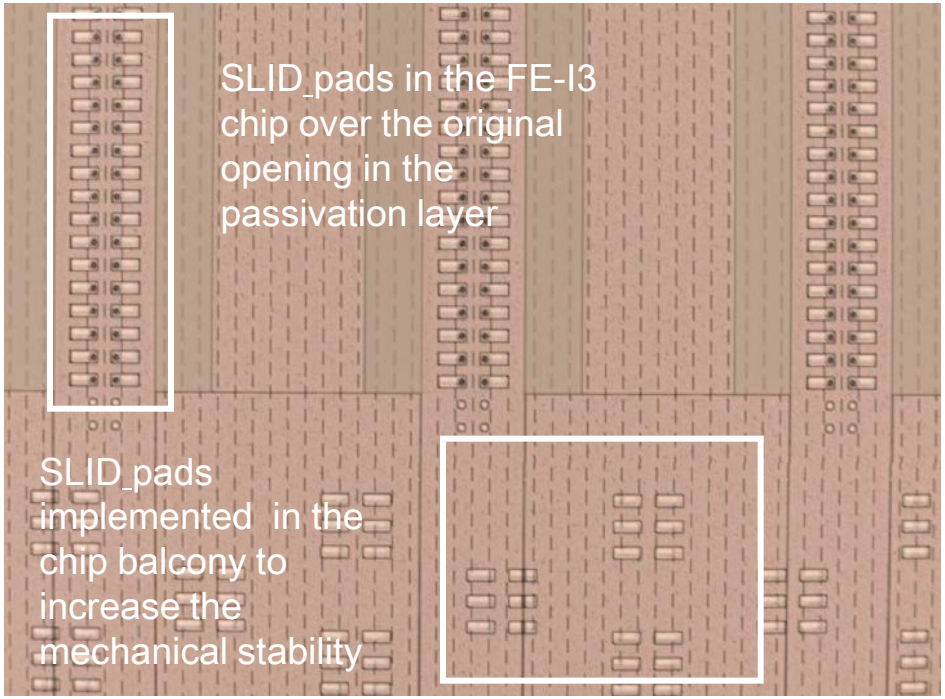
Infrared pictures of the daisy chain with ATLAS pixel geometry

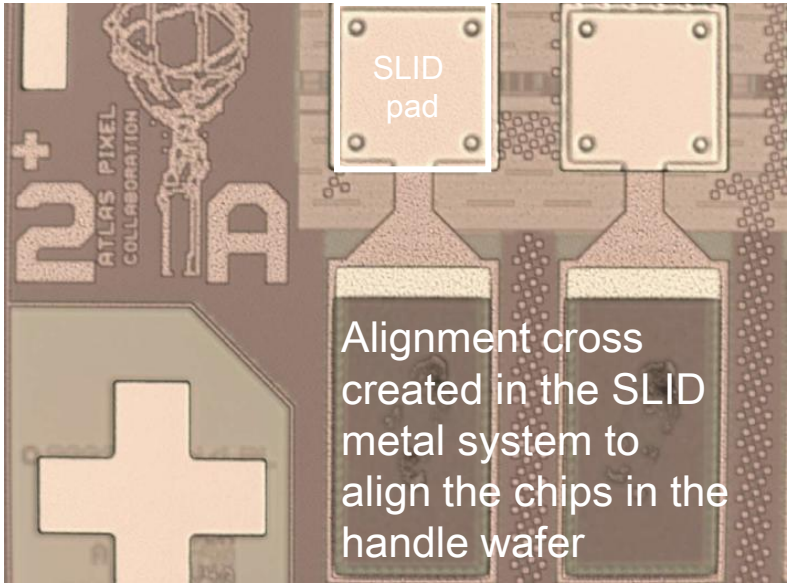


- Successful SLID interconnection for daisy chains whit the "ATLAS pixel" SLID pads : 27 x 60 μm²
- Interconnection inefficiency of $(5\pm1)\times10^{-4}$
- Infrared microscope analysis did not reveal any problem, like e.g. shorts due to possible outflows of Sn from the pads

Step I: SLID interconnection without TSV (II)

FE-I3 chips after electroplating of the SLID pads

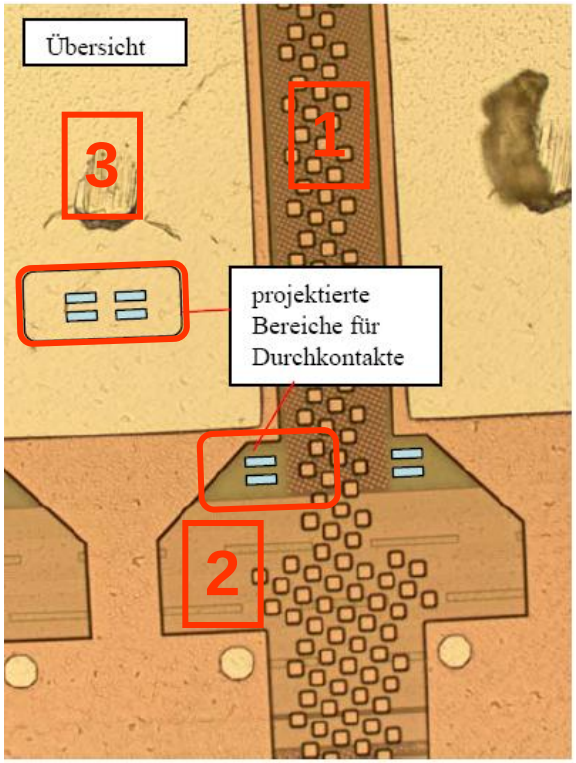


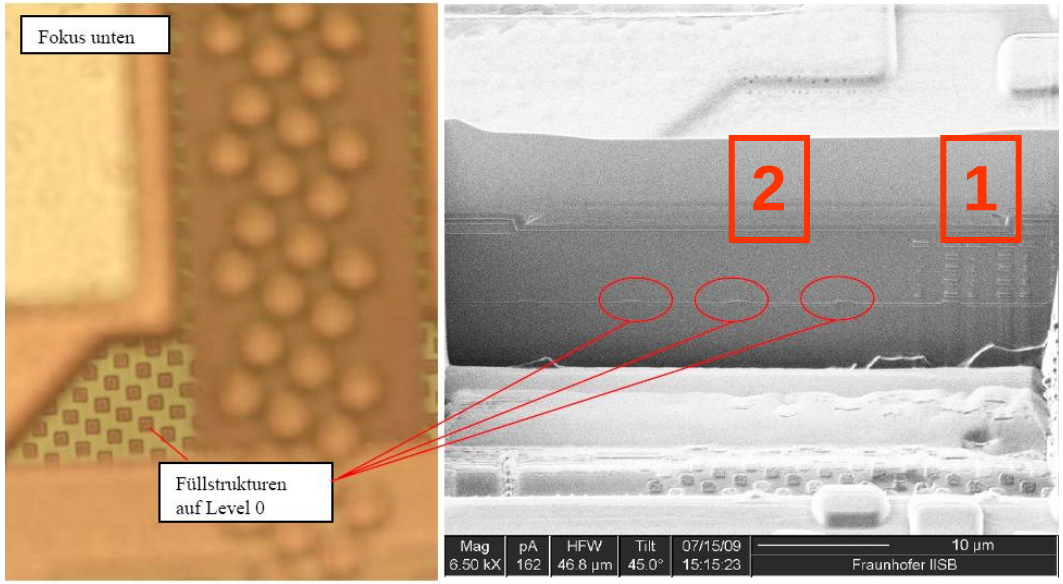


- SLID metal system has been created also in the read-out pads the chip, to allow for their connection to the fan-out structure on the sensors

Investigation of FE-I3 for 3D integration

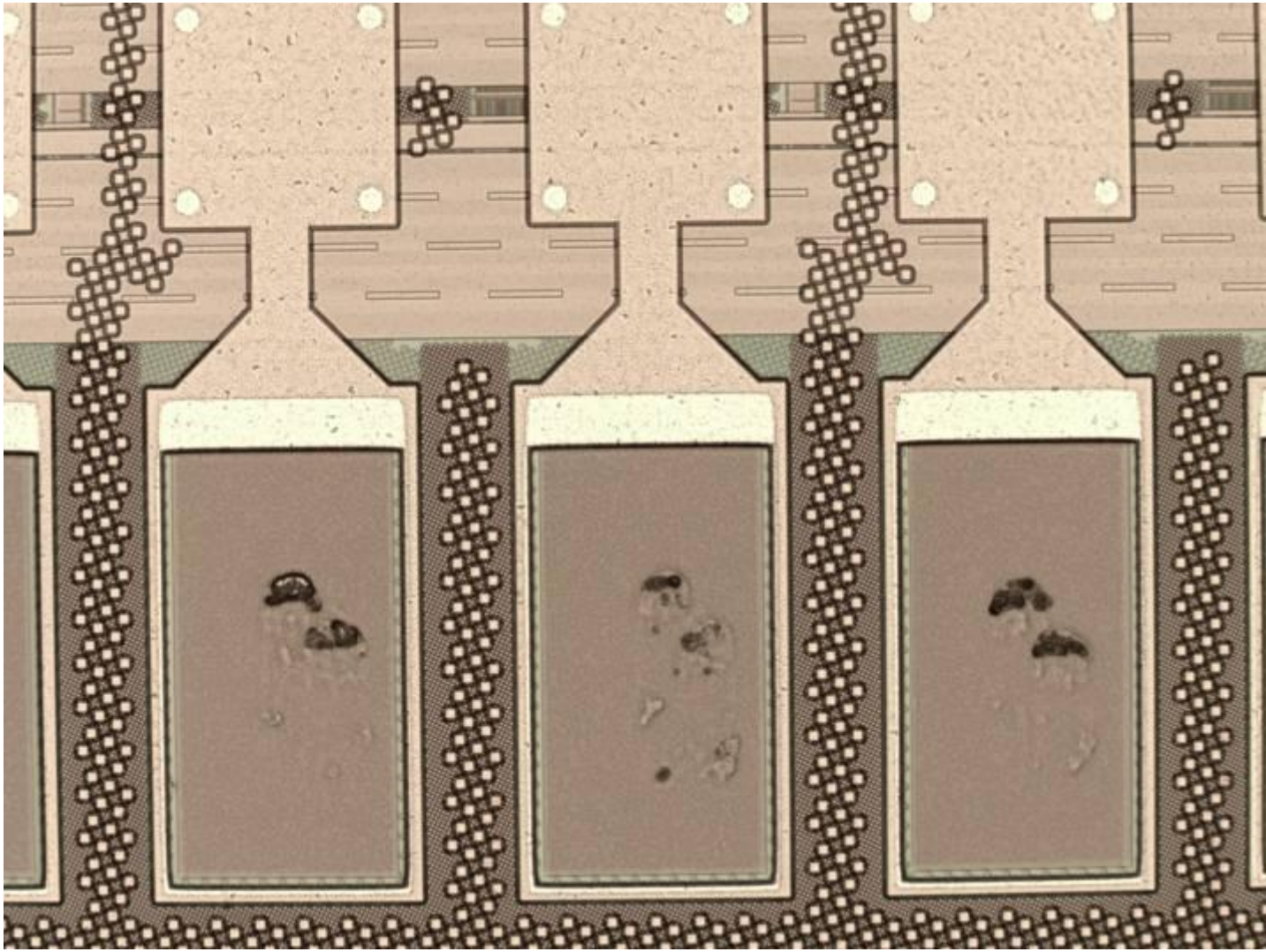
- Identification of Target area for TSV etching:
  We plan to route the signal and services in the FE-I3 ASIC from the wire bond pads to the chip backside using TSVs. Investigation with a FIB analysis to identify possible areas for TSV etching:
  1) Central region between pads: filling structures with superimposed tungsten plugs and metal layers
  2) Covered by top metal layer in some pads
  3) ICV directly over the pad area after having etched away the top aluminum layer





FIB analysis of the FE-I3 chip: Scan of the central region between two wire bond pads.

Topview on FEI2 – pads prepared for TSV-structuring and etching



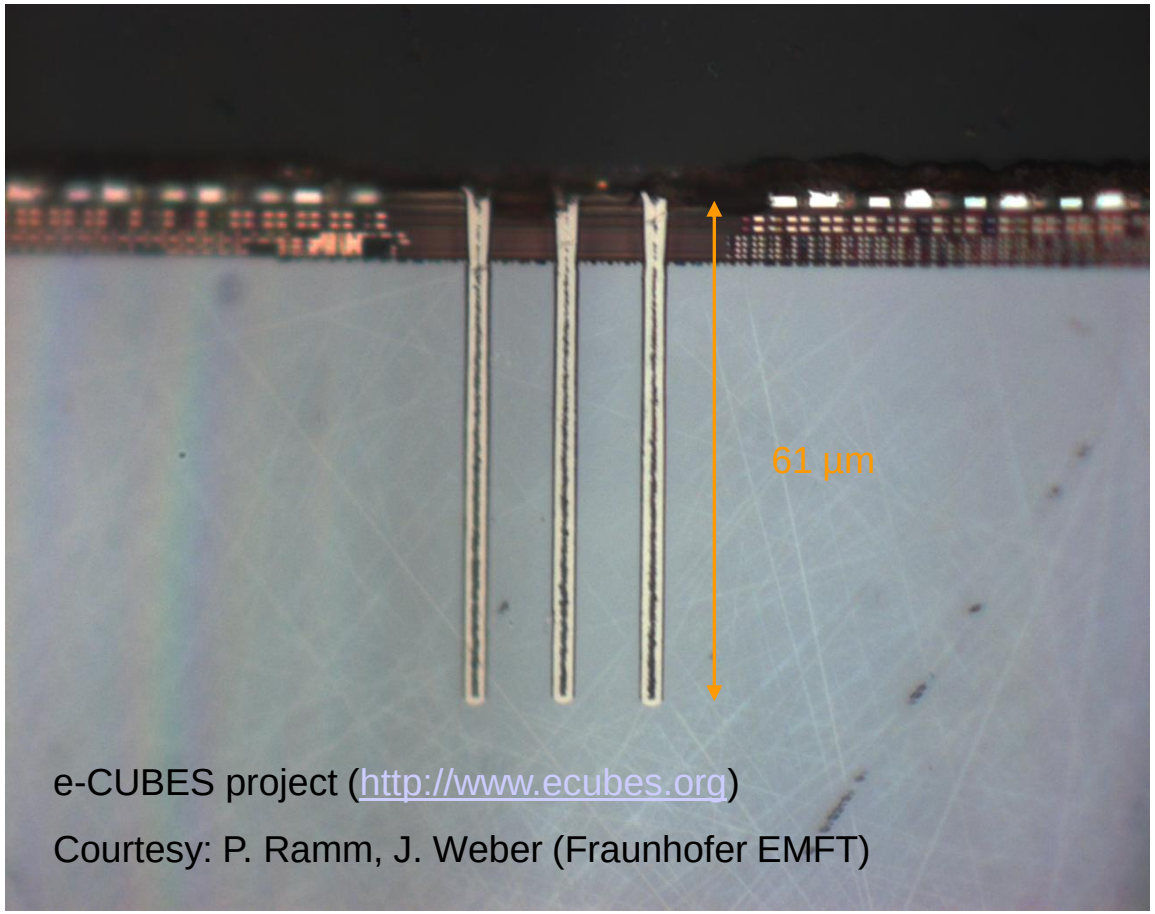
Nitride etch

Local planarisation by depositing and etching of SACVD-Oxide

Hardmask deposited

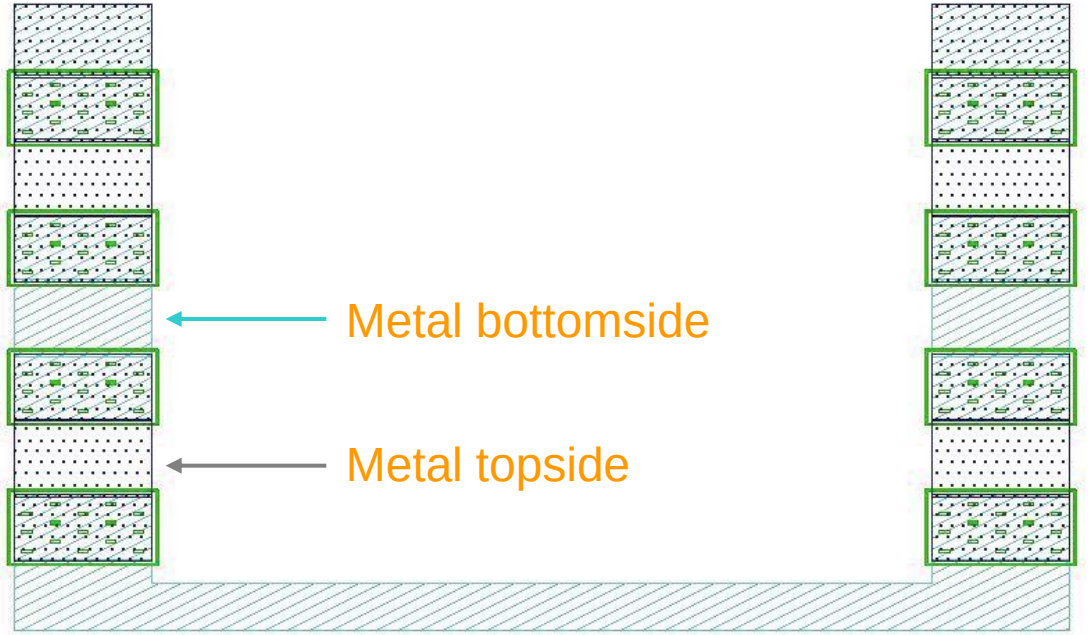
Post BEOL TSV processing

W-filled High aspect ratio TSVs before thinning of the wafer



e-CUBES project (http://www.ecubes.org)

Courtesy: P. Ramm, J. Weber (Fraunhofer EMFT)



Layout of Process control module (PCM) integrated in test-modules of FEI-wafer for evaluating the TSV array:

Daisychain of TSV arrays can be measured after thinning and processing the bottomside