Monolithic pixel detector in high-voltage technology - new achievements

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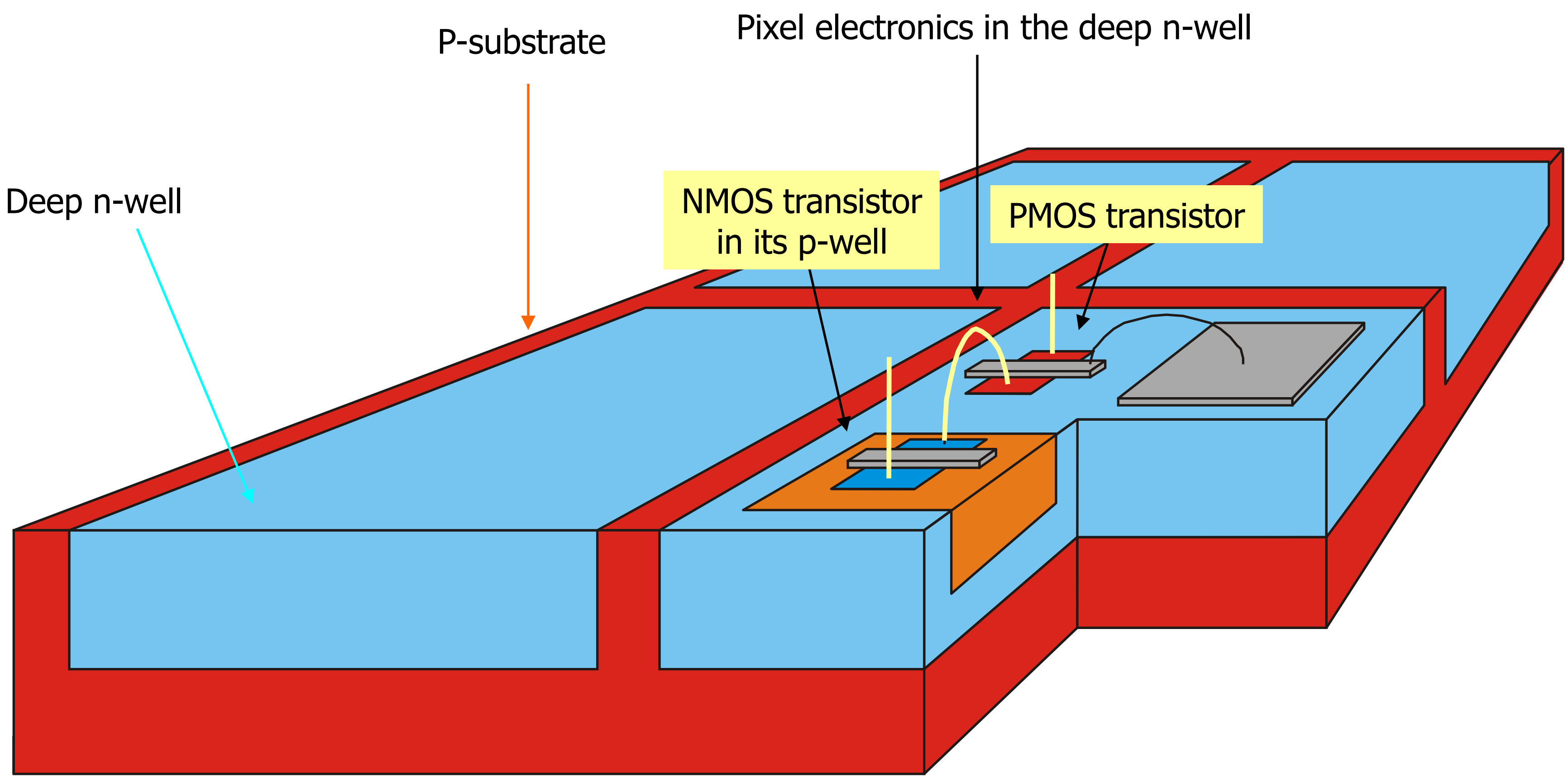
Pixel detector in HV CMOS technology

- Monolithic sensor
- 100% fill-factor
- In-pixel CMOS signal processing
- Radiation hard (tested to 50 MRad (x-rays) and 10^{15} n_{eq} (protons))
- Excellent SNR (seed 21 µm-pixel SNR for high energy betas > 80)
- Allows thinning below 50 µm without signal decrease
- Good timing properties (theoretically 40 ps signal collection time)
- Not expensive (standard technology used, wafer run costs 98 k€)

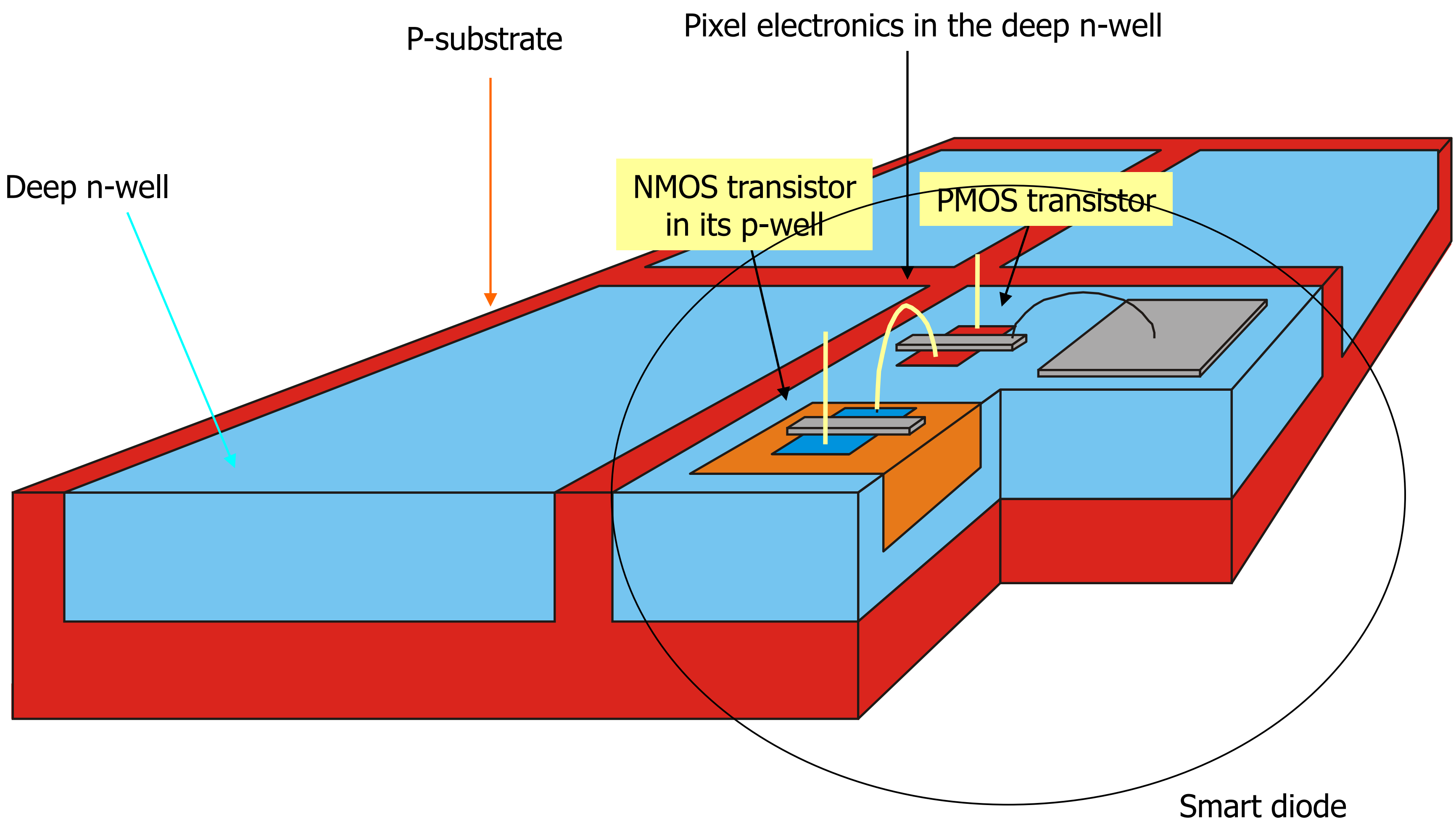
The detecor stucture

Based on twin-well structure



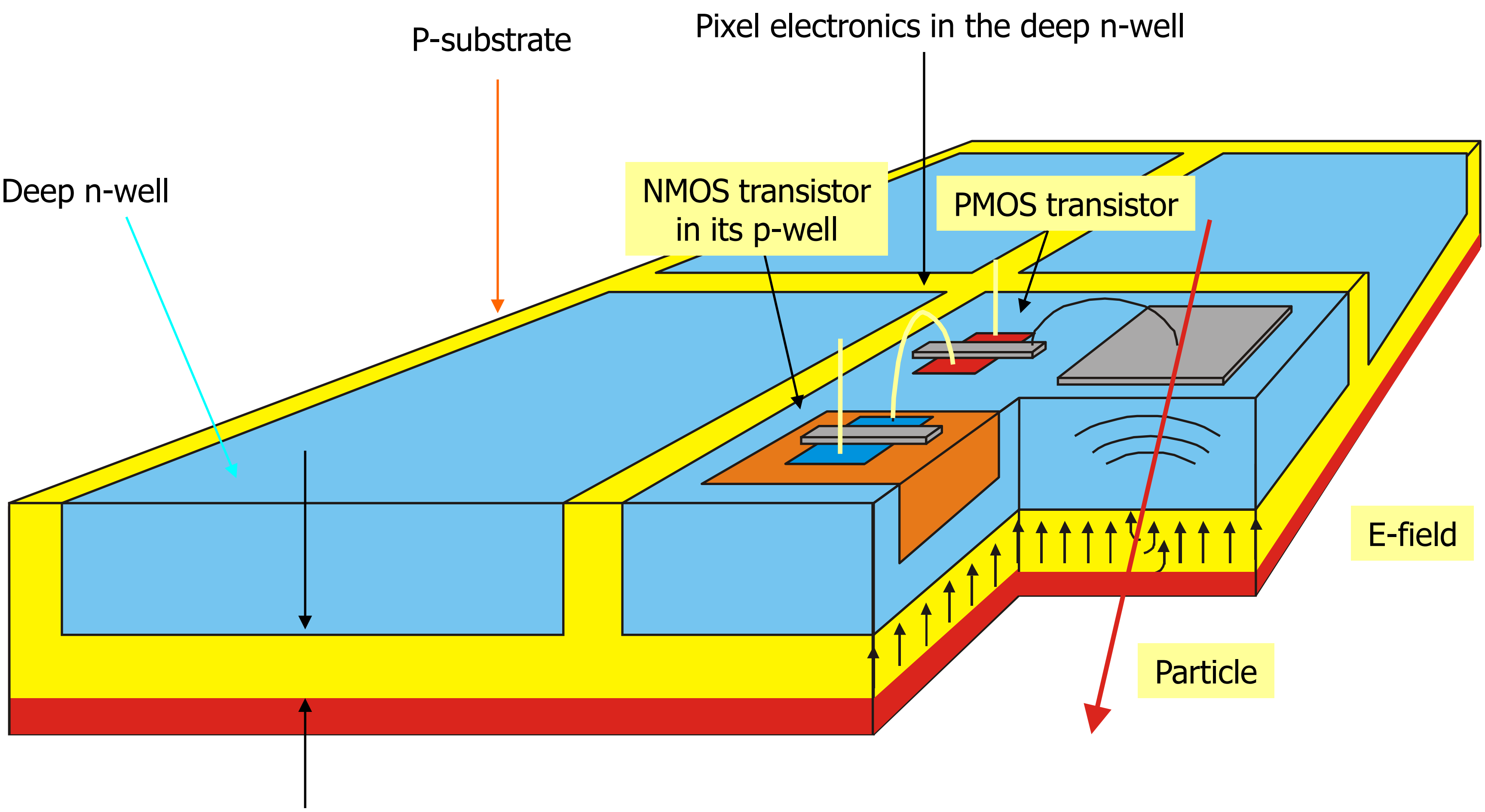
“Smart” diode array

Based on twin-well structure



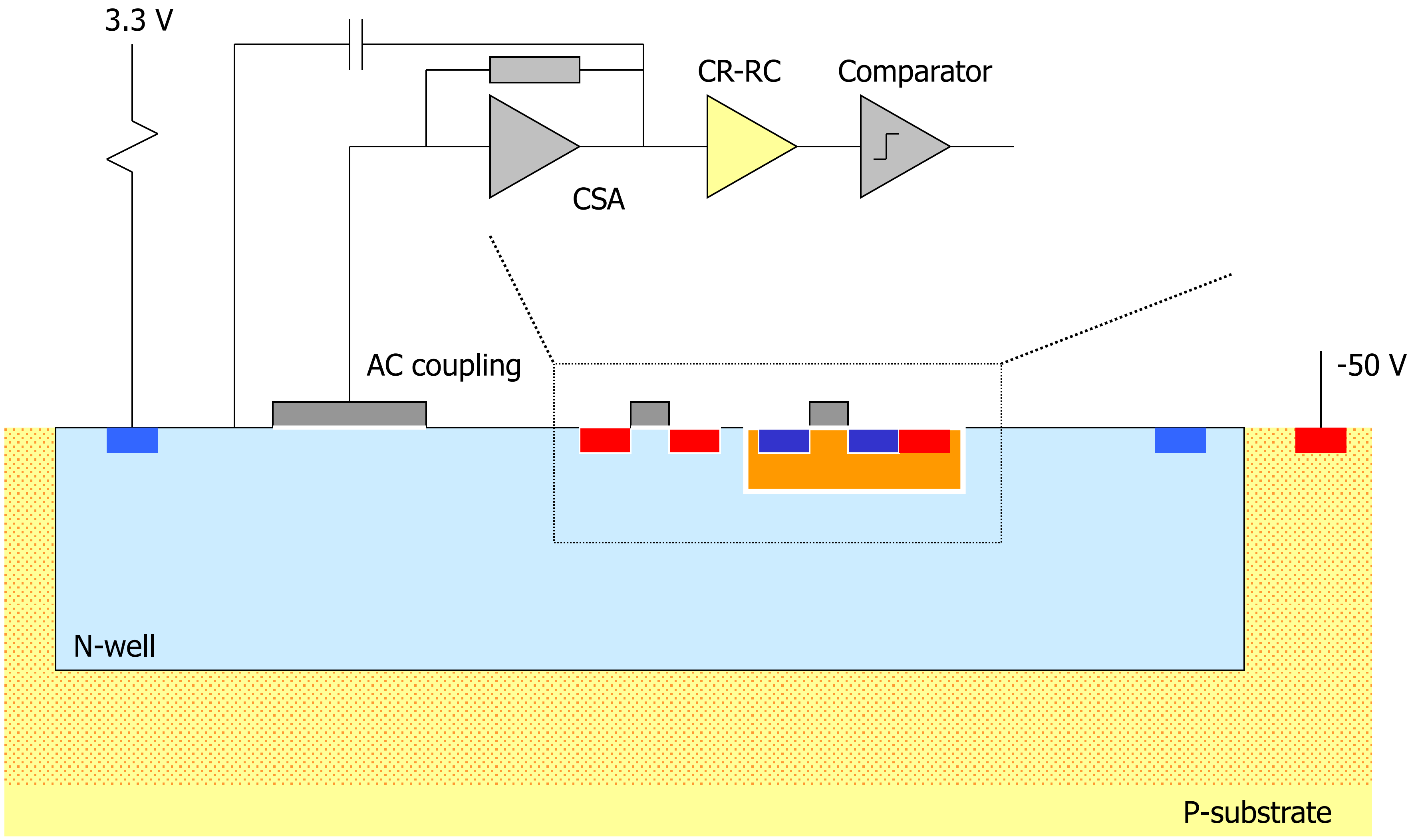
“Smart” diode array in HV CMOS technology

High voltage deep n-well used

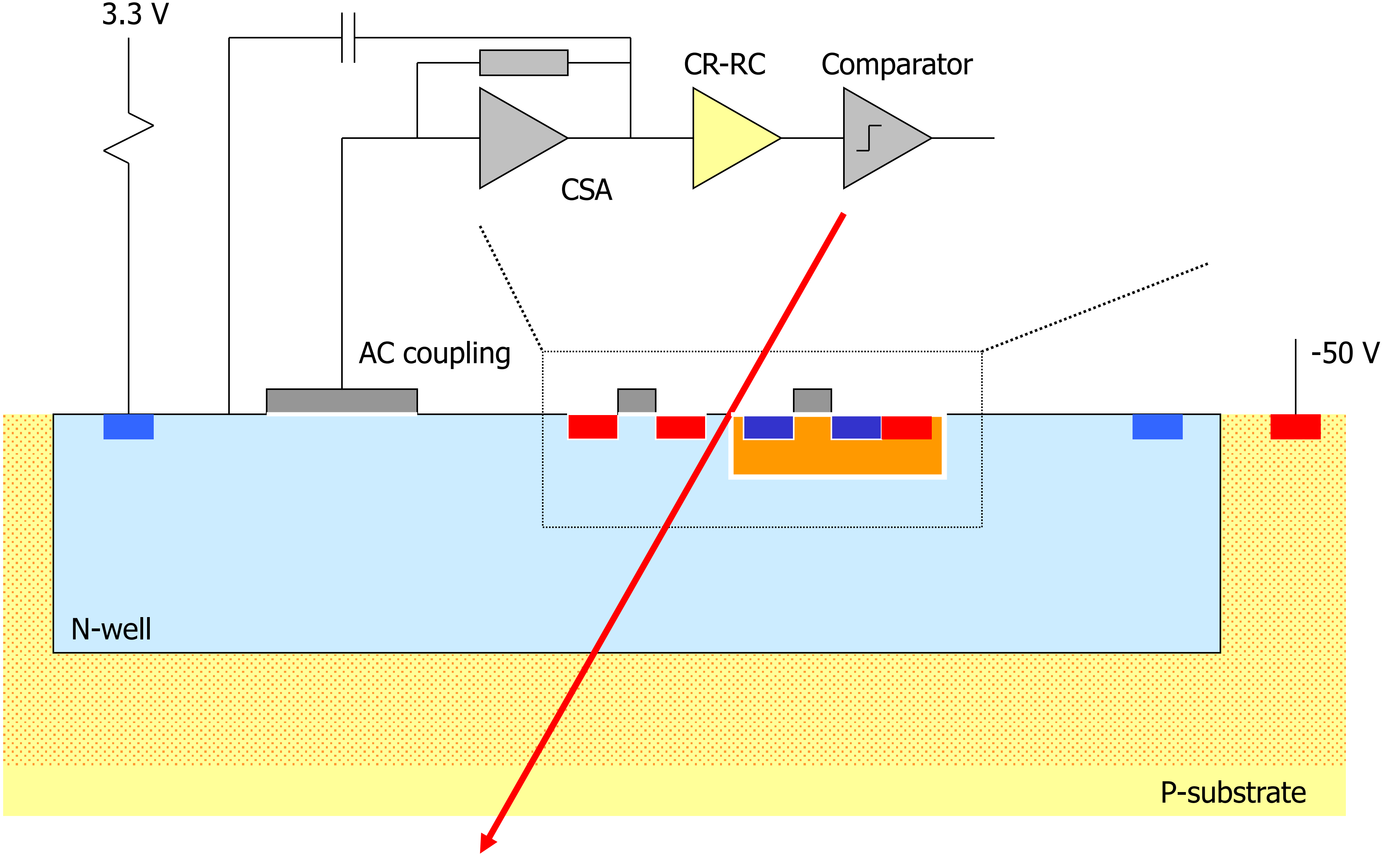


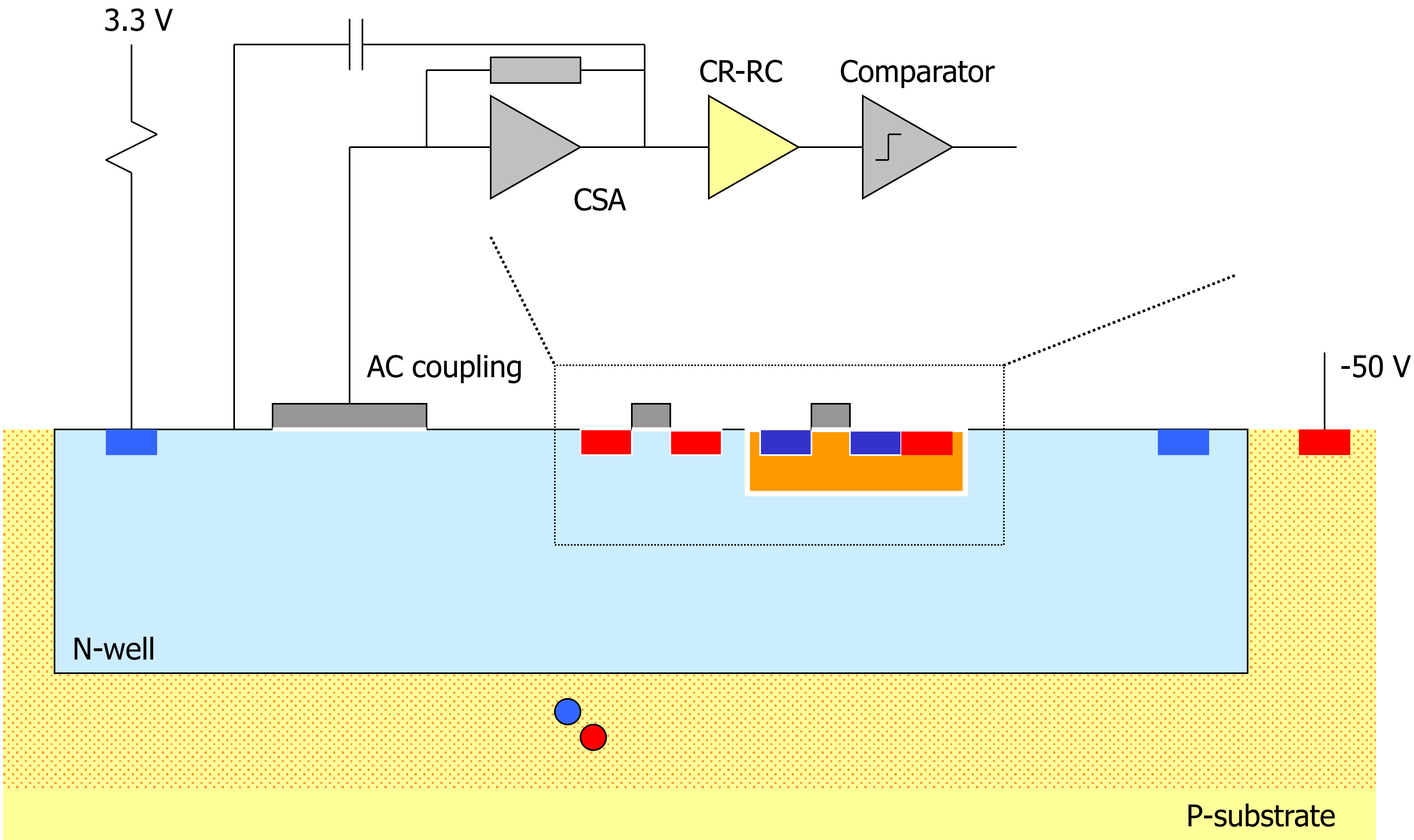
14 μm at 100V bias
(MIP: **1080e from depleted layer**)

Signal detection



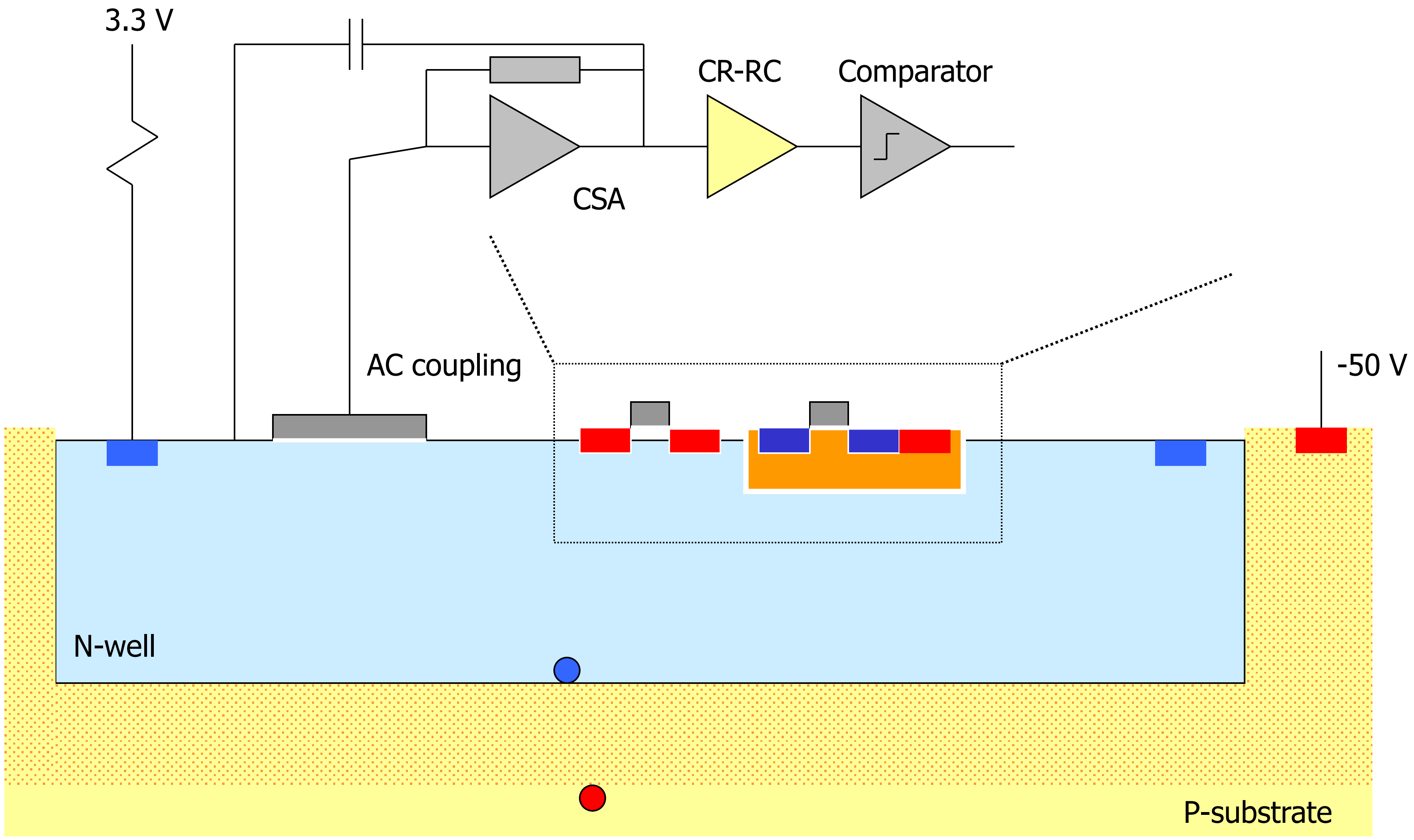
Signal detection



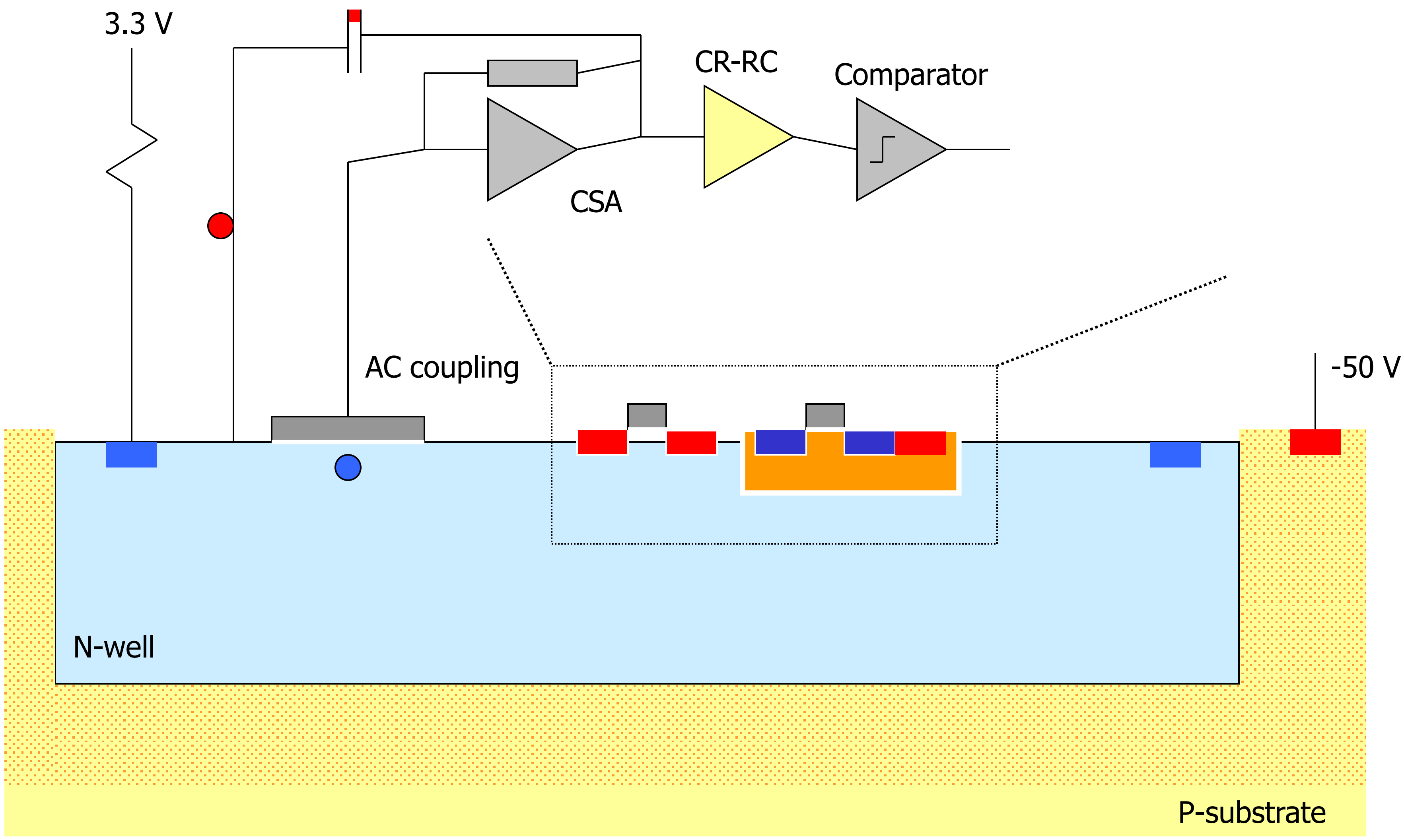


3.3 V
CR-RC
Comparator
CSA
AC coupling
-50 V
N-well
P-substrate

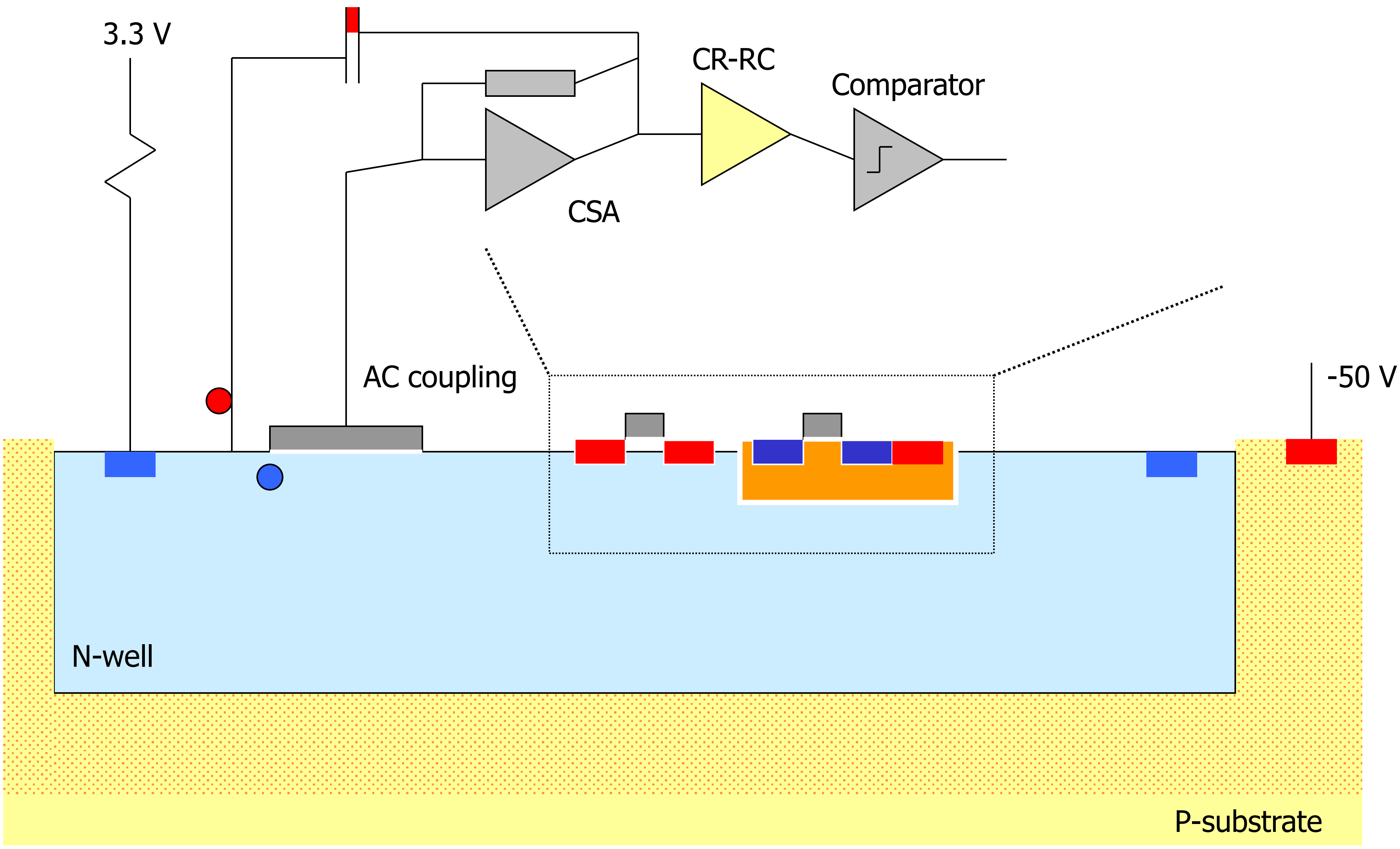
Signal detection



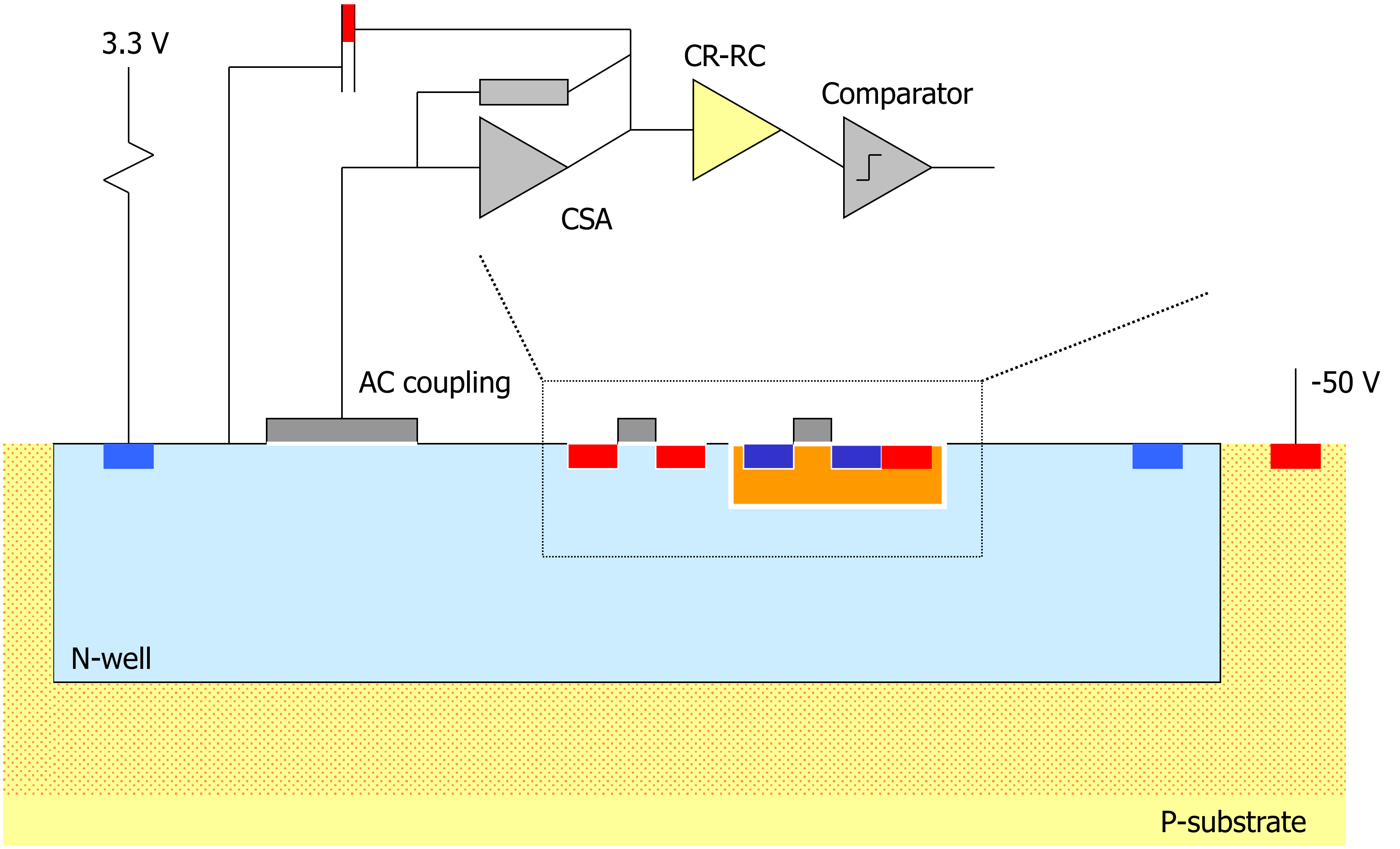
Signal detection



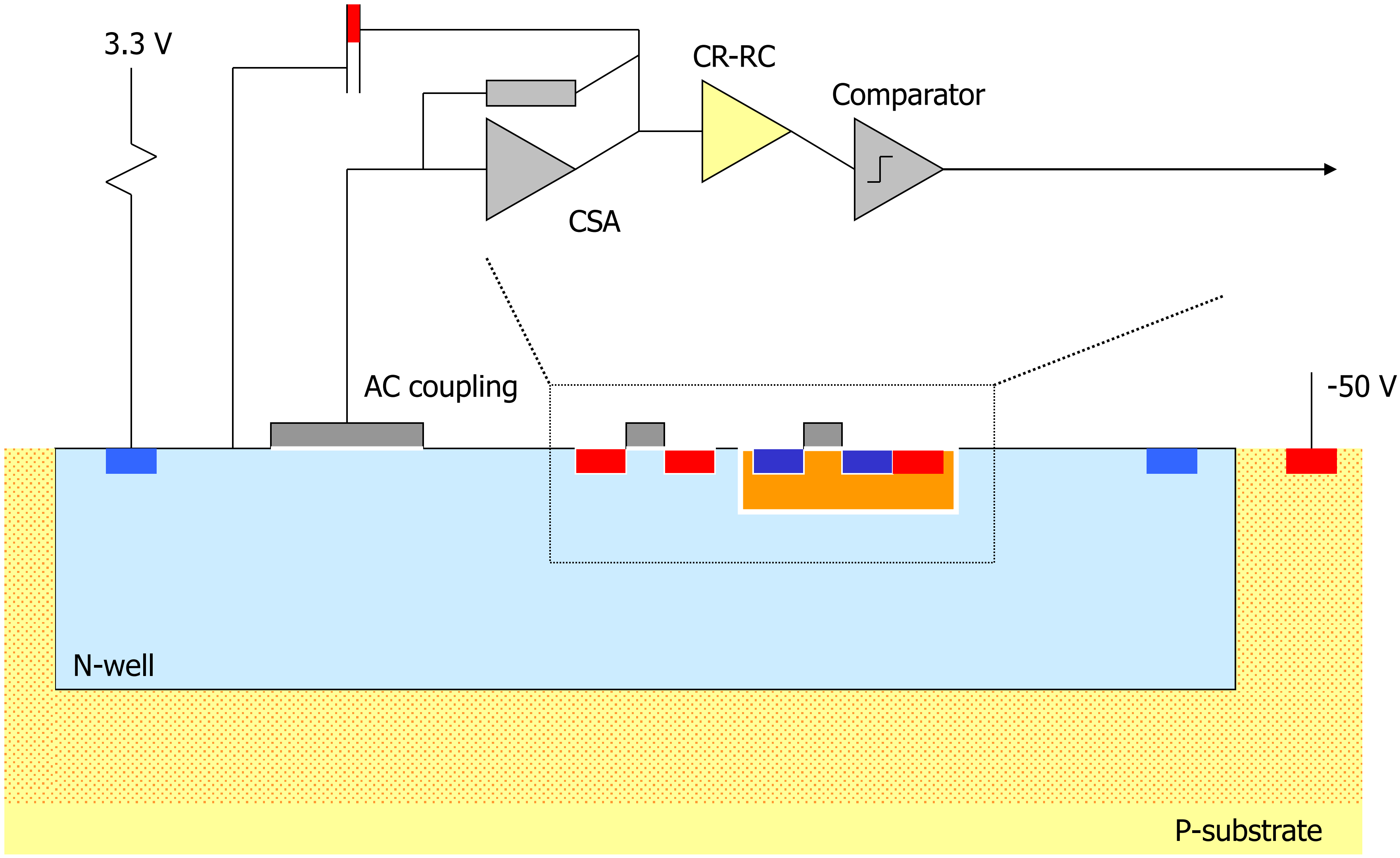
Signal detection



Signal detection



Signal detection



Project overview

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

Bumpless hybrid detector

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e

CCPD2 Chip
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

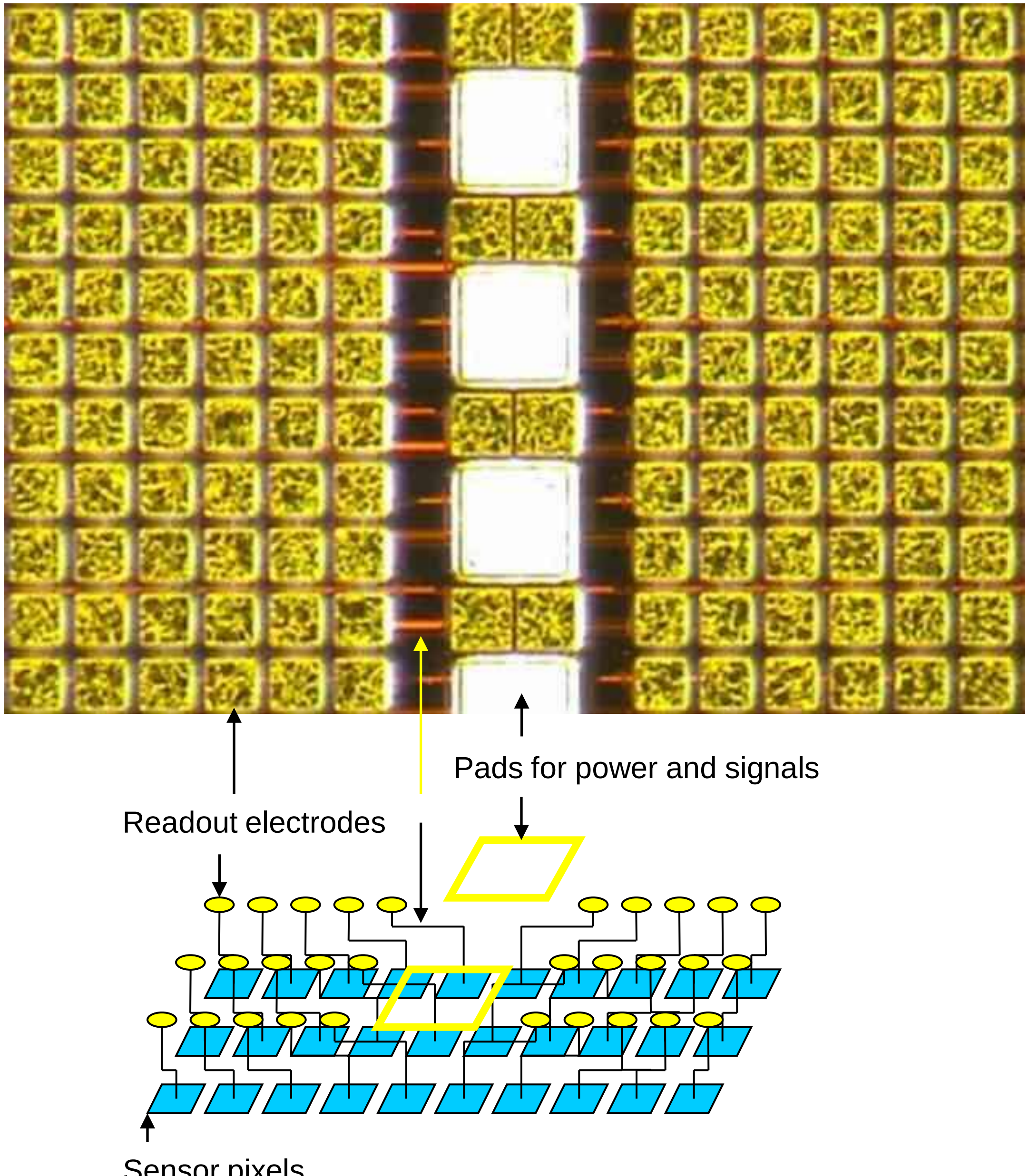
Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}$ SNR 50 at 10C (CCPD2)

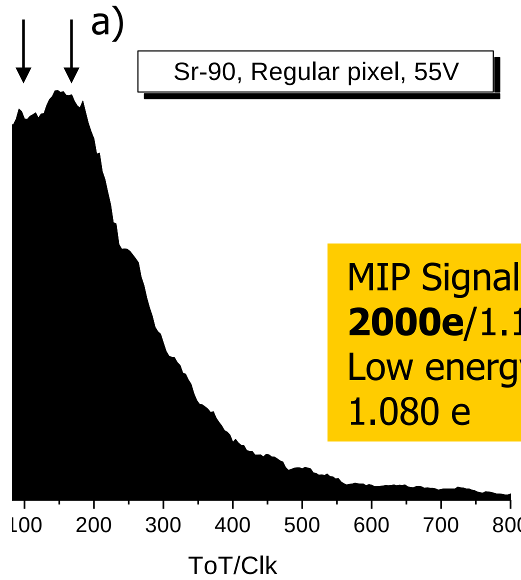
Frame readout - monolithic

PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

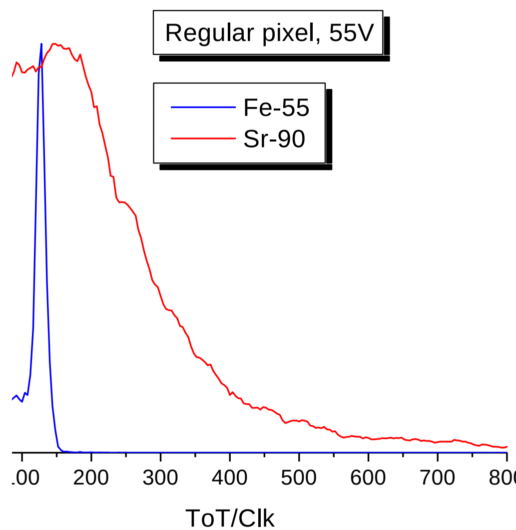
PM2 Chip
Noise: 25e, Seed MIP SNR ~ 100
Test beam planned

Tes





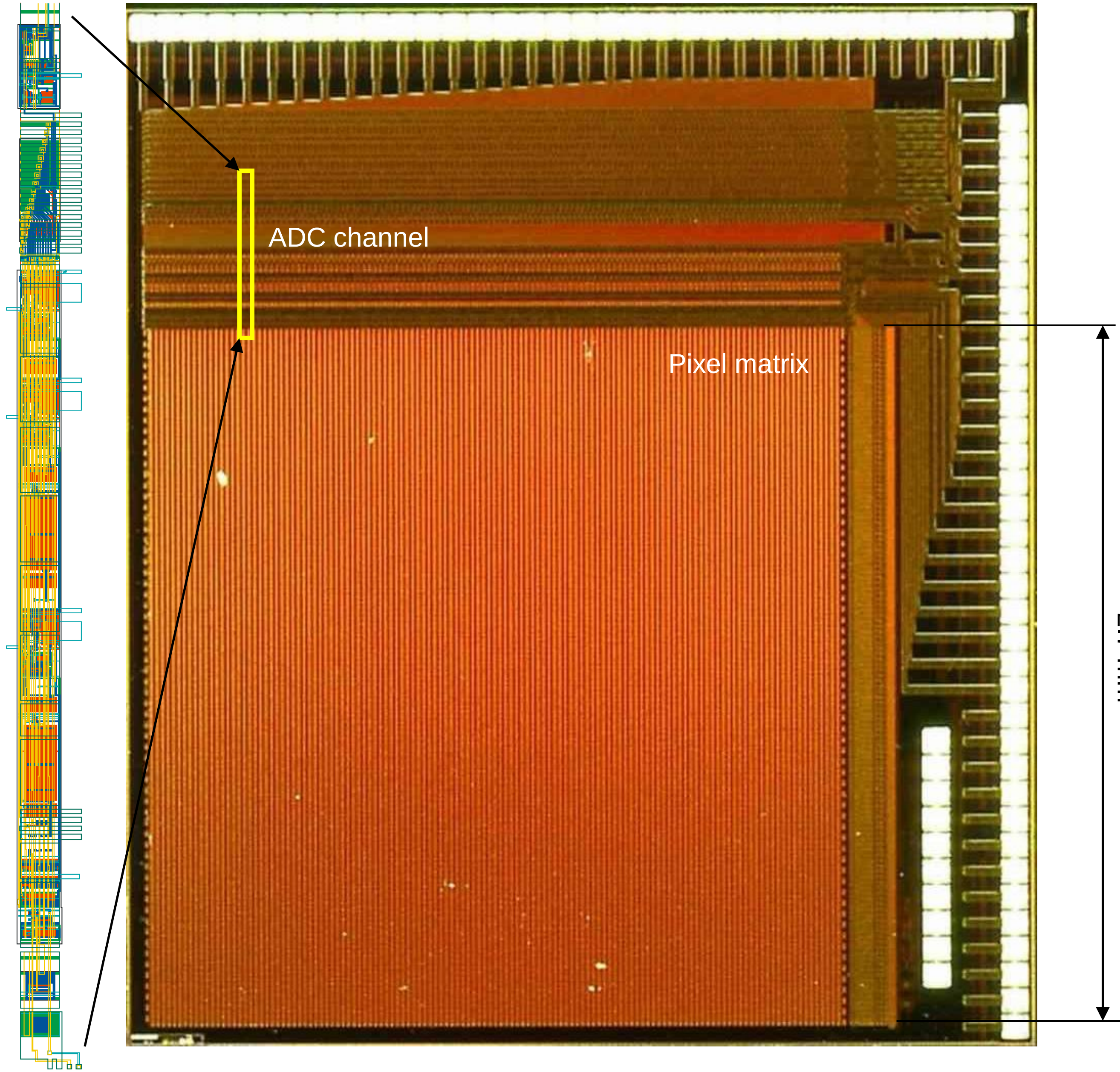
MIP Signal:
2000e/1.17 = **1710 e**
Low energy peak:
1.080 e

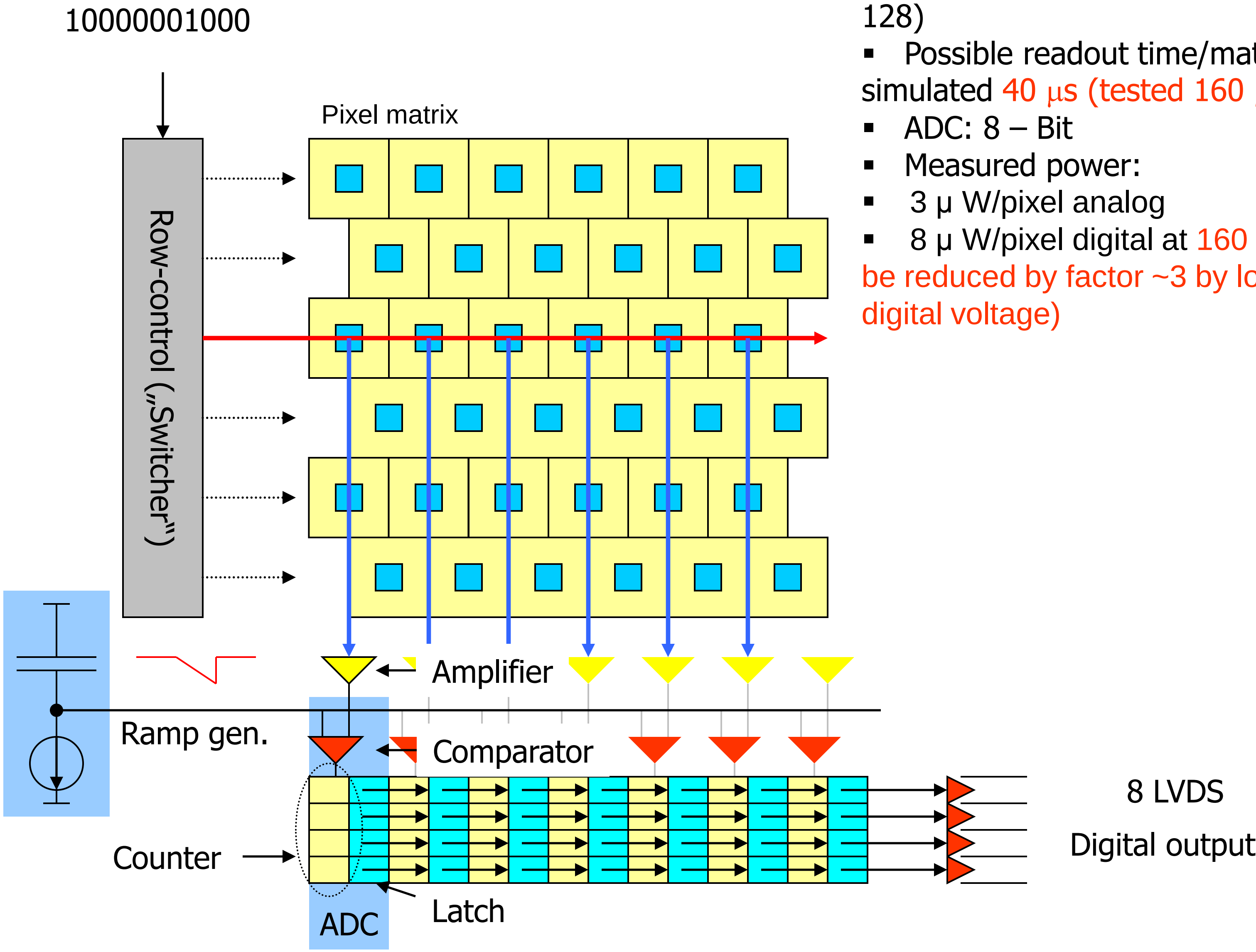


Experimental results

- Measurements with HVPixelM2

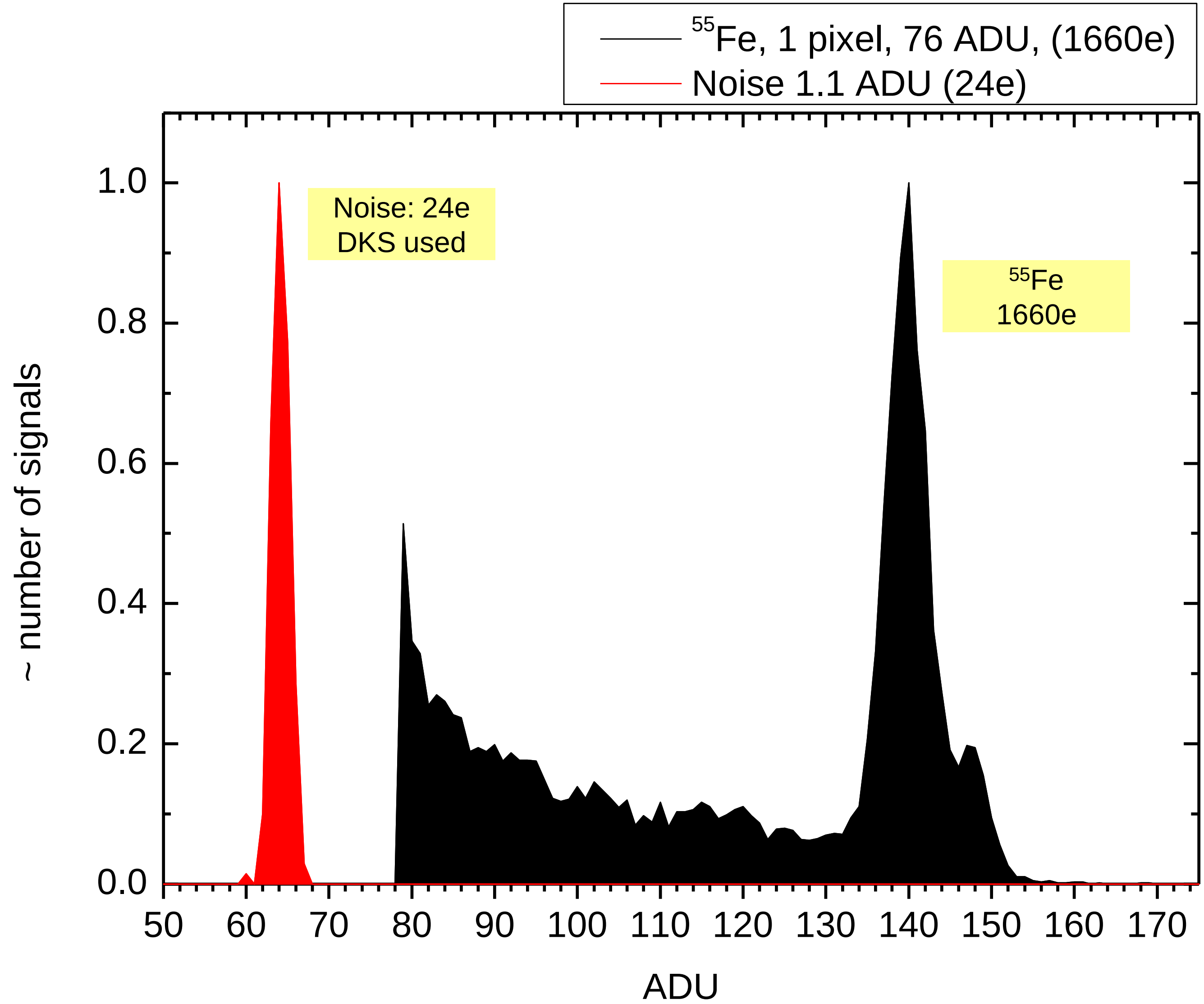
HVPixelM2 chip





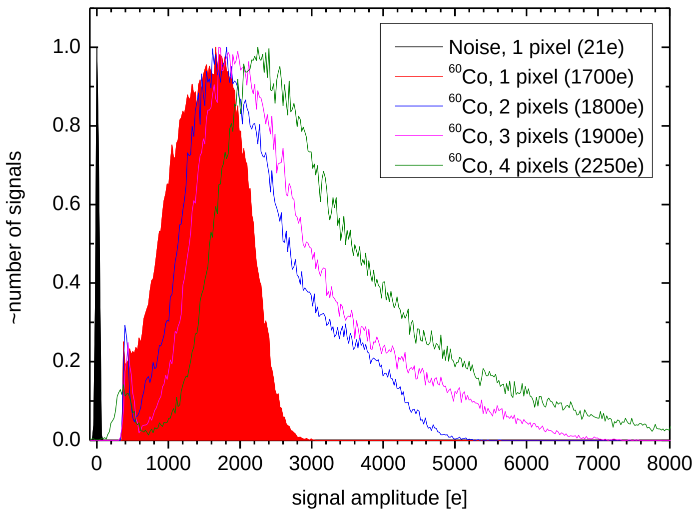
- Pixel size: 21 X 21 µm
- Matrix size: 2.69 X 2.69 mm (128 X 128)
- Possible readout time/matrix: ~ simulated 40 µs (tested 160 µs/matrix)
- ADC: 8 – Bit
- Measured power:
- 3 µ W/pixel analog
- 8 µ W/pixel digital at 160 µs/matrix (can be reduced by factor ~3 by lowering the digital voltage)

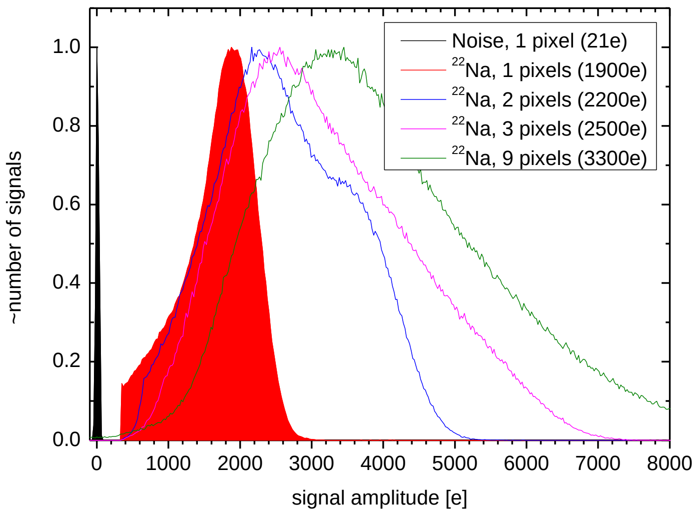
Noise measurement and ^{55}Fe spectrum (HVPixelM2)



^{60}Co betas (about 10% higher signals than MIPs)
Seed signal: 1700e
Cluster signal: 2250e
Noise: 21e
Seed SNR: 81
Cluster signal/seed noise: 107

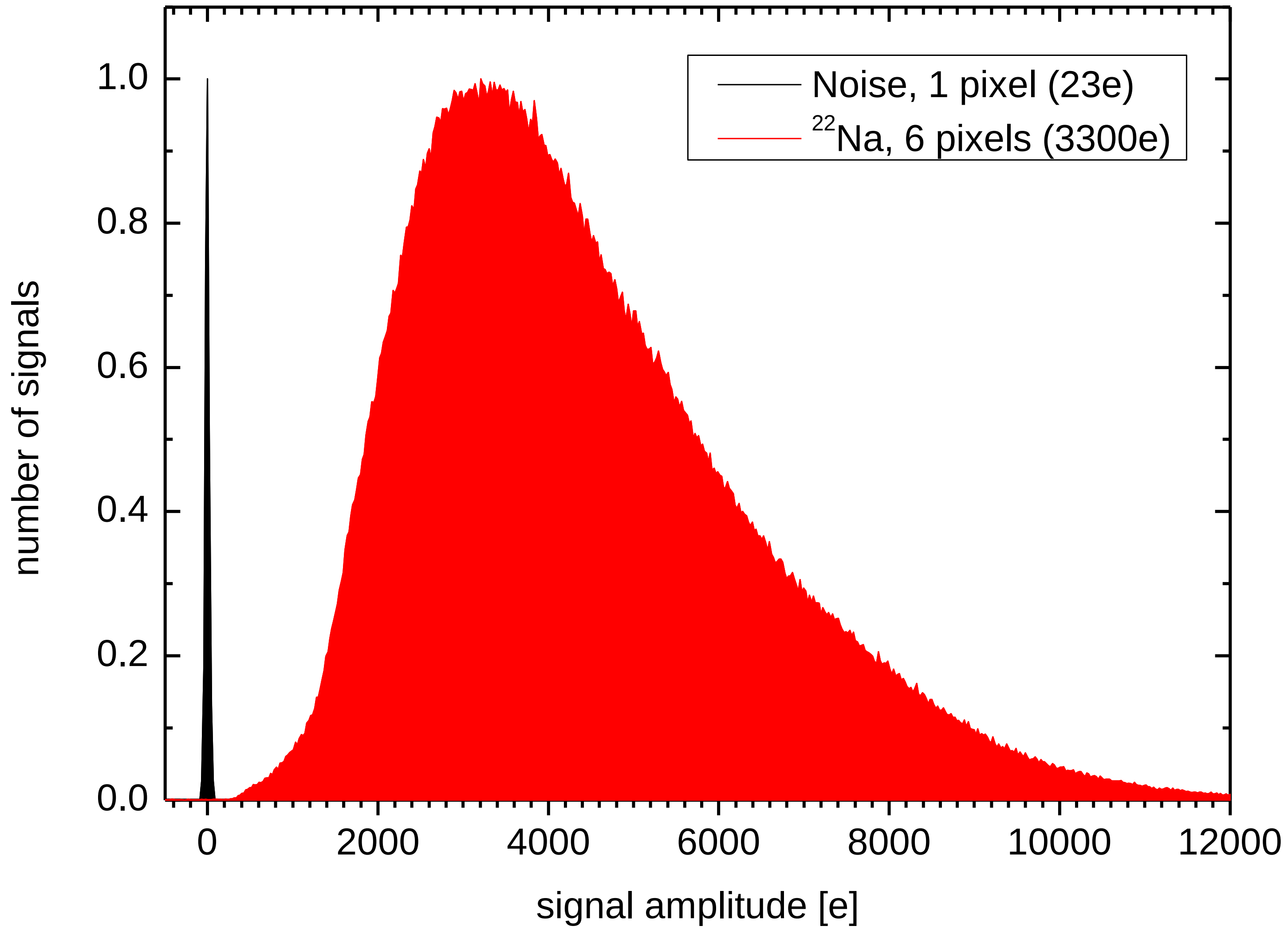
^{55}Na betas
Seed signal: 1900e
Cluster signal: 3300e
Noise: 21e
Seed SNR: 90
Cluster signal/seed noise: 157





Estimated MIP seep pixel SNR 70

High-energy beta spectra (HVPixelM2)



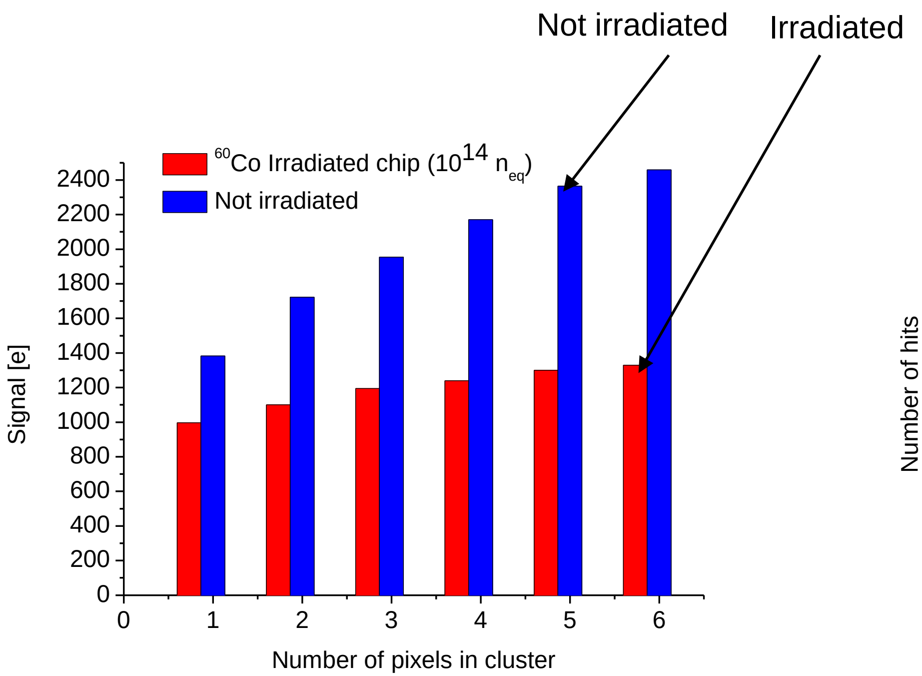
Radiation tolerance

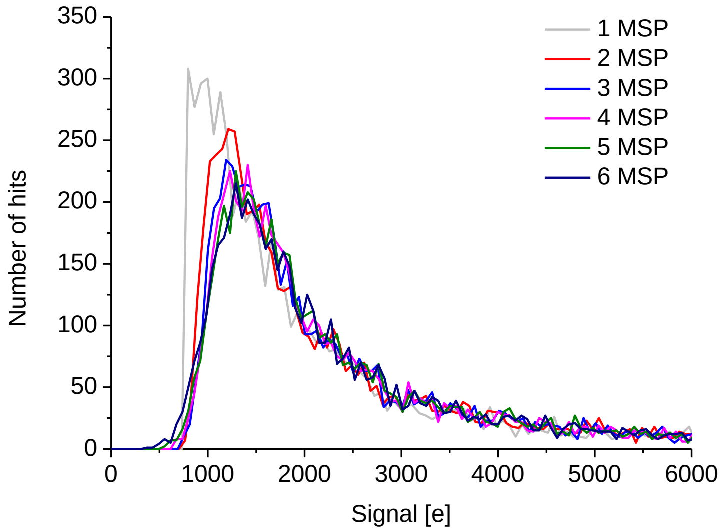
- **We expect a good tolerance to non-ionizing damage** thanks to the **small drift distance** and **high drift speed in the depleted area**. Due to high dopant density the type inversion should occur at higher fluencies.
- Concerning the **ionizing damage**, we can benefit from the **properties of the used deep submicron CMOS technology**. In **contrast to the most of the MAPS**, we can **rely on PMOS transistors** inside pixels that are more radiation tolerant than NMOST.

Experimental results – irradiation studies

- Besides HVPixelM1 (first version) we have used for the irradiation tests the pixel matrices for the CCPD. They contain pixels with charge sensitive amplifiers, and leakage current compensation.
- Due to the continuous-mode leakage current compensation, these pixels are less sensitive to the increase of the leakage currents

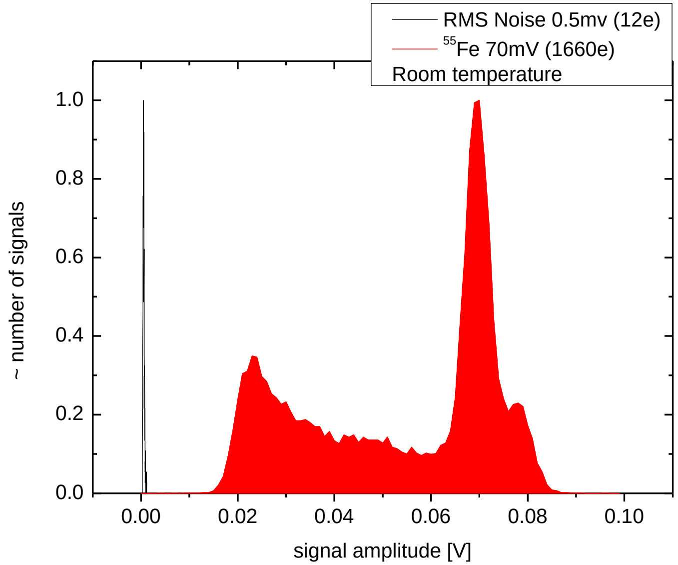
Increase of the detector leakage current from 350fA to 130pA per pixel
Seed pixel signal decrease from 1300e to 1000e.
The measurement has been performed at 0C



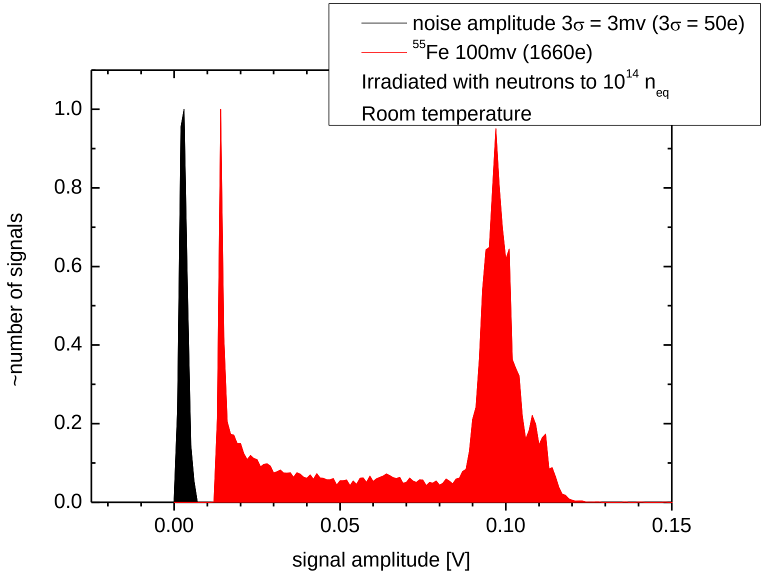


Irradiation with neutrons (10^{14} n_{eq}/cm^2) – noise

^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e

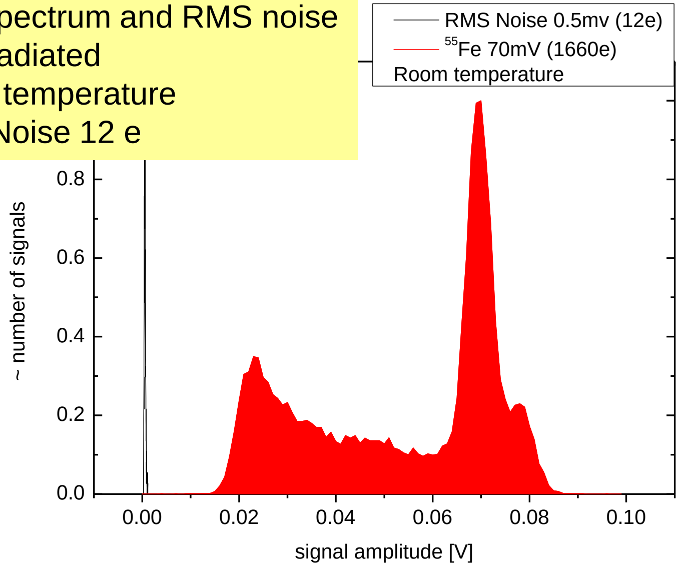


^{55}Fe spectrum and noise amplitude
Irradiated with neutrons (10^{14} n_{eq})
Room temperature
Noise amplitude (~3 sigma) ~ 50 e

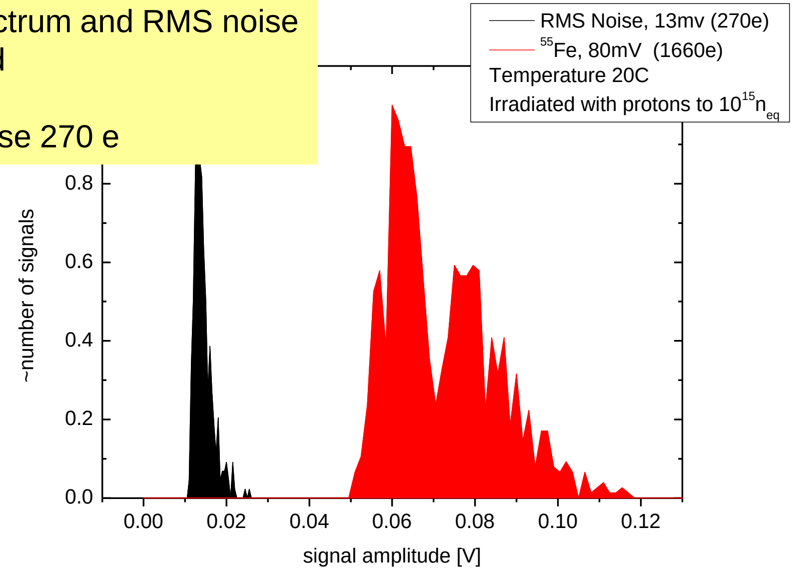


Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)

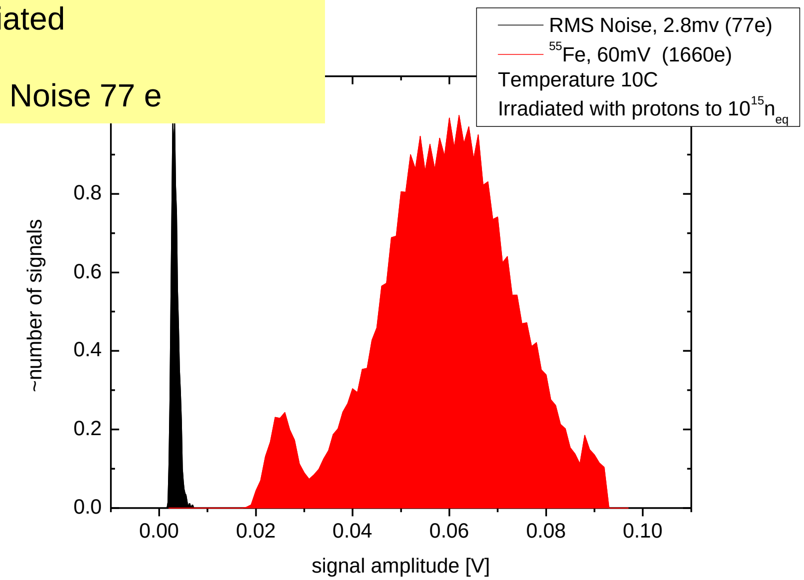
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



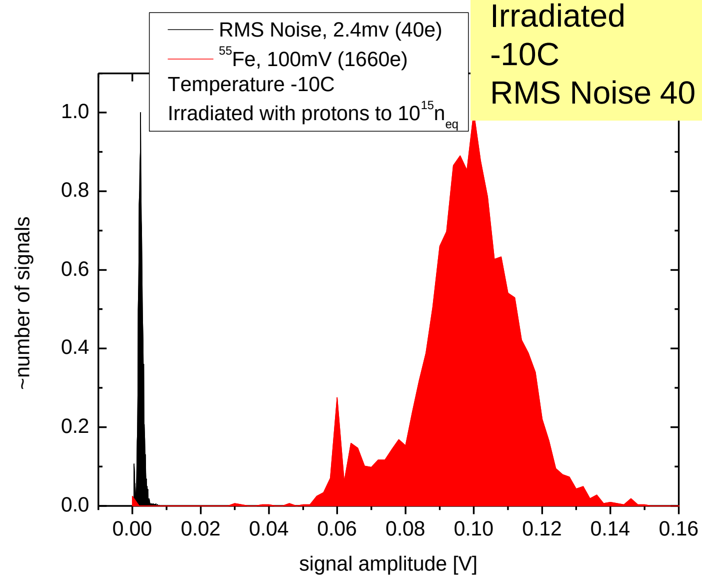
^{55}Fe spectrum and RMS noise
Irradiated
20C
RMS Noise 270 e



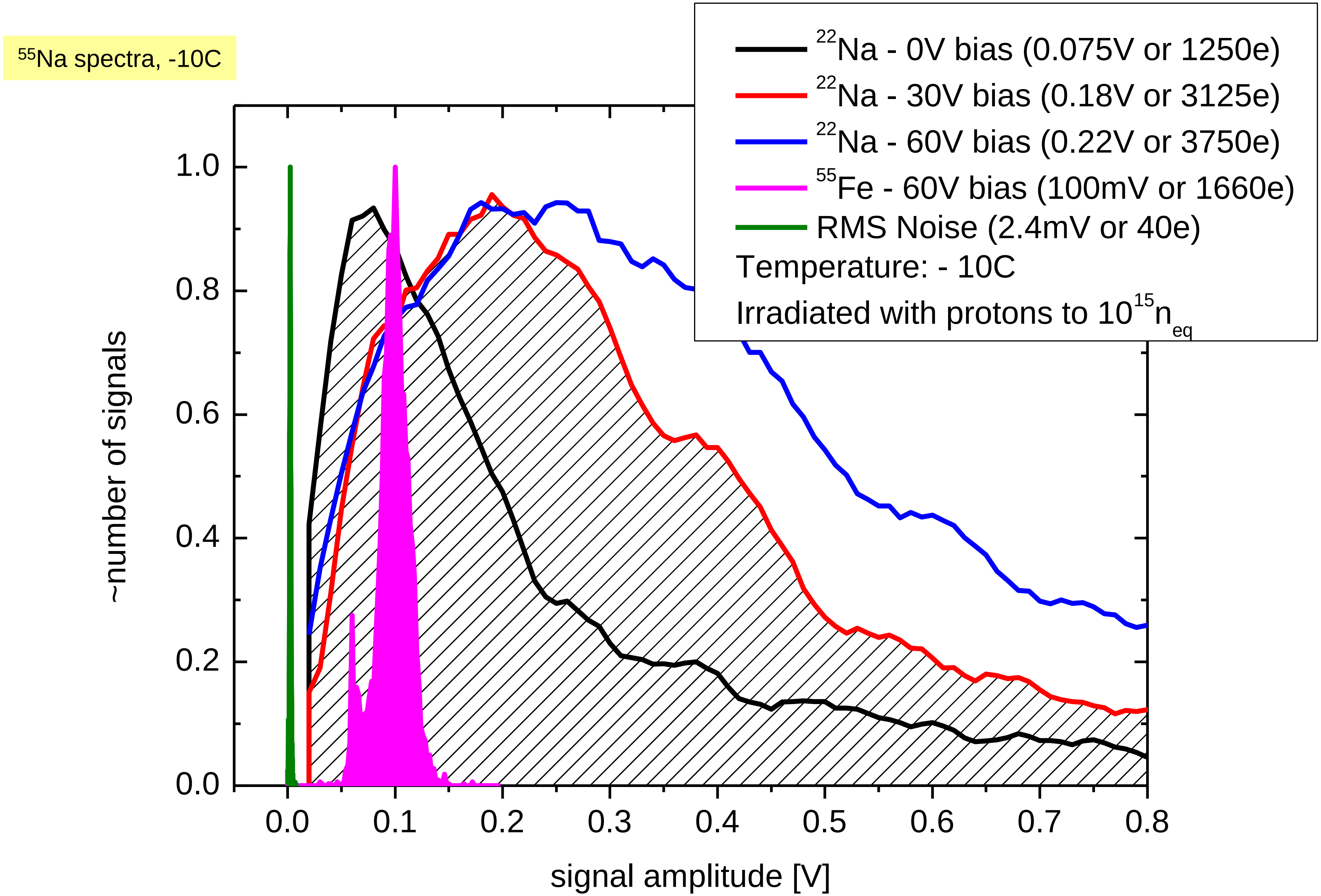
^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e



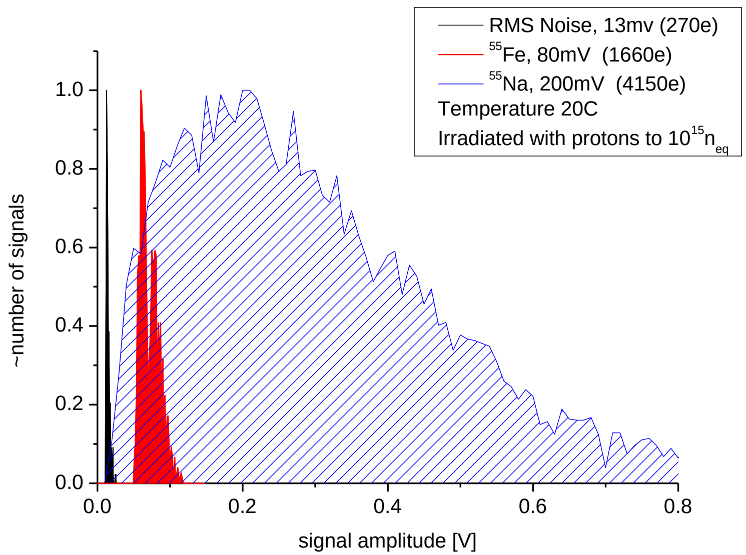
^{55}Fe spectrum, RMS noise
Irradiated
-10C
RMS Noise 40 e

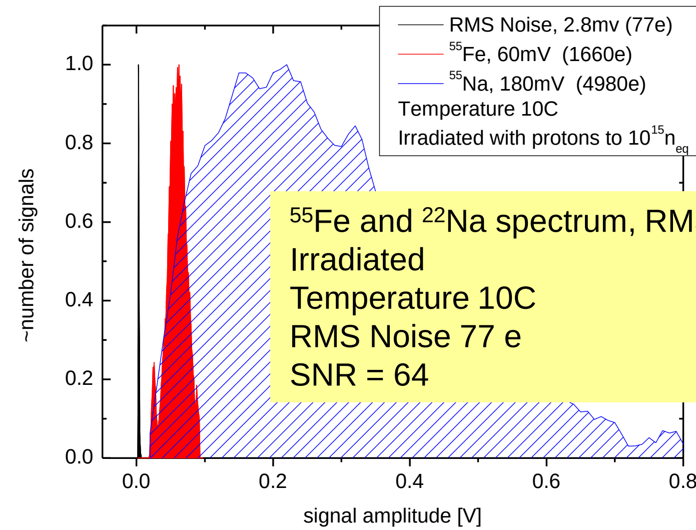


Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)



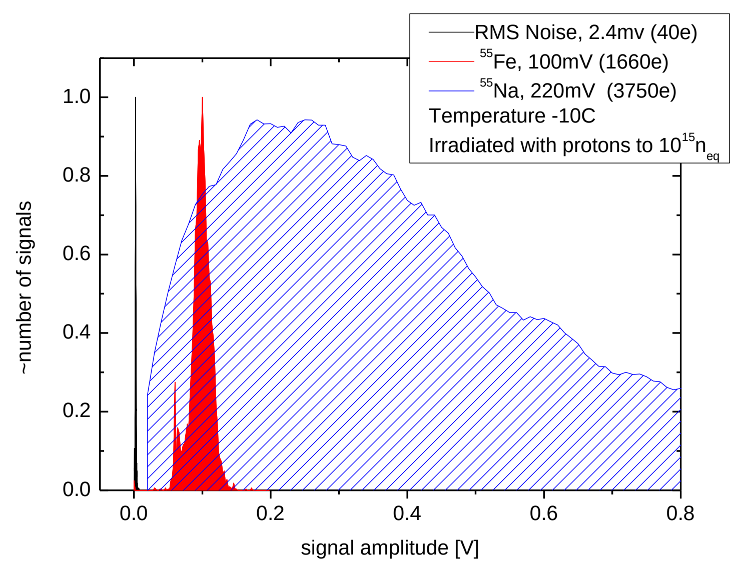
Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)





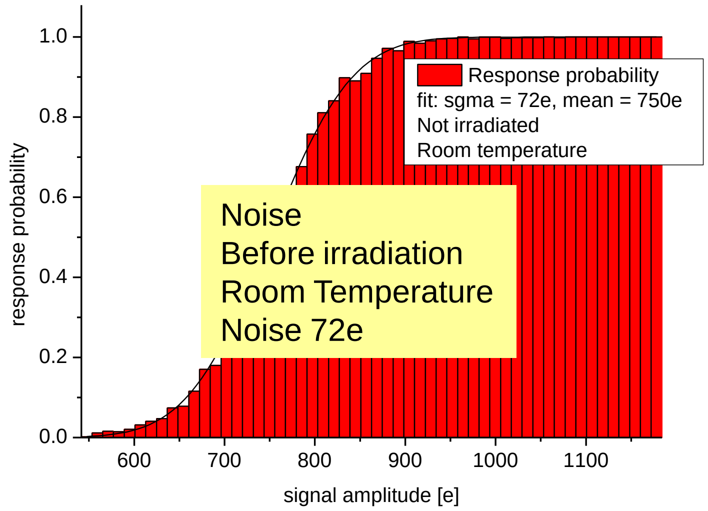
^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature 10C
RMS Noise 77 e
SNR = 64

^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature 20C
RMS Noise 270 e
SNR = 15

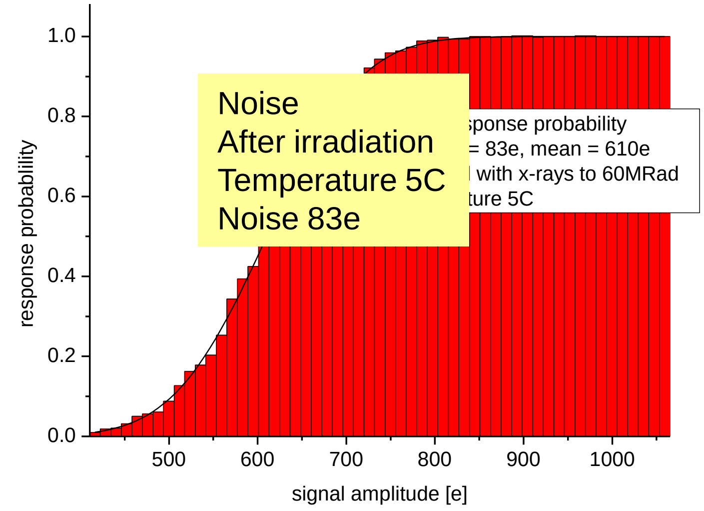


^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature -10C
RMS Noise 40 e
SNR = 93

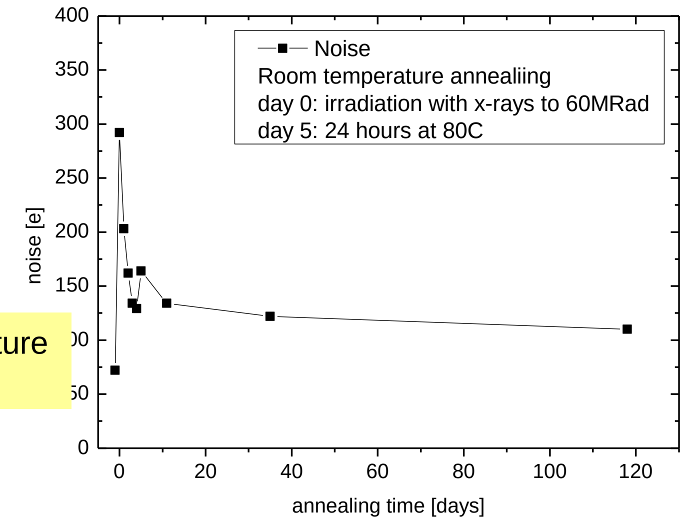
Irradiation x-rays (50 MRad)



Noise
Before irradiation
Room Temperature
Noise 72e

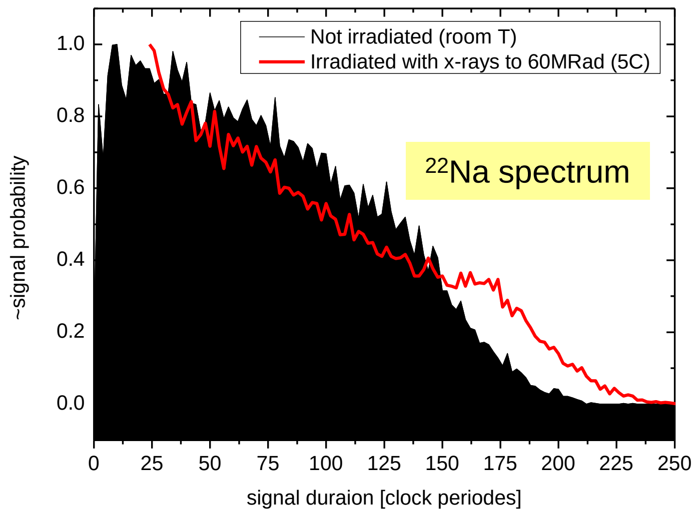


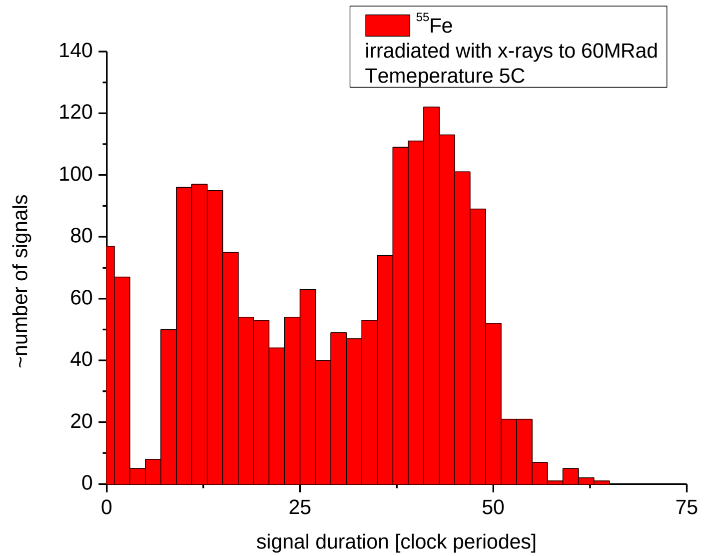
Noise
After irradiation
Temperature 5C
Noise 83e



Noise at room Temperature
Vs. annealing time

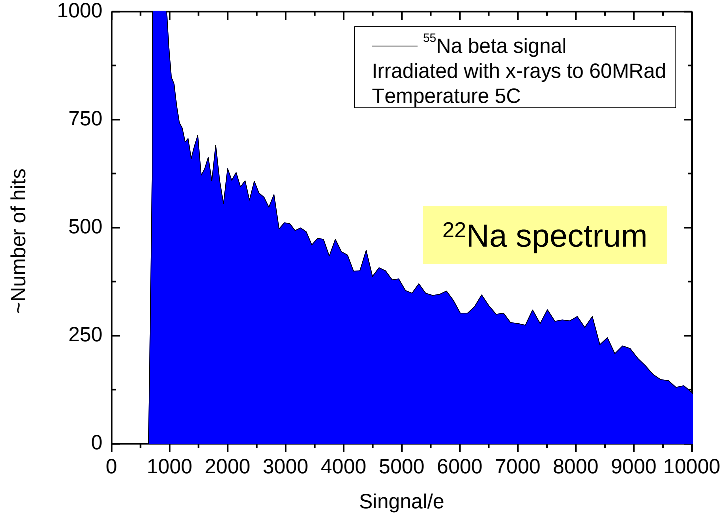
Irradiation x-rays (50 MRad)





^{22}Na spectrum

^{22}Fe spectrum



^{22}Na spectrum

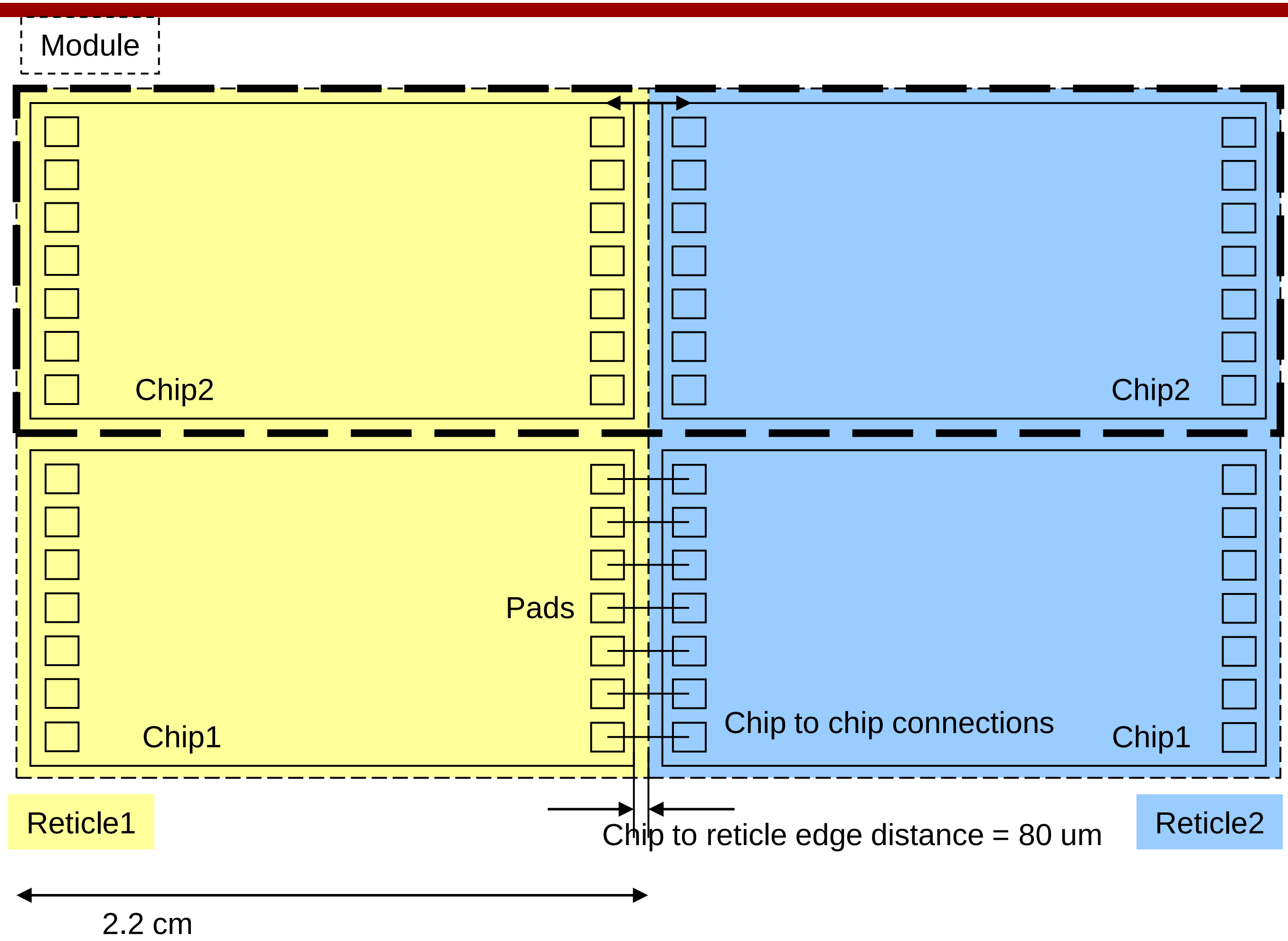
Summary

- We have developed a new pixel sensor structure (smart diode array) for high energy physics that can be implemented in a high voltage CMOS technology
- The sensor has 100% fill-factor and can have in-pixel electronics implemented with p- and n-channel transistors
- We have implemented the sensor structure in various variants
- 1) Sensor with in-pixel hit detection and sparse readout
- 2) Sensor with fast frame readout and simple pixel electronics
- 3) sensor with capacitive readout
- We measure excellent SNR in all three cases
- We have done a test-beam measurement with the first version of the frame readout detector with good results
- The SNR of the second chip version is four times better
- Excellent seed pixel SNR of almost 100 has been achieved
- We have irradiated the chips with neutrons, protons and x-rays to test radiation tolerance
- After irradiation with protons up to extremely high fluence 10^{15} n_{eq} and dose 300MRad, we have still very large SNR (>40) for high energy beta particles at nearly room temperatures (10C)

Outlook

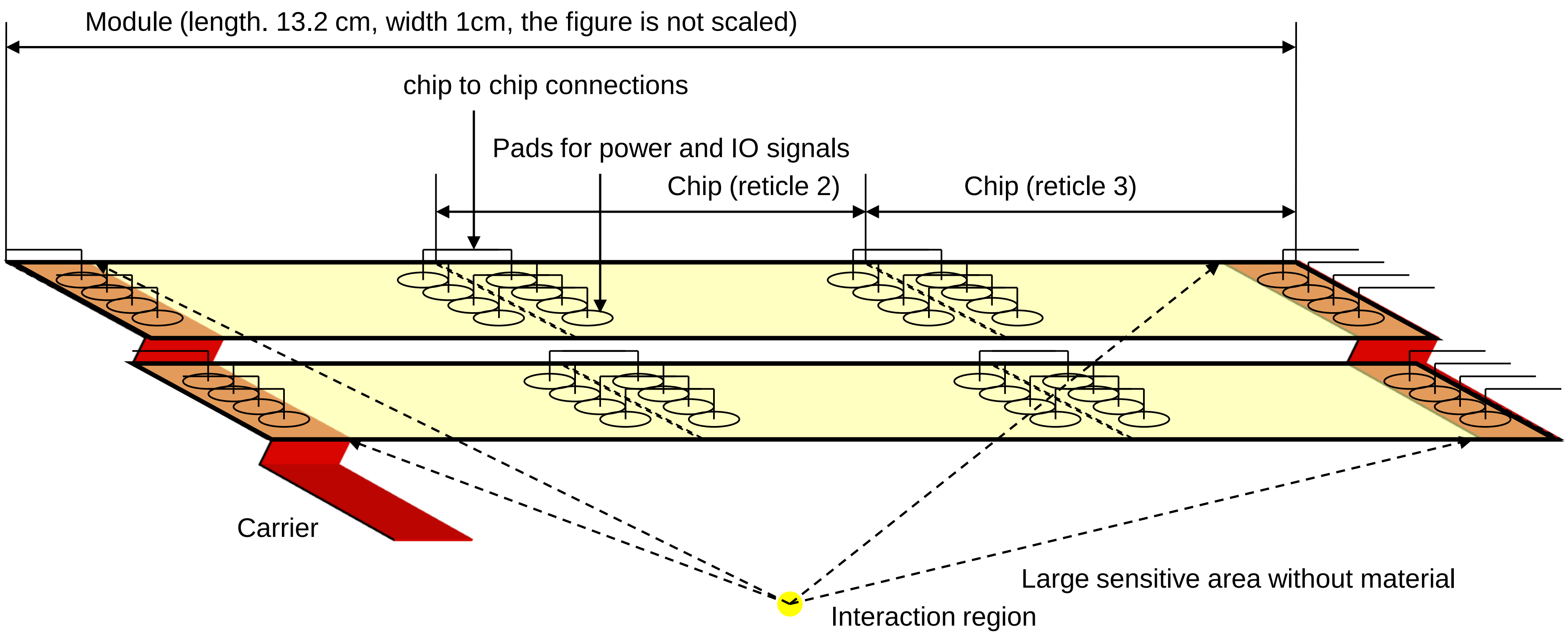
- The engineering run in the used technology costs only 98k €
- By proper arrangement of the dices, we can obtain long monolithic multi-reticle sensors with 13.2cm length and 1cm width
- We would have 8 such modules per wafer and one engineering run could give us up to 48 modules

Multi-reticle module



Very long low-cost pixel modules with (almost) no insensitive area can be produced
Reticle-reticle connections can be made easily by wire bonding
Instead of wire-bonding, an extra metal layer can be used as well

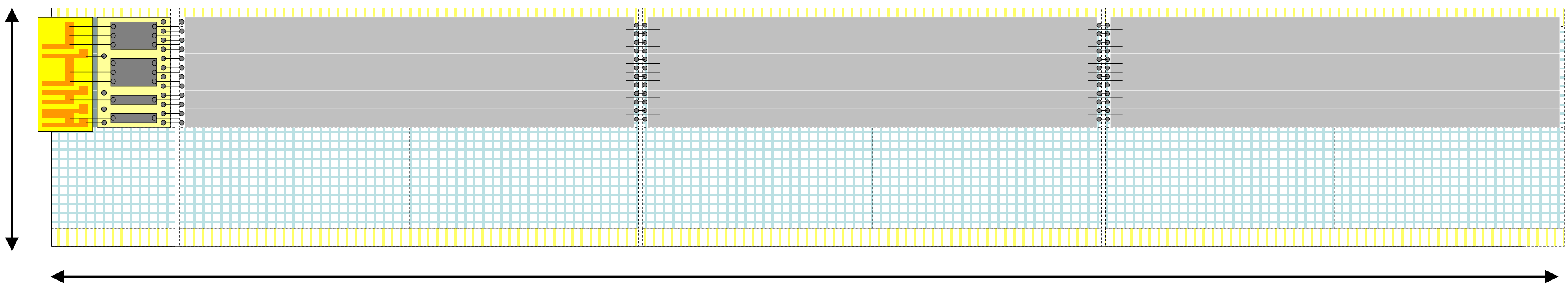
Multi-reticle module



Very low-mass only silicon modules are possible as well (similar to DEPFET module for Belle II)

SDA long module

1 cm



13.2 cm (one half of the module shown)

Thickness: below 50 µm possible
Achieved performances by scaling up of the present design:
Pixel size: 40 x 80 µm (or less)
Number of pixels: 256 x 768
Readout time: 40 µs
Radiation tolerance: at least 10^{15} n_{eq} and 50 Mrad
Power consumption (~frame rate): 2 W/module (10 µW/pixel)

- Thank you!

- Backup slides

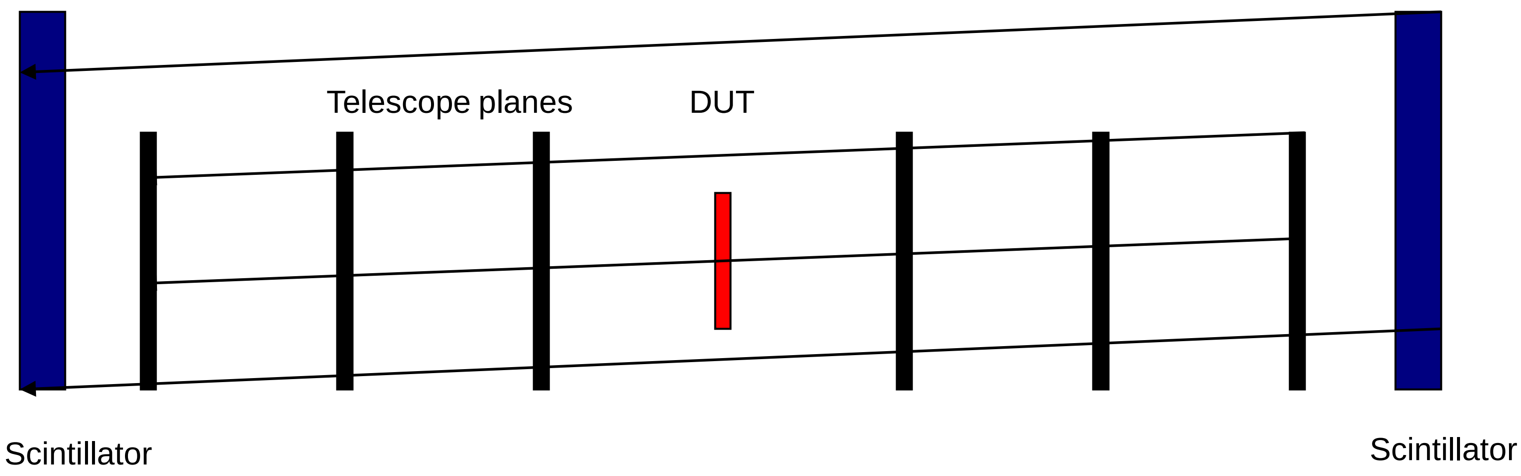
Strong points

- 1) CMOS in-pixel electronics
- 2) Good SNR
- 3) Fast signal collection
  - Theoretically 40ps
- 4) High tolerance to non-ionizing radiation damage
  - High drift speed
  - Short drift path
- 5) High tolerance to ionizing radiation
  - Deep submicron technology
  - Radiation tolerant design can be used
  - Radiation tolerant PMOS transistors can be used (in contrast to MAPS with high-resistance substrate)
- 6) Thinning possible
  - Since the charge **collection is limited to the chip surface**, the **sensors can be thinned**
- 7) Price and technology availability
  - Standard technology without any adjustment is used
  - Many industry relevant applications of HV CMOS technologies assure their long tern availability

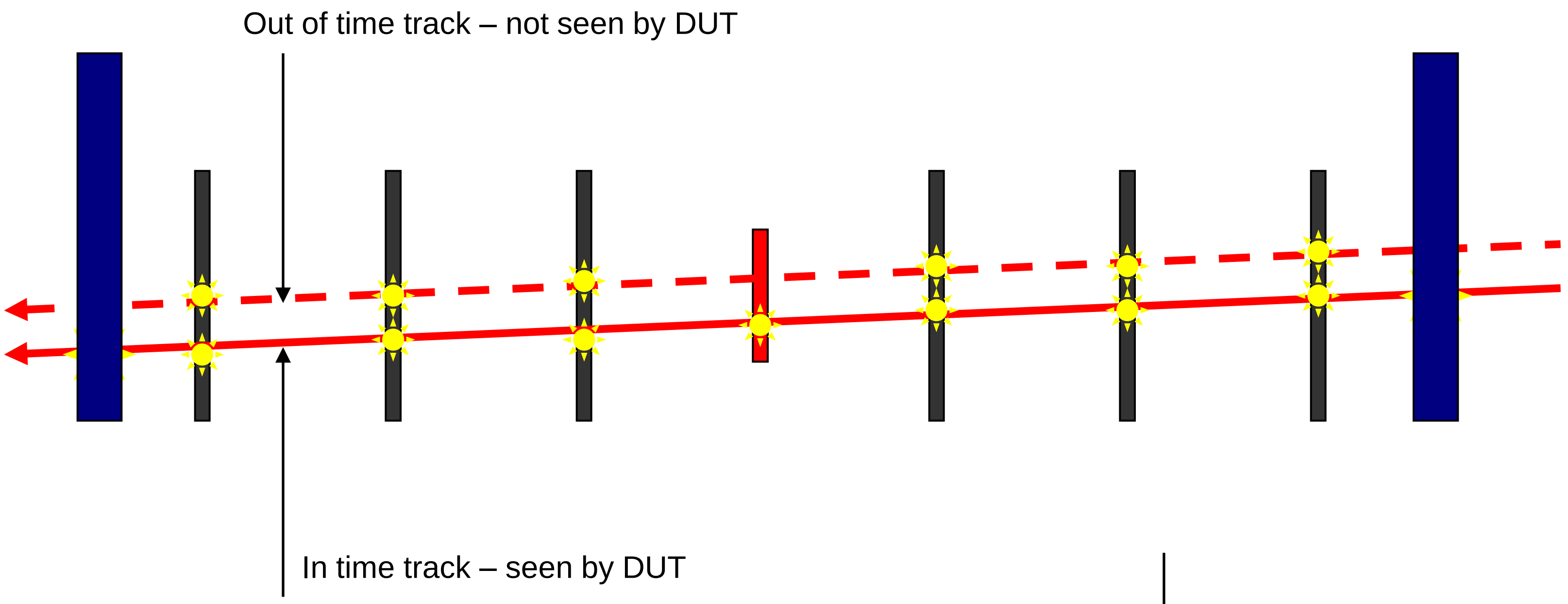
Drawbacks

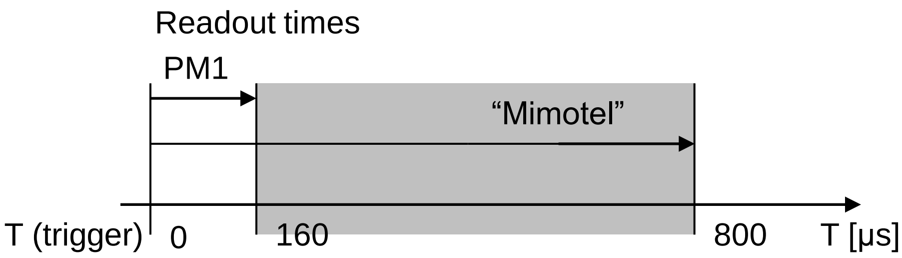
- 1) Capacitive feedback
  - must be taken into account when the pixels are designed and simulated.
  - In some cases the capacitive feedback can be used, for instance if provides a feedback capacitance for the charge sensitive amplifier.
  - **Despite some limitations**, we can implement the majority of important pixel circuits in CMOS, like the charge sensitive amplifier, shaper, tune DAC, SRAM…
  - Note that PM2 achieves 21 e noise despite oh huge charge injection (10 fC = 60000 e)
  - **Charge injection does not mean high noise**
- 2) Relatively large size of the collecting electrode
  - However the high voltage deep n-well has relatively **small area capacitance**.
  - Typical values for the total n-well capacitance are from 10fF (small pixels and simple pixel electronics) to 100fF larger CMOS pixels.
  - Despite of the capacitance, we achieve excellent SNR values.

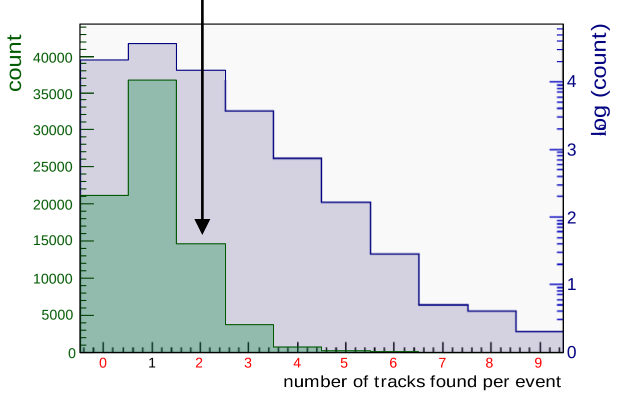
Track and system geometry



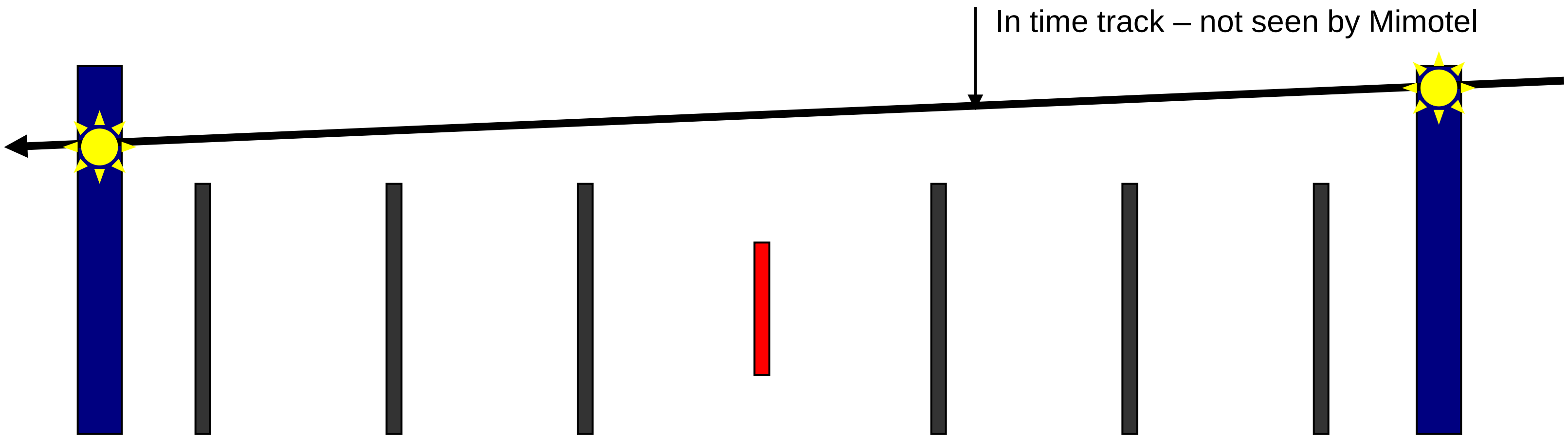
(Irregular events) double track event

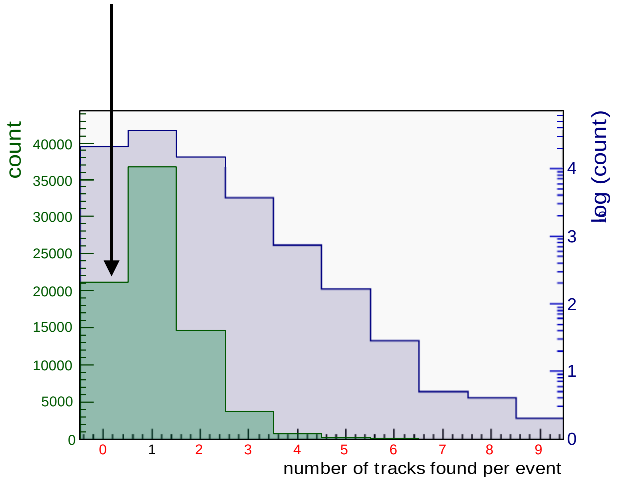




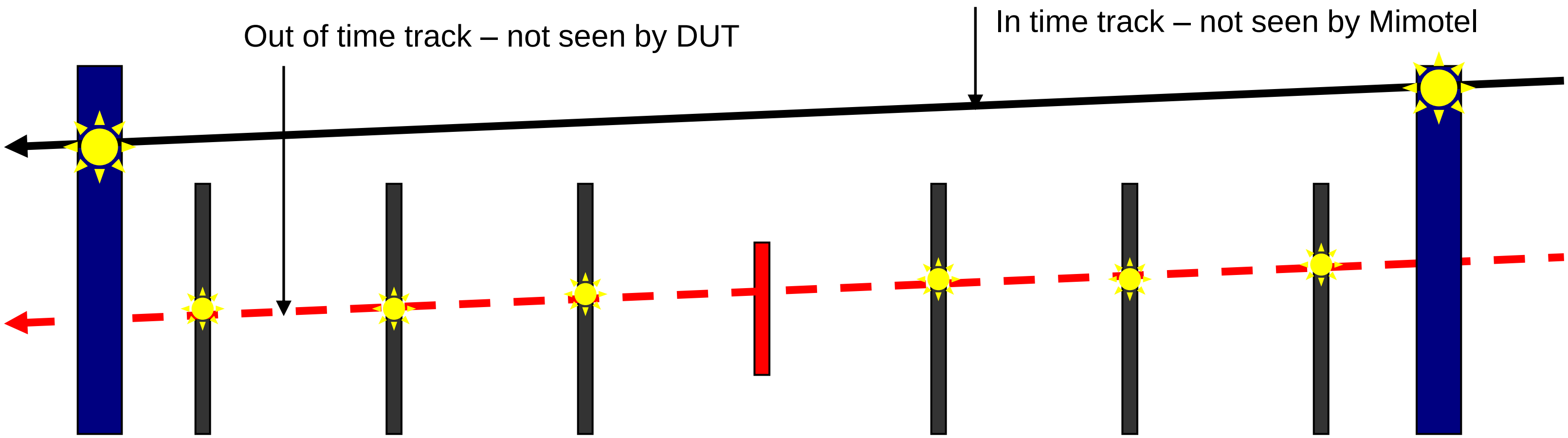


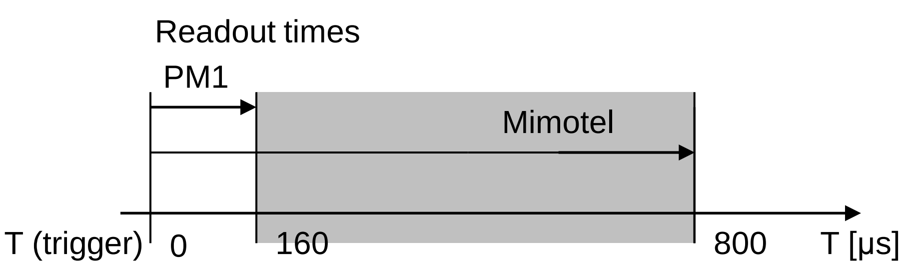
(Irregular events) empty event

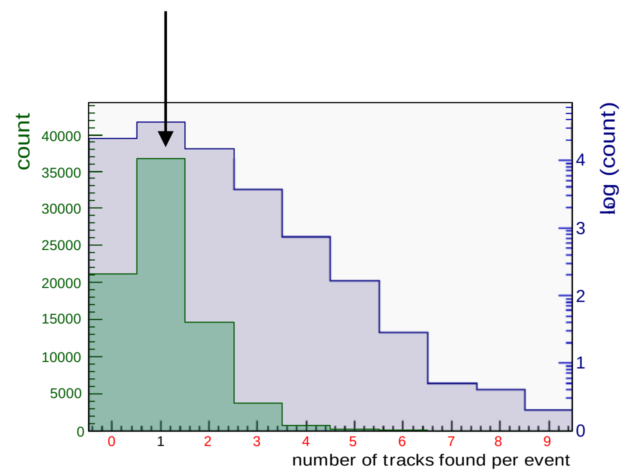


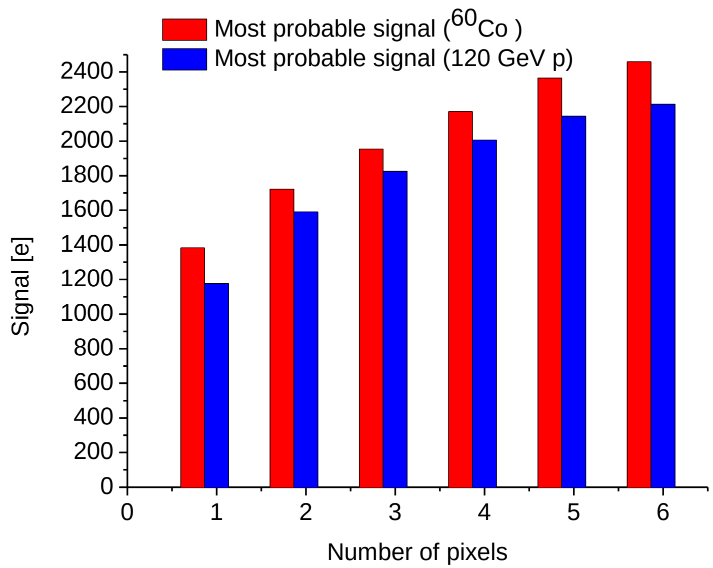


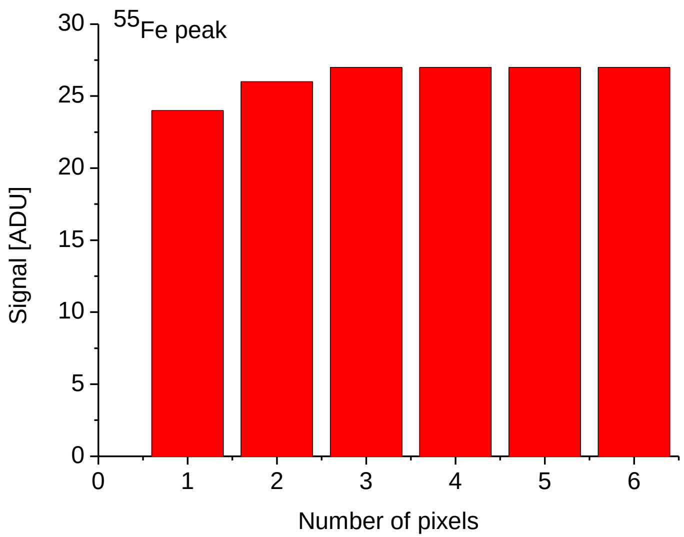
(Irregular events) double track event seen as a single track event









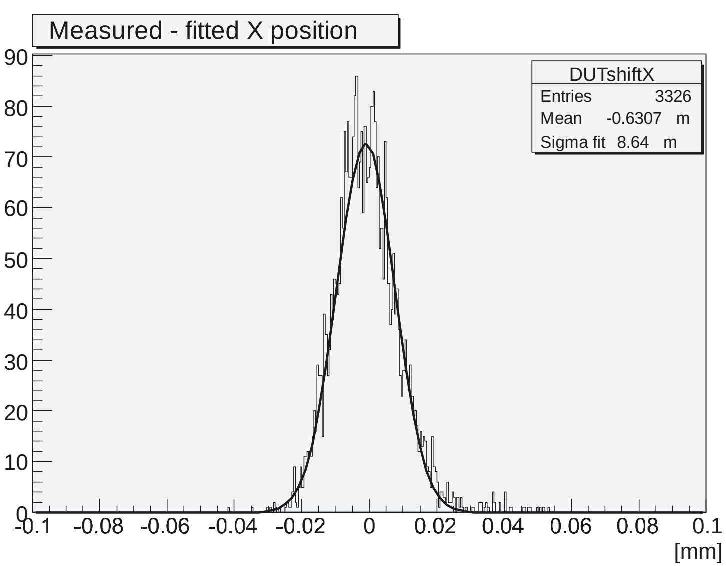


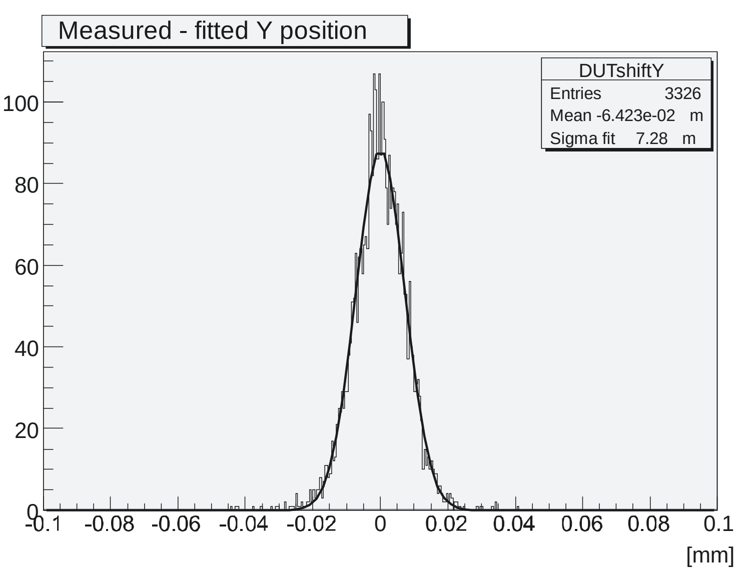
Comparison between **^{60}Co** and **120GeV proton** spectra
^{60}Co signals higher by 10% - expected from theory due to lower particle energy
Seed pixel sees about 50% of the total signal
The next MSP sees only 25% of the seed pixel signal
Cluster size is 6 pixels
Moderate charge sharing (the seed gets the most)

As comparison **^{55}Fe**
Seed pixel sees about 90% of the total signal
Cluster size is 3 pixels
No charge sharing

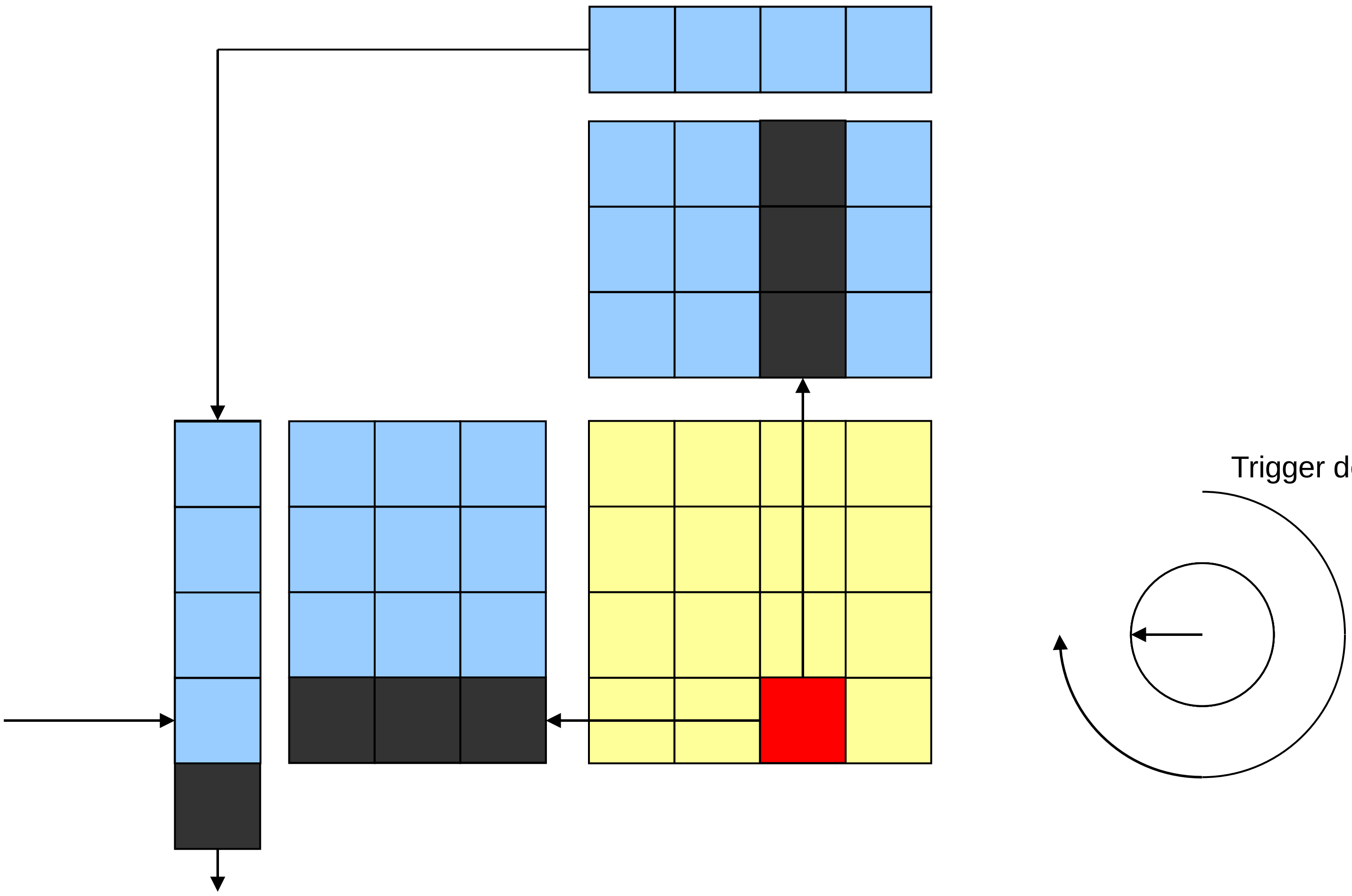
Spatial resolution

- Spatial resolution
- Sigma residual **X: 7.3 μm**
- Sigma residual **Y: 8.6 μm**
- The **difference** is probably caused by the **bricked pixel geometry** – still not understood completely, simulations will be done
- The spatial resolution is **not as good as in the case of standard MAPS** due to **absence of charge** sharing in the case of primary signal

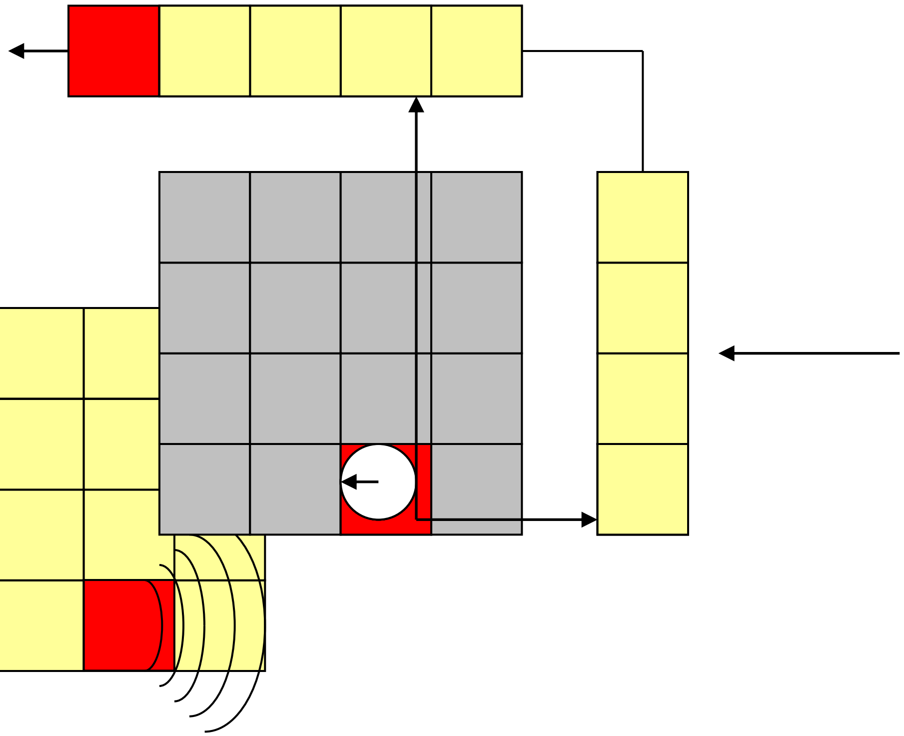




Sparse readout for monolithic detector

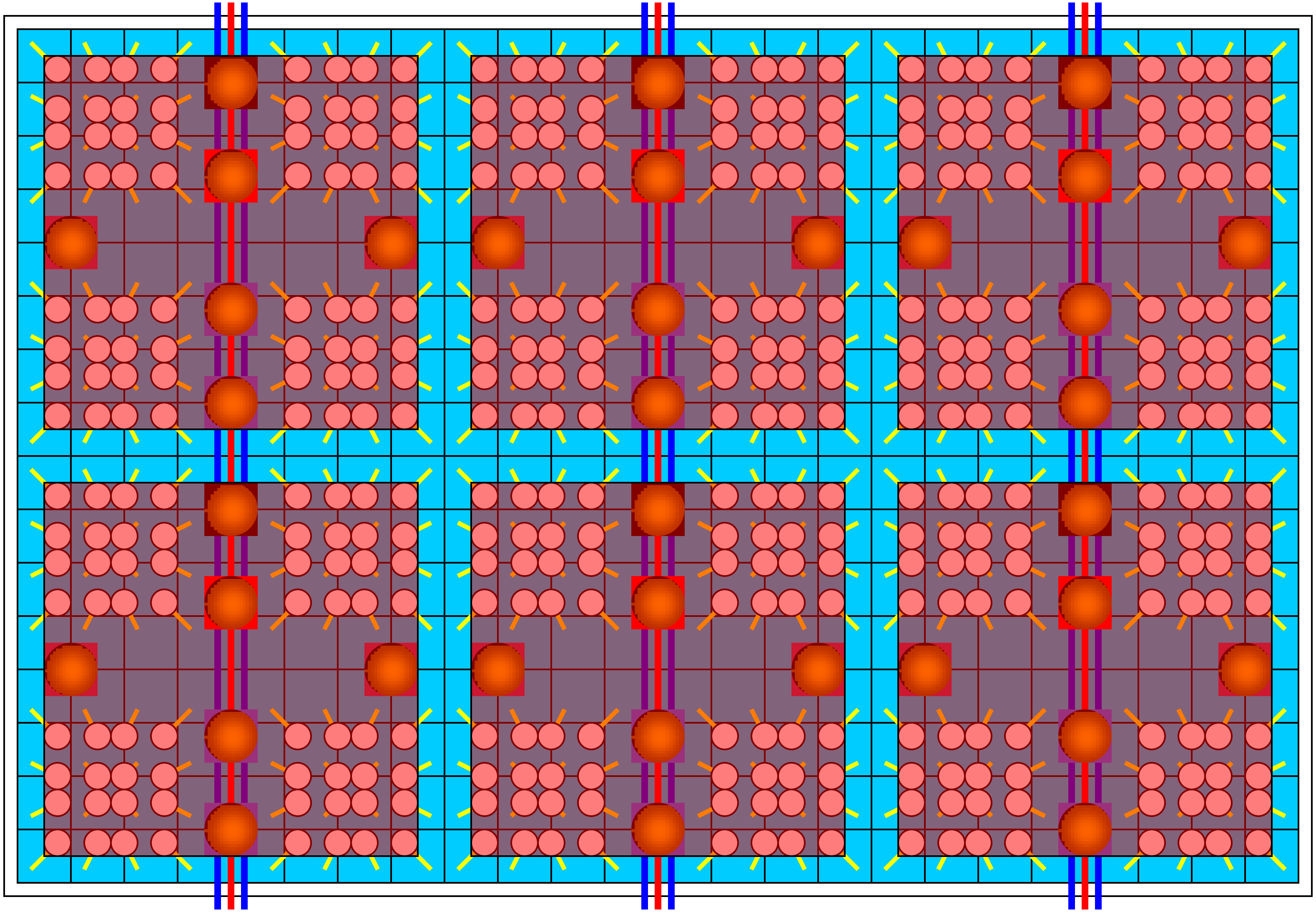


Sparse readout for CCPD

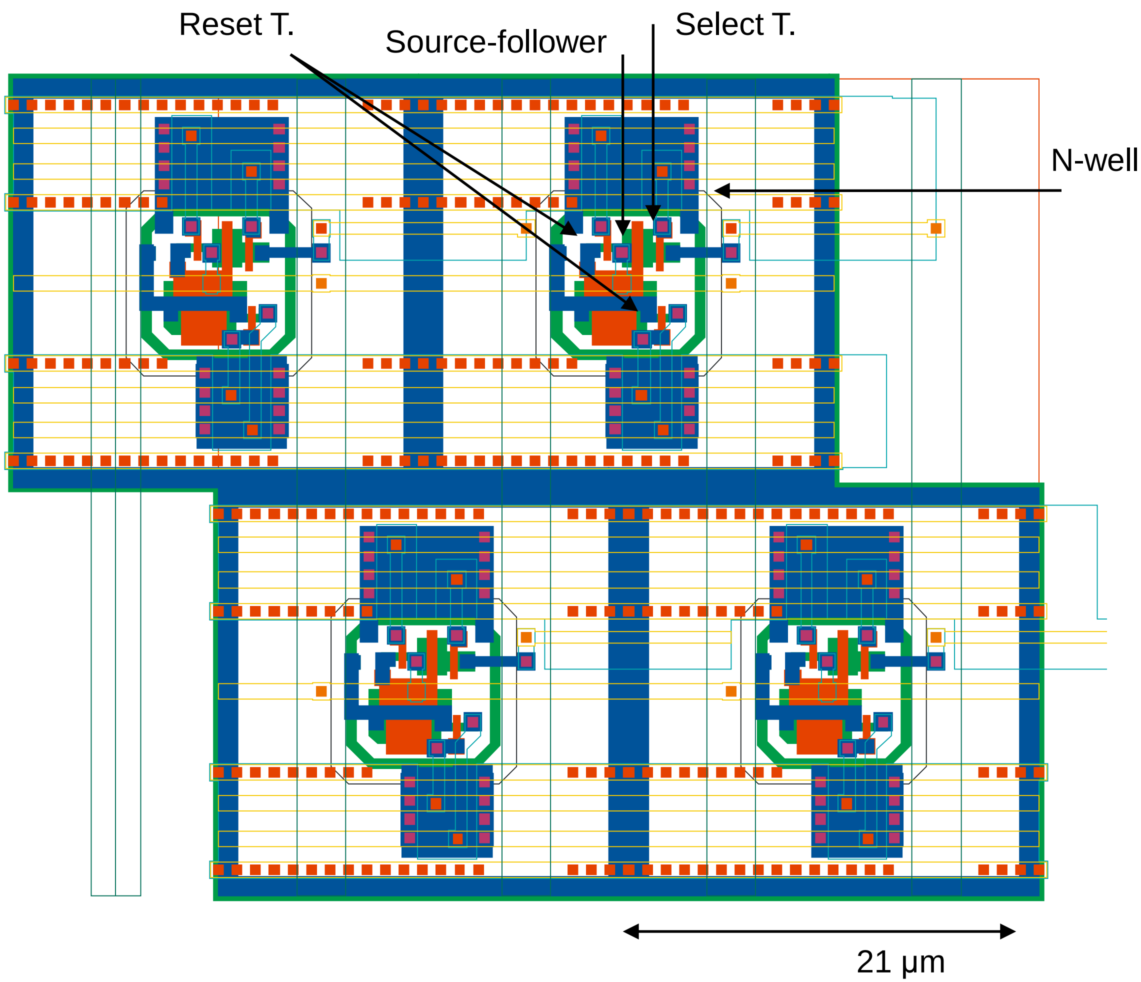


CCPD2 sensor concept

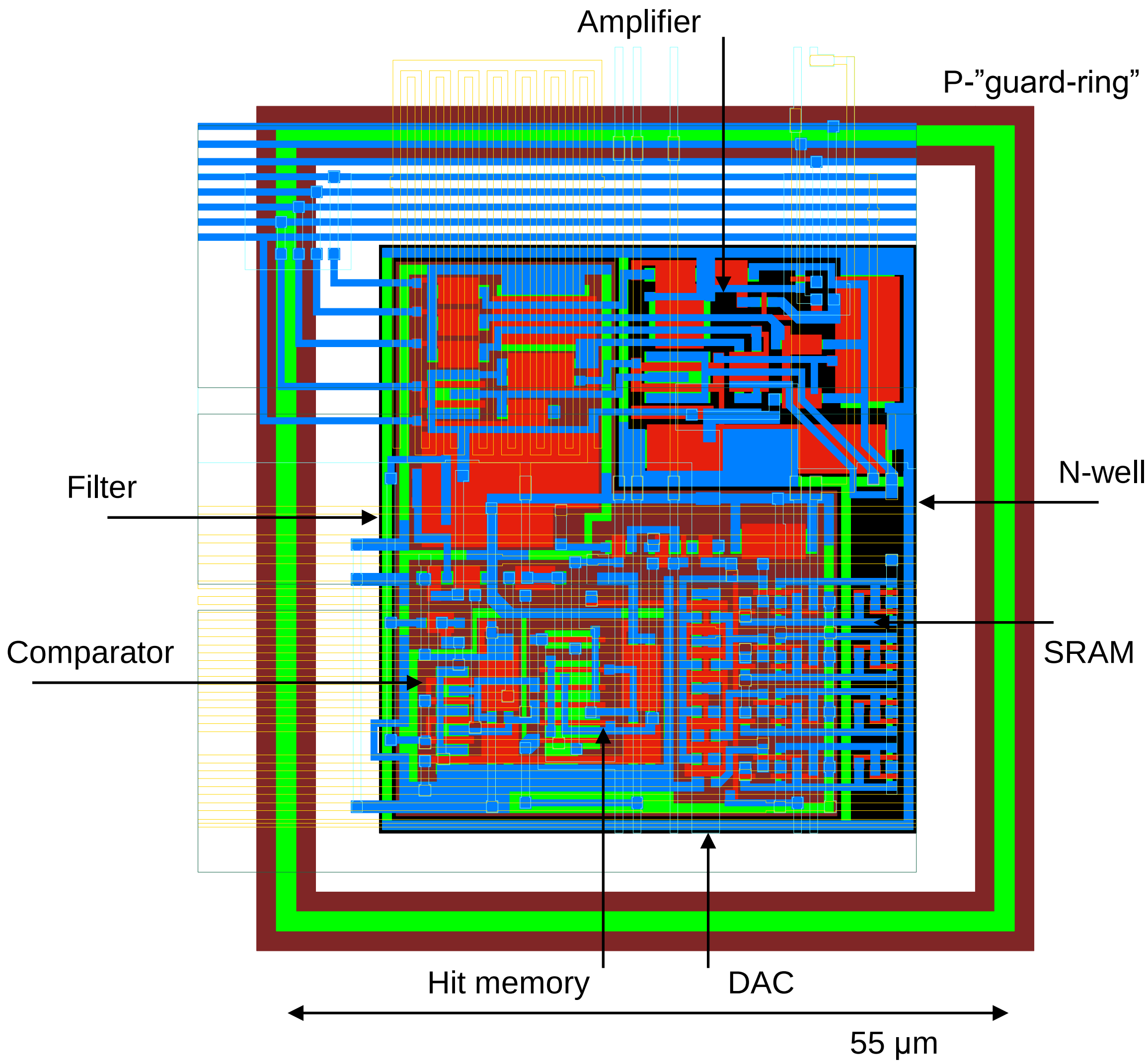
PixeSensor elecrodes for ROC placed under the flipchip ROC area Space for bumps by ROCs



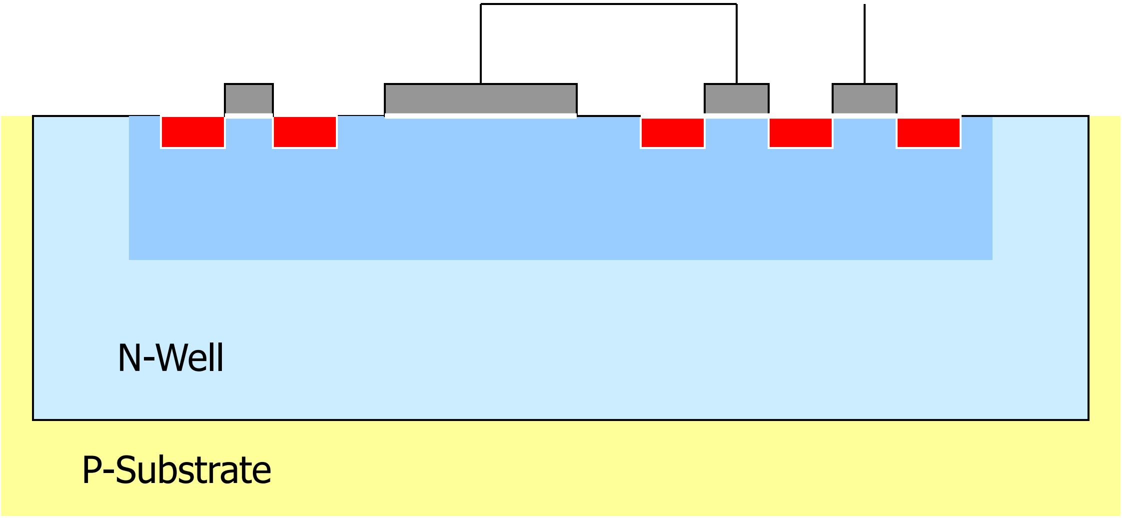
PM2 pixel layout

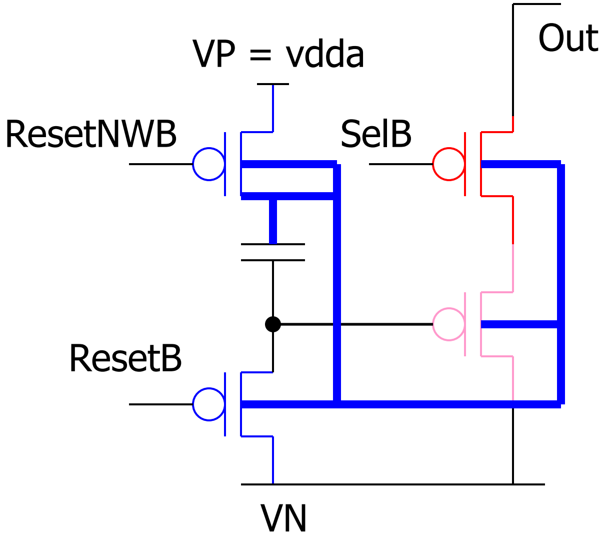


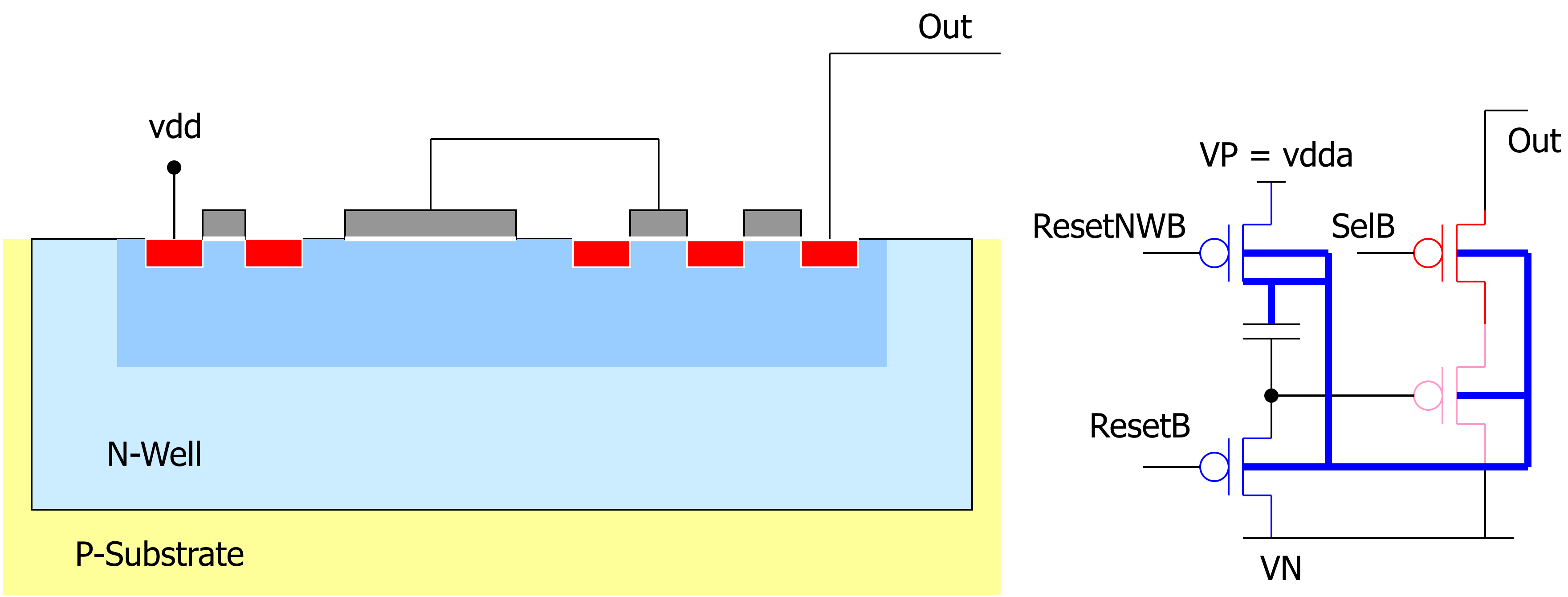
HV1 pixel layout



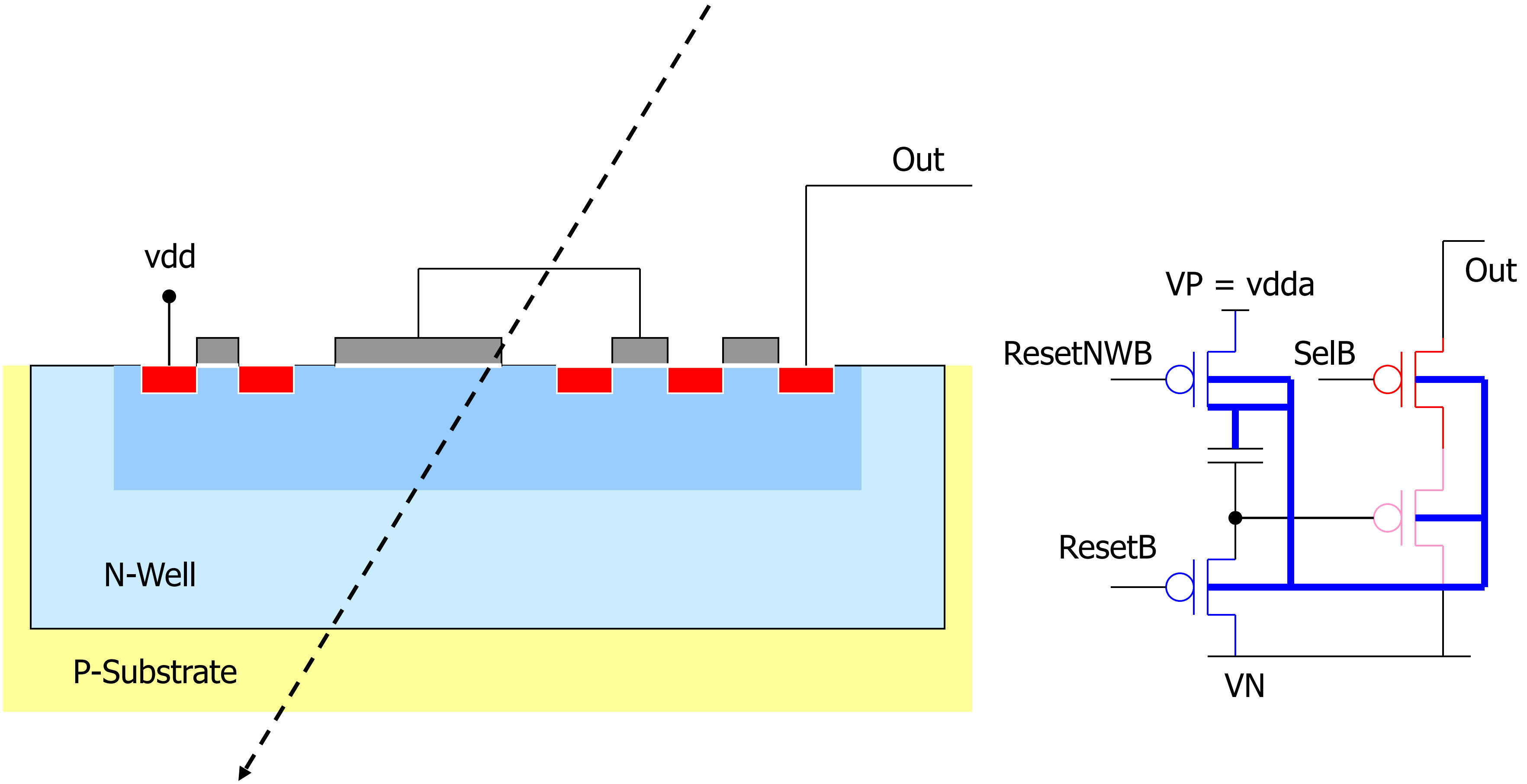
Simple pixel cross-section



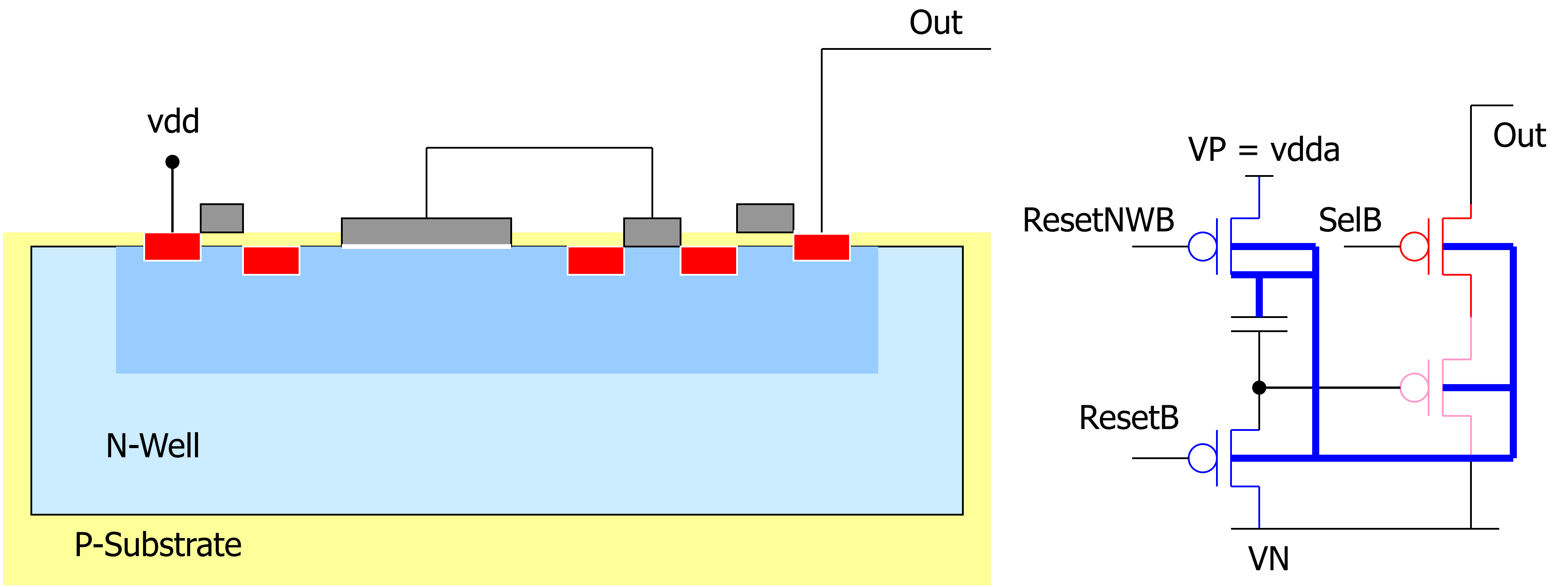


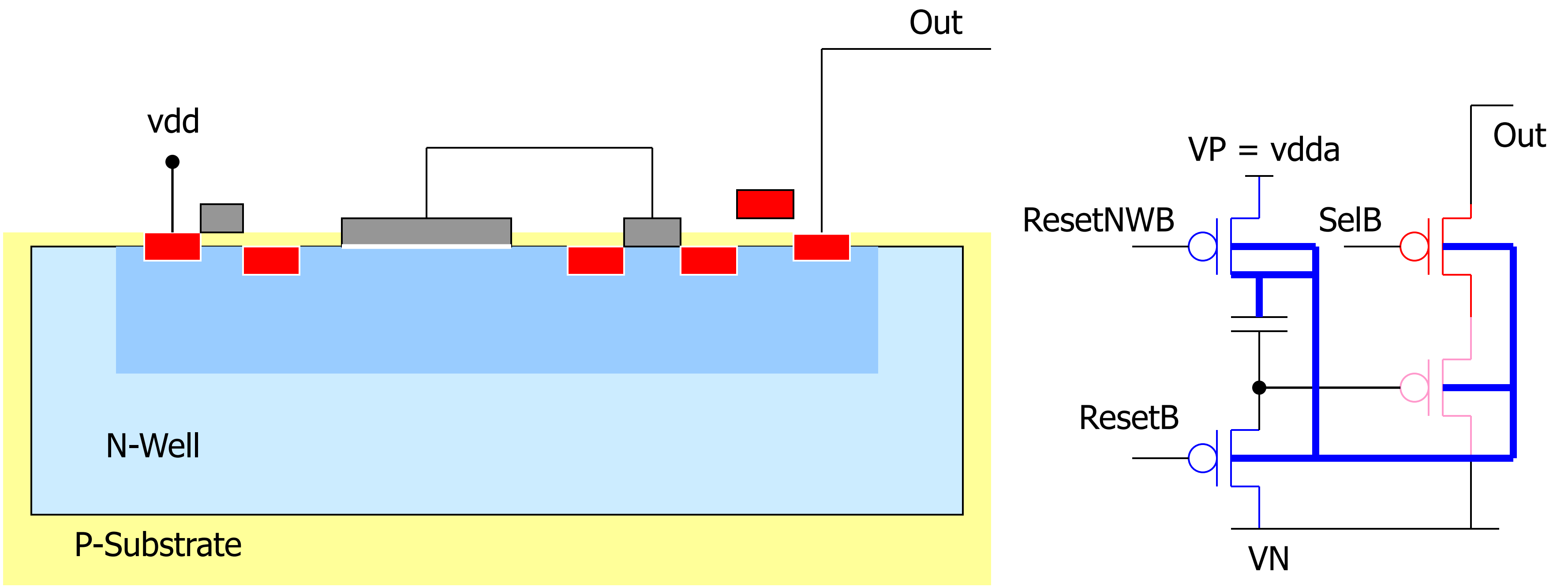

Out
vdd
N-Well
P-Substrate
VP = vdda
Out
ResetNWB
SelB
ResetB
VN

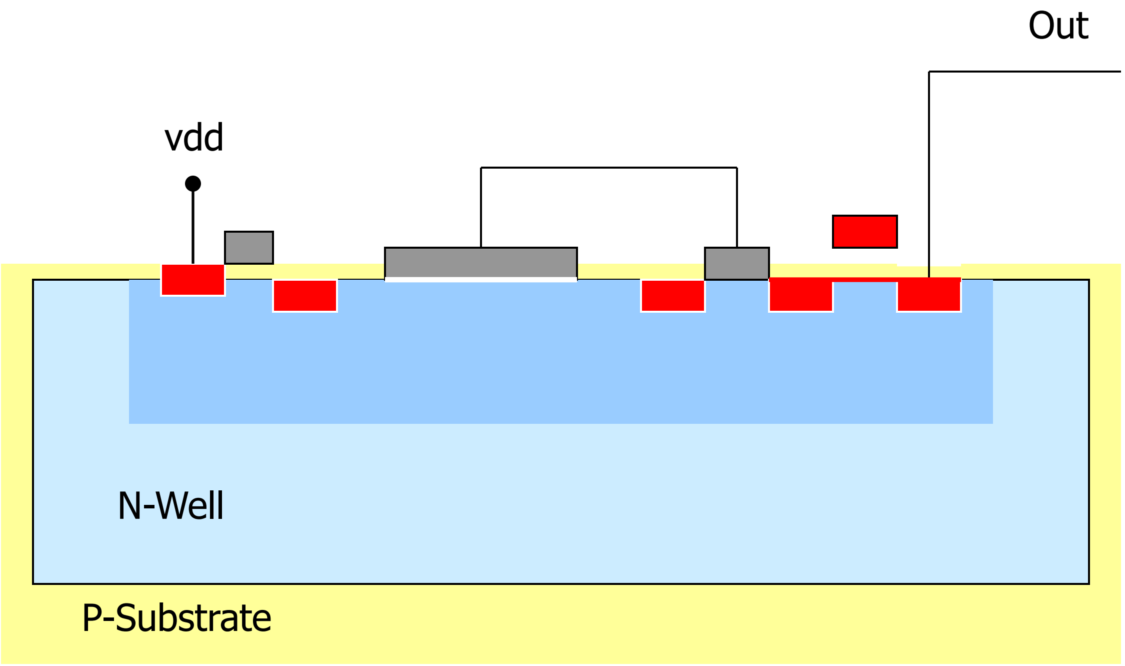
Hit

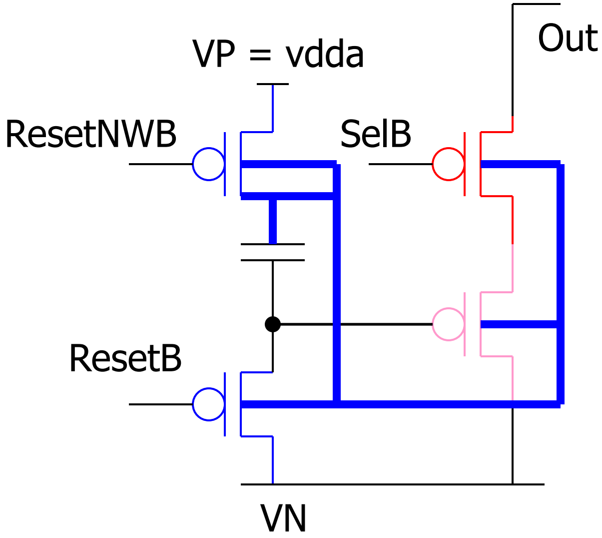


Out
vdd
N-Well
P-Substrate
VP = vdda
Out
ResetNWB
SelB
ResetB
VN

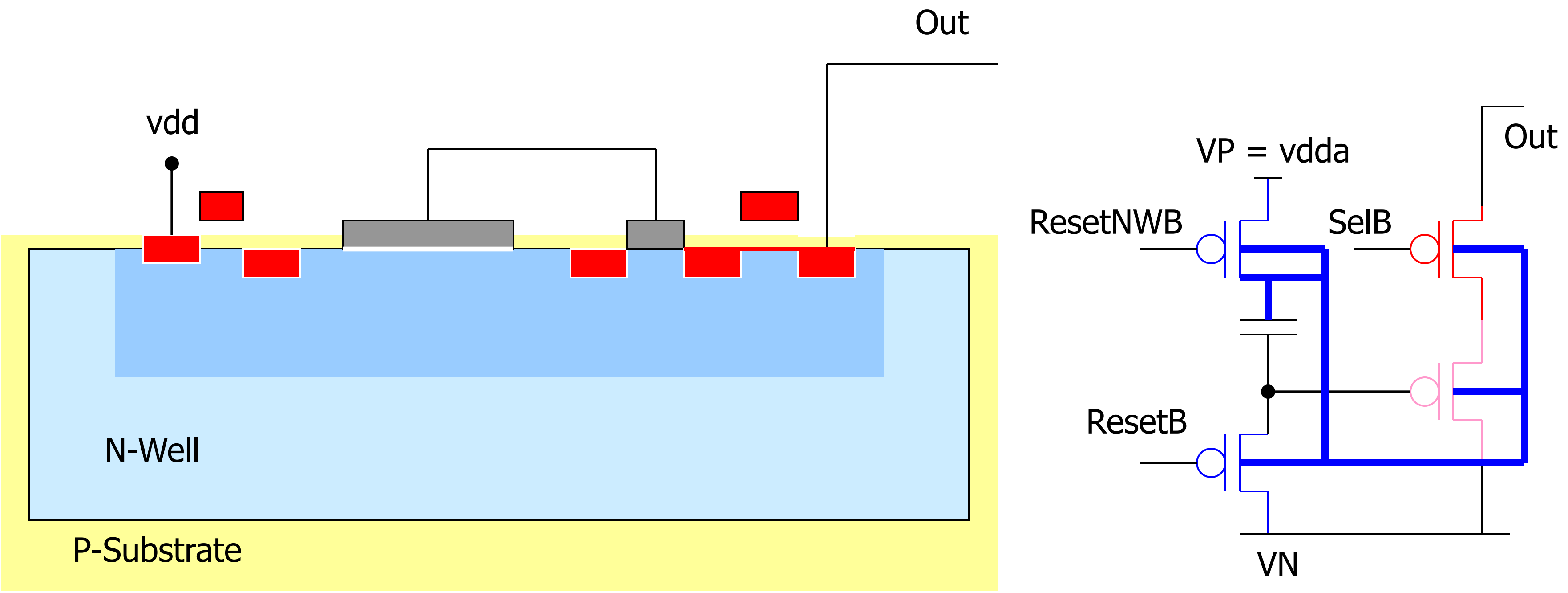

Out
vdd
N-Well
P-Substrate
VP = vdda
Out
ResetNWB
SelB
ResetB
VN


Out
vdd
N-Well
P-Substrate
VP = vdda
Out
ResetNWB
SelB
ResetB
VN

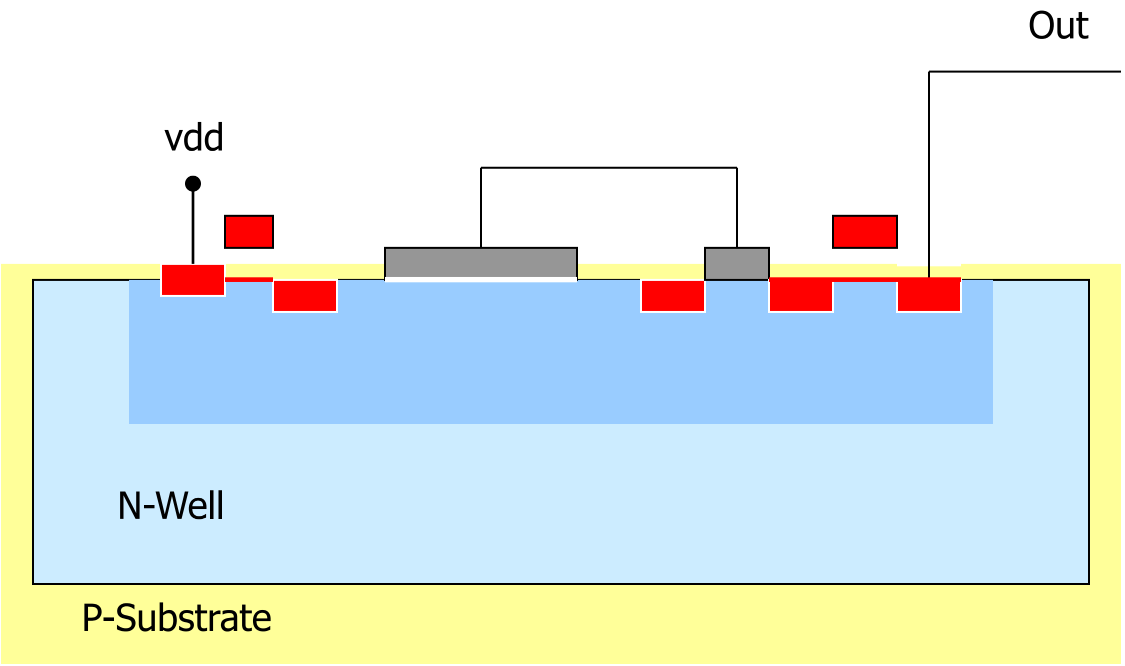

Out
vdd
N-Well
P-Substrate


Out
VP = vdda
ResetNWB
SelB
ResetB
VN

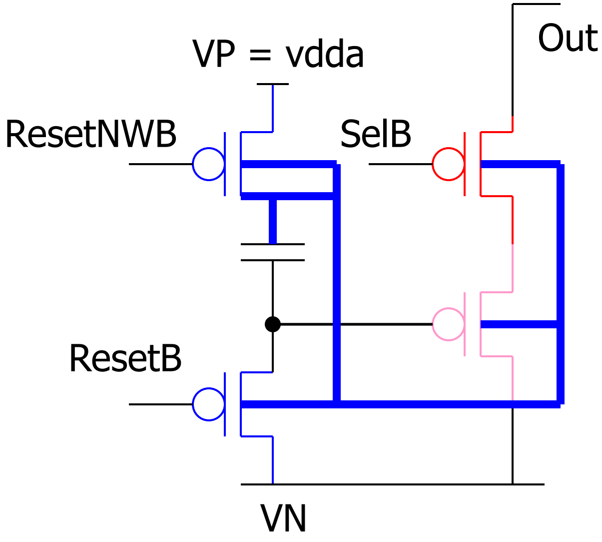
Reset


Out
vdd
N-Well
P-Substrate
VP = vdda
Out
ResetNWB
SelB
ResetB
VN

Reset

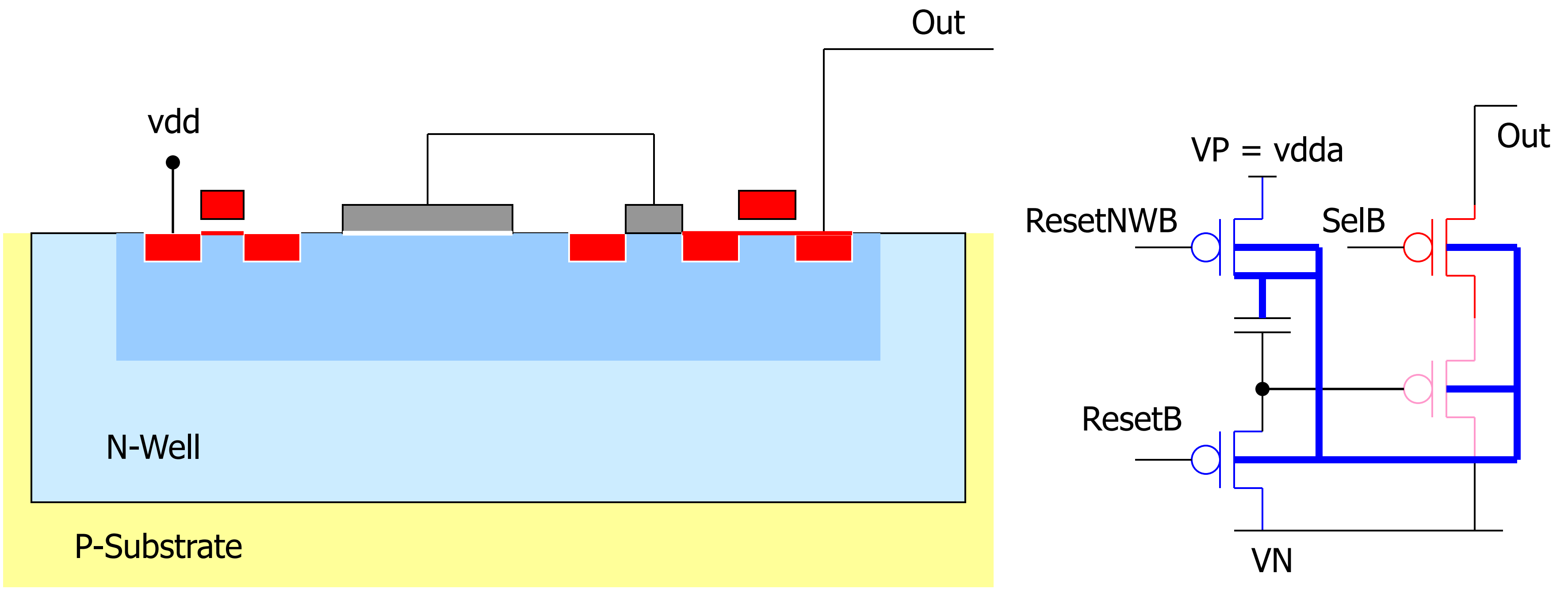


Out
vdd
N-Well
P-Substrate



Out
VP = vdda
ResetNWB
SelB
ResetB
VN

Reset + offset readout



End of readout