Monolithic Active Pixel Sensors with high-density readout electronics in a 65 nm CMOS technology

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Outline

- Motivation
- **Noise and radiation tolerance** of 65 nm CMOS devices
- **Monolithic Active Pixel Sensors** and **fast front-end electronics** in 65 nm CMOS
- The **APSEL65** chip
- Conclusion

Motivation

- **Vertex detectors** for HEP experiments at the next generation colliders will need to fulfill very stringent requirements on position and timing resolution, material budget, readout speed and radiation tolerance

- The demand for higher in-pixel functionalities along with the reduction of pixel cell size has driven the interest of the designers community towards **sub-100 nm CMOS** processes in the design of mixed signal front-end electronics

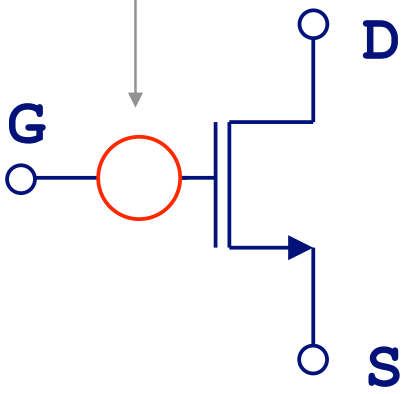
- The move to more scaled processes is dictated by improving **digital performance**. In a 65 nm process the impact of new dielectric materials and processing techniques (silicon strain, gate oxide nitridation, …) on the analog behavior of MOSFETs, specifically in terms of **noise performance** and **radiation hardness**, has to be carefully evaluated

- Here we focus on **Low-Power 65 nm CMOS** where the supply voltage (1.2 V) does not scale with respect to 130 nm CMOS and the gate leakage current is very low

Noise in CMOS transistors

- Noise in the drain current of a MOSFET can be represented through an equivalent noise voltage source in series with the device gate

$$S_e^2(f) = S_W^2 + S_{1/f}^2(f)$$



S_W - white noise

- channel thermal noise (main contribution in the considered operating conditions)

$$S_{ch}^2 = \frac{4k_B T \Gamma}{g_m}$$

  - k_B Boltzmann's constant
  - T absolute temperature
  - Γ channel thermal noise coefficient

- contributions from parasitic resistances

$S_{1/f}$ - 1/f noise

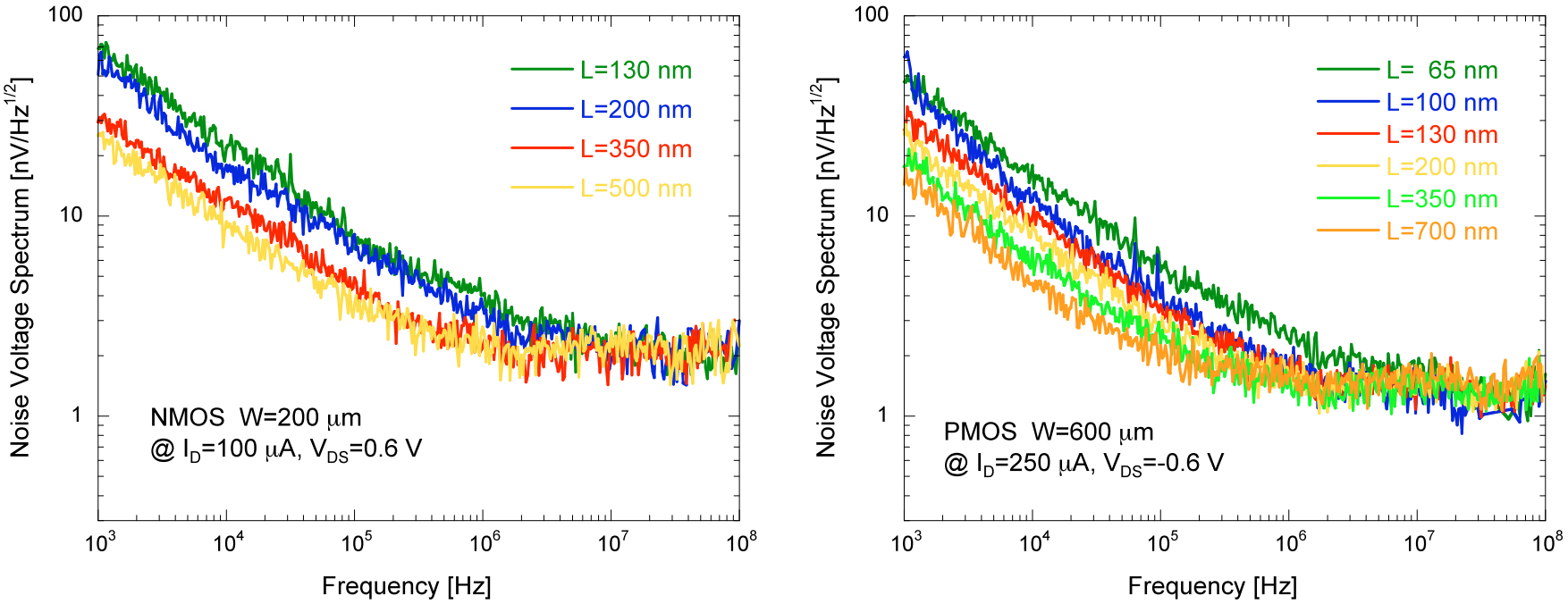
- technology dependent contribution

$$S_{1/f}^2(f) = \frac{k_f}{C_{OX} W L f^{\alpha_f}}$$

  - k_f 1/f noise parameter
  - α_f 1/f noise slope-related coefficient

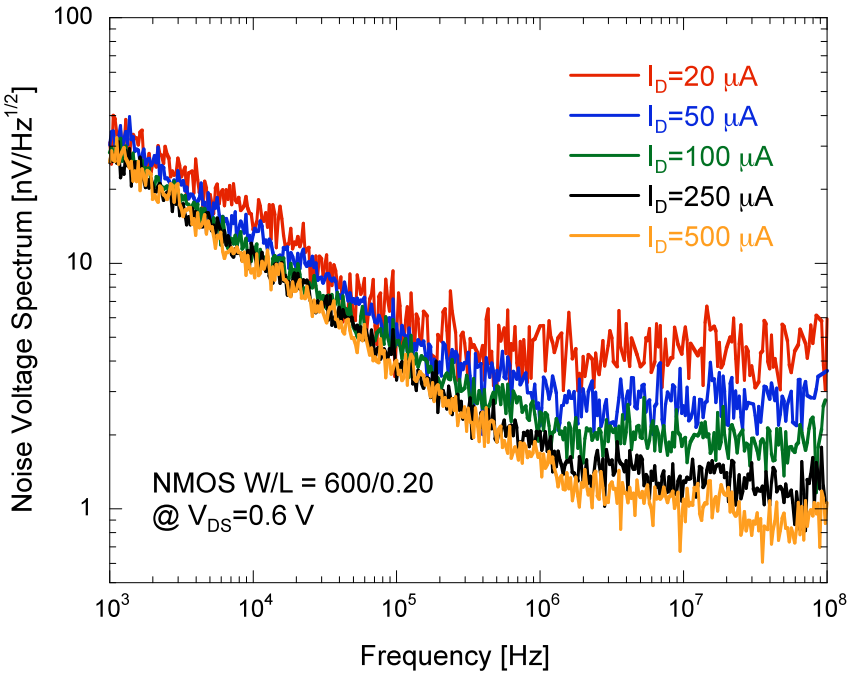
- **White** and **1/f noise** have been measured on test devices with different geometries and biased at different drain currents

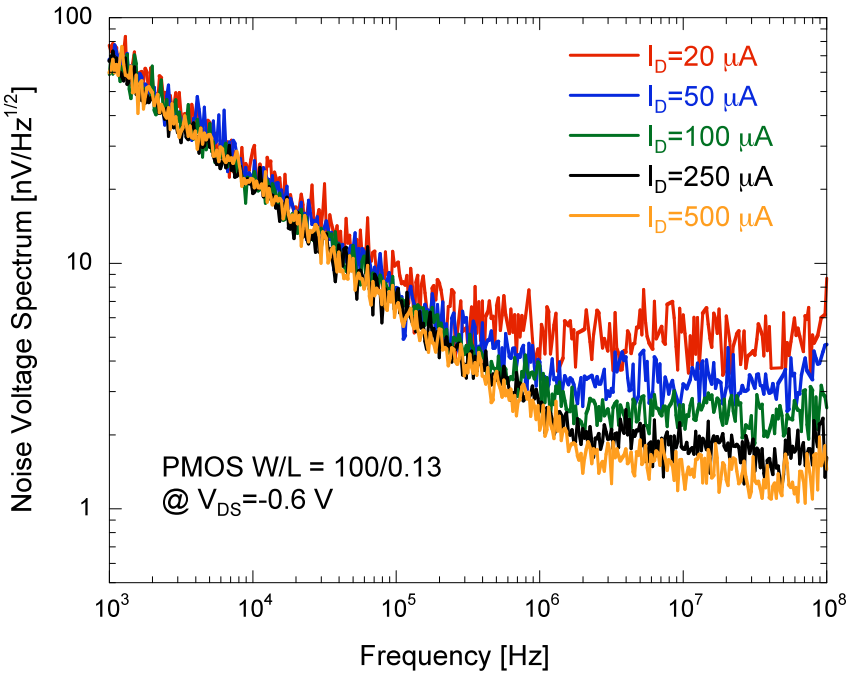
Noise vs gate length



- **White noise** virtually independent of the gate length L and device polarity, in agreement with g_m behavior in weak/moderate inversion
- **1/f noise** contribution decreases with increasing channel length, as predicted by the noise equation

Noise vs drain current





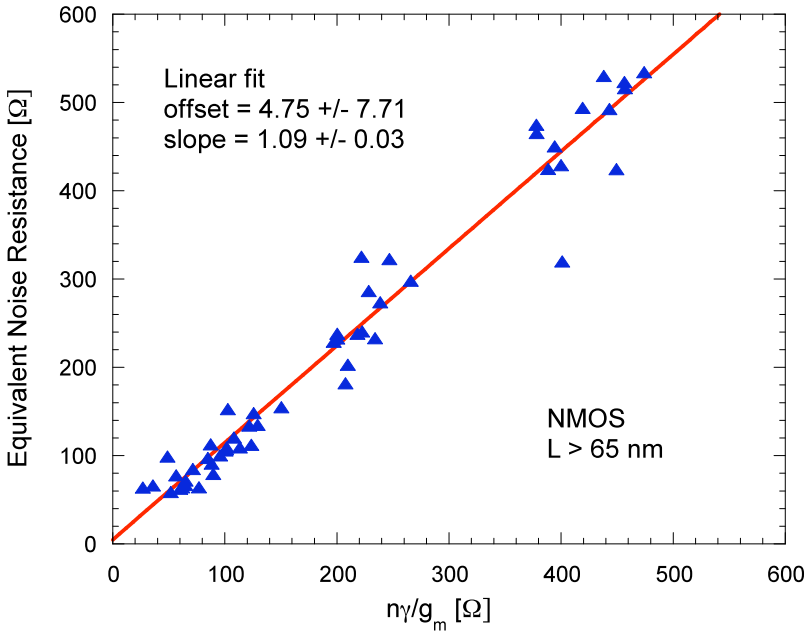
- **White noise** decreases with increasing drain current in both NMOS and PMOS devices, in agreement with g_m behavior in weak/moderate inversion
- **1/f noise** contribution is to a large extent independent of the drain current

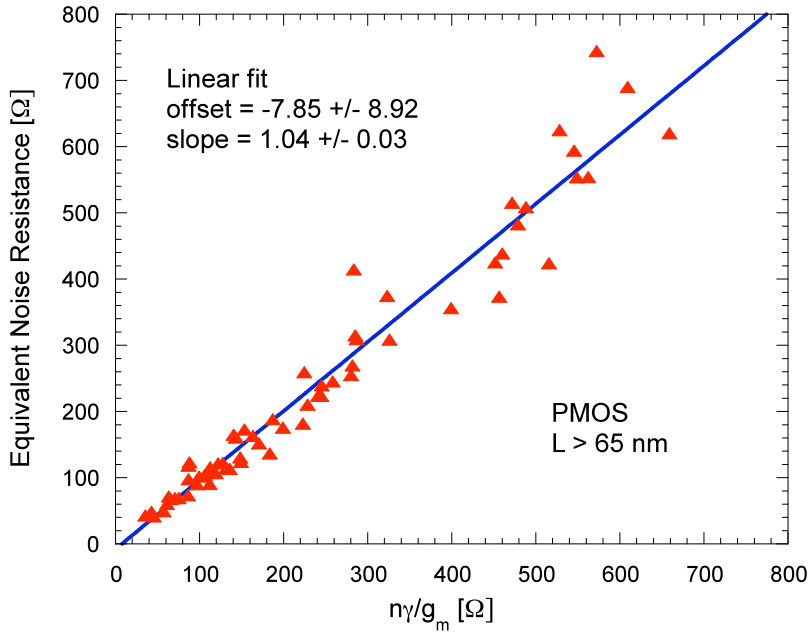
White noise - S_W

- Evaluated in terms of the **equivalent channel thermal noise resistance**:

$$R_{eq} = \frac{S_W^2}{4k_B T} = \alpha_W \frac{n\gamma}{g_m}$$

- α_w excess noise coefficient
- n proportional to $I_D(V_{GS})$ subthreshold characteristic
- γ channel thermal noise coeff.

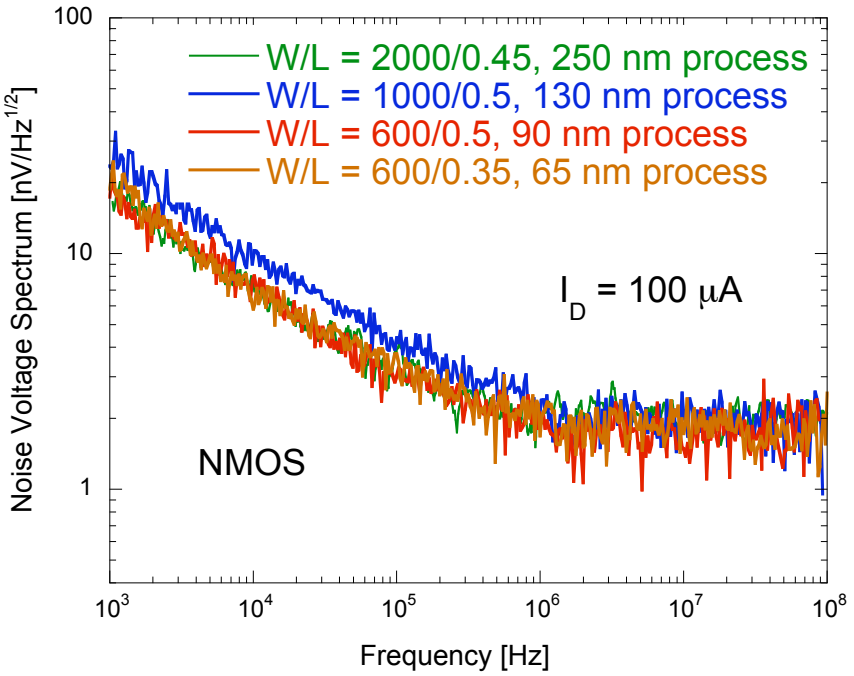


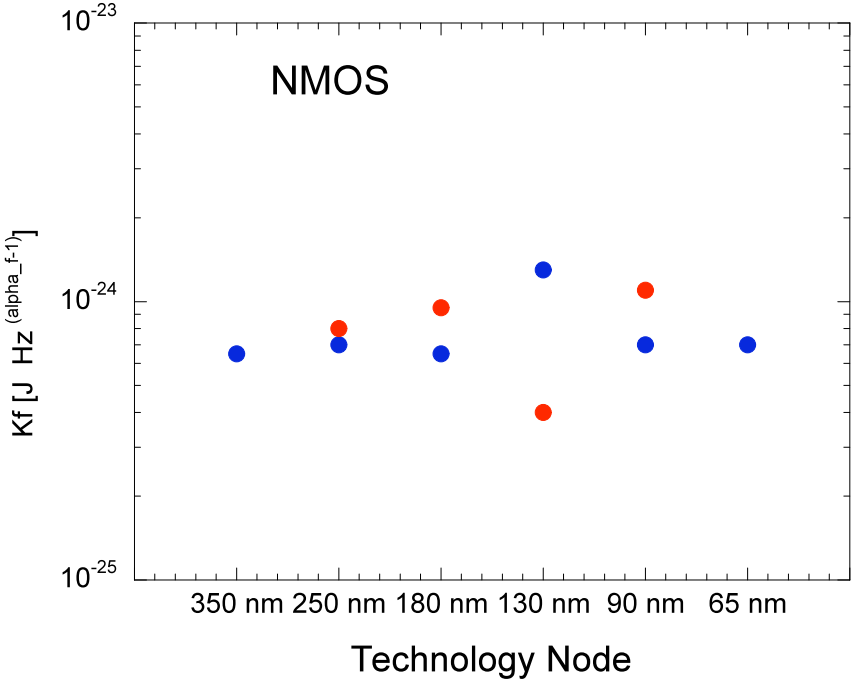


- α_w close to unity for NMOS and PMOS with L > 65 nm → **no sizeable short channel effects** in the considered operating regions (except for 65 nm devices with $\alpha_w \approx 1.3$)
- Negligible contributions from **parasitic resistances**

Noise in different CMOS nodes

- **The 1/f noise** of the 65 nm devices we tested is of the same order as in previous CMOS nodes

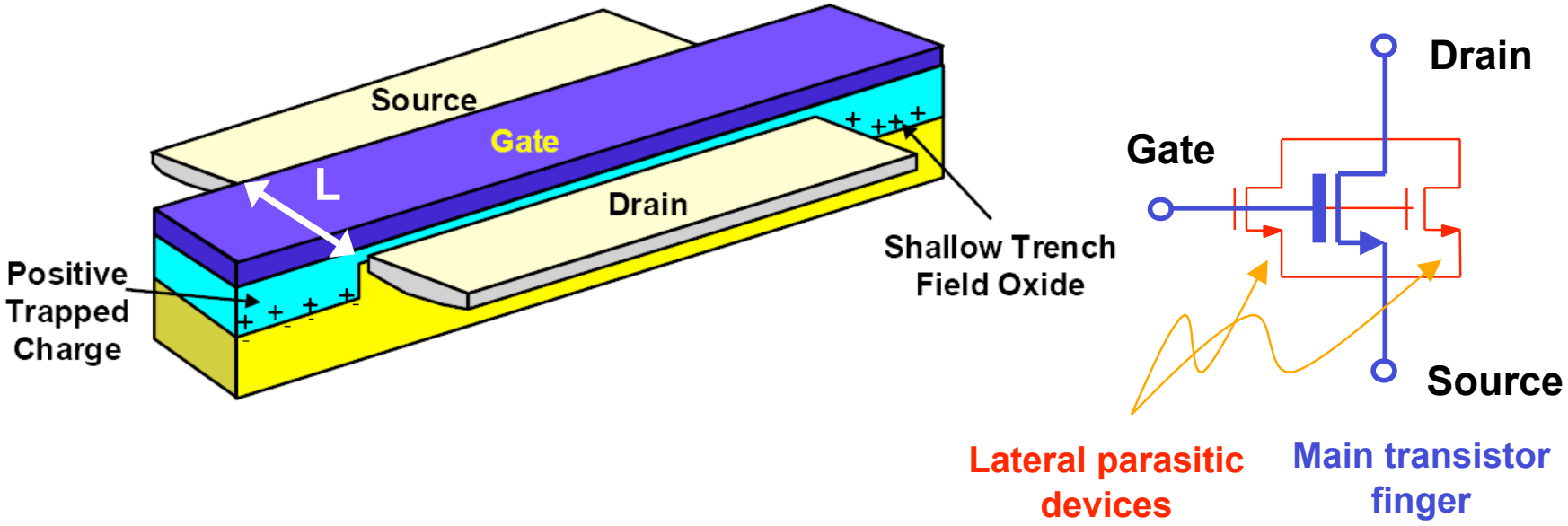




- The 1/f noise parameter **Kf** does not show dramatic variations across different CMOS generations and foundries
- **White noise** is also very similar (weak/moderate inversion)

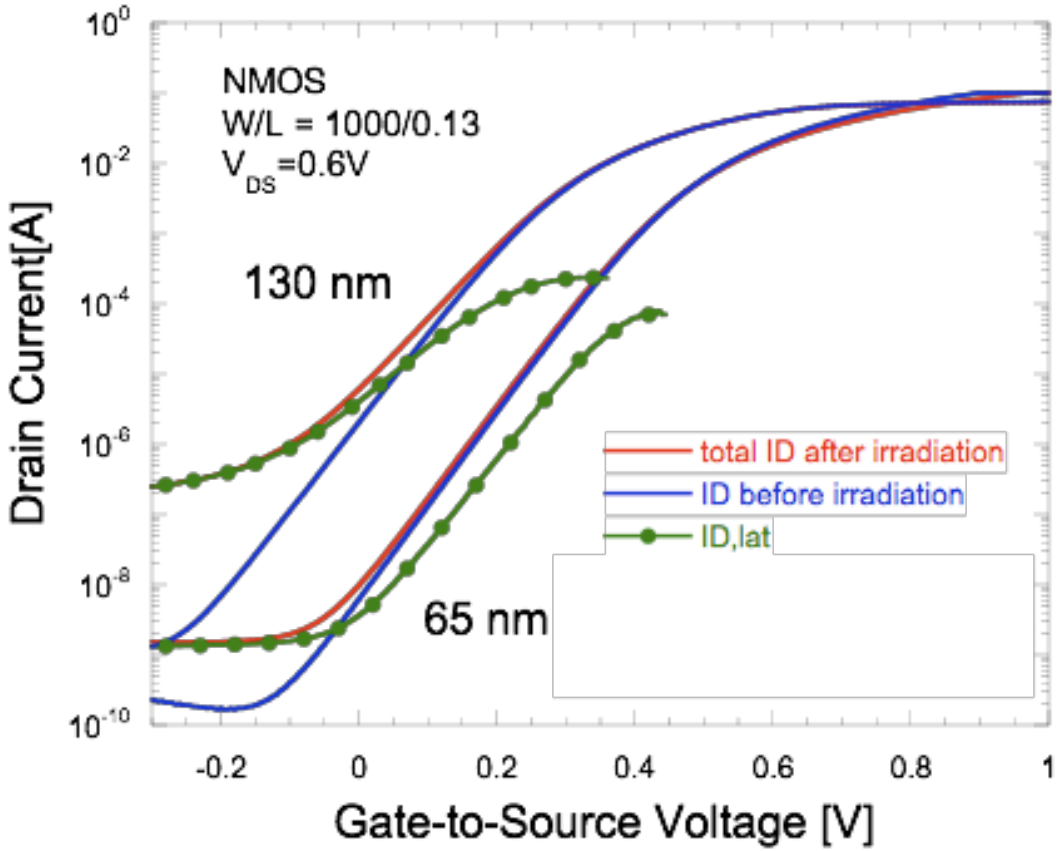
Ionizing radiation effects in sub-100 nm CMOS

- In deep submicron bulk CMOS devices exposed to ionizing radiation, the main degradation effects are associated to the thick (~ 100 nm) **lateral isolation oxides** (STI = Shallow Trench Isolation).



- **Radiation-induced positive charge** trapped in isolation oxides may invert a P -type region in the well/substrate of NMOSFETs creating a **leakage path** between source and drain

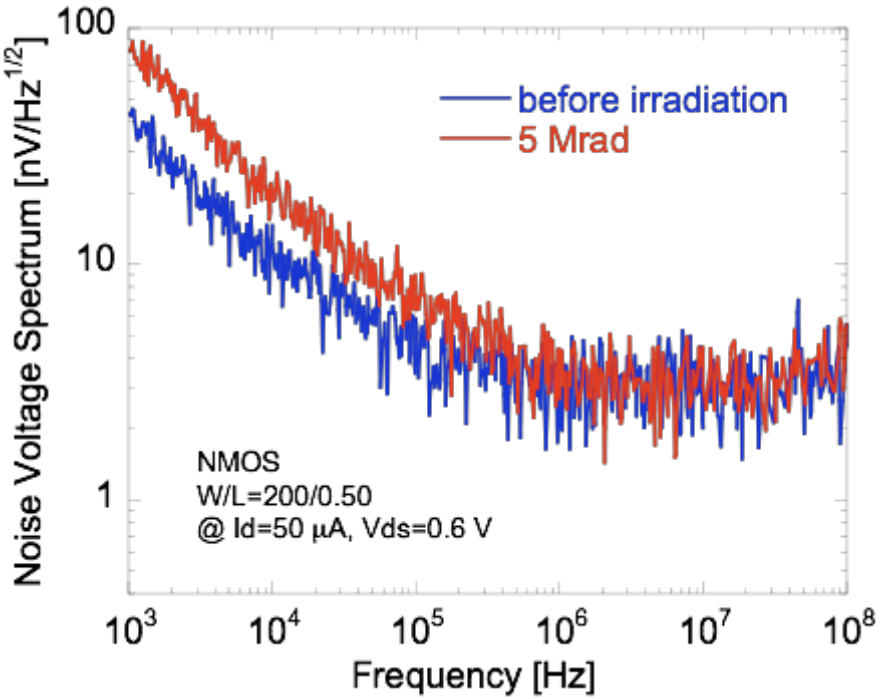
Radiation test - Static Characteristics

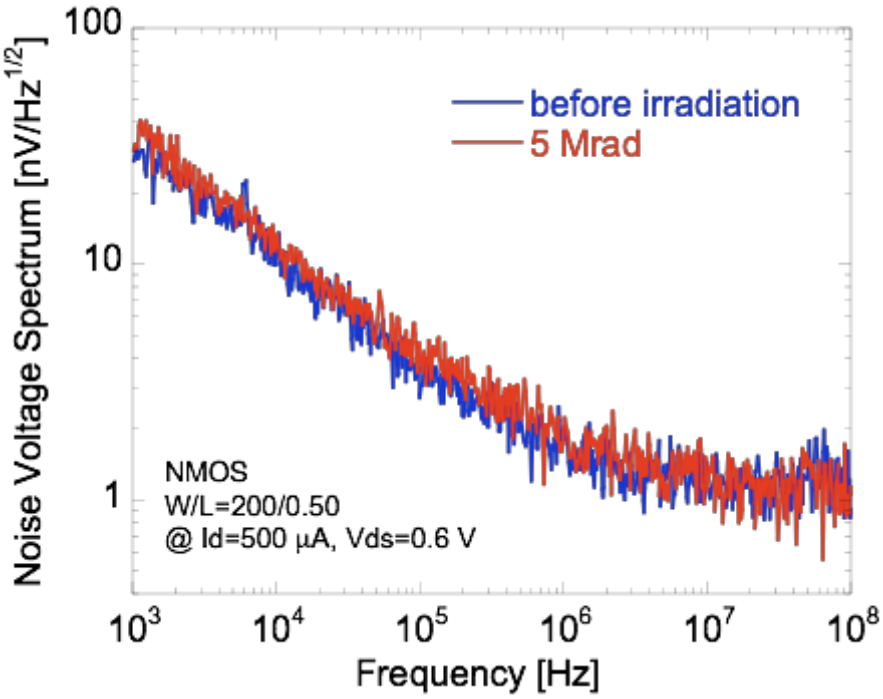


ID(Vgs) before and after exposure to a **10 Mrad** total dose of γ-rays

- A larger amount of **lateral leakage** takes place in 130 nm devices
- The smaller $I_{D,lat}$ 65 nm devices suggests that the sensitivity to positive charge buildup in STI oxides is mitigated by the higher doping of the P-type body with respect to less scaled processes

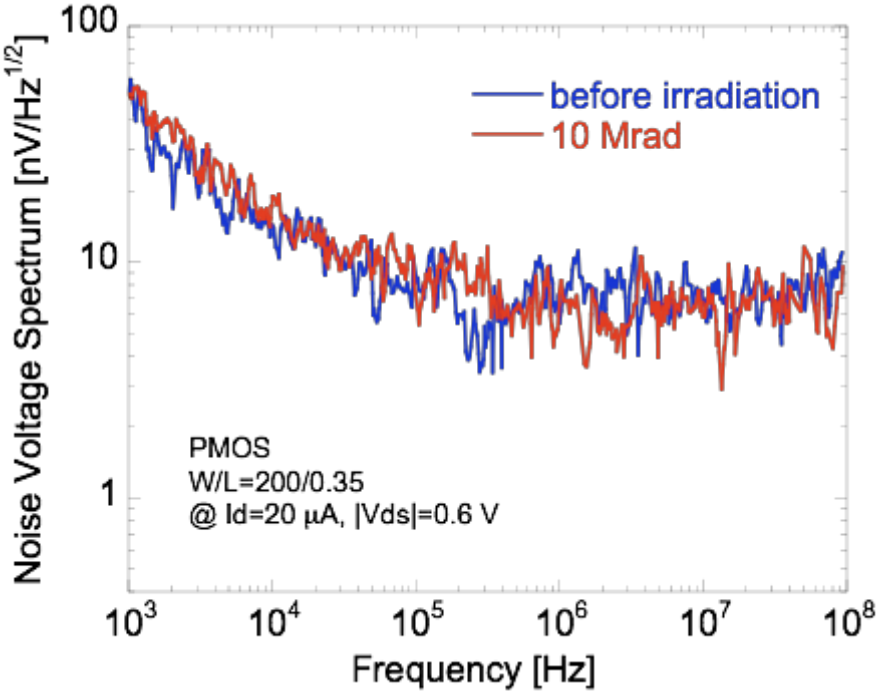
Radiation test - NMOS

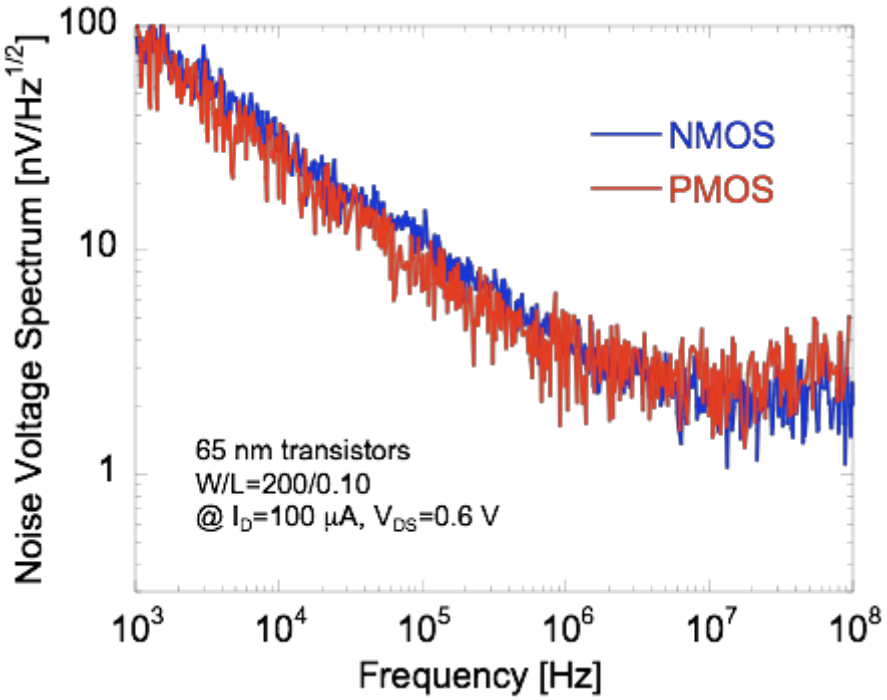




- **Moderate 1/f noise increase** at low current density, due to the contribution of lateral parasitic devices
- At **higher currents** the degradation is almost negligible because the impact of the parasitic lateral devices on the overall drain current is much smaller
- **No increase** in the **white noise** region is detected

Radiation test- PMOS





- NMOS and PMOS devices have **similar 1/f noise** (especially for longer transistors)
- **Very small increase** in the **low-frequency** part of the noise voltage spectrum, even at low current density
- **No increase** in the **white noise** region is detected

some remarks …

- Behavior of the **white noise** term is **consistent with equations valid in weak inversion**, as observed in other fabrication processes

- **Low-noise analog design** will pose challenges but, according to the study of key analog parameters, appears to be **still viable**. PMOSFETs appear to gradually lose their 1/f noise advantage over NMOSFETs

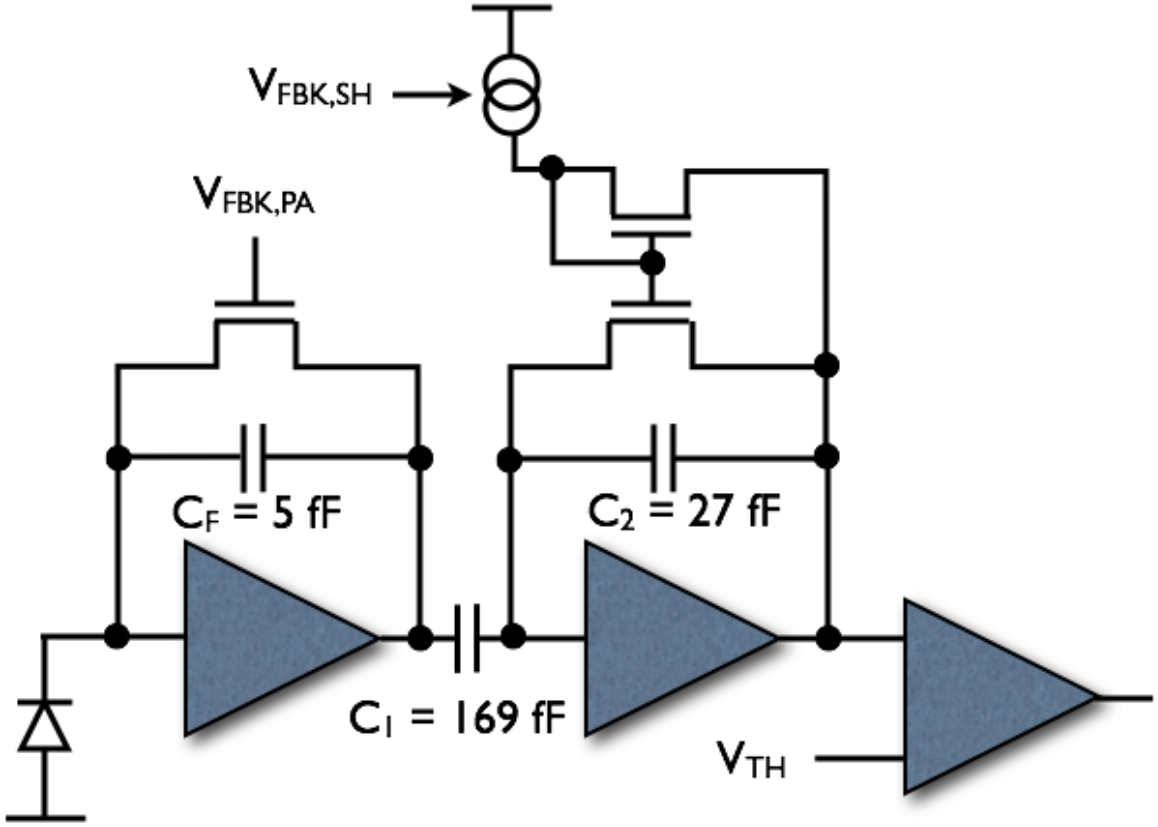
- Data analysis does not point out **any novel damage mechanism** which could be related to the technological advances associated to an aggressively scaled process

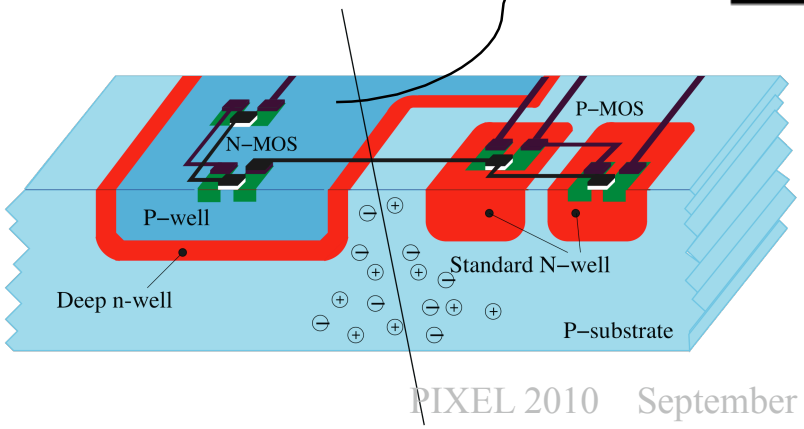
- The comparison with data from previous CMOS generations confirms the **high degree of tolerance to ionizing radiation** that appears to be typical of sub-100 nm technologies

- **We designed a prototype chip with mixed-signal readout circuits in a 65 nm CMOS process manufactured by IBM (10LPE/10RFE) → APSEL65**

APSEL65: deep n-well monolithic active pixel sensor

- **Classical signal processing** chain for capacitive detector
- The analog processor includes a charge sensitive amplifier, a shaping stage and a threshold discriminator → **binary readout**





Features & Post layout simulation results

- W/L PA input device: 27/0.25

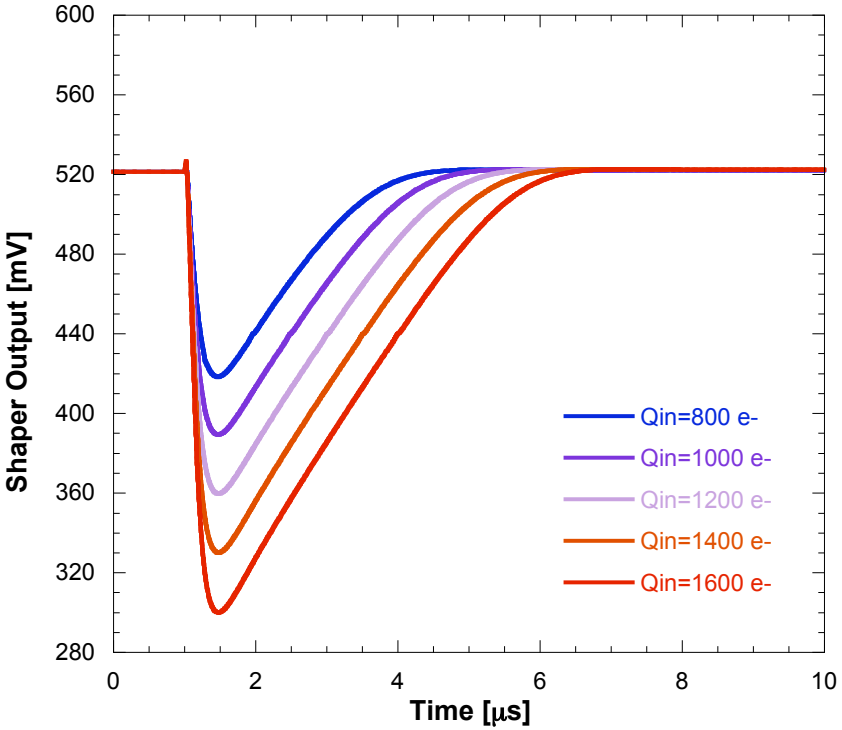
Power consumption: 20 μW

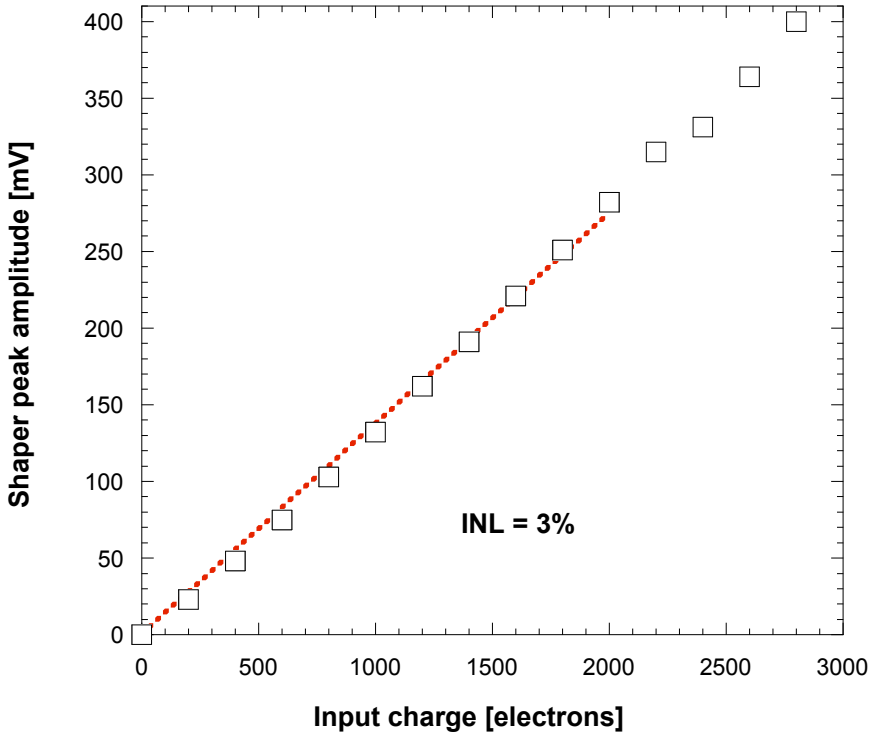
Equivalent noise charge: 38 e^-

Threshold dispersion: 38 e^- (main contributions from shaper input device and NMOS and PMOS pair in the discriminator)

Charge sensitivity: 725 mV/fC

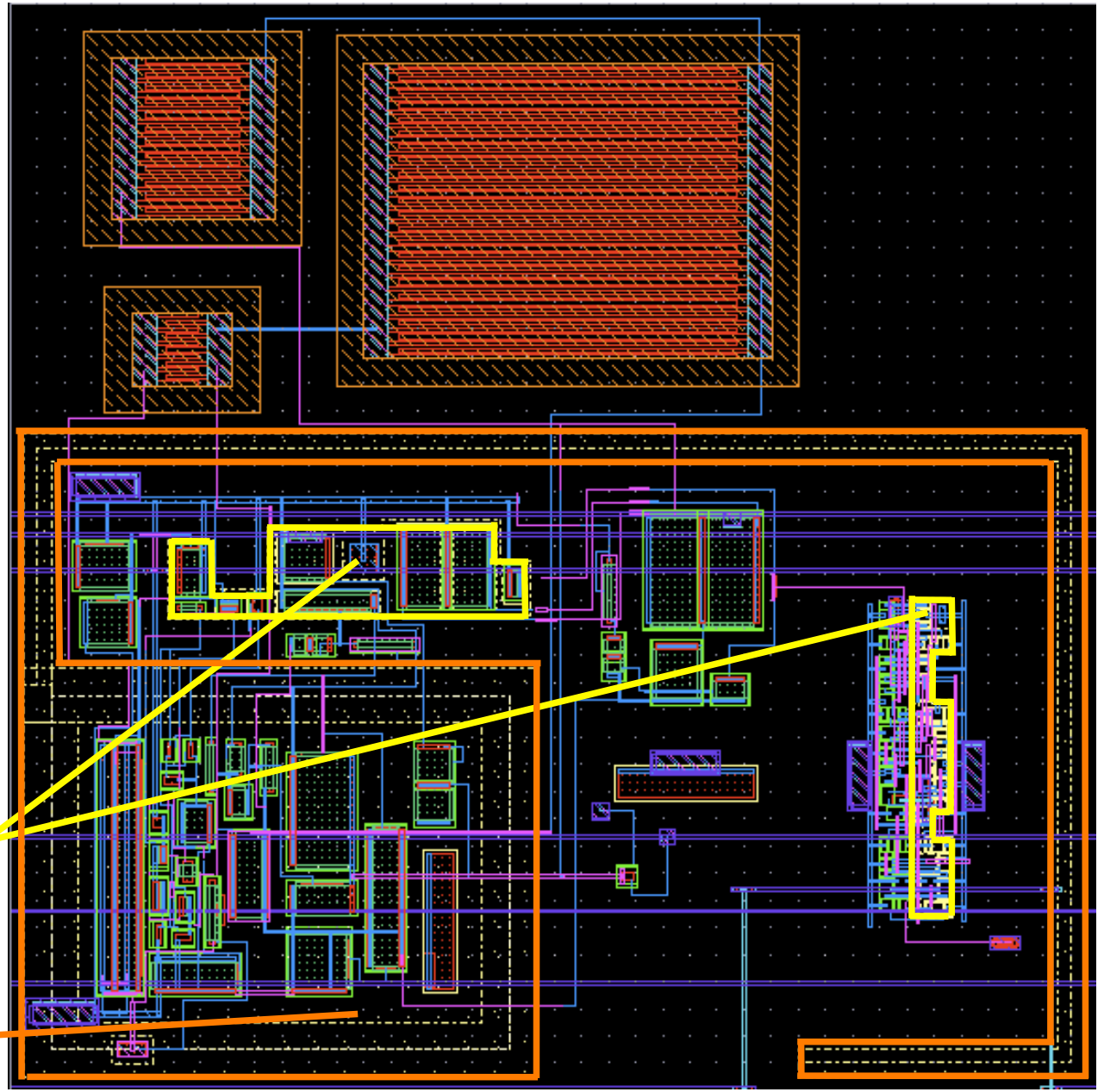
Peaking time: 300 ns





Cell layout

- In this prototype the digital section is kept to a minimum (latch, OR gate, tri -state buffer). It is planned to include sparsification and time-stamping logic at the pixel level in more advanced versions (room for this already available)



Fast FE for high resistivity pixels

- W/L PA input device: 27/0.25

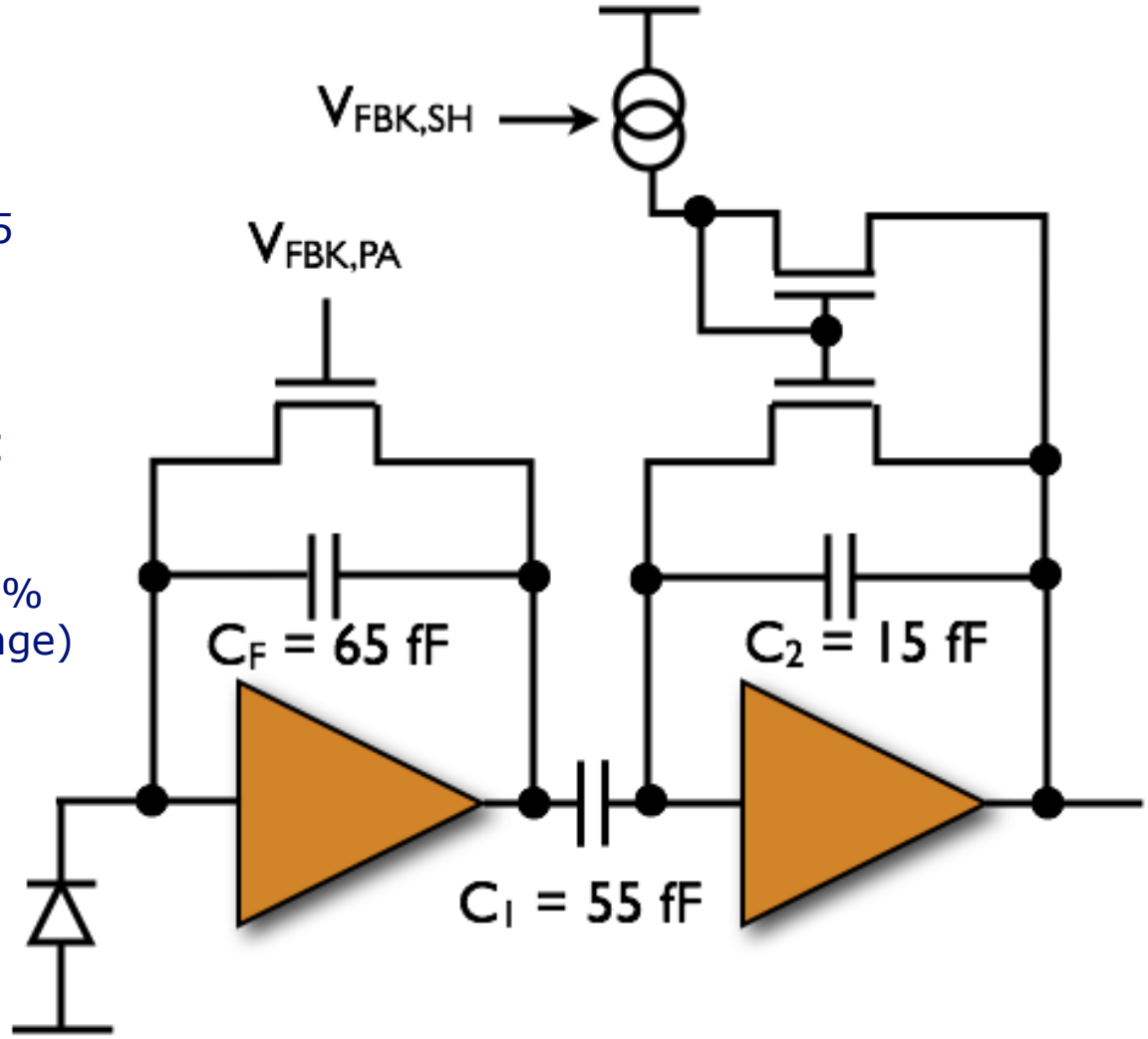
  Power consumption: 6 μW

  ENC = 204 e^- @ C_D = 100 fF

  Charge sensitivity: 42 mV/fC

  Peaking time: ~ 25 ns

  Integral non linearity: ~ 3.5 %
  (32000 e^- input dynamic range)



Test chip layout

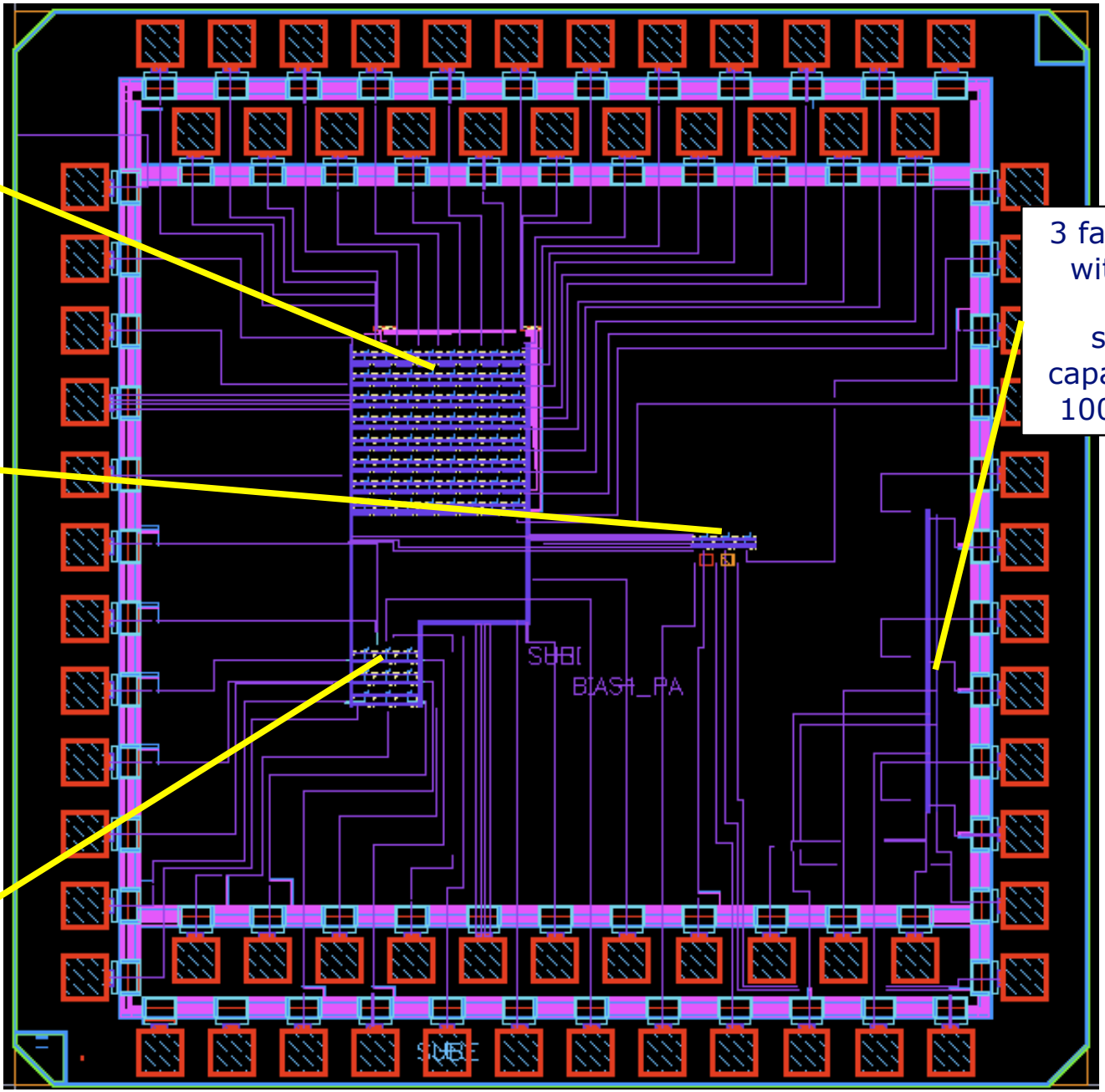
8x8 DNW MAPS matrix

- digital outputs
- outputs of the shapers can be accessed through row and column decoders and read out one at time

3 standalone channel with Cinj and detector simulating capacitor (250 fF, 350 fF, 450 fF)

3x3 DNW MAPS matrix

- 9 analog outputs
- Digital output of the central pixel
- Cinj on central pixel



3 fast-channels with Cinj and detector simulating capacitor (50 fF, 100 fF, 150 fF)

Conclusions

- **Noise measurements and radiation tests** have been performed on devices belonging a **65 nm CMOS process**
- Behavior of the **white noise** term is consistent with equations valid in weak/moderate inversion
- Comparison with **previous CMOS nodes** shows that scaling to the 65 nm process does not affect 1/f noise performances significantly
- **Radiation tests** confirm the high degree of tolerance to ionizing radiation that appears to be typical of sub-100 nm technologies
- A test chip including **DNW MAPS** and a **fast front-end** for the readout of high-resistivity pixel sensors has been submitted in a 65 nm CMOS process provided by IBM. This prototype will provide useful information for future submissions and larger chips

Backup slides

Transconductance and Channel thermal noise coefficient

- Transconductance in all inversion regions (*)

$$g_m = \frac{I_D}{nV_T}\frac{2}{\sqrt{1+4u}+1}, \qquad u = \frac{I_D L}{I_z^* W}$$

- Channel thermal noise coefficient (*)

$$\gamma = \frac{1}{1+u}\left[\frac{1}{2}+\frac{2}{3}u\right], \qquad u = \frac{I_D L}{I_z^* W}$$

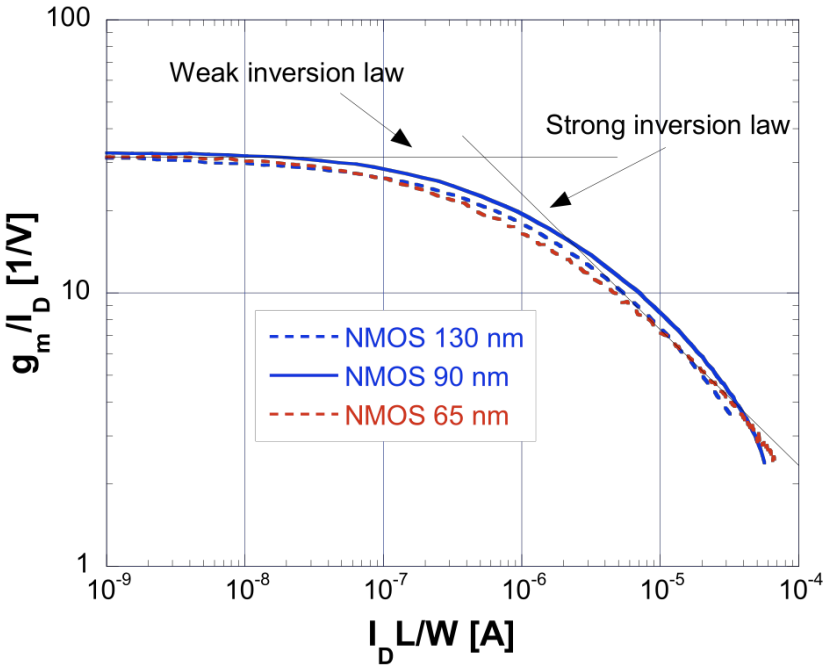
(*) G. De Geronimo, P. O'Connor, "**MOSFET optimization in deep submicron technology for charge amplifiers** ", *IEEE Trans. Nucl. Sci.*, vol. 52, n. 6, Dec. 2006.

Device operating region

- At the considered drain currents, DUTs work in weak or moderate inversion region
- Characteristic normalized drain current I^*_Z provides a reference point to define device operating region

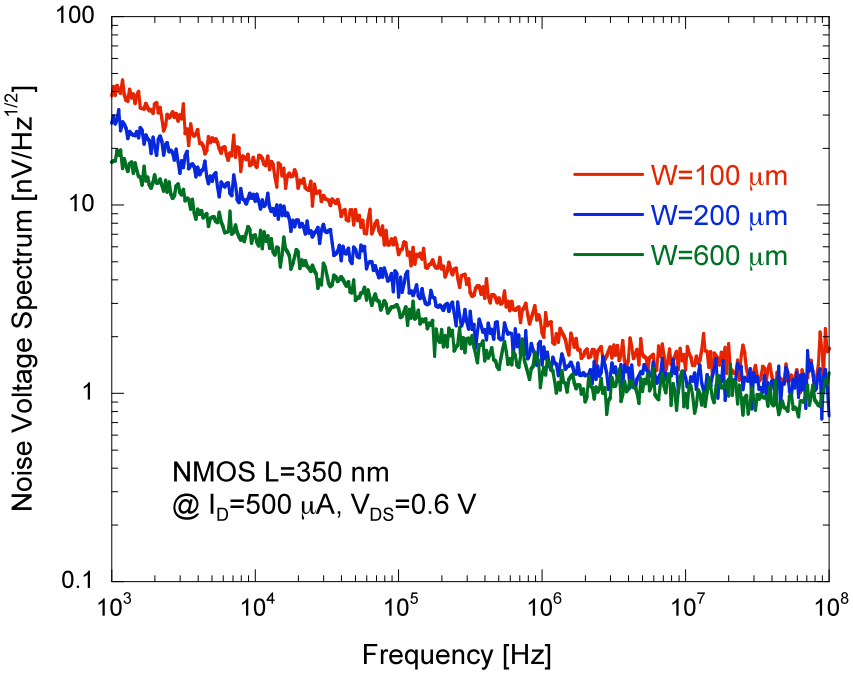
$$I_Z^* = 2\mu C_{OX} n V_T^2$$

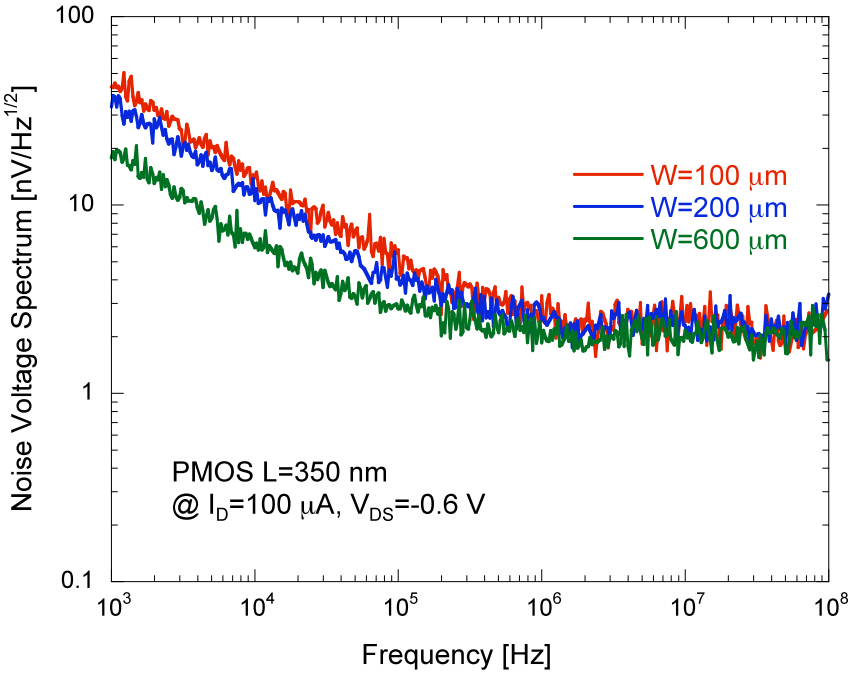
- μ carrier mobility
- C_{OX} specific gate oxide capacitance
- V_T thermal voltage
- n proportional to $I_D(V_{GS})$ subthreshold characteristic



- At a given drain current, operation is shifted towards weak inversion region with technology scaling

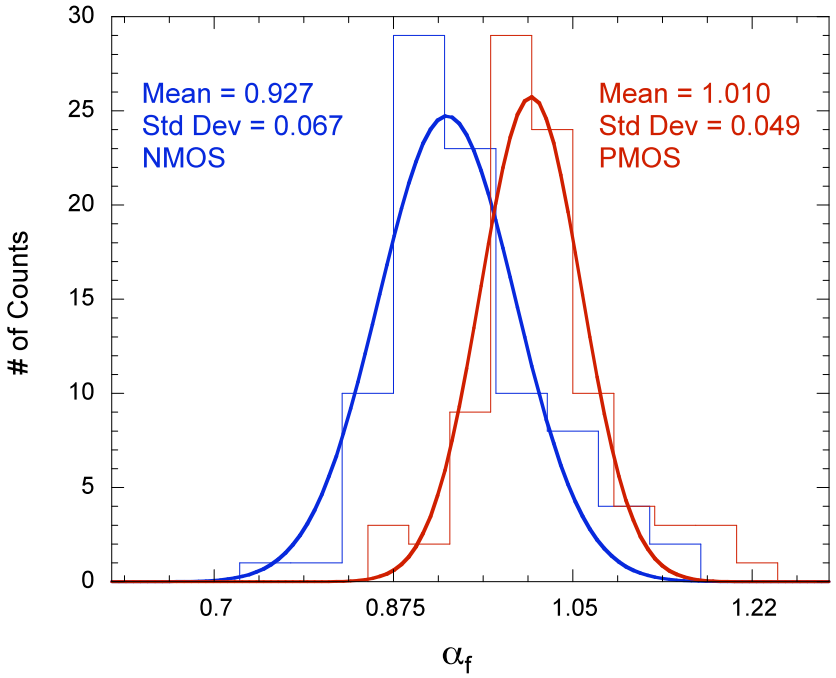
Noise vs gate width

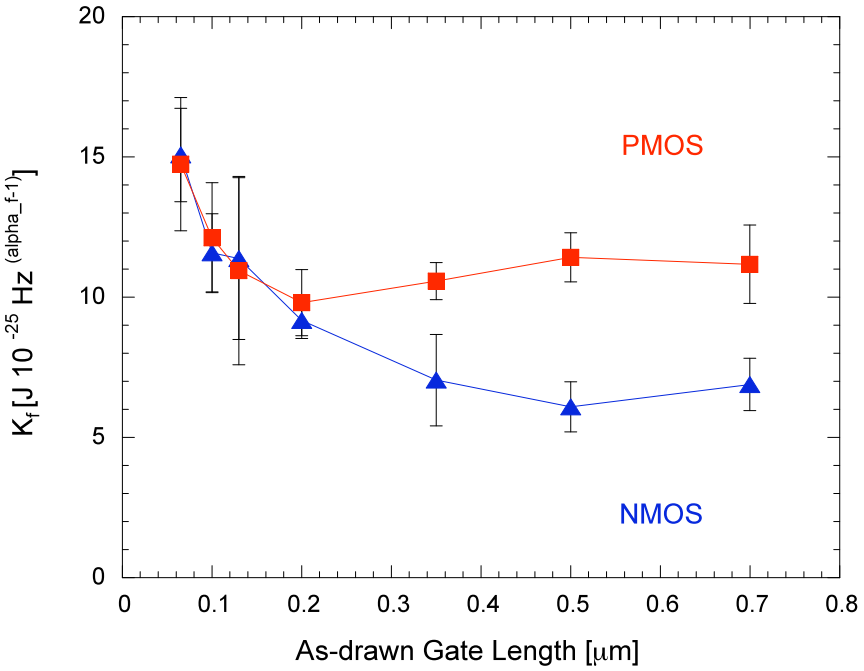




- **1/f noise** increases with decreasing W, as predicted by the noise equation
- **White noise** is not sizeably affected by W variation for PMOS devices while it slightly decreases with increasing channel width for NMOS

Flicker noise - $S_{1/f}(f)$

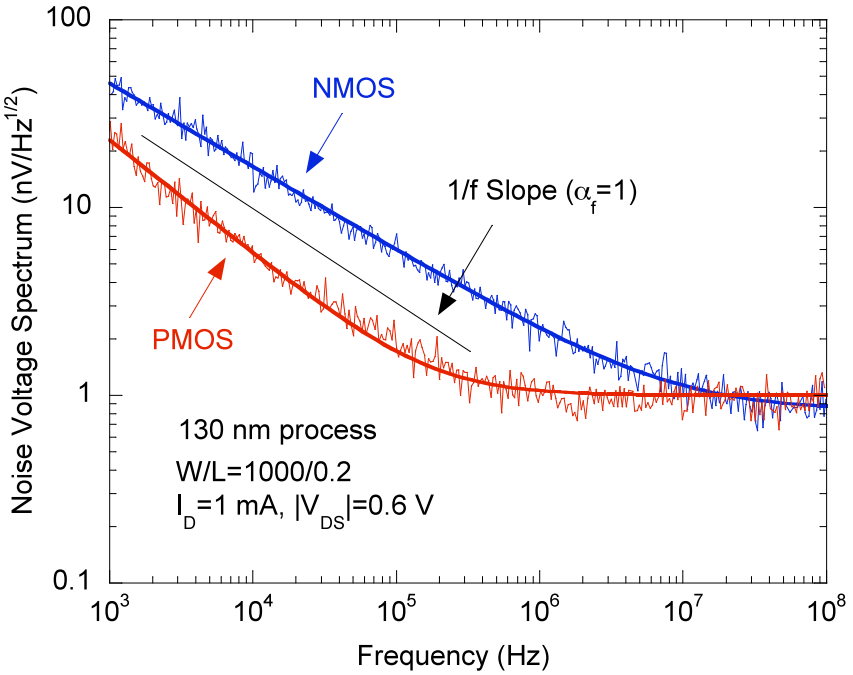


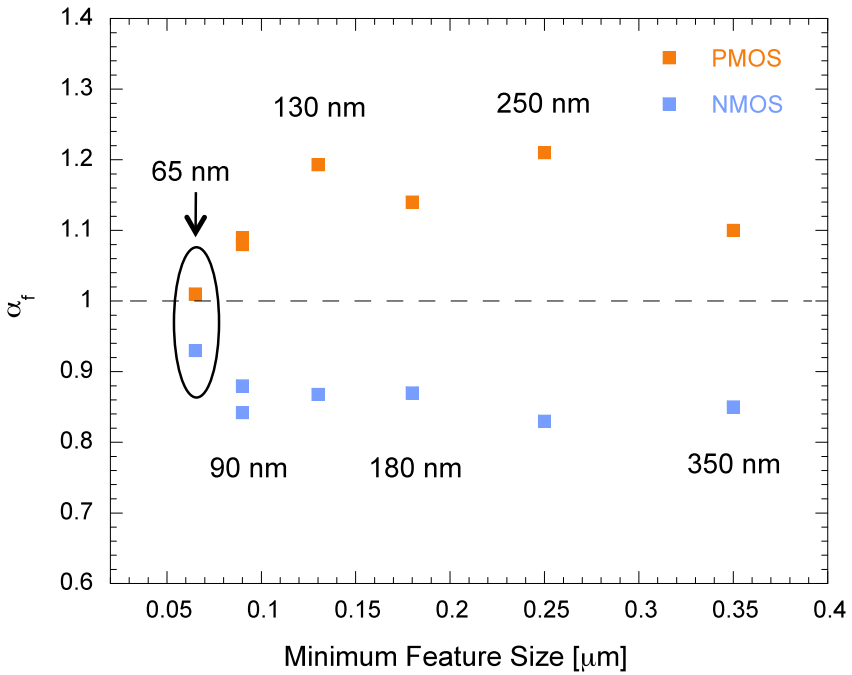


- **Slope α_f** of the 1/f noise term is smaller than 1 in NMOSETs and close to 1 in PMOSETs
- In the examined operating region, α_f does not exhibit any clear dependence on the drain current or on the channel geometry
- In both polarities **Kf** is strongly dependent on the channel length while it is almost independent of the device bias conditions

Noise in different CMOS nodes

- **Slope** of the 1/f noise in previous CMOS nodes is dependent of the device polarity

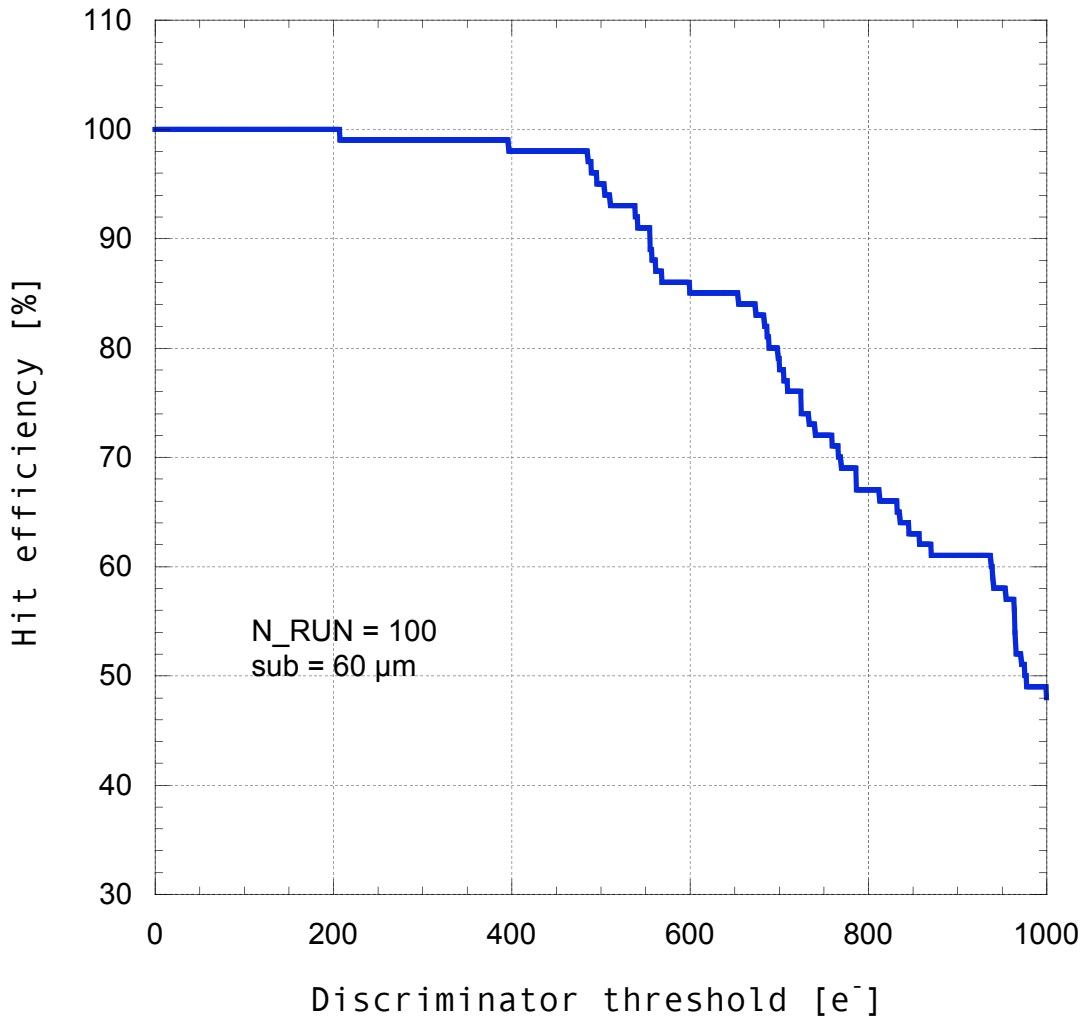




- α_f > 1 for PMOSETs and < 1 in NMOSFETs for previous technology nodes
- α_f values are close to unity for both NMOS and PMOS devices in the 65 nm process

Preliminary Monte Carlo simulations

- Very preliminary Monte Carlo simulations on a 3x3 cluster featuring the APSEL65 sensor layout (100 experiments, 60 μm thick substrate)



Characterization of 65 nm CMOS devices

- Single transistors, **Low Power 65 nm** CMOS process

NMOS

Technology features:

- V_{DD} = 1.2 V
- t_{OX}= 2.6 nm
- C_{OX}=13 fF/μm^2

Available geometries

- W = 0.2 – 0.8 - 20 – 100 – 200 – 600 1000 μm
- L = 0.065 - 0.10 - 0.13 – 0.20 0.35 – 0.50 - 0.70 μm

PMOS

Technology features:

- V_{DD} = 1.2 V
- t_{OX}= 2.8 nm
- C_{OX}=12 fF/μm^2

Available geometries

- W = 0.2 – 0.8 – 2 - 20 – 100 – 200 – 600 1000 μm
- L = 0.065 - 0.10 - 0.13 – 0.20 0.35 – 0.50 - 0.70 μm

- Devices under test are NMOS and PMOS transistors with standard open layout, interdigitated configuration
- Drain current in DUTs: from tens of μA to 1 mA → **low power operation**