# Towards minimum material trackers for HEP experiments at upgraded luminosities

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Low material @ (S)LHC: a challenge for trackers

- ATLAS pixel detector @LHC: **3.5% X0** per layer[(*)]
  - Stave structure: 1.47% X0
  - Services: 0.92% X0
    - Services also dominate the material budget @ large η
    - Main contribution comes from power cables
- Insertable B-Layer (**IBL**): current estimate **1.5% X0**
- ATLAS pixels @ Super LHC (**SLHC**): **≤2% X0**
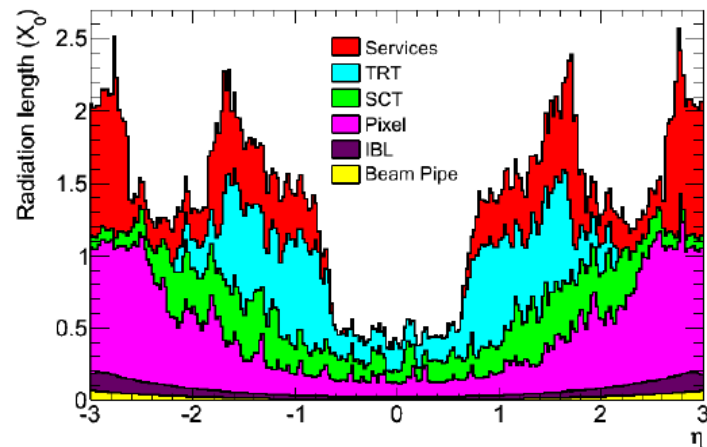
ATLAS inner det. material distribution (incl. IBL)
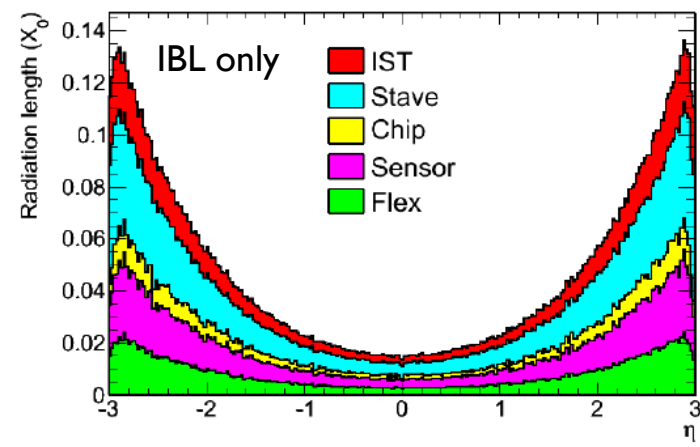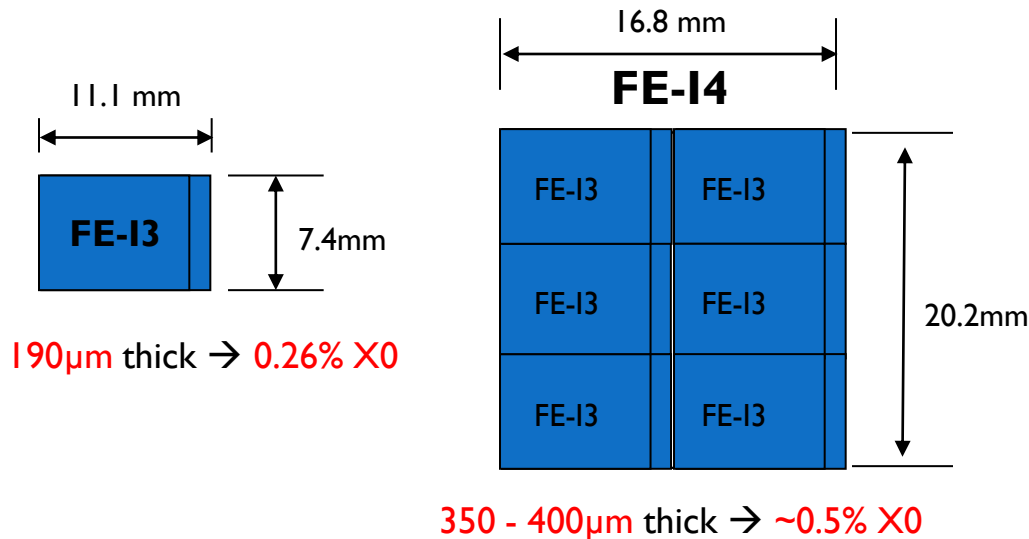

Current IBL material distribution estimation

(*) all x/X0% numbers in the talk are given per pixel layer
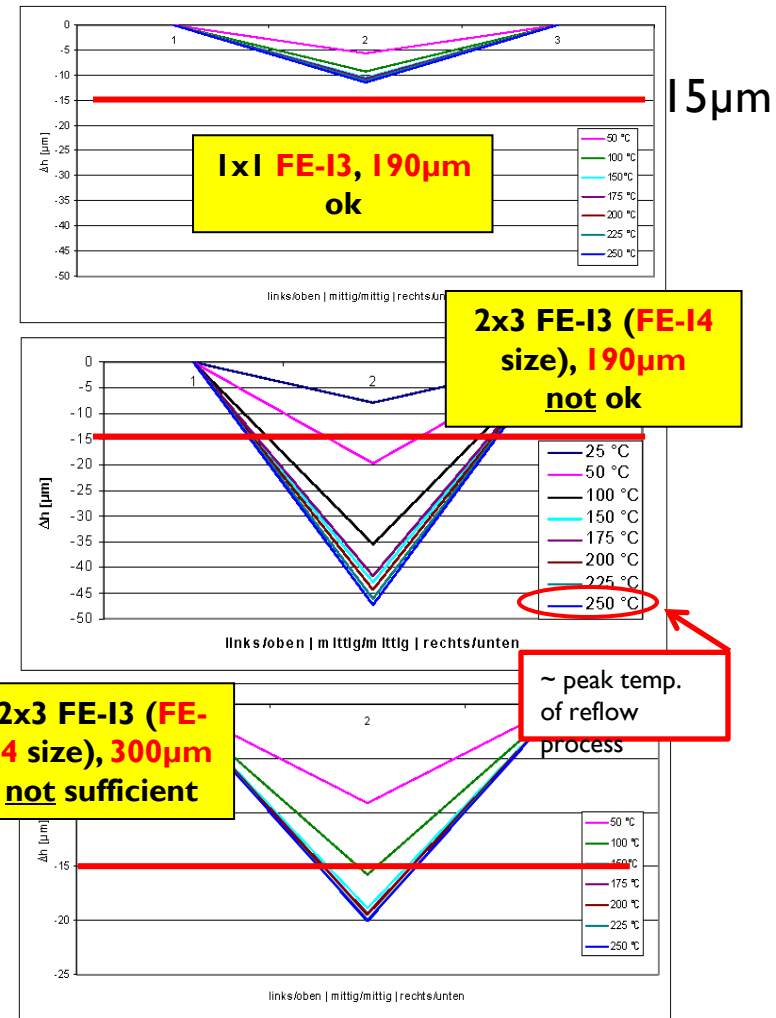
Material reduction strategy

- Address known sources of material
  - Reduction of stave structure material
    - CC foam
  - Less massive (and more efficient) powering scheme
    - Serial powering
    - DC-DC conversion
  - Light services, especially in active area
    - Al flex cables
    - Through Silicon Via (TSV)

- Prevent new significant contributions to the material budget
  - Electronics
    - Thin FE chip

Work ongoing in Bonn

Thin FE chip

11.1 mm

FE-I3

7.4mm

190µm thick → 0.26% X0

16.8 mm

FE-I4

FE-I3	FE-I3
FE-I3	FE-I3
FE-I3	FE-I3

20.2mm

350 - 400µm thick → ~0.5% X0

Bow profile along a diagonal

15µm

1x1 **FE-I3, 190µm** ok

2x3 FE-I3 (**FE-I4 size), 190µm not** ok

2x3 FE-I3 (**FE-I4 size), 300µm not** sufficient

~ peak temp. of reflow process

- ▸ Current flip chip technique: IZM solder SnAg
- ▸ Chip bow during flip chip
  - ▸ Due to CTE mismatch between Si bulk and metals
  - ▸ ~ $1/d^3$, d = chip diagonal
- ▸ New techniques using handle-wafers during flip chip and lift-off after flip chipping are needed
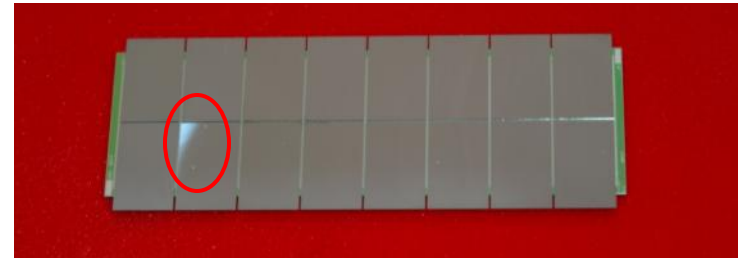 - ▸ 3 methods studied so far with IZM Berlin

First investigations and problems

- First two methods used resp. a **wax** and a **Brewer glue** for carrier bonding
- Not successful
  - thinning ok, but **chips bent up** at the corners, opposite to the End Of Column region
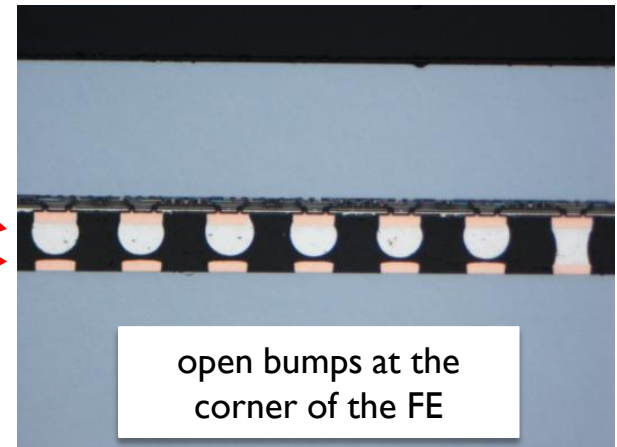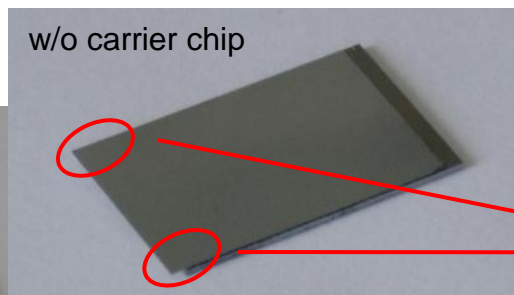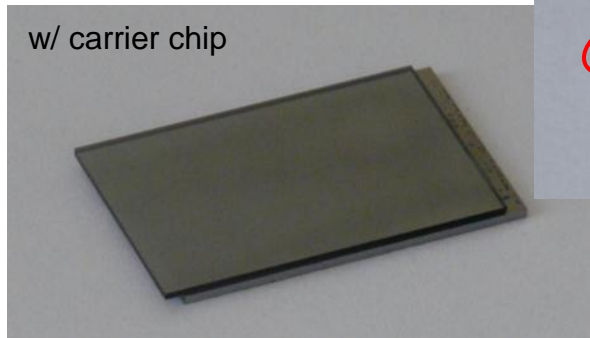 - **Bump bonds do not connect** in this area

1st method: wax

ATLAS pixel module with **90 μm** thick FE-I2

2nd method: Brewer glue

2x2 FE-I3 array = **66% FE-I4, 90 μm,** on dummy sensor

w/ carrier chip

w/o carrier chip

open bumps at the corner of the FE

Polyimide method

Process steps:

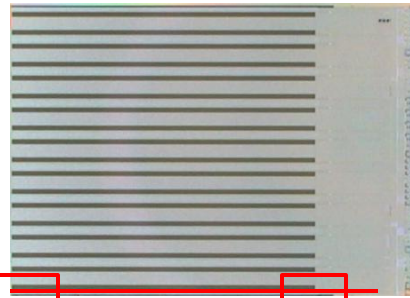| |
|---|
| thinning of FE wafer |
| Mounting on glass carrier wafer using polyimide glue |
| Bumping process on FE frontside |
| Dicing of FE wafer and carrier wafer package |
| FE flip chip bonding to sensor tile |
| Laser exposure of chip backside |
| Carrier chip detach |

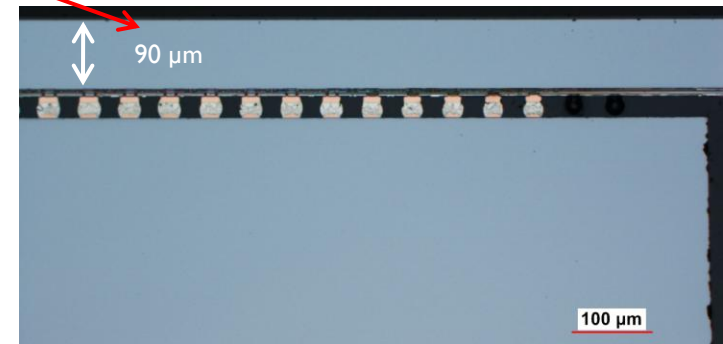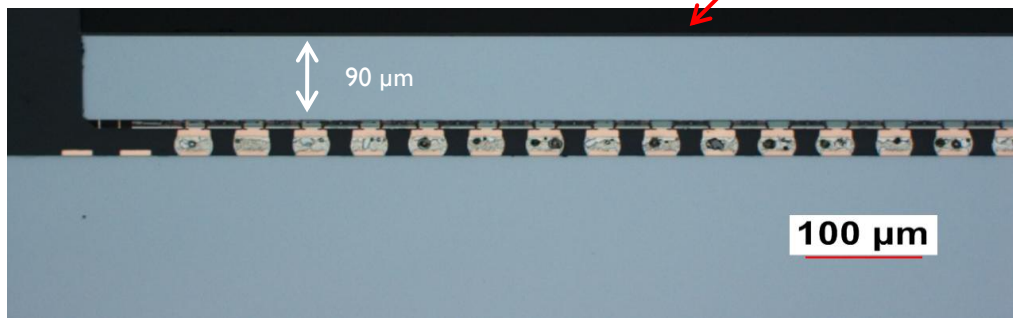Glass carrier on Si testchip before laser exposure_25x

Glass carrier on Si testchip after laser exposure_25x

2x2 FE-I2 array, **90um**, on dummy sensor

Cross section cut of first column →
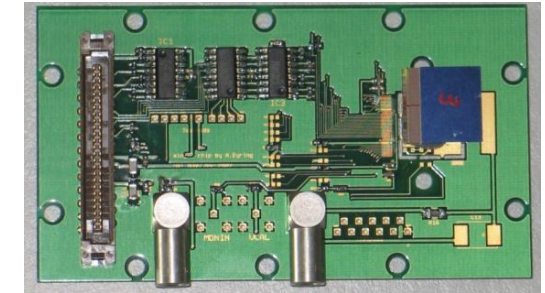**all bumps are connected!!!**

90 µm
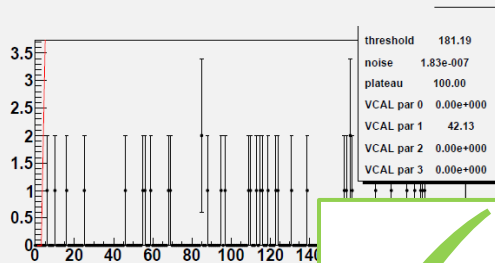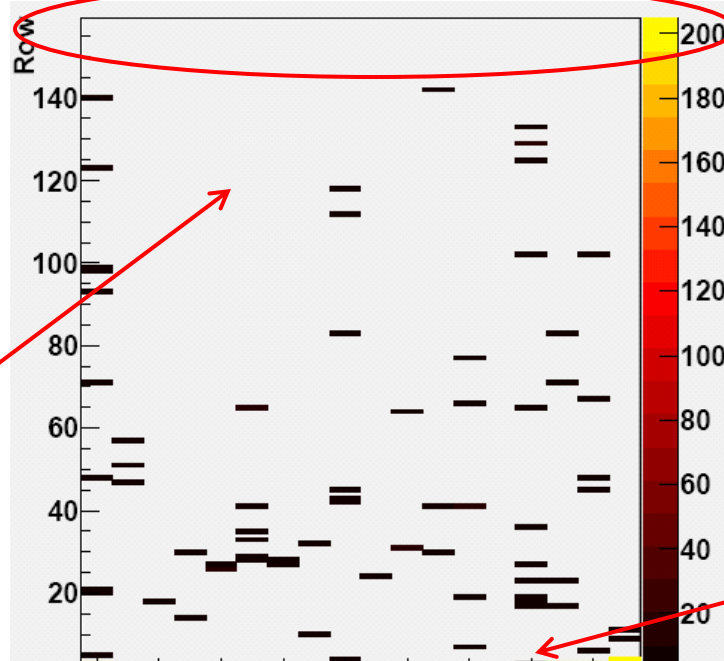
100 µm

90 µm

100 µm

Results of electrical tests

Normal threshold behavior = unconnected bumps

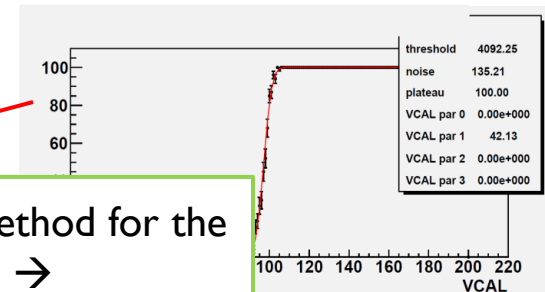All bumps
connected in
"critical" area…

..and across the chip

Some disconnected
bumps close to the End
of Column region →
**Handling problems
during wire bonding**

Polyimide method works. Chosen thinning method for the
FE-I4 thin chip modules prototyping program →
FE-I4 will be 16.8 x 20.2mm², 90μm thick

Serial powering

- Allows transmitting power at low currents and high voltages
  - A chain of n modules is powered in series by a constant current I
  - Current to voltage conversion is performed locally (on chip/module) by regulators
- Key facts
  - I scales of a factor n, wrt parallel powering
  - V_{drop} is limited only by the power density and the current source output voltage capability

→Low I + high V_{drop} tolerance = reduced power cable cross section
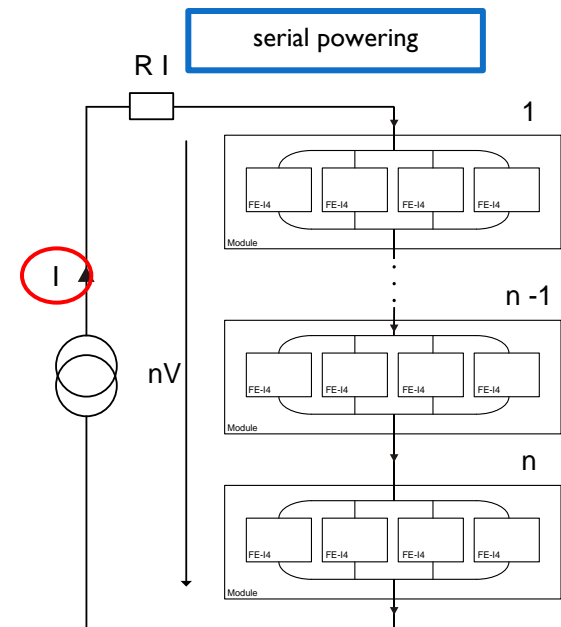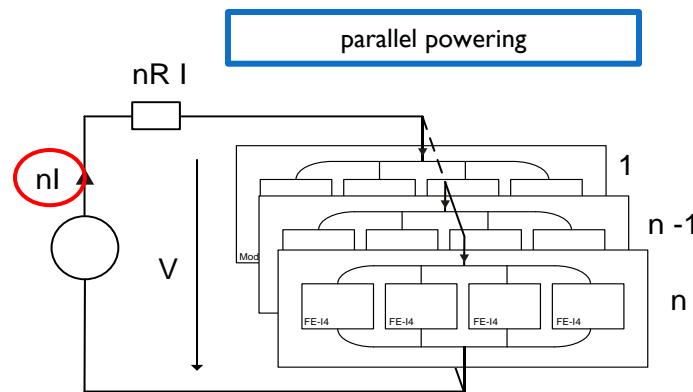
LV cables x/X0%: SP vs. DC-DC

Direct powering with DC-DC conv → fixed V_{drop} between V source and converter
@SLHC: 0.2V on stave, 0.8V on Type 1 services
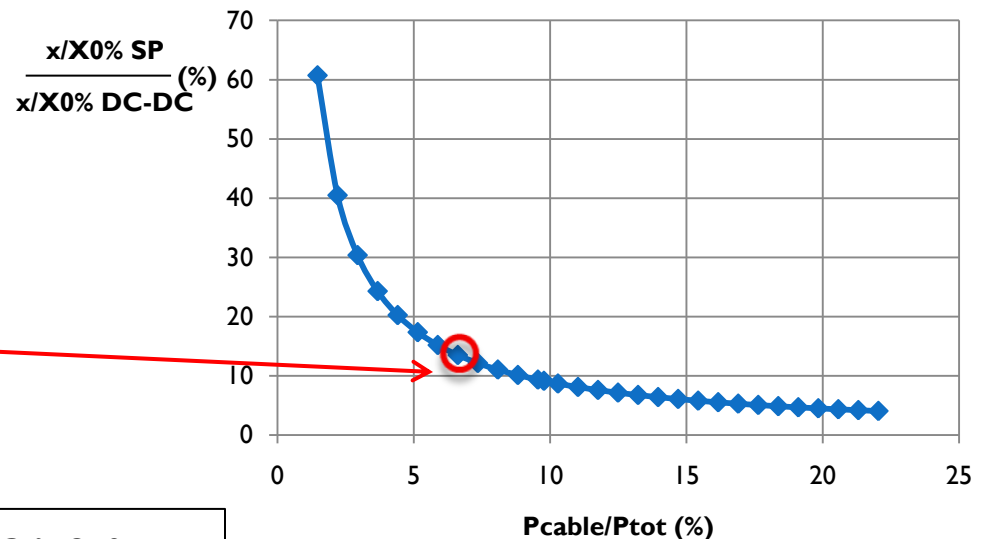
| Active area |

DC-DC conv: Vdrop = 0.2V
→ P_{cable} = 5.56% P_{tot}
→ LV cables: 0.1% X0
SP @ P_{cable} = 5.88% P_{tot}
→ LV cables = 0.014% X0
→ ~85% less material

$\frac{x/X0\% \ SP}{x/X0\% \ DC\text{-}DC}$ (%)

Pcable/Ptot (%)

| Large η |

DC-DC conv: V_{drop} = 0.8V → LV cables: 2827.2mm^2 x-section
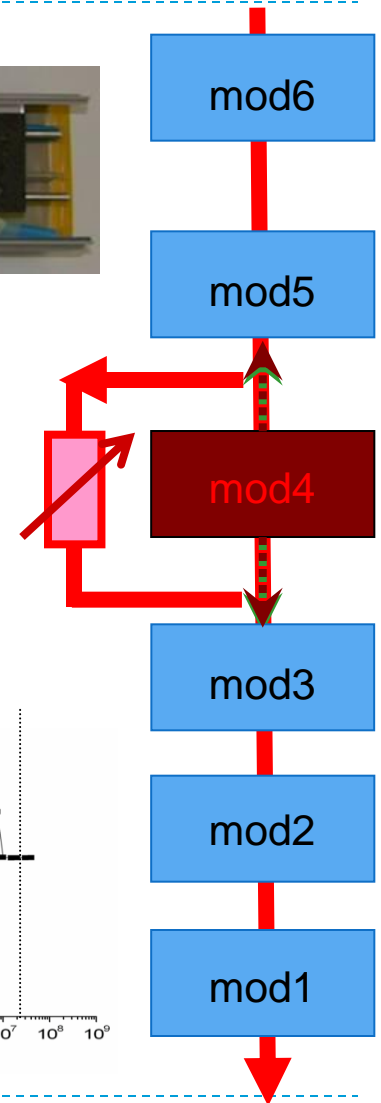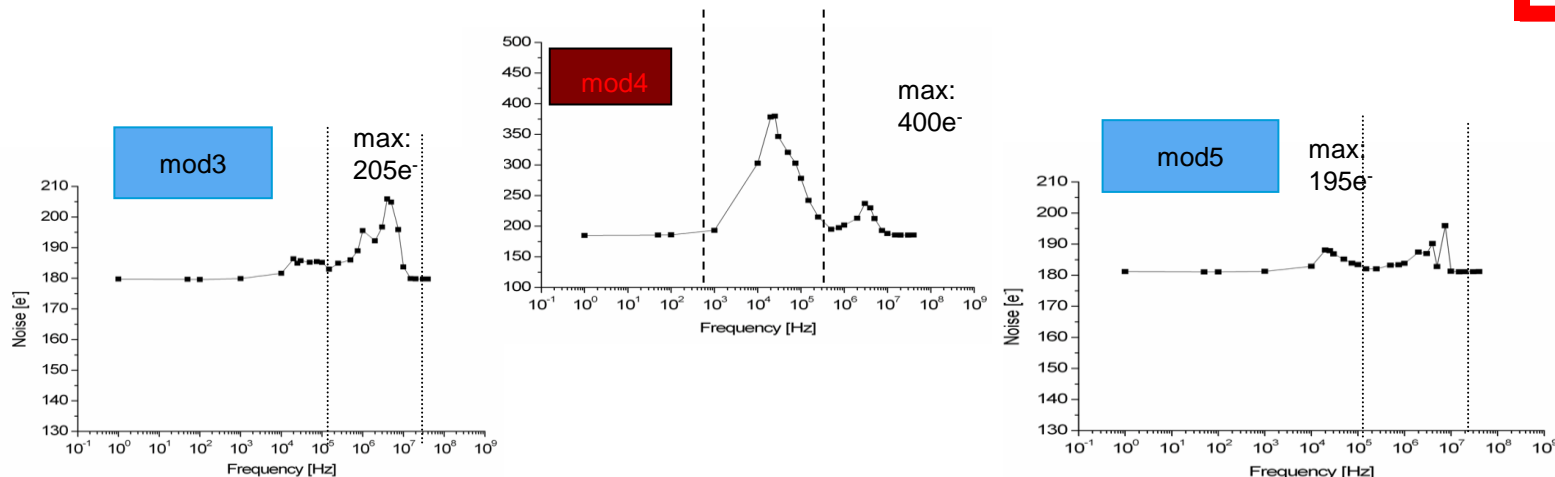SP @ V_{drop} = 0.8V → LV cables = 684mm^2 x-section
x/X0% SP = 0.25 x/X0% DC-DC

Serial powering proof of principle (2005)

(D.B. Ta *et al*, NIM A 557 (2006) 445-459)

▶ **Half stave of the current ATLAS pixel detector powered in series**

 ▶ No performance degradation due to powering scheme, in particular wrt noise pickup

Switchable load to induce noise

mod6

mod5

mod4

mod3

mod2

mod1

mod3 — max: 205e⁻

mod4 — max: 400e⁻

mod5 — max: 195e⁻

… cont'd work… serial powering for SLHC

▸ New regulator concept targeting serial powering application developed: Shunt-LDO

  ▸ 2 prototypes confirmed working principle and good performance

    ▸ Tested as a single chip and in a serial powering chain with the pixel stave emulator

  ▸ 2 Shunt-LDOs integrated in FE-I4

▸ FE-I4 LVDS receiver design w/ self biased inputs for AC-coupling

▸ Protection scheme is proposed

  ▸ Main element: Module Protection Chip

    ▸ Features slow control and fast response
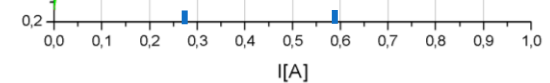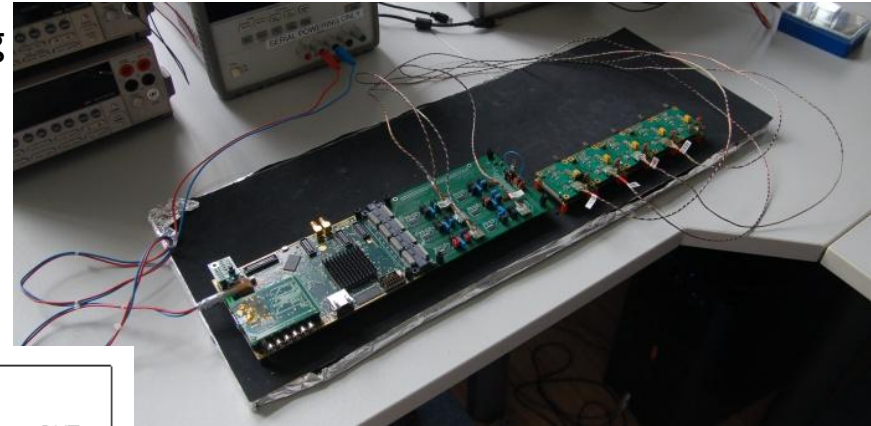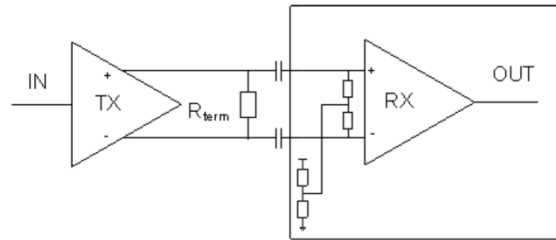
MPC slow ctrl simulation
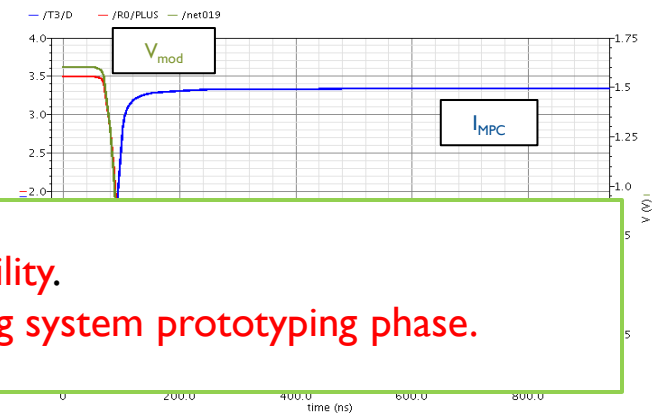
✓ Proof of principle demonstrated feasibility and reliability.
Development of serial powering for SLHC is entering system prototyping phase.
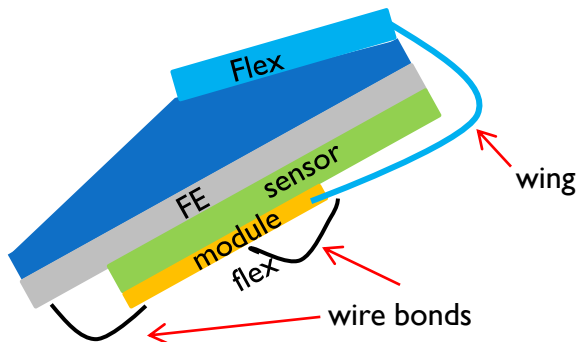
Light Al flex cables

- ATLAS pixels stave services are composed of
  - Module flex (Cu lines) + passive comp → 0.38% X0
  - Pigtail → 0.05% X0
  - Connector + PCB → 0.16% X0
  - Type0 cables (Cu lines) → 0.28% X0

Type 0 cable

ATLAS pixel detector stave services
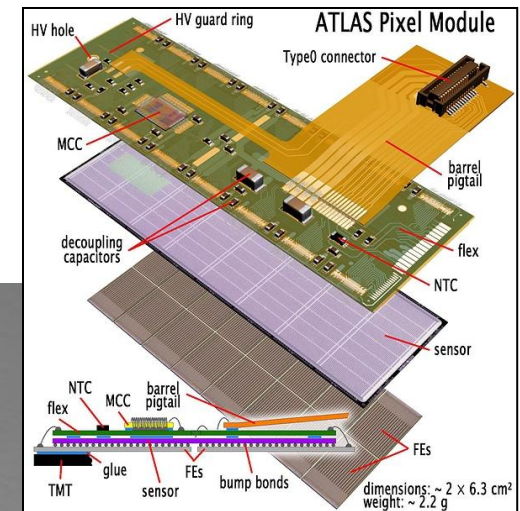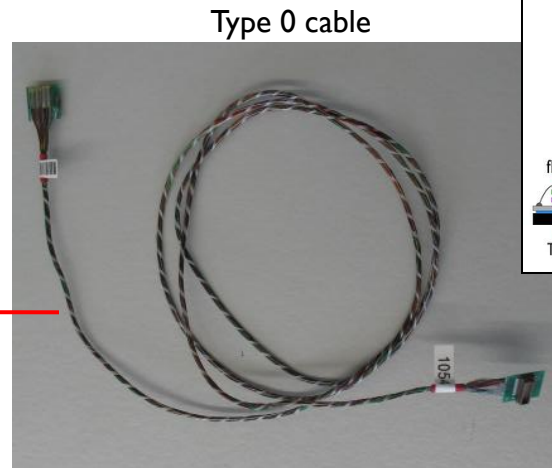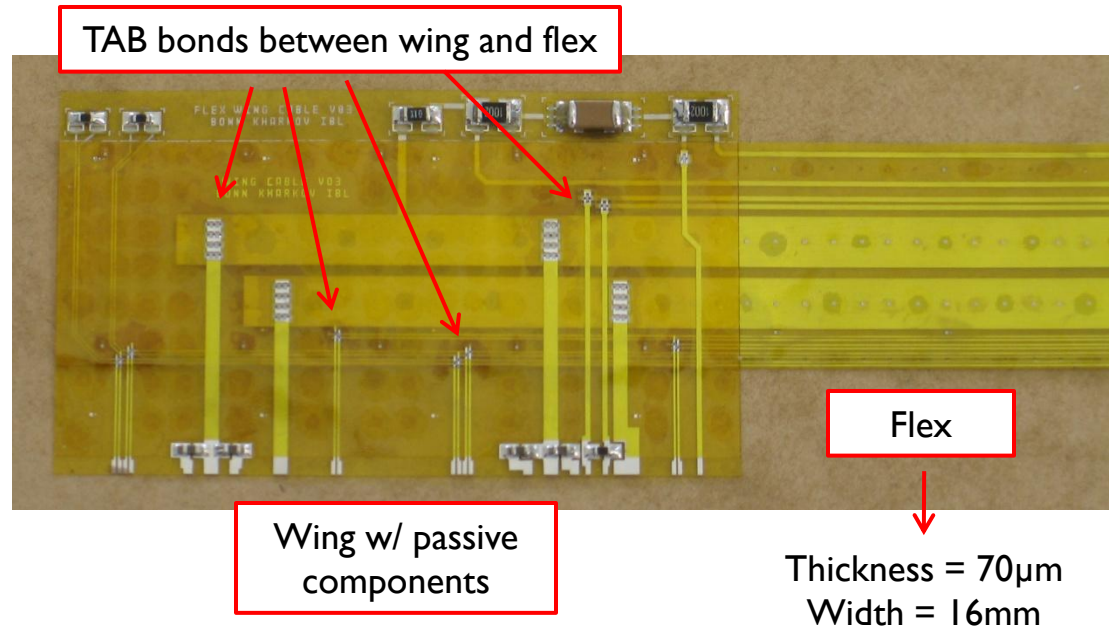

- Lighter alternative for services in active area: flex cables with Al traces
  - X0(Al) factor 6 smaller than X0(Cu)
  - Connection can be done via wire bonds or tab bonding, no need for connectors
- For IBL → stave services with Al flex

Al flex for IBL

- A stack of single sided Al flex running on the back of the stave
- Connection to the modules is done via wings, tab bonded to the flex

TAB bonds between wing and flex

Flex

FE
sensor
module
flex
wing
wire bonds

Wing w/ passive components

Flex

Thickness = 70µm
Width = 16mm

Module flex + pass. comp → stay   0.38% X0 → 0.27% X0
Connector + PCB → wire bonds   0.16% X0 → negligible
Pigtail → wing   0.05% X0 → 0.01% X0
Type 0 cables → Al Flex   0.33% X0 → 0.12% X0

0.92% X0 → ~0.40% X0

Electrical and mechanical tests

Data Source: MATH1	Data Rate: 160 Mbps	Filter: None
SSC: Off	Pattern: 10230 bits	Channel: None
Phase Reference: None	Sample Count: 1.06 M	Equalizer: None

Jitter (Decision Threshold: 173.43 uV)

Random Jitter		
RJ (RMS)	=	31.23 ps
RJ(h) (RMS)	=	23.07 ps
RJ(v) (RMS)	=	21.05 ps
Deterministic Jitter		
DJ	=	1.61 ns
DDJ	=	1.44 ns
DCD	=	44.79 ps
DDPWS	=	1.40 ns
PJ	=	10.40 ps
PJ(h)	=	10.40 ps
PJ(v)	=	0 s
Total Jitter @ BER		
TJ (1E-12)	=	1.93 ns
Eye Opening (1E-12)	=	4.32 ns
Dual Dirac		
RJ(d-d)	=	39.16 ps
DJ(d-d)	=	1.38 ns

Noise (Sampling Phase: 0 UI)

| Random Noise | | |
RN (RMS)	=	5.07 mV
RN(v) (RMS)	=	5.07 mV
RN(h) (RMS)	=	2.18 uV
Deterministic Noise		
DN	=	180.79 mV
DDN	=	180.10 mV
DDN(level 1)	=	161.42 mV
DDN(level 0)	=	167.67 mV
PN	=	983.34 nV
PN(v)	=	0 V
PN(h)	=	983.34 nV
Total Noise @ BER		
TN (1E-12)	=	241.29 mV
Eye Opening (1E-12)	=	330.43 mV
Eye Amplitude	=	571.72 mV
SSC Modulation		
Magnitude	=	0 ppm
Frequency	=	0 Hz

BER Contour

BER Bathtub
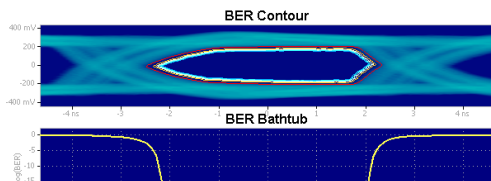
Eye diagram for signal on flex and 6m Type1 cables:
160Mbps, 8b10b encoded prbs
Eye amplitude ~570mV → **OK**
Total jitter 4.32ns → **OK**
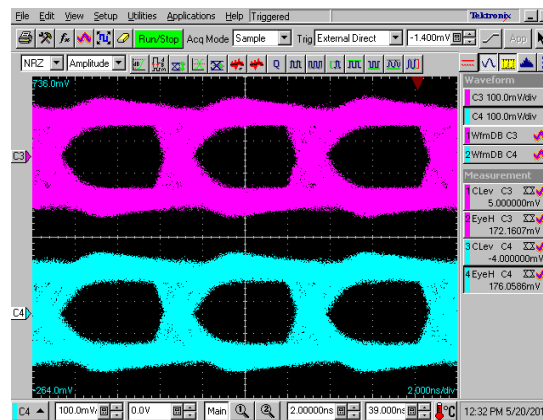
Bending tests (preliminary)
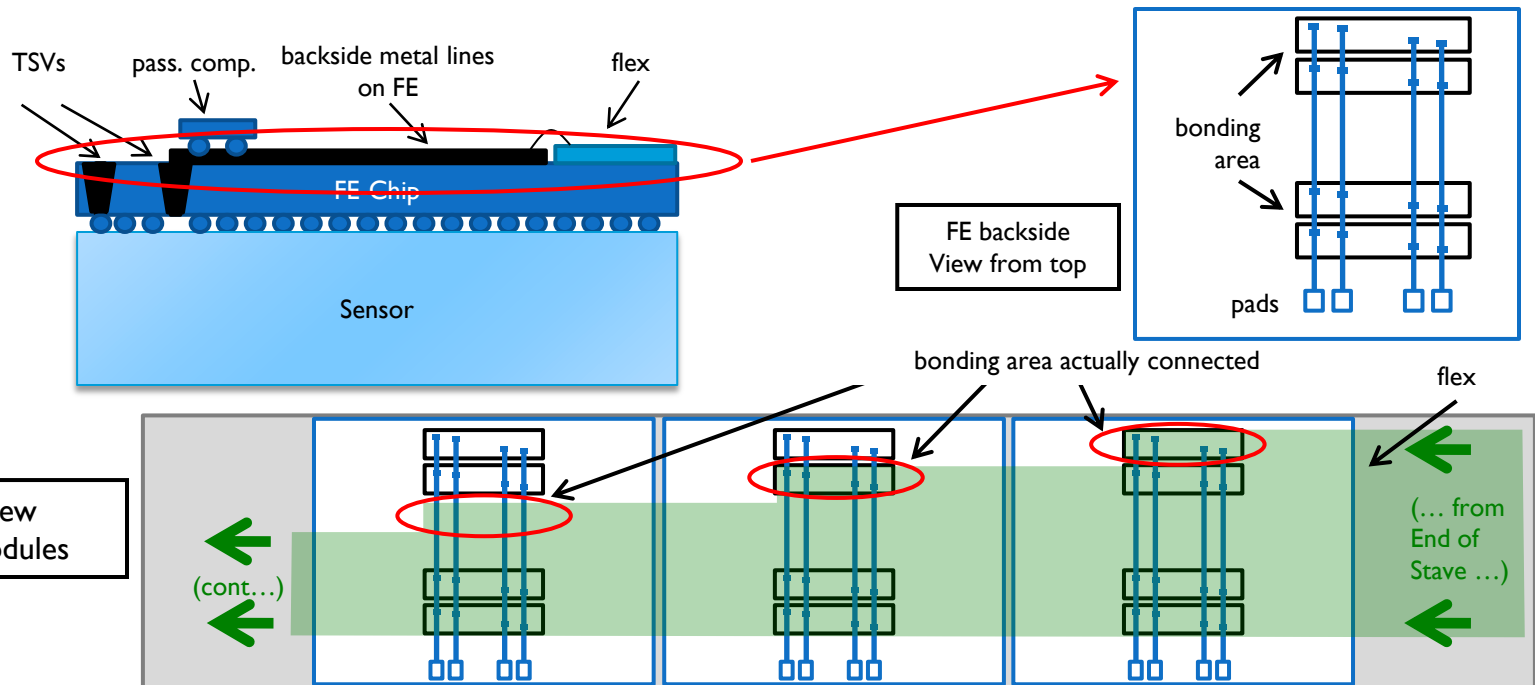Bending radius 0.5mm
No cracks visible → **OK**

PCB — 0,5mm
CC structure — 1mm
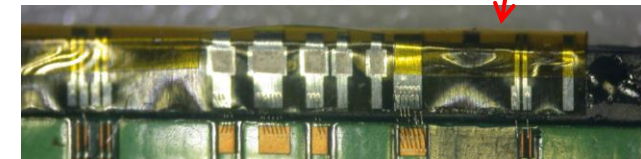
✓ Electrical and mechanical tests on first Al flex prototypes for IBL show good performance.
Final prototype design targeting IBL stave services specs is being designed.
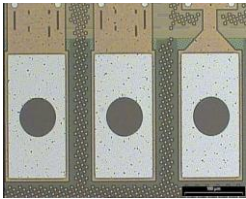
Module concepts with TSV

- TSV is a 3D interconnection technique that allows routing of signals on the FE backside → **direct connection of service flex on FE backside** (via wire bonding for instance)
  - Less material: no need for wings, module flex, connectors
    - Using the IBL as an example (note: TSV will not be used for the IBL!): Al flex + wire bonds + pass. comp.: **~0.13%X0**
  - Easy interconnection scheme
- 2 processes studied so far with IZM Berlin: Straight Side Walls and Tapered Side Walls TSVs
  - Both working, tapered side walls TSVs faster process → preferred method for prototyping program
  - An ATLAS pixel module with 90μm thick FE-I2 and tapered TSVs with simple backside metallization is being build at IZM Berlin

TSVs
pass. comp.
backside metal lines on FE
flex
FE Chip
Sensor

FE backside
View from top

bonding area

pads

bonding area actually connected

flex

Stave top view
Single chip modules

(cont…)

(… from End of Stave …)

Tapered TSVs processing on ATLAS FE-I2

Front side processing

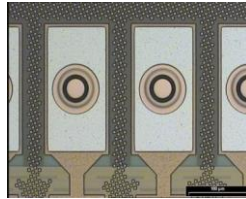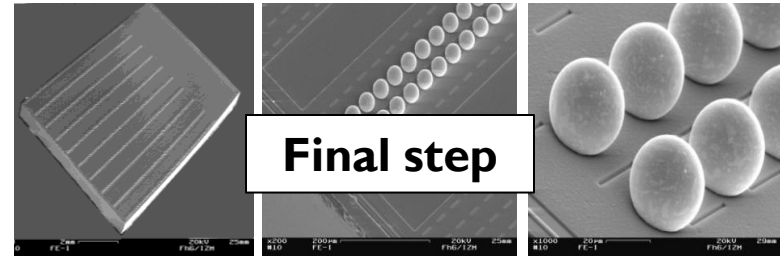Al pad opening by wet etching

BEOL SiO2 stack etching

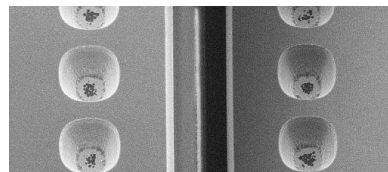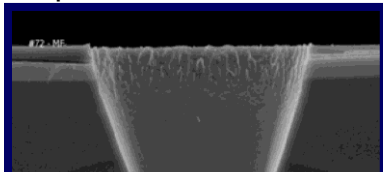Cu electroplating – interconnection plug to Al pad
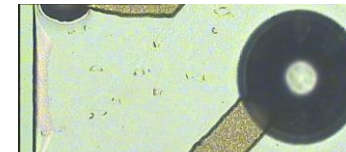
Done

Bump deposition and dicing

Final step

Back side processing

Thin chip!
90μm

Tapered side walls TSV

Backside redistribution

Ongoing

✓ Process demonstrated on Monitor- and ATLAS FE-I Wafer → Prototyping of an ATLAS pixel module with 90μm thin FE-I2, Tapered TSVs, and simple backside metallization is ongoing with IZM Berlin. First samples expected in 04/2011

Conclusions and Next Steps

▸ Possible ways of reducing material budget in trackers for HEP experiments at high luminosity are studied in Bonn, namely

  ▸ Thin chips

  ▸ Serial powering

  ▸ Al flex cables & TSV

▸ The feasibility of all methods has been demonstrated and they are now entering the final prototyping phase

▸ Case study: upgrades of the ATLAS pixel detector

  ▸ Thin chips: FE x/X0% = 0.54% X0 (400μm) → 0.12% X0 (90μm)

  ▸ Serial powering:

    ▸ on stave: LV cables x/X0% SP ≤ 15% LV cables x/X0% DC-DC

    ▸ Type1 services: LV cables x/X0% SP ≤ 25% LV cables x/X0% DC-DC

  ▸ Al flex (+TSV): stave services @LHC = 0.92% X0 → @IBL = ~0.40% X0 (~0.13% X0)