PAUL SCHERRER INSTITUT

PSI

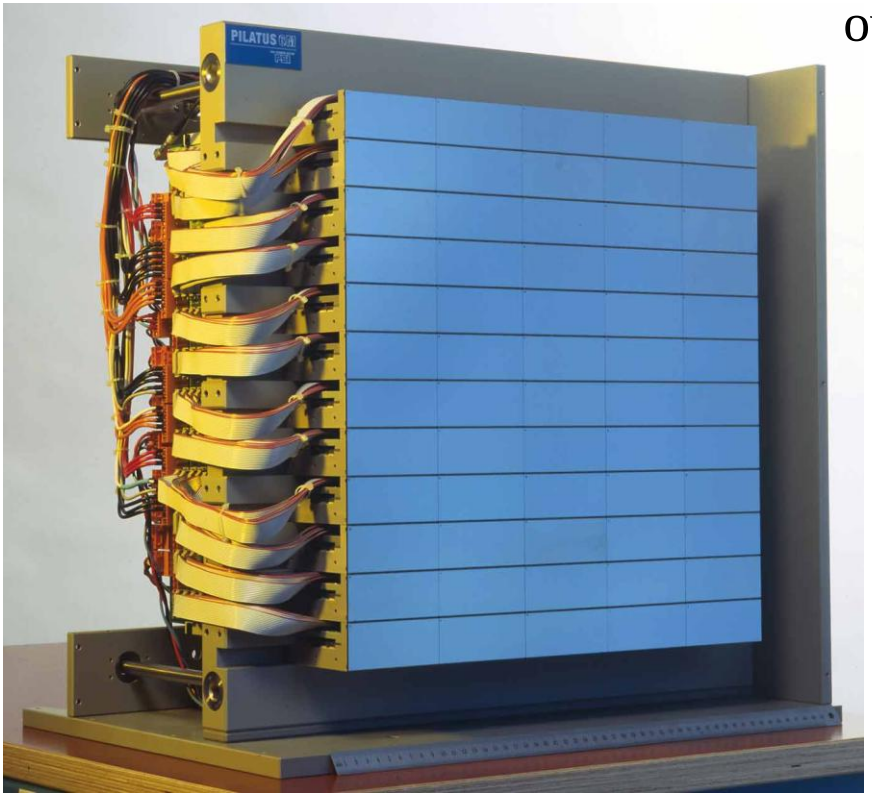
Wir schaffen Wissen – heute für morgen

Paul Scherrer Institut
Roberto Dinapoli

EIGER: next generation single photon counting detector for X-Ray applications

EIGER motivation

Pilatus II, 6M



•PILATUS II is a hybrid, single photon counting pixel detector for synchrotron radiation, which showed very good performance.

•The EIGER design targets several improvements over PILATUS, the main ones are:

- •Decrease the pixel size (still keeping radiation tolerant design)
- •Increase the frame rate
- •Minimize the dead time
- •Keep the frame rate independent of the detector size

•EIGER is focused towards diffractive experiments:

- Coherent Small Angle X-ray Scattering
- Coherent Diffractive Imaging
- X-ray Photon Correlation Spectroscopy
- Scanning SAXS
- Protein Crystallography

EIGER main features (I)

Technological process	**UMC 0.25 µm**
Radiation tolerance	**Full radiation tolerant design (>4Mrad)**
Analog Parameters	**30 ns peaking time** **~150 ns ret. Zero** **8.8 µW/pixel = 2.3 /** **Gain: 44.6 µV/e-**
Chip size	**19.3 x 20.1 mm^2 (active 19.2x19.2mm^2)** **> 2 x**
Pixel size	**75 x 75 µm^2** **= / 5.3**
Pixel array	**256 x 256 = 65536** **= 11.3 x**
Count rate	**3.4 x 10^9 x-rays/mm^2/s = 5.3 x**
Transistors, Matrix: **Periphery:** **Transistors density:**	**28.44M = 9.5 x** **>120 000** **430/pixel, ~5 x**

In red:
Improvement factor with respect to PILATUS

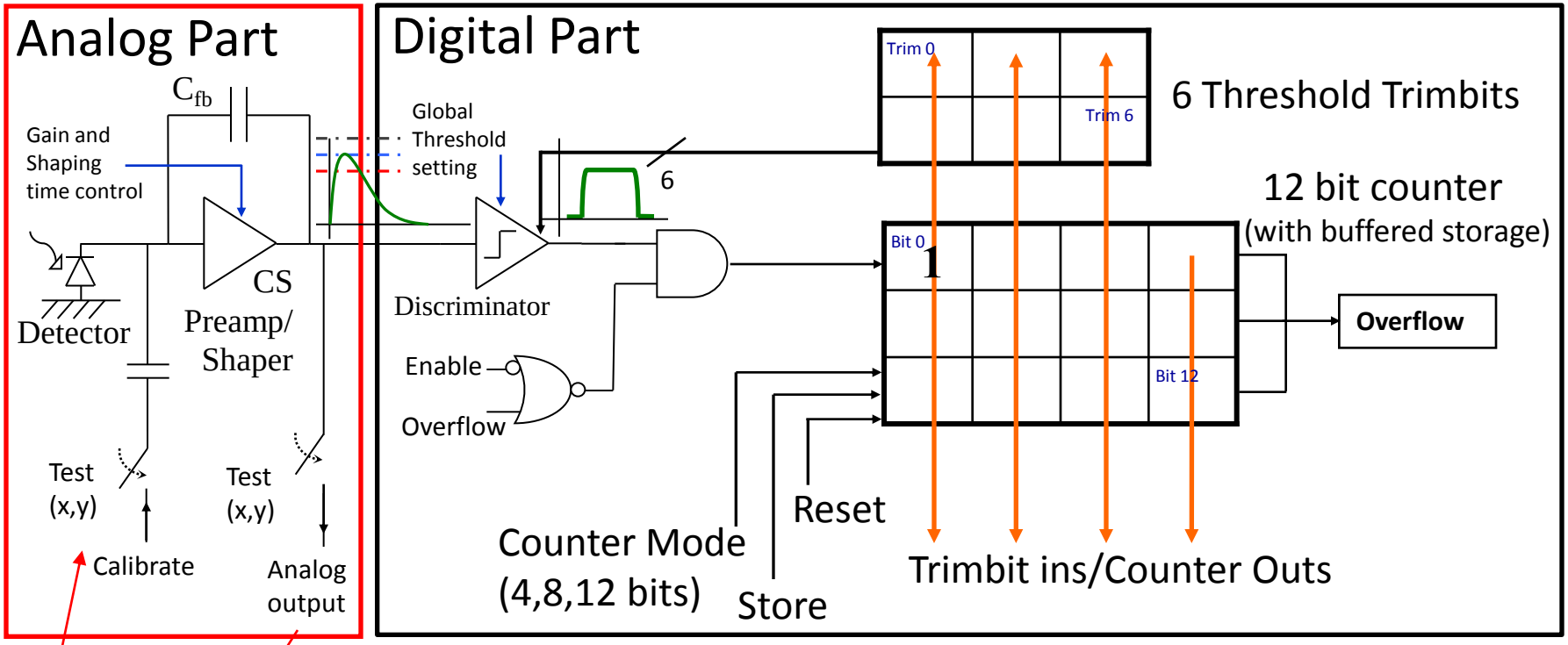
EIGER main features (II)

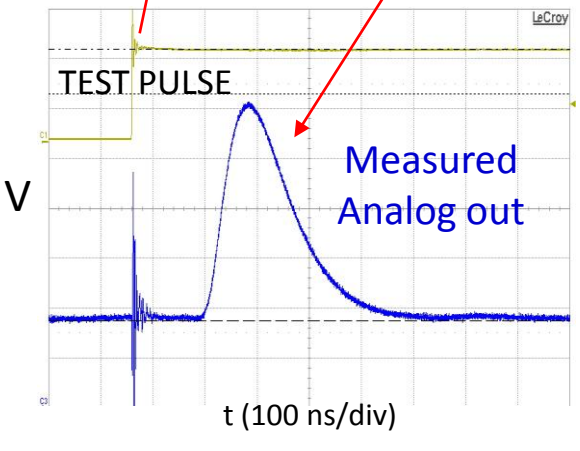
Nominal power supplies	**1.1 V (analog), 2V (digital), 1.8V (I/O)**
Counter	**12 bits, binary, configurable (4,8,12 bit mode), double buffered**
Continuous readout	**yes**
Detector readout speed	**~12 KHz @ 8 bit mode (Detector size doesn't matter) = up to ~2000 x (Clock=100 MHz DDR)**
Threshold adjustment	**6 bit DAC**
XY-addressable analog out for testing	**yes**
Overflow control	**yes**

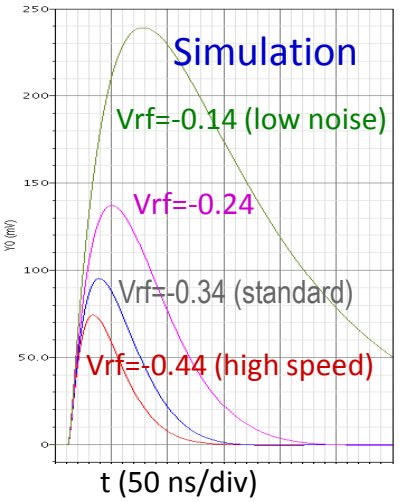
Both the chip and the readout electronics were totally redesigned, and almost all chip blocks are on silicon for the first time.

Project start: 02.2005, chip design as a one man project

The EIGER pixel

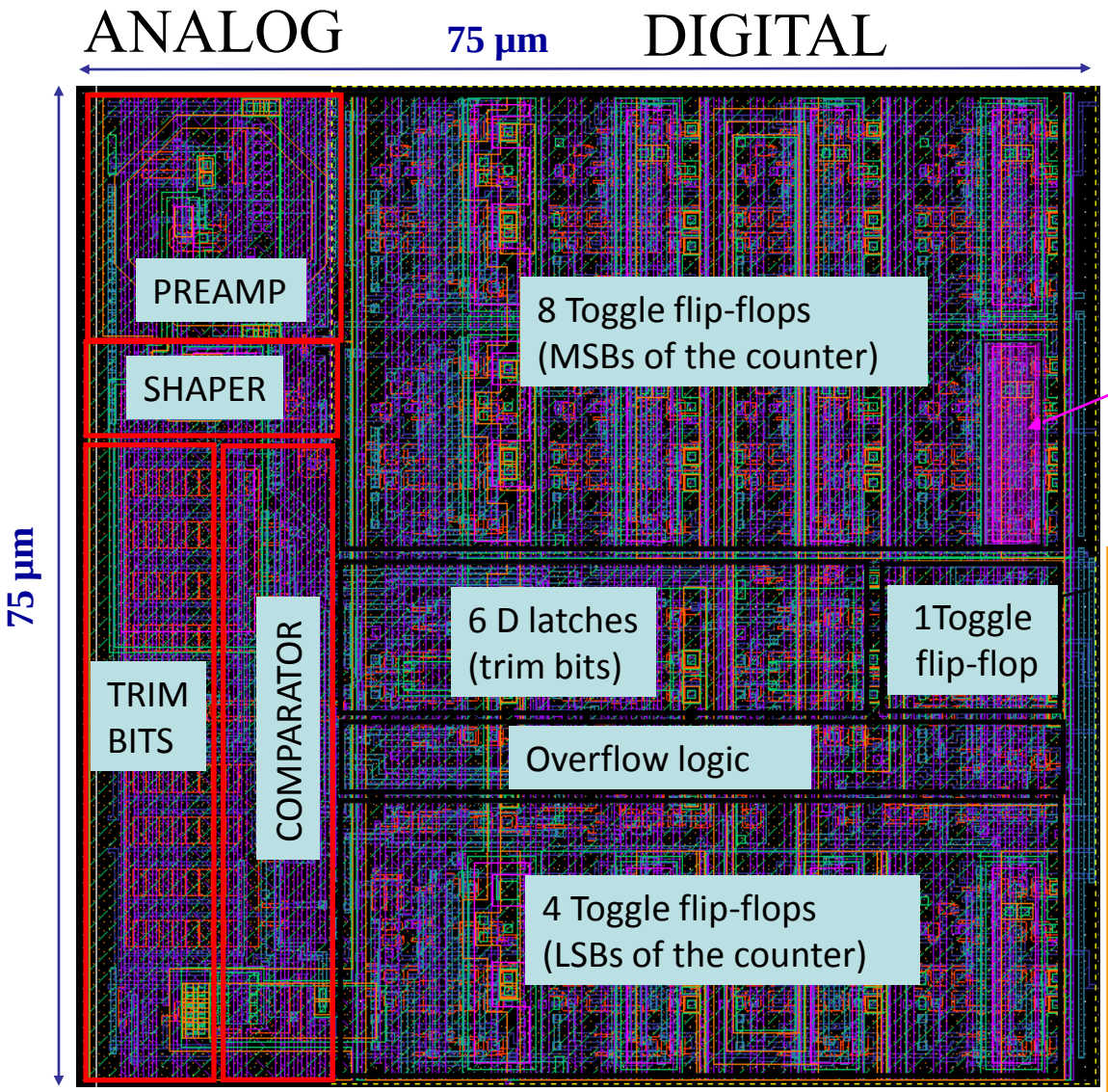




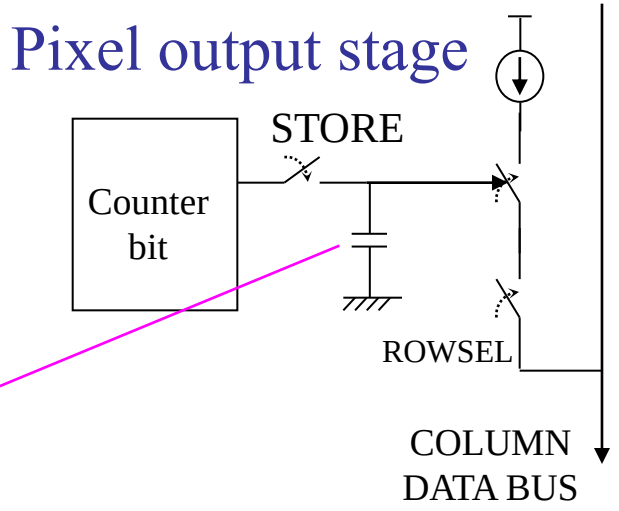


Gain	**44.6 µV/e-**
Timing	**151 ns (Ret.to 0 @ 1%)**
Noise (simul.)	**135 e-rms**
Static power	**8.8 µW/pixel (~0.6W/chip)**
Pixel counter	**12 bits, binary, double buffered (cont. readout), configurable (4,8,12 bit mode)**
Threshold adj.	**6 bit DAC/pixel**

The EIGER pixel on silicon

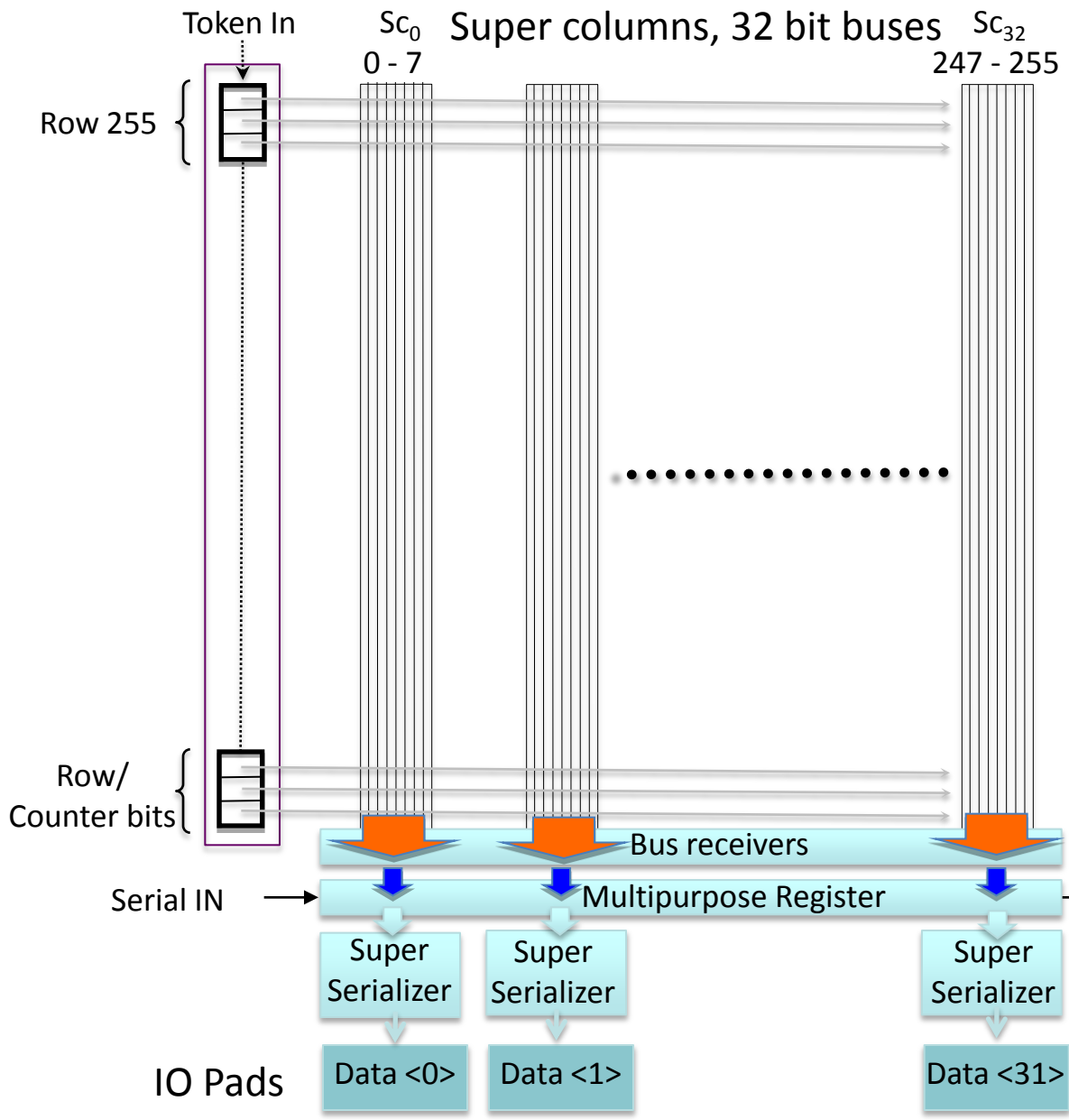


UMC 0.25 µm Technology, full radiation tolerant layout



- Bump bond connection
- Preamp (TWELL)/shaper
- Comparator
  - Global threshold plus pixel trimming (6 bits)
- 12 bit counter
  - Counter logic
  - Buffered storage
  - Trim latches
  - Overflow logic

EIGER readout architecture



Super column structure

- 8 columns/super column
- 32 super columns
- Current mode data buses

Token Shift Register

- Connects 4 bits of the counter storage cells or trimbits of a row to the bottom register

Bus receivers

- Perform I/V conversion

Multipurpose register

- Configurable serial/parellel I/O

Super serializers

- Serialize data sent to the pad

32 Data pads

- 100 MHz DDR,TWELL

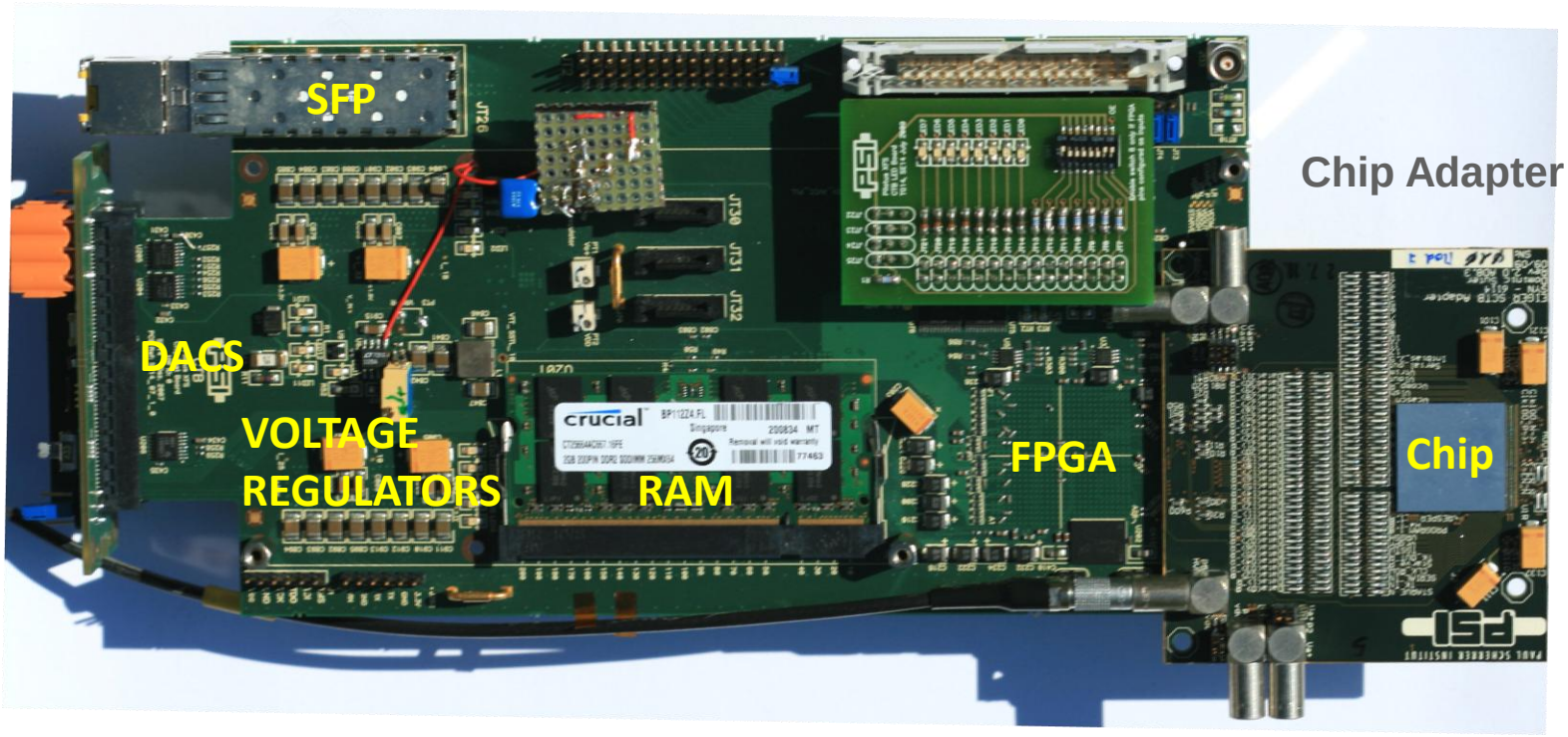
Modes of operation:

- Data taking
- Test
- RO test
- Program
- Serial readout

Single chip test setup

- Pattern generator
- Python scripts
- Full Detector control GUI

1Gb Ethernet Data Link

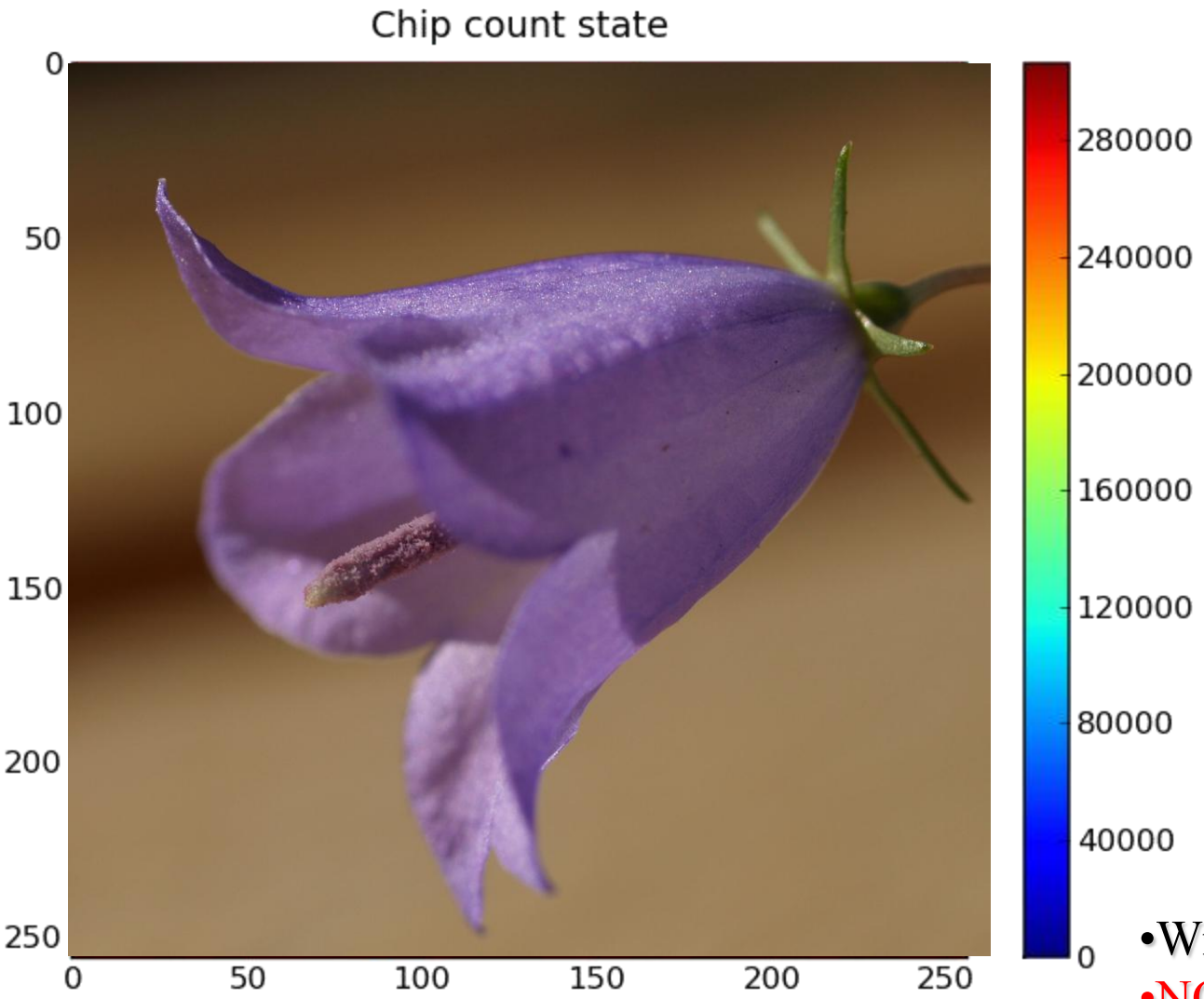


Chip Adapter Board

2GBytes DDR RAM

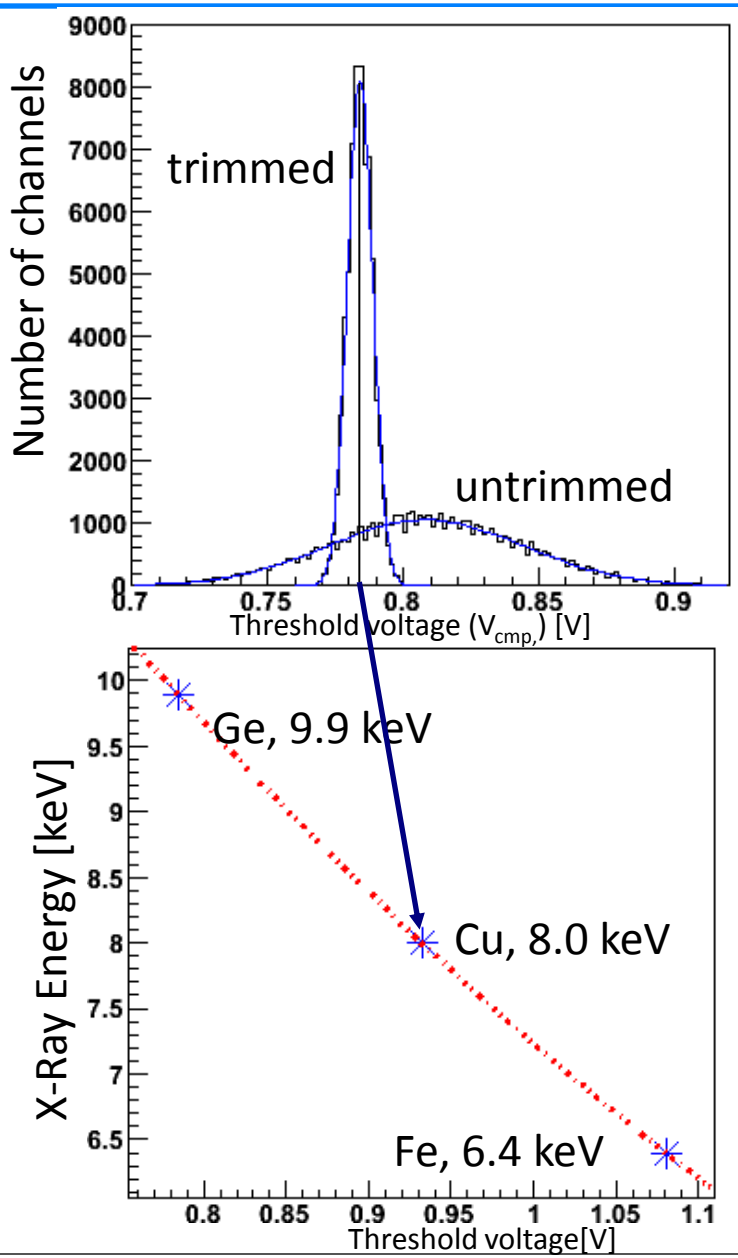
EIGER Single Chip Detector

EIGER absorption images

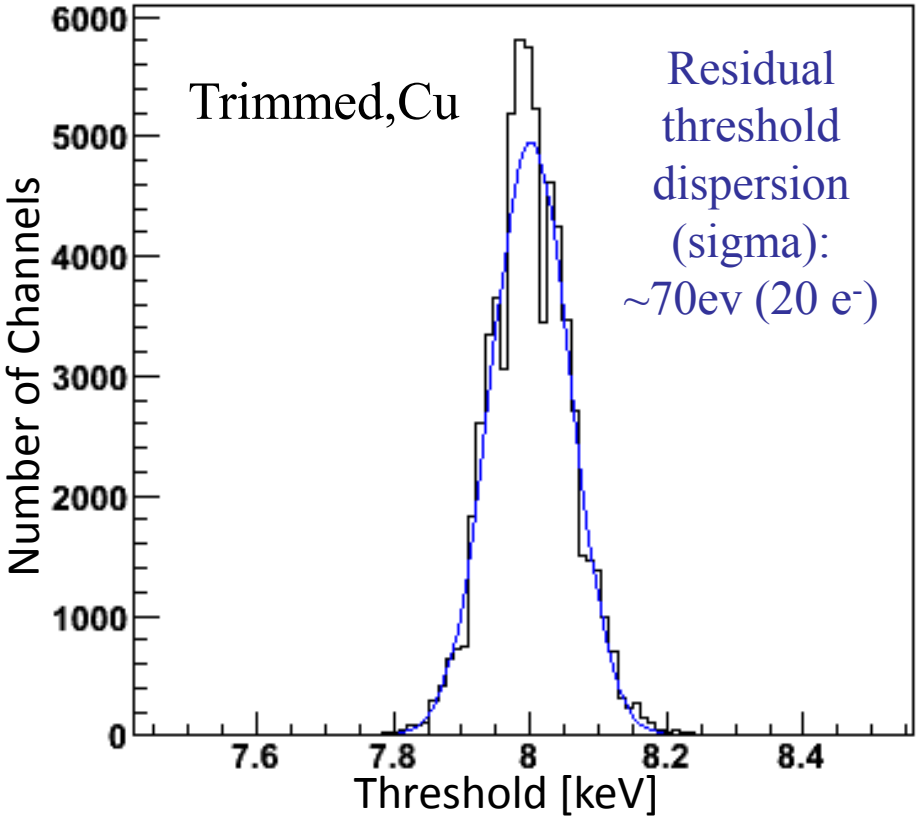


- With flat field
- NO trimming

Trimming and energy calibration



- Data taken with our X-ray box, single chip test system with high gain settings, no continuous readout.



- Noise (sigma) ~650 eV (=180 e^-)
- Minimum threshold ~4.5 keV (=1250 e^-)
- Threshold dispersion (sigma) ~70 eV (=20e^-)

Analysis: Ian Johnson

EIGER trimmed absorption images

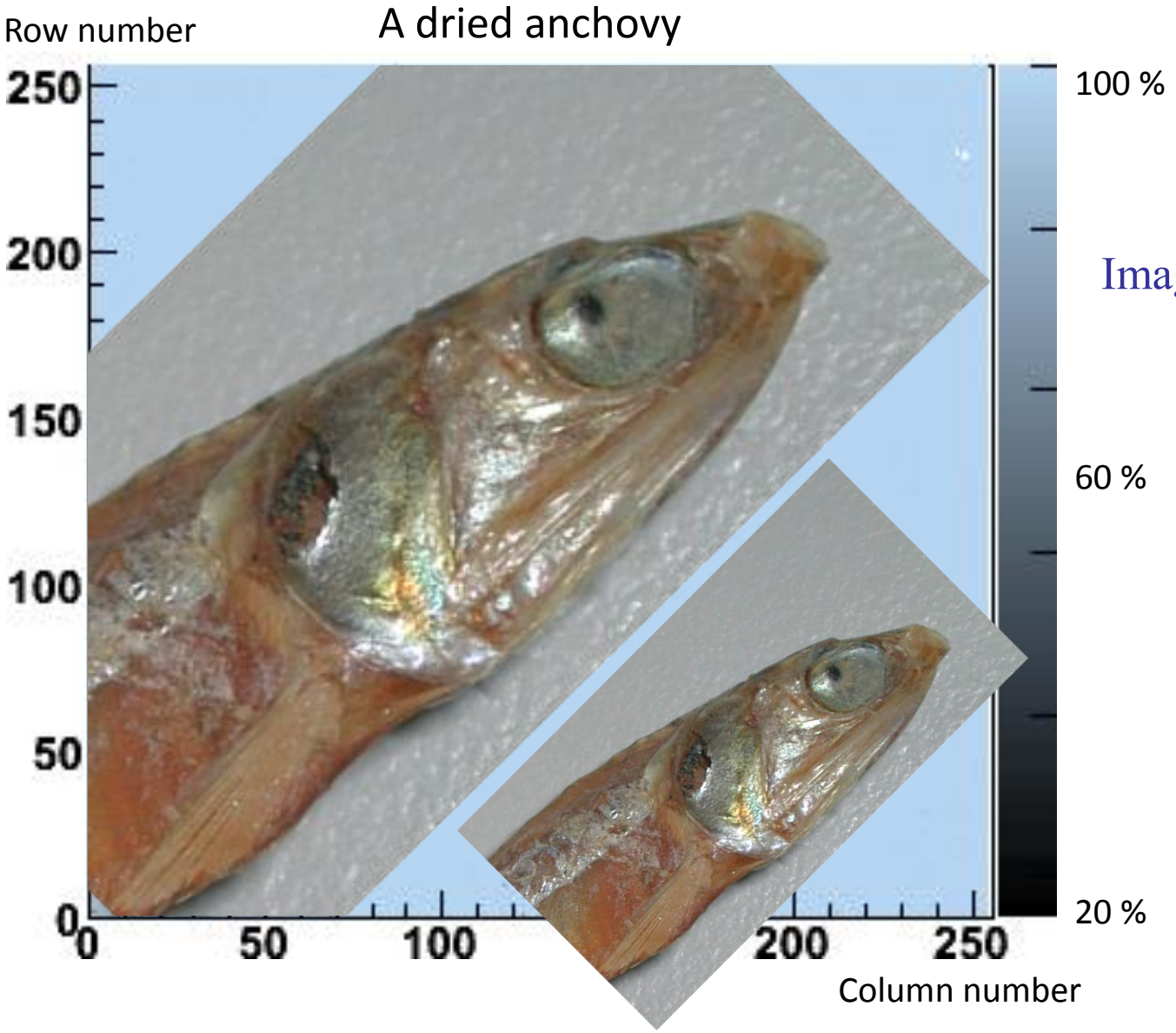
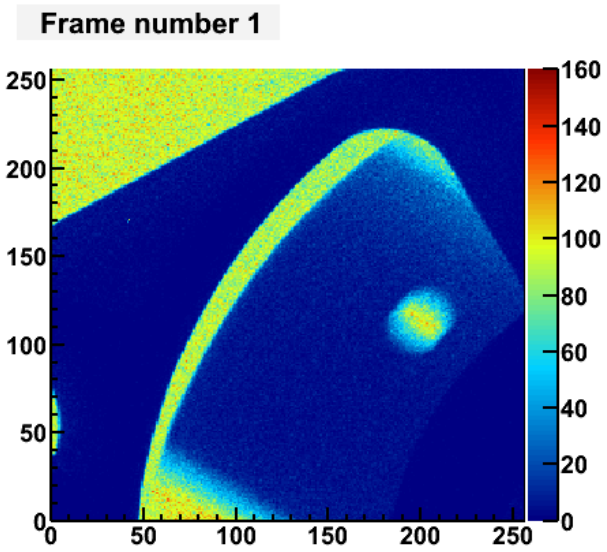


Image directly from detector

- No image processing
- Pixel to pixel differences corrected by trimming

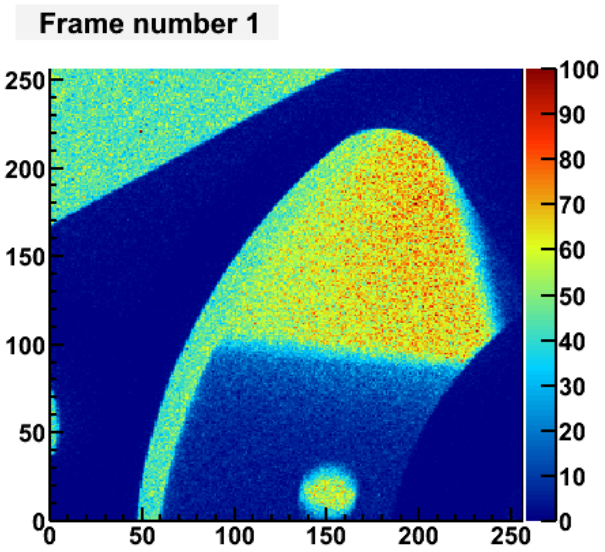
EIGER high frame rate Demo

V = 50KV, I = 0.4mA



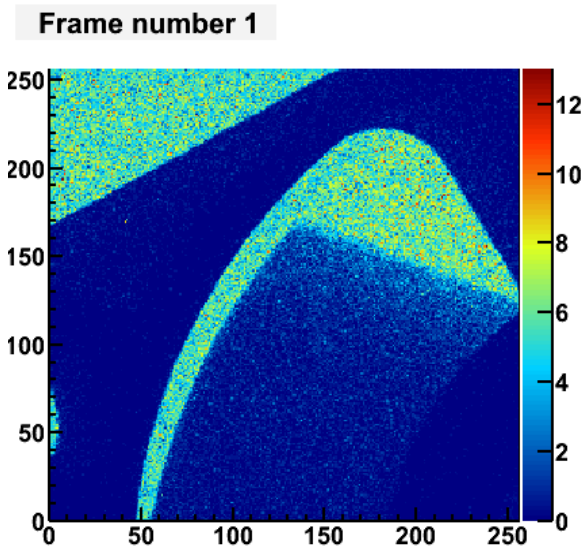
Chip in 12 bit Mode
Exposure time 125µs
Dead time 3µs
Frame rate 7.8 kHz

V = 50KV, I = 1 mA



Chip in 8 bit Mode
Exposure time 85µs
Dead time 3µs
Frame rate 11.4 kHz

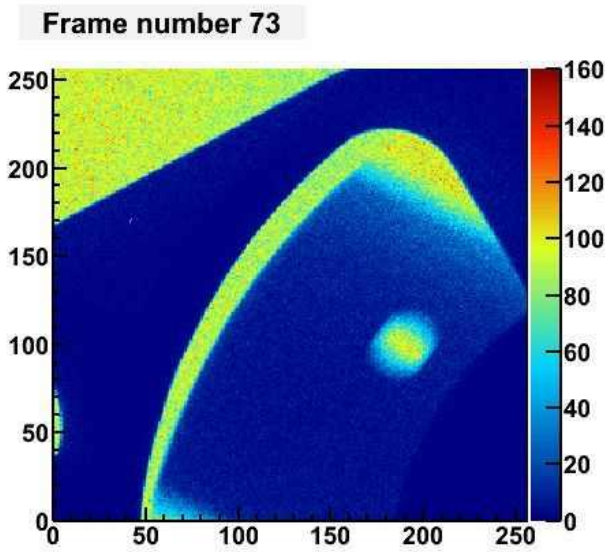
V = 50KV, I = 1 mA



Chip in 4 bit Mode
Exposure time 45µs
Dead time 3µs
Frame rate 20.8 kHz

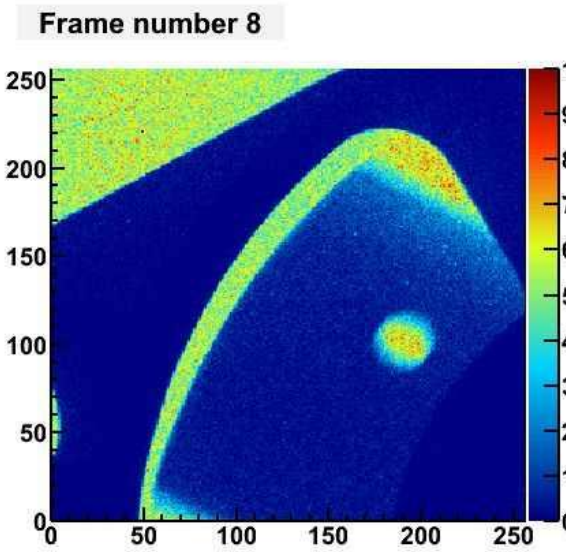
EIGER high frame rate Demo

V = 50KV, I = 0.4mA



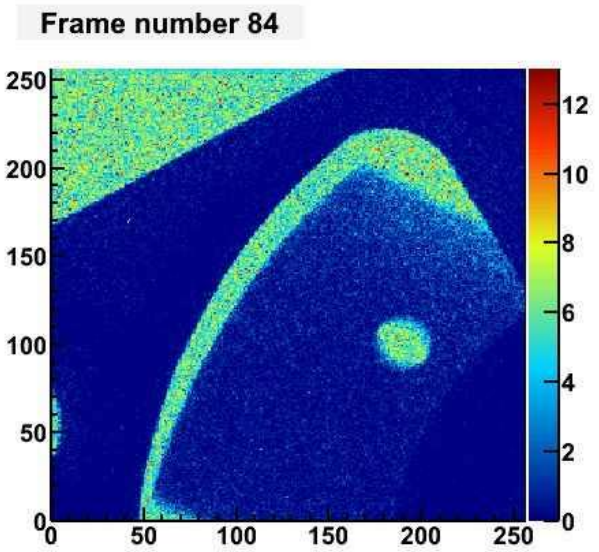
Chip in 12 bit Mode
Exposure time 125µs
Dead time 3µs
Frame rate 7.8 kHz

V = 50KV, I = 1 mA



Chip in 8 bit Mode
Exposure time 85µs
Dead time 3µs
Frame rate 11.4 kHz

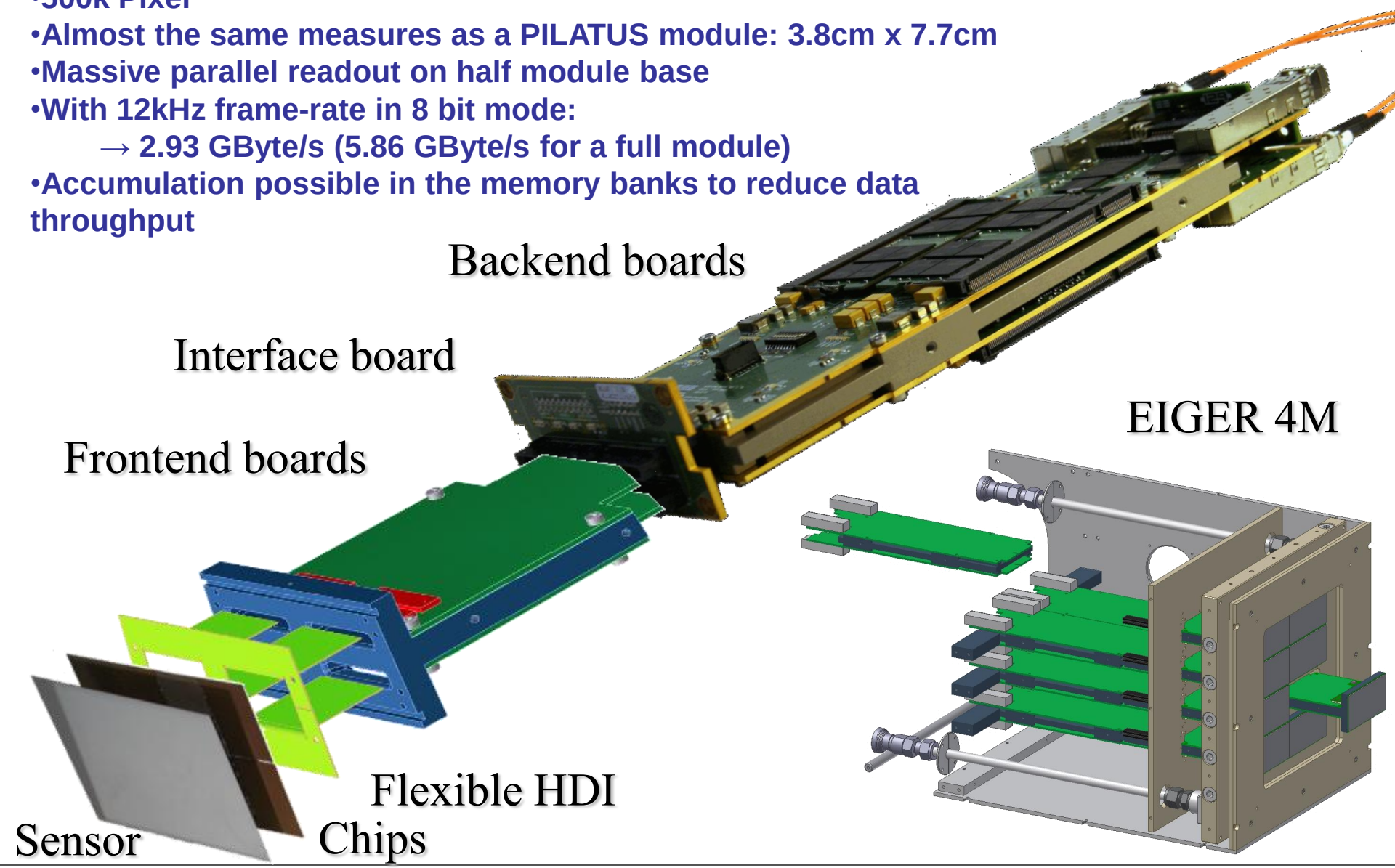
V = 50KV, I = 1 mA



Chip in 4 bit Mode
Exposure time 45µs
Dead time 3µs
Frame rate 20.8 kHz

From chip to module to system

- 500k Pixel
- Almost the same measures as a PILATUS module: 3.8cm x 7.7cm
- Massive parallel readout on half module base
- With 12kHz frame-rate in 8 bit mode:
  → 2.93 GByte/s (5.86 GByte/s for a full module)
- Accumulation possible in the memory banks to reduce data throughput



Present status

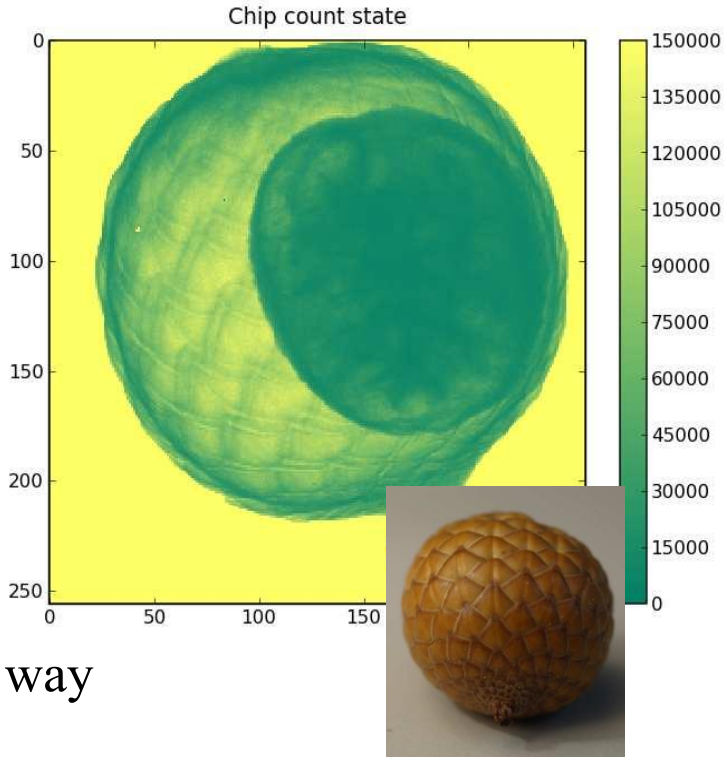
Chip and Sensor •
Produced and tested
Bump bonding •

•Interface board
Produced and tested
•Backend board

Conclusions and future work

- EIGER targets mainly synchrotron based (diffractive) experiments.

- Readout chip main features:
  - smaller pixels (75x75 μm^2)
  - frame rates up to ~ 24 kHz
  - almost dead time free readout (<3µs)



- Single chip assemblies results:
  - The chip meets all the specs
  - After trimming in high gain mode:
    - Noise (sigma): ~650 eV (180 e^-)
    - Minimum threshold: ~4.5 keV (1250e^-)
    - Threshold dispersion (sigma) : ~70 eV (20 e^-)

- We are working toward multi-chip modules
  - All readout electronics working (preliminary)
  - HDI, bump bonded module and firmware on the way
  - Mechanics and cooling ready
  - First prototype modules by the end of this year

- Larger detector systems (possibly up to 16 Mpixel) are planned

ACKNOWLEDGMENTS

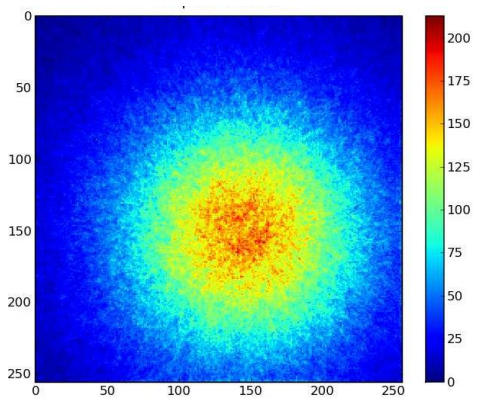
Many thanks to:
Anna Bergamaschi, Heiner Billich, Beat Henrich, Roland Horisberger, Ian Johnson, Philipp Kraft, Beat Meier, Aldo Mozzanica, Peter Oberta, Lukas Schaedler, Elmar Schmid, Bernd Schmitt, Xintian Shi, Silvan Streuli, Dominic Suter, Gerd Theidel.

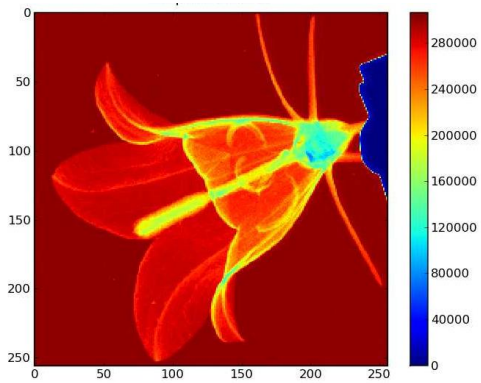
SLS Detector Group

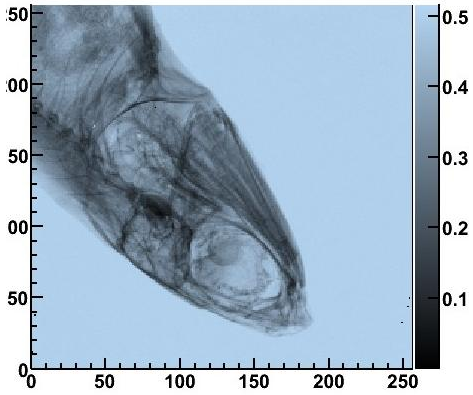
Starting soon:

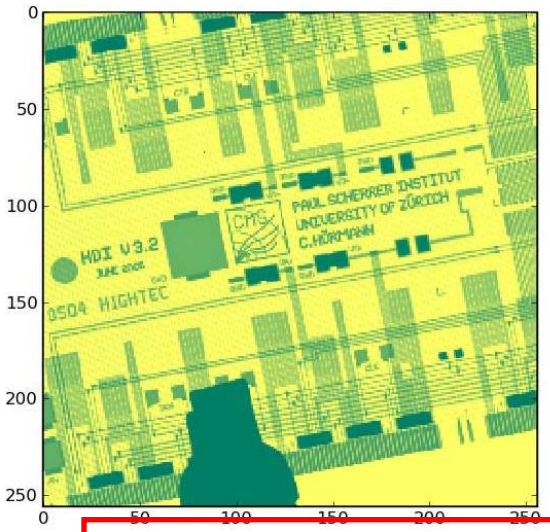
- 2 technicians
- 1 Post-doc for AGIPD (Pixel detector for the European XFEL)

1 Post-doc for EIGER, Valeria Radicci





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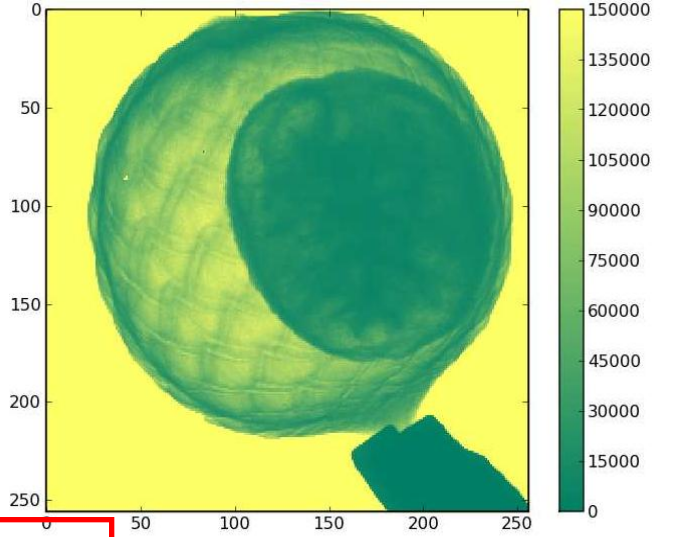
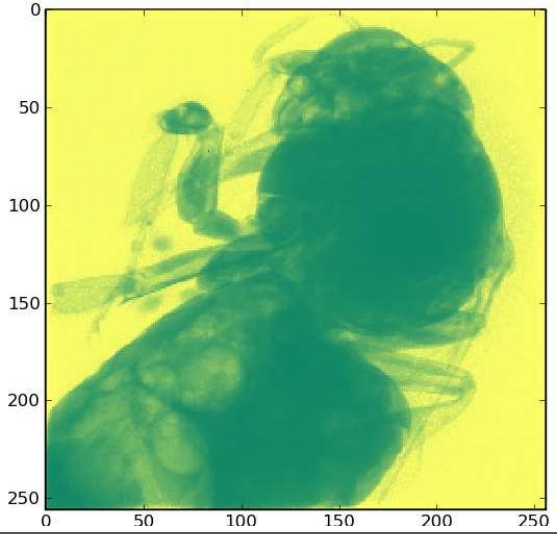
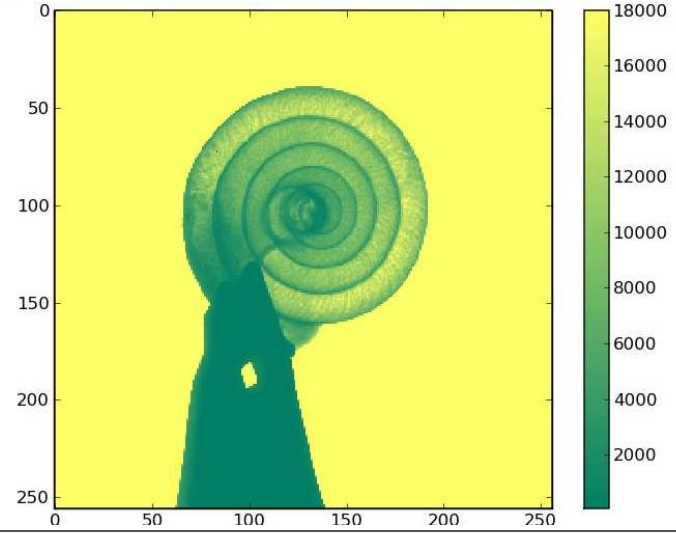
C.HÖRMANN
HDI V3.2
0504 HIGHTEC



THANKS!





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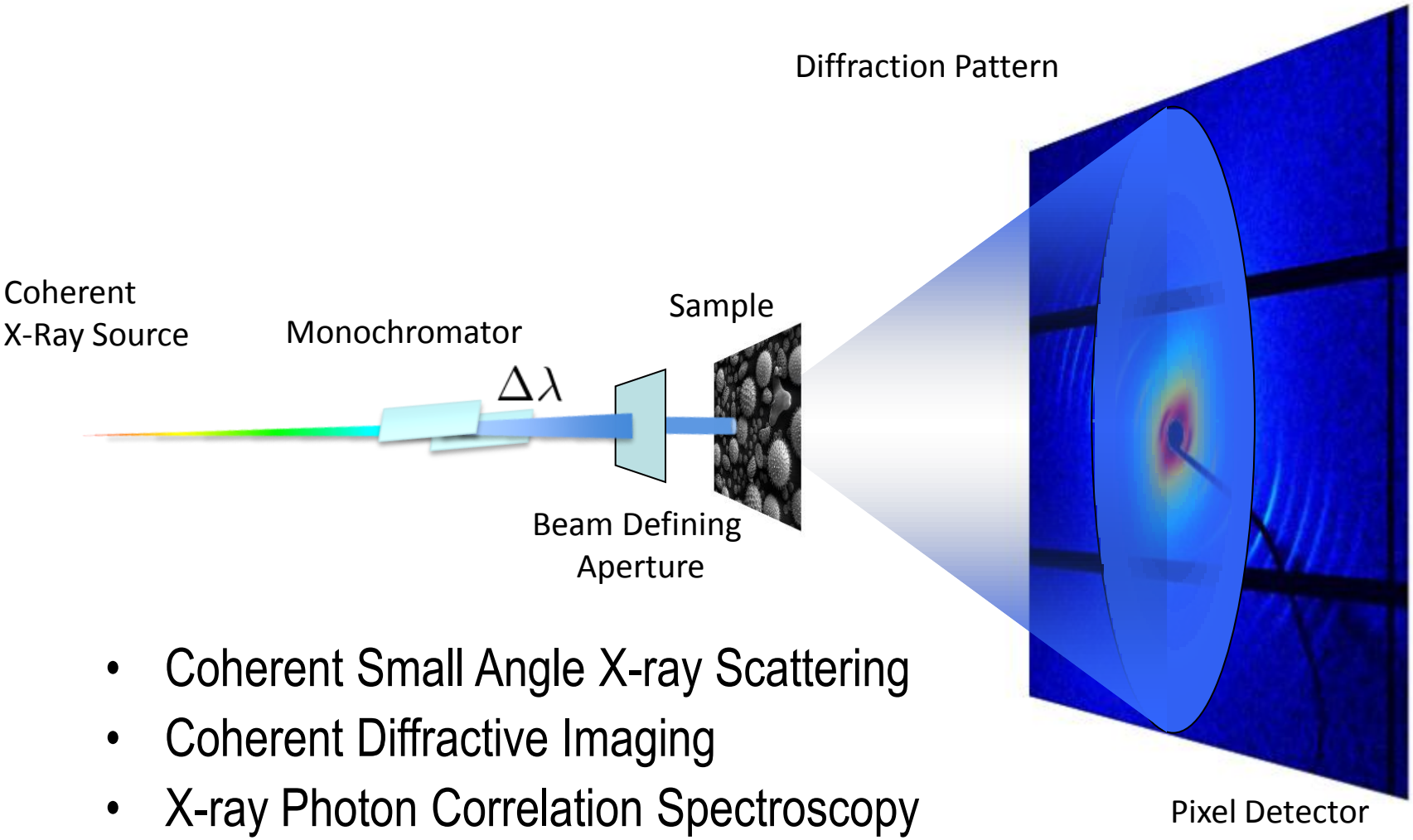
EIGER: How to make Pilatus good for a museum

Eiger is Focused towards Diffractive Experiments



- Coherent Small Angle X-ray Scattering
- Coherent Diffractive Imaging
- X-ray Photon Correlation Spectroscopy
- Scanning SAXS
- Protein Crystallography

EIGER main features (I)

	Pilatus II	EIGER
Technological process	UMC 0.25 µm	The same
Radiation tolerance	Full radiation tolerant design (>4Mrad)	The same
Analog Parameters	30 ns peaking time ~150 ns ret. Zero 20 µW/pix	The same The same 8.8 µW/pixel = 2.3 / Gain: 44.6 µV/e-
Chip size	17.54 x 10.45 mm^2	19.3 x 20.1 mm^2 (active 19.2x19.2mm^2) > 2 x
Pixel size	172 x 172 μm^2	75 x 75 μm^2 = / 5.3
Pixel array	60 x 97 = 5820	256 x 256 = 65536 = 11.3 x
Count rate	1.8 x 10^8 x-rays/mm^2/s	3.4 x 10^9 x-rays/mm^2/s
Transistors, Matrix: **Periphery:** **Transistors density:**	~3M	28.44M = 9.5 x >120 000 430/pixel, ~5 x

EIGER main features (II)

	Pilatus II	EIGER
Nominal power supplies	1.1 V (analog), 2.5V (digital)	1.1 V (analog), 2V (digital), 1.8V (I/O)
Counter	20 bits, pseudo-random, not configurable	12 bits, binary, configurable (4,8,12 bit mode), double buffered
Continuous readout	no	yes
Detector readout speed	~200Hz for 100k 5-10Hz for 6M (Clock=100 MHz)	~12 KHz @ 8 bit mode (Detector size doesn't matter) = up to ~2000 x (Clock=100 MHz DDR)
Threshold adjustment	6 bit DAC	The same
XY-addressable analog out for testing	yes	The same
Overflow control	No	yes

Both the chip and the readout electronics were totally redesigned, and almost all chip blocks are on silicon for the first time.

Project start: 02.2005, chip design as a one man project

EIGER main features (III)

- **Count rate: 1MHz/pixel (1.8 x 10^8 x-rays/mm^2/s)**

  Max. frame exposure time before overflow:

  - **T_{max} @ 4 bit mode = 16 µs**
  - **T_{max} @ 8 bit mode = 256 µs**
  - **T_{max} @ 12 bit mode = 4 ms**

- **100 MHz DDR readout (PII:100 MHz)**
  - **T_{ro} @ 4 bit mode = 40.96 µs**
  - **T_{ro} @ 8 bit mode = 81.92 µs**
  - **T_{ro} @ 12 bit mode = 122.9 µs**
  - **In continuous readout mode, max. frame rate=1/readout time;**
    12.5 KHz @ 8 bit mode

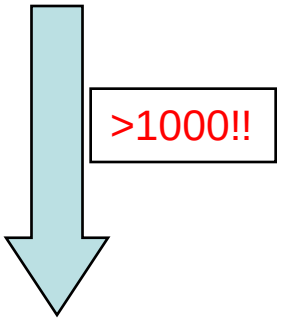
Pilatus II:

- **Same count rate**
- **T_{max} is about a second**

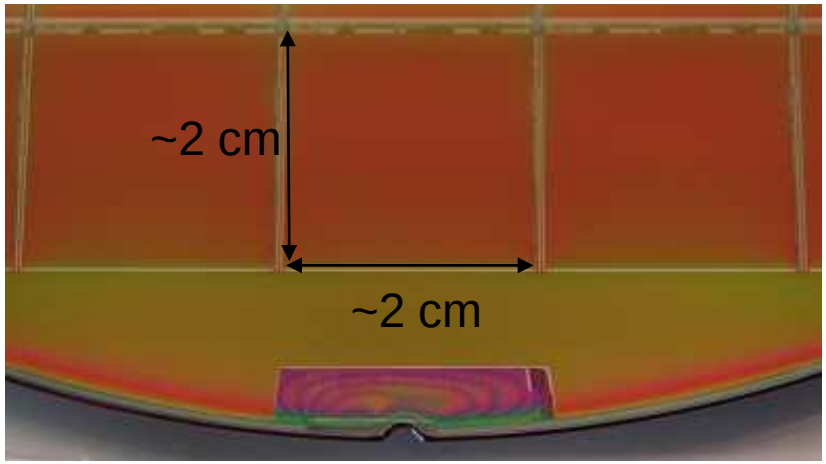
(but no continuous readout!)

Pilatus II:

- **100 MHz LVDS readout**
- **T_{ro} =1.2 ms**
- **BUT: Detector frame rate 5-10 Hz**



Short EIGER history



Design started: 02.2005
→Design supervision: almost none
→Software and system management support: almost none

Tape-out to EUROPRACTICE: 26.02.09

->>Almost all chip blocks are on silicon for the first time

First wafer (with some parameters off-specs) received back from foundry: 03.06.09

Testing started: 10.06.09, the chip is not “smoking”

First image with a Strontium source: 24.08.09

First “high quality” image: 02.09.09

First time at a beamline: 11.09.09

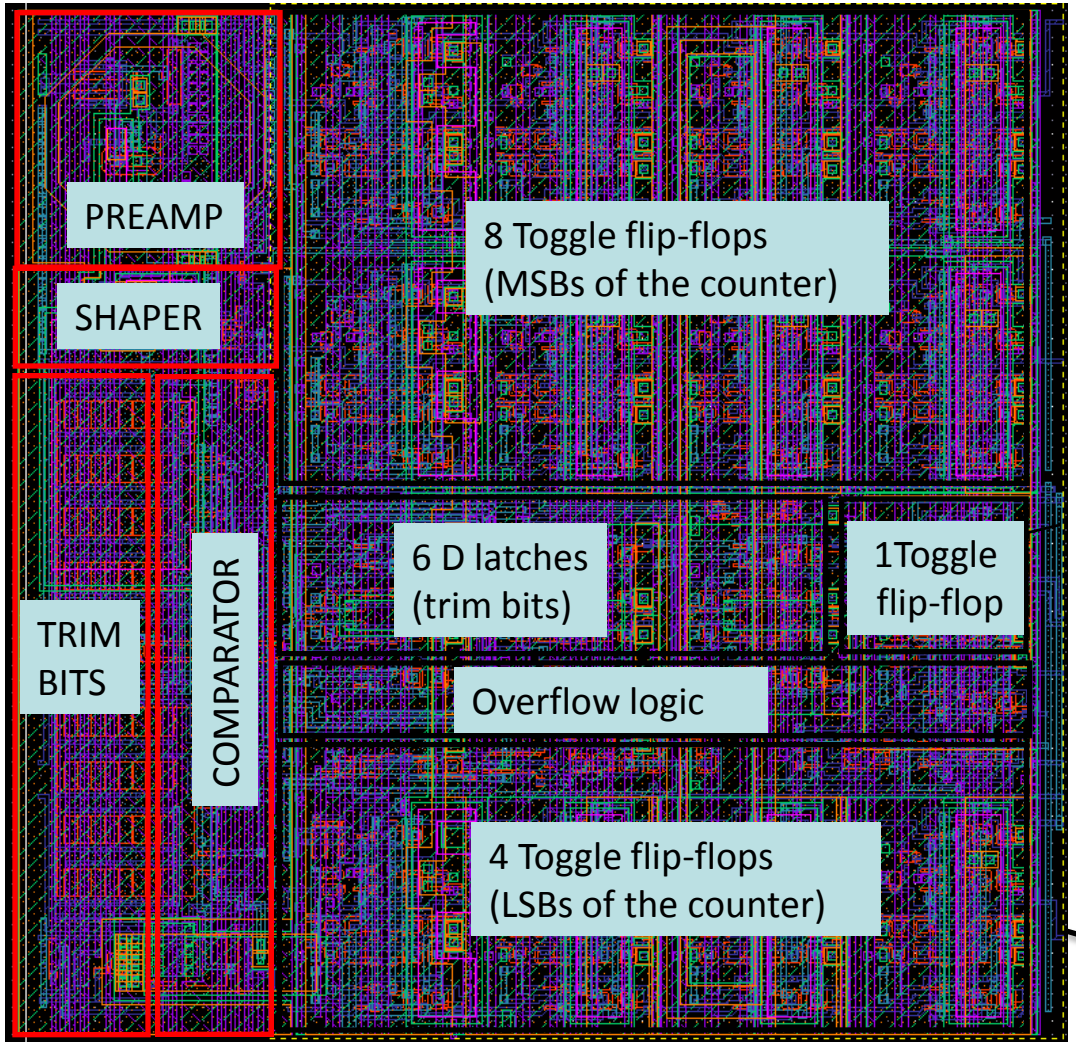
First maximum speed x-ray movie: 28.09.09

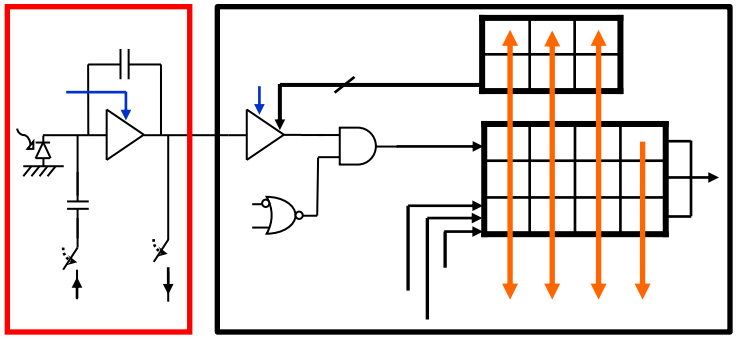
First wafer map: 23.08.10

First conference proceeding paper (ELBA ’09):

“A new family of pixel detectors for high frame rate X-ray applications”
Nuclear Inst. and Methods in Physics Research, A
DOI information: 10.1016/j.nima.2009.10.043

The EIGER pixel on silicon





- Bump bond connection
- Preamp (TWELL)/shaper
- Comparator
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- 12 bit counter
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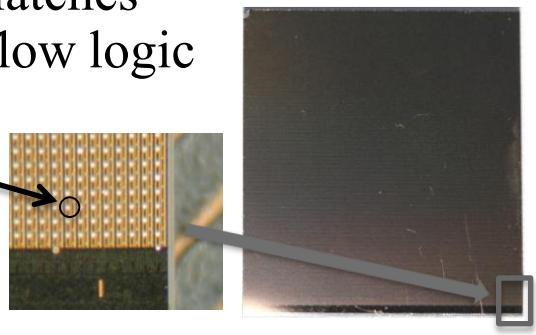
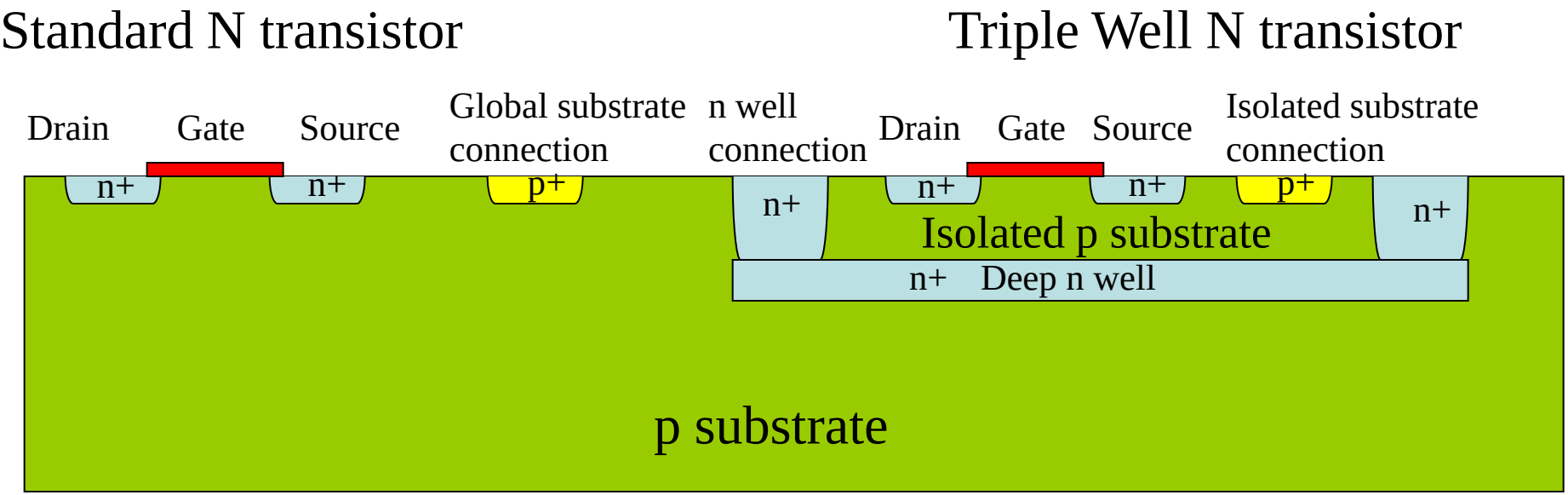


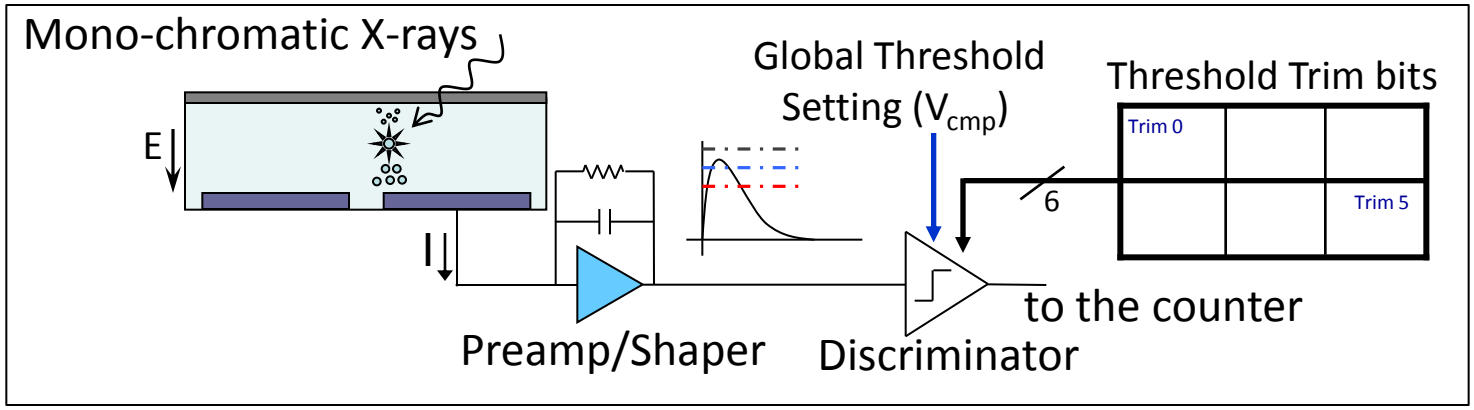
UMC 0.25 µm Technology, full radiation tolerant layout

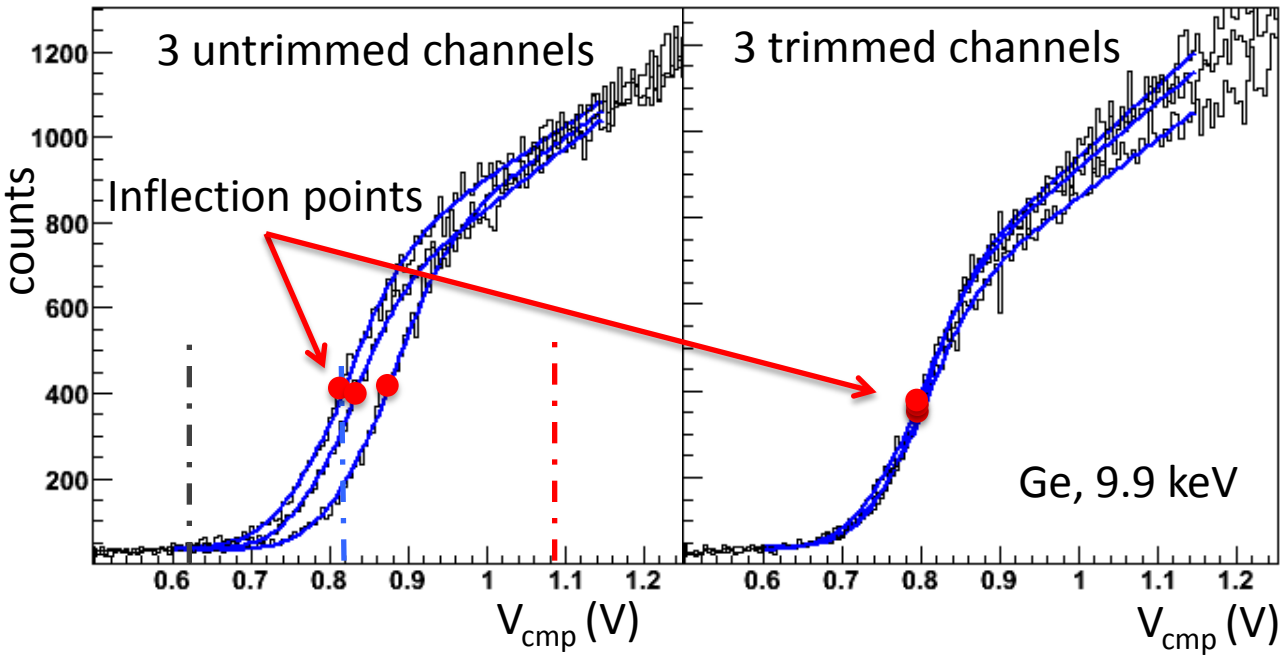
Triple well principle

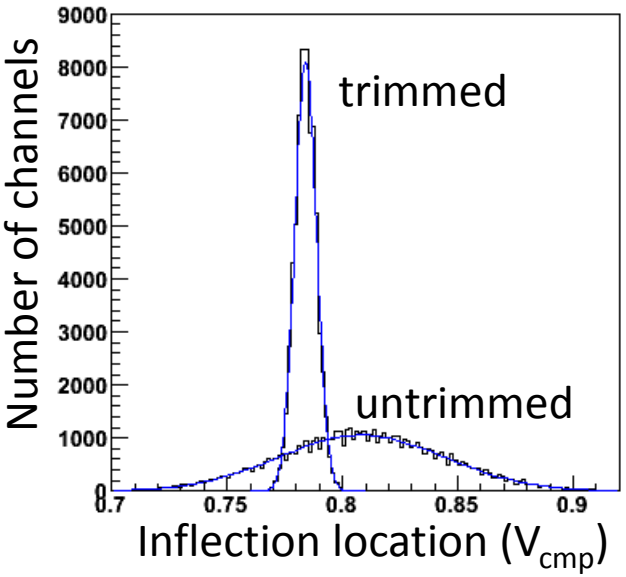


Channel alignment by trimming

•Data taken with our X-ray box

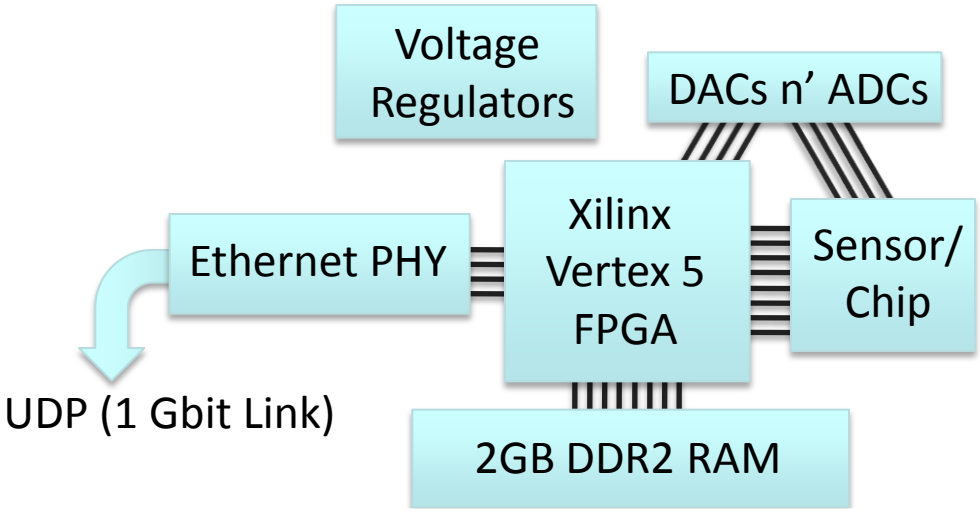




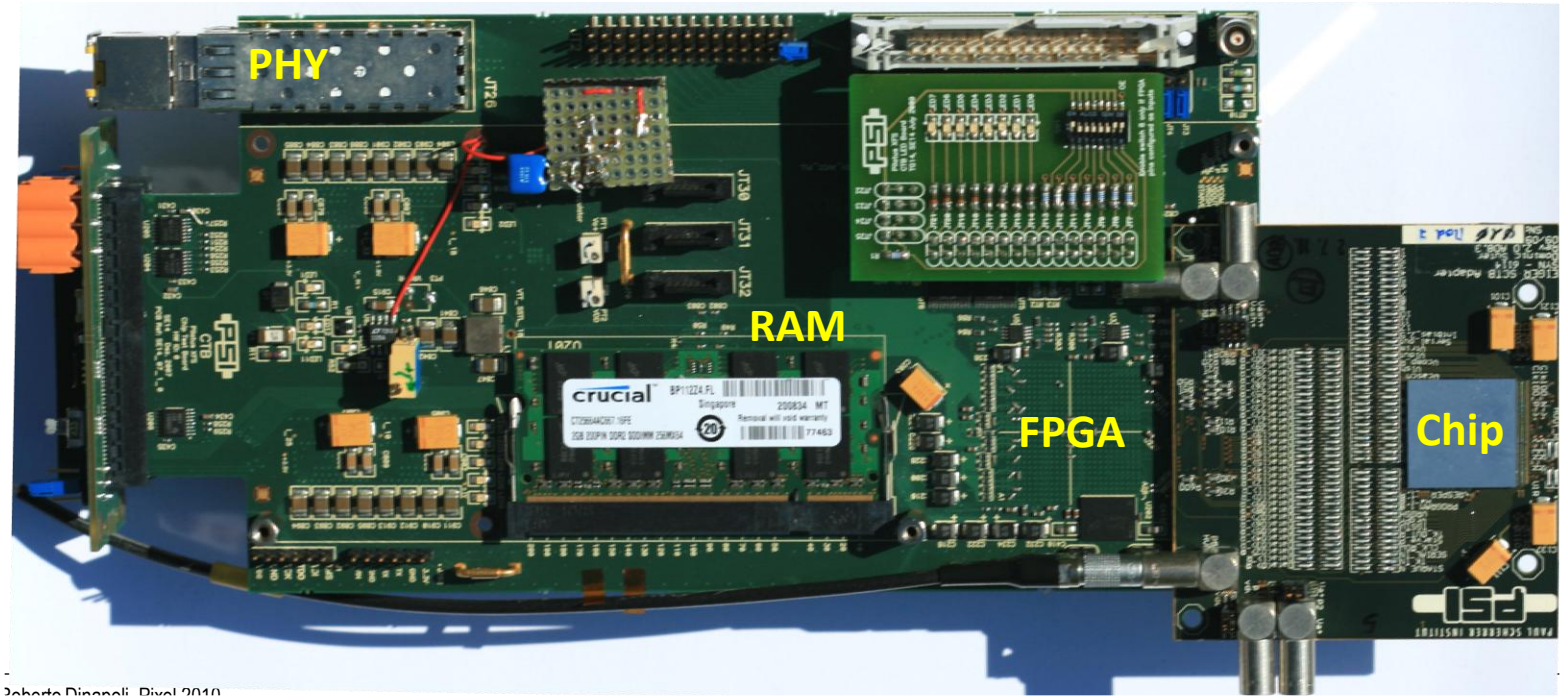


Analysis: Ian Johnson

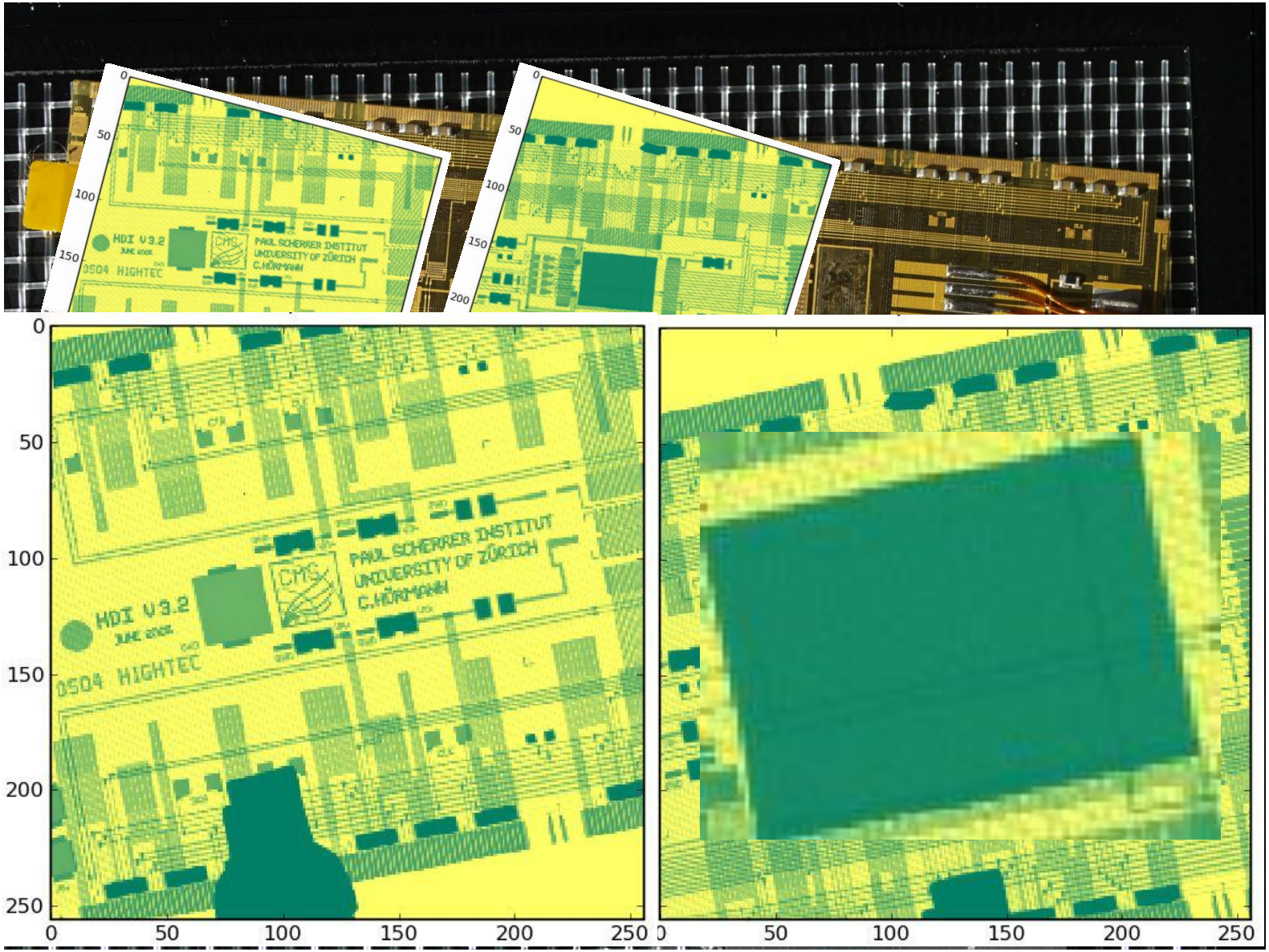
Single chip readout system



Fully functional single chip test system
- DACs n' ADCs
- set/read voltages on the chip
  - Chip control firmware
  - 2GB Local data storage
- Run at full speed 24k frames/s (4 bit mode)
  - Standard UDP communication

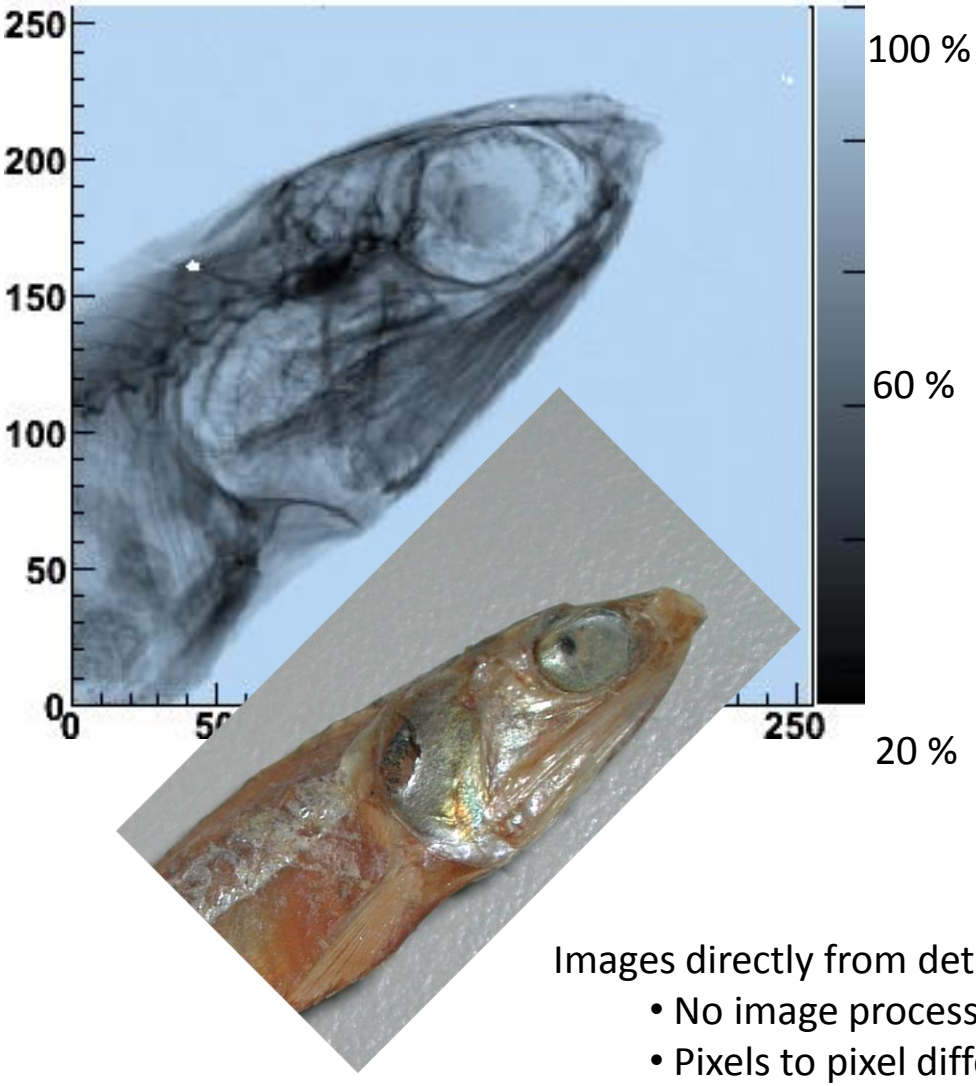


EIGER absorption images



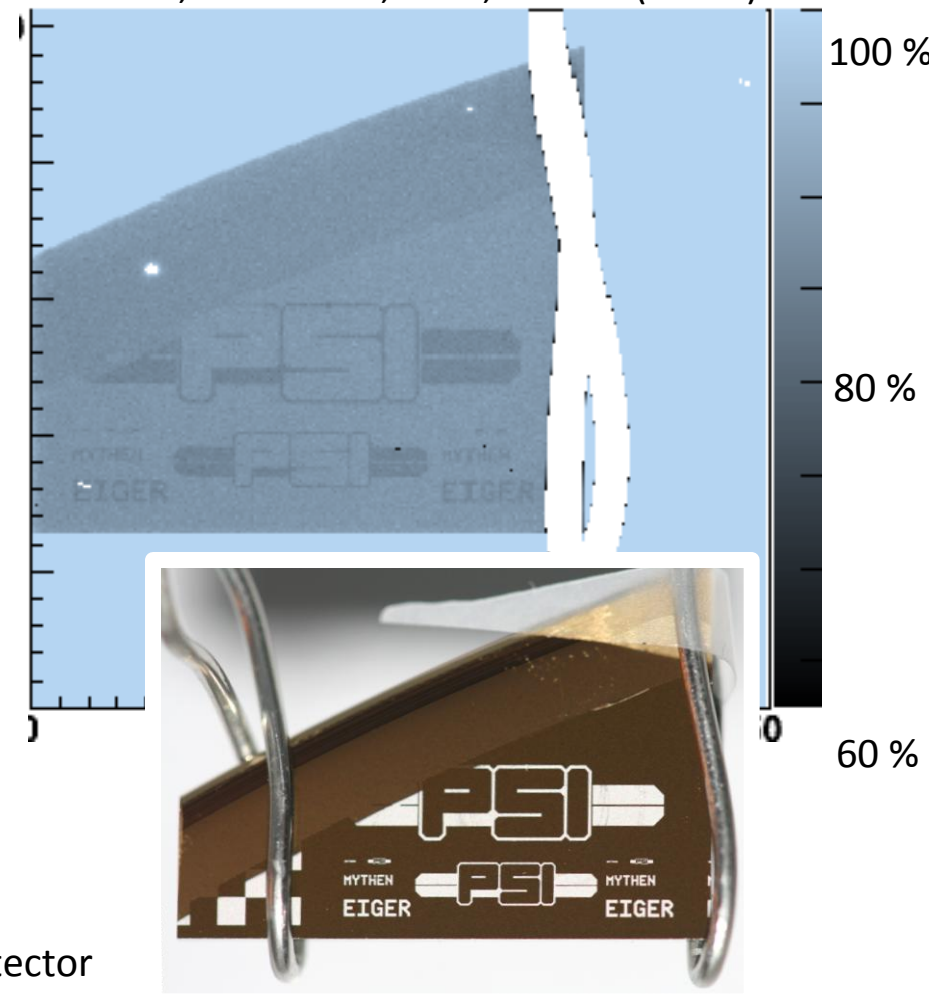
EIGER trimmed absorption images

An Anchovy



Under-bump/Bump Logos:

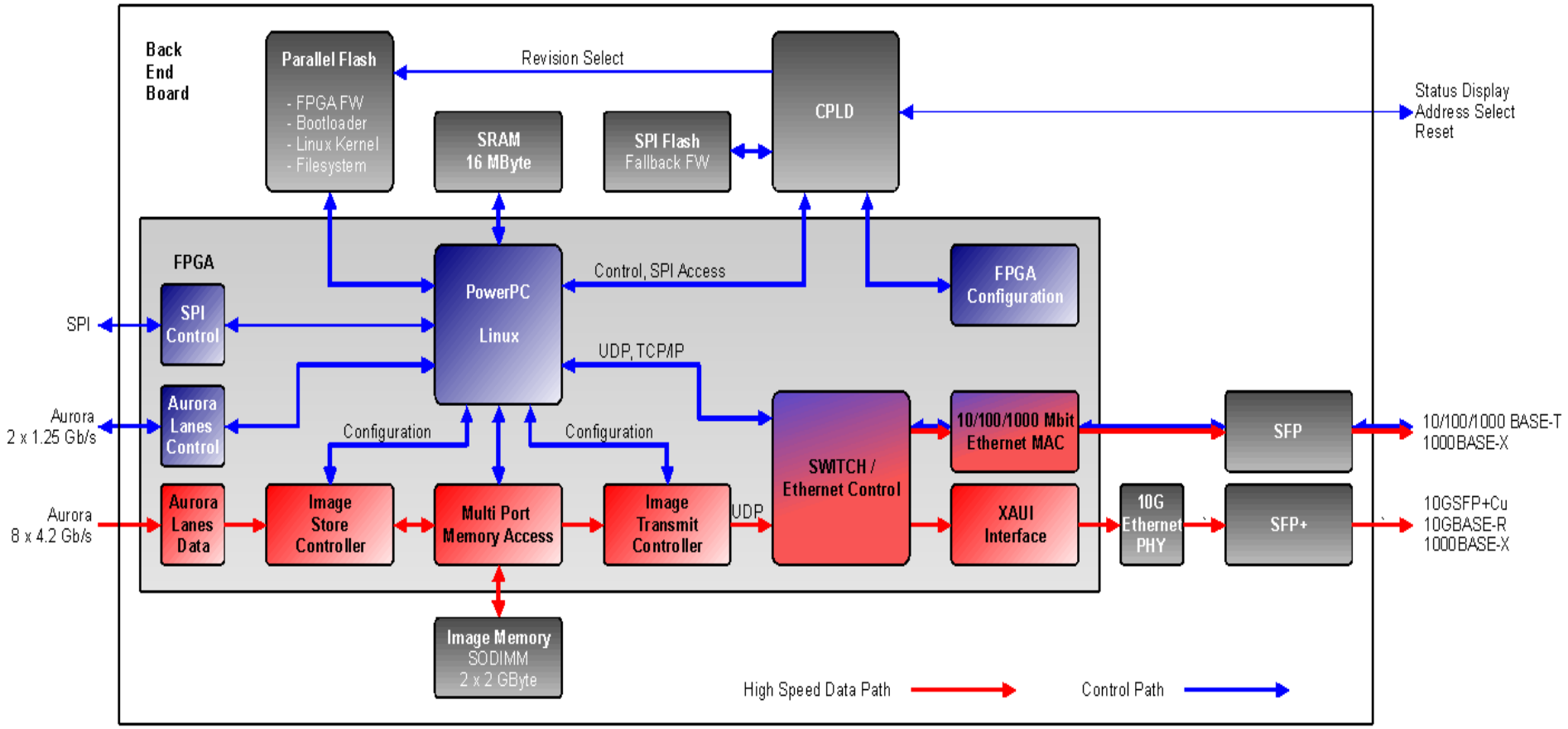
Nickel, Chromium, Gold, Indium (~1um)



Images directly from detector

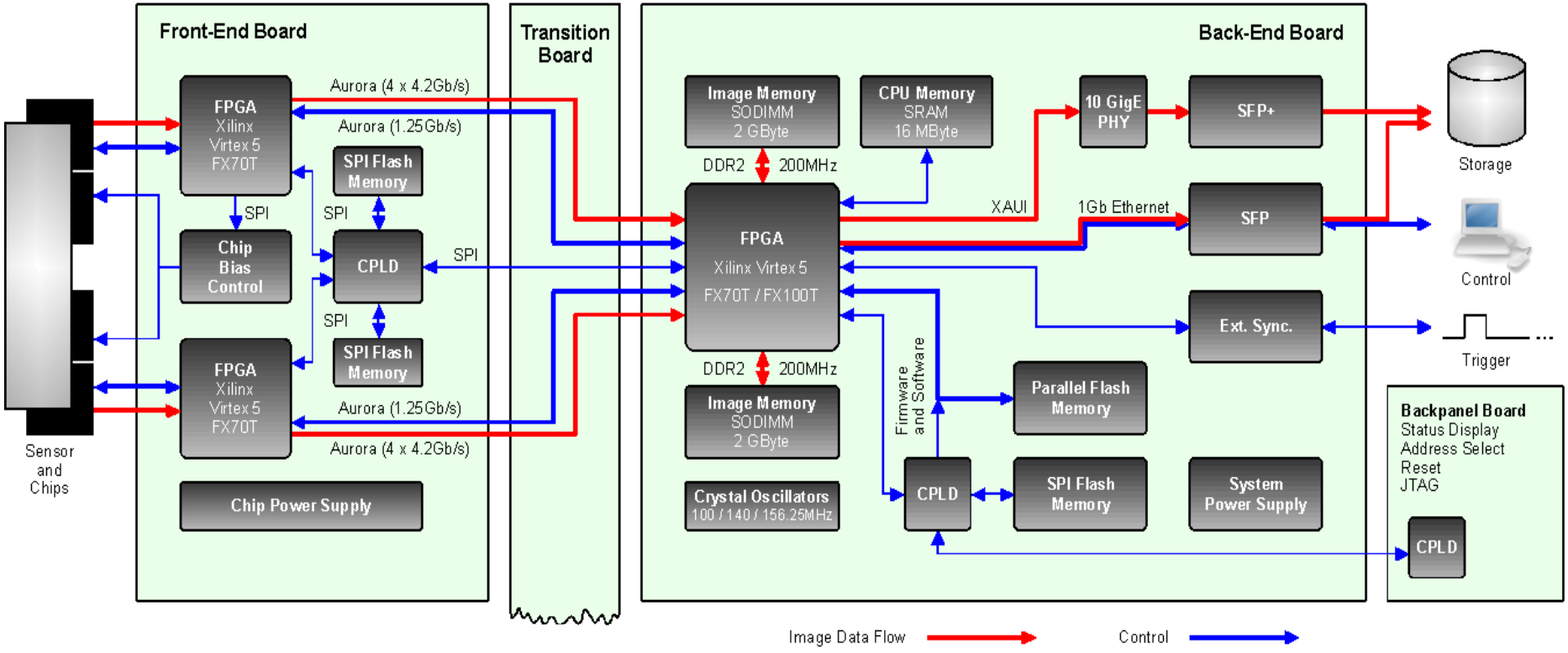
- No image processing
- Pixels to pixel differences corrected by trimming

Back End Board Firmware

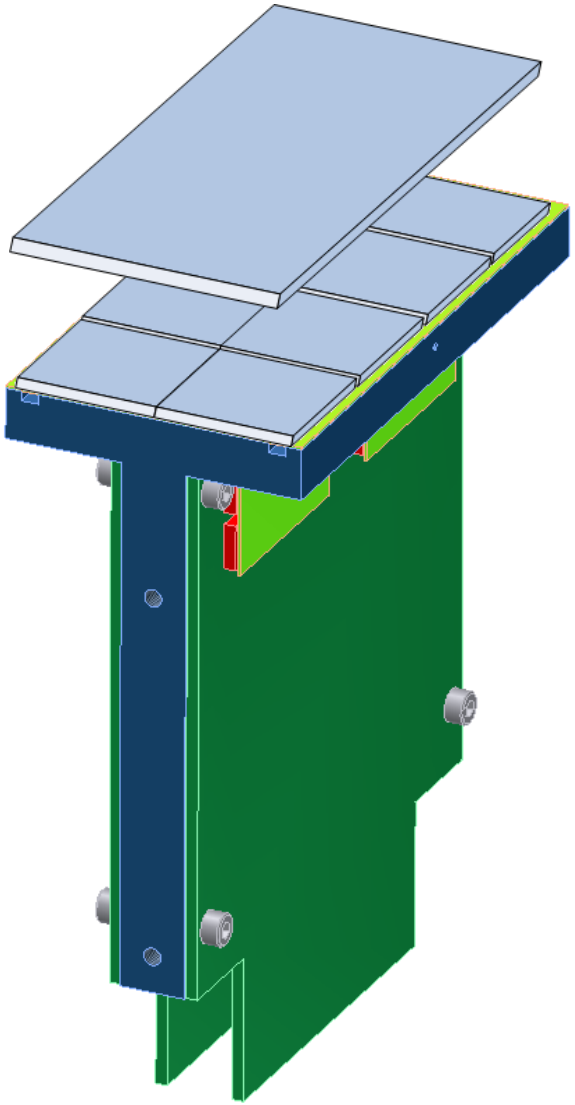


Readout Architecture and Data Volume

Half Module Architecture



EIGER Module

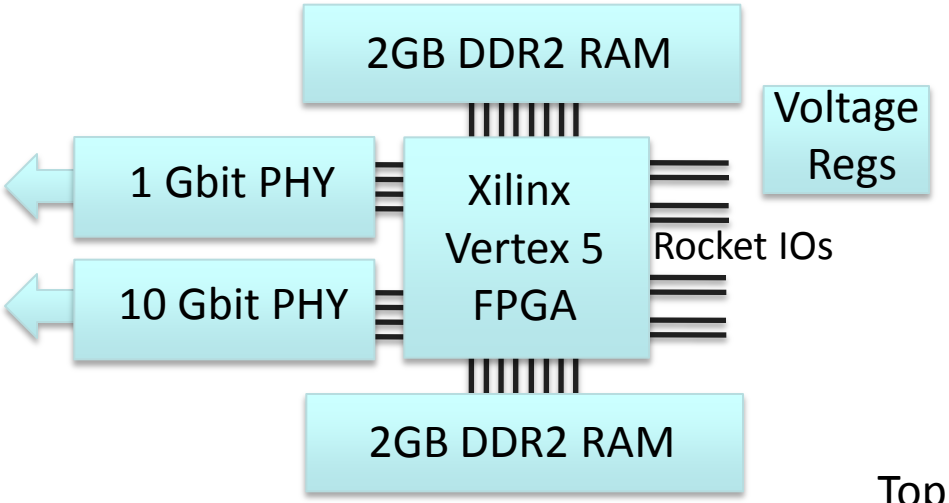


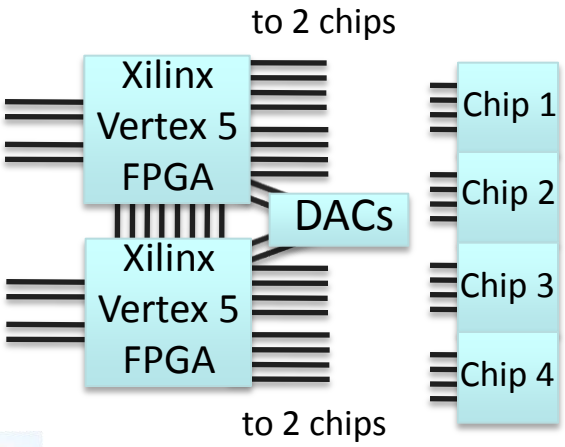
2 x 4 Chips
512 x 1024 (.5 M) Pixels

Almost the same as a PILATUS II module:
39 x 78 mm^2

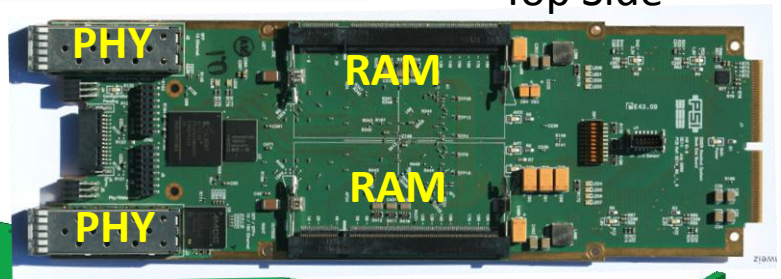
Massive parallel readout on a half module base with current 11.4kHz frame-rate in 8 bit mode
→ 2.78GB/s

Detector Module





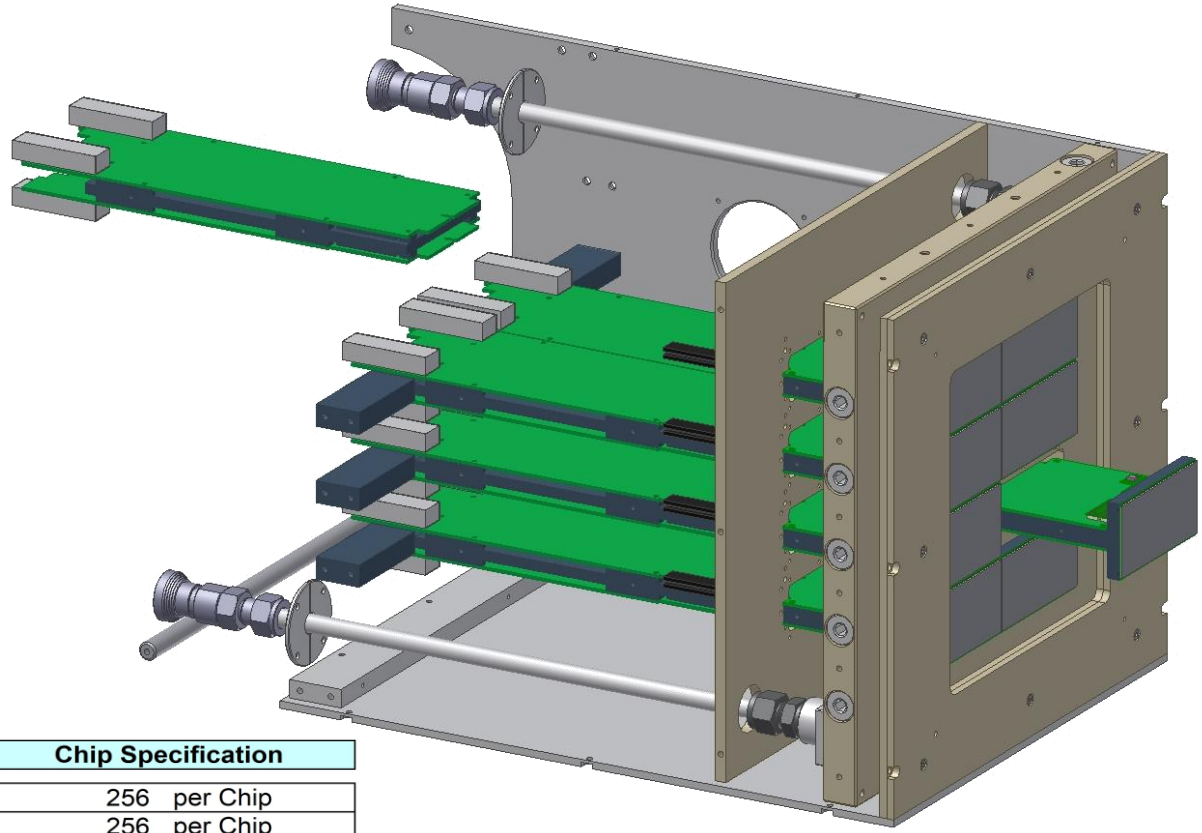
Top Side



Single sensor
8 chip module

Bottom Side

EIGER 4M, four million pixel detector



Chip Specification		
Columns	256	per Chip
Rows	256	per Chip
Bits	8	per Pixel
Framerate	12 000	Hz

[1] 1 Gbit / s = 10^9 bit / s

[2] 1 MByte / s = 1024 * 1024 * 8 bit / s

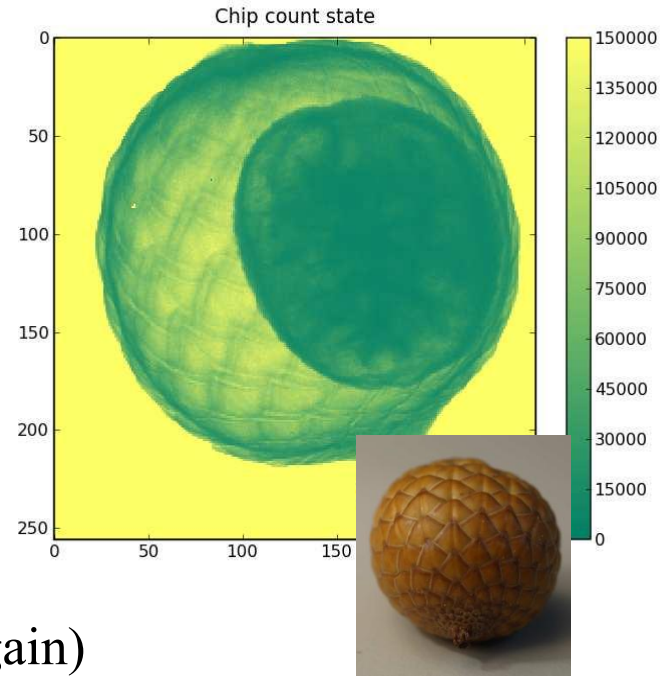
	Detector Specification			Data Size		Data Rate	
	Modules	Chips	Pixel	Bit	Byte	Gbit / s [1]	MByte / s [2]
Chip		1	65 536	524 288	65 536	6.3	750
Half-Module	0.5	4	262 144	2 097 152	262 144	25.2	3 000
Module	1	8	524 288	4 194 304	524 288	50.3	6 000
4M Detector	8	64	4 194 304	33 554 432	4 194 304	402.7	48 000
9M Detector	18	144	9 437 184	75 497 472	9 437 184	906.0	108 000

Conclusions and future work

•We are developing EIGER, a high frame rate, large area pixel detector which targets mainly synchrotron based (diffractive) experiments.

•The readout chip implements several big improvements with respect to PILATUS: much smaller pixels, extremely high frame rates, almost dead time free readout.

- Single chip assemblies show promising results:
  - High bump bond yield between the sensor and chip
  - The Eiger chip is operational
    - First x-ray images
    - Achieved a 24 kHz frame rate in 4 bit mode
    - Trimmed in high gain mode:
    - Noise sigma -> ~650 eV or 180 e^-
    - Minimum threshold ~4.5 keV
    - Inflection point dispersion of ~70 eV (sigma)
    - First trimmed images



- We are working toward multi-chip modules
  - All readout electronics working (preliminary)
  - High density interconnect board is in production (again)
  - We have mechanical prototypes
  - We should have the first modules by the end of this year

- Larger detector systems (possibly up to 18 Mpixel) are planned