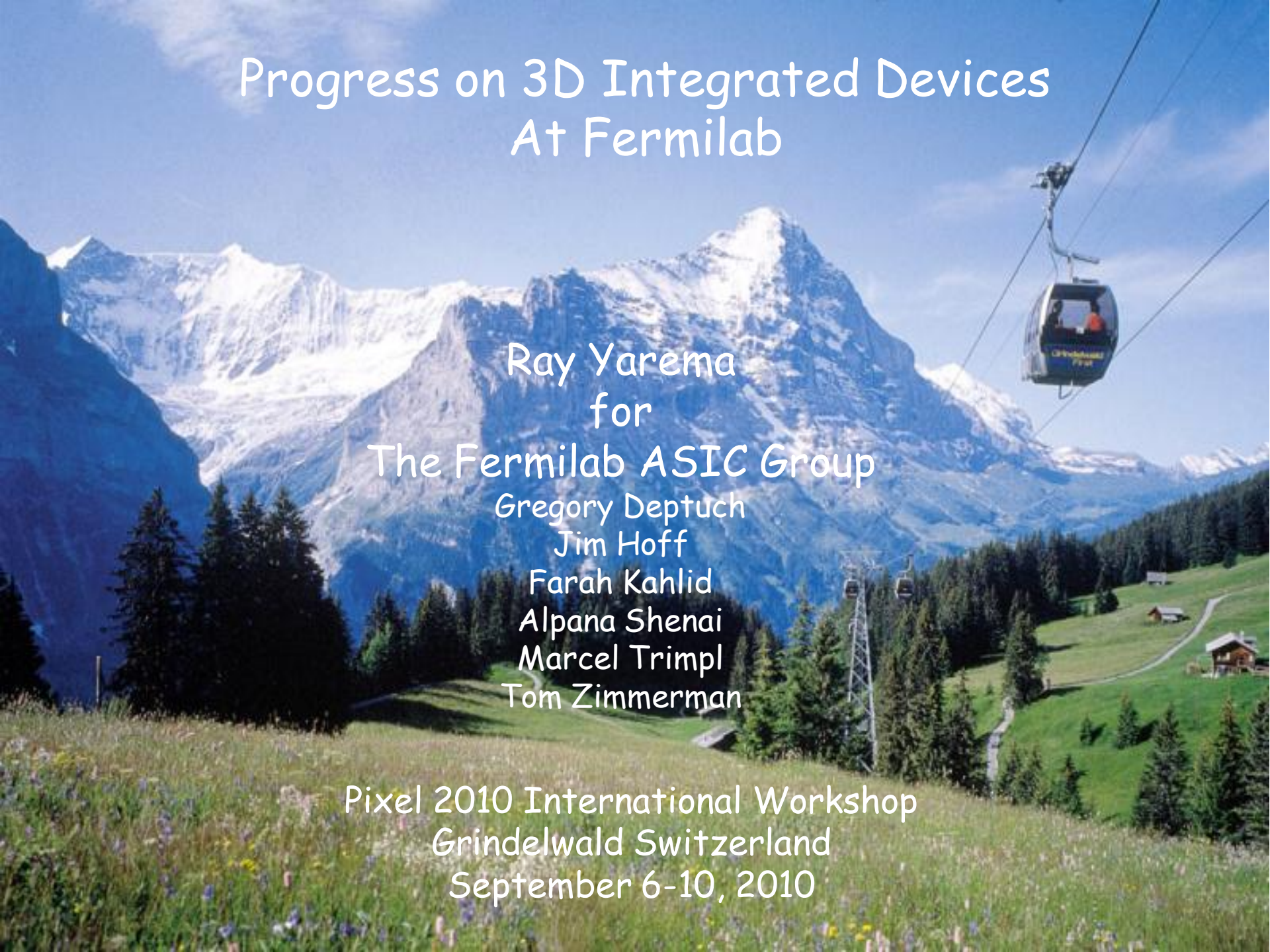
Progress on 3D Integrated Devices At Fermilab



Ray Yarema
for
The Fermilab ASIC Group
Gregory Deptuch
Jim Hoff
Farah Kahlid
Alpana Shenai
Marcel Trimpl
Tom Zimmerman

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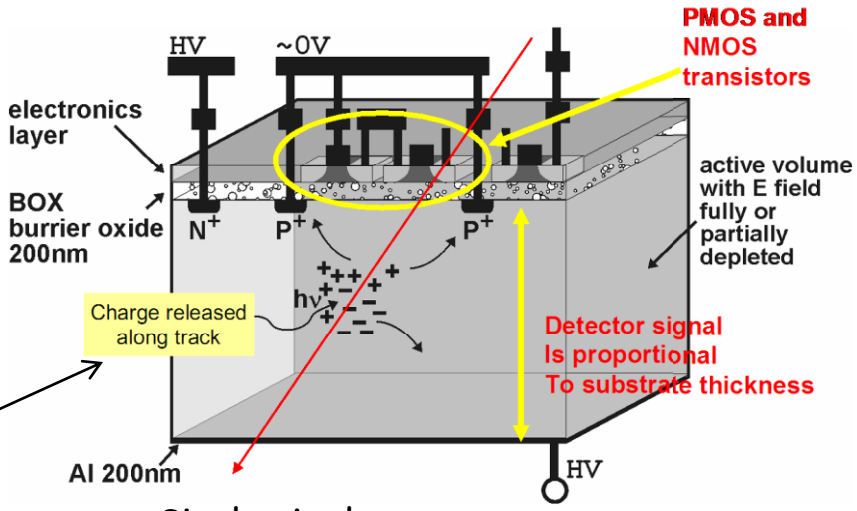
Introduction

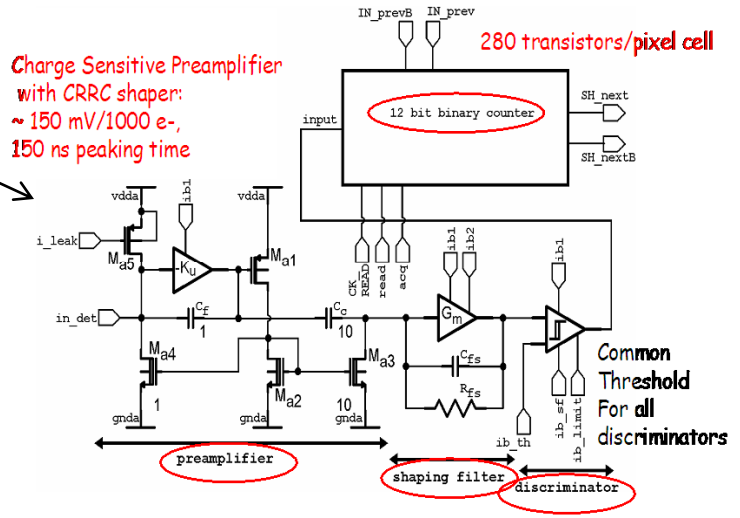
- Work has been continuing for several years at Fermilab on 3D integrated circuit development and SOI MAPS. SOI MAPS can be considered to be similar to 3DICs in that they use short vias to connect between different layers.
- By working with several different vendors we have found that progress is generally slow and each has its' own challenges. I will try to convey our experiences.
- This talk will also provide some background material to place the recent work and status in perspective.
- Three different areas will be covered.
  - Progress in SOI 3D and MAPS with OKI
  - Progress in MIT LL 3D chip development
  - Progress in Tezzaron 3D chip development

Progress at OKI with SOI MAPS

- Several versions of a Monolithic Active Pixel Matrix device with Binary Counters (MAMBO) capable of counting individual radiation events up to 1 MHz per pixel have been designed in OKI SOI processes. [1]
- The process used is a fully depleted SOI process where vias are formed through the BOX and implants at the bottom of the vias form sensing diodes in a detector grade silicon substrate.
- Basic pixel cell is comprised of CSA, shaper, discriminator, and reconfigurable 12 bit binary counter for counting and readout.
- Advantages include full CMOS processing when compared to some MAPS devices
- Applications include direct electron detection and soft X-ray imaging.
- From the start some inherent problems were recognized and the design has been continually modified to improve performance



Single pixel sensor

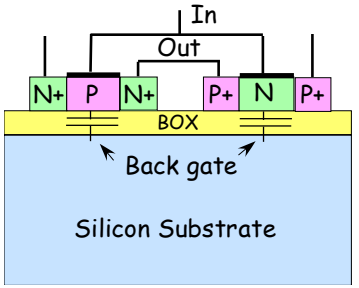


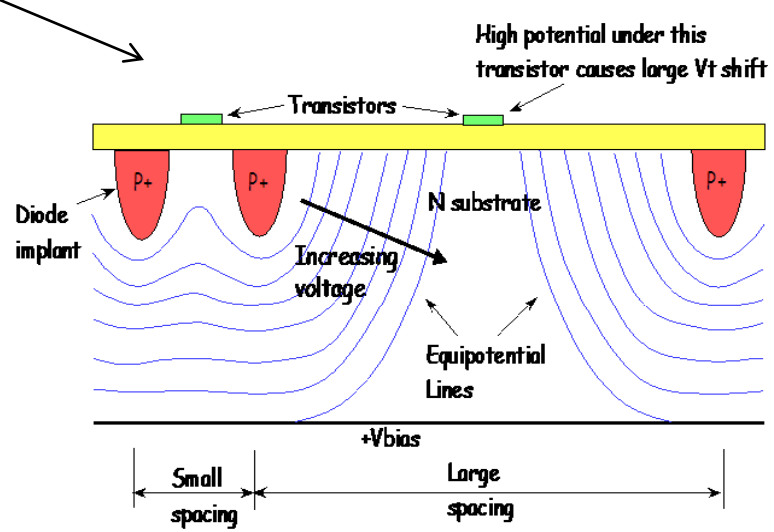
Single Pixel Schematic from MAMBO

MAMBO 1 & 2

- MAMBO1 was a 64 x 64 array of 26 um pixels with 4 parallel sensor diodes/pixel to attempt to reduce the back gate effect caused by applying voltage to the substrate. [2]
- Some problems with MAMBO 1 were improved in MAMBO2 by moving to a process with better transistor characteristics, improved counter design, better equalization of potential under BOX by close spacing of sensor diodes.
- The problem of charge injection from the CMOS circuitry through the BOX into the substrate, however, was still present.

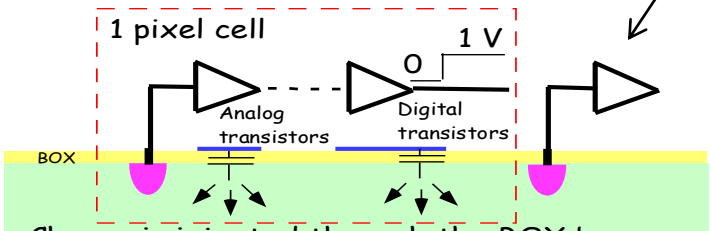
The BOX acts as a back gate for the NMOS and PMOS transistors





To reduce voltage under the transistors, keep P+ implants close together.

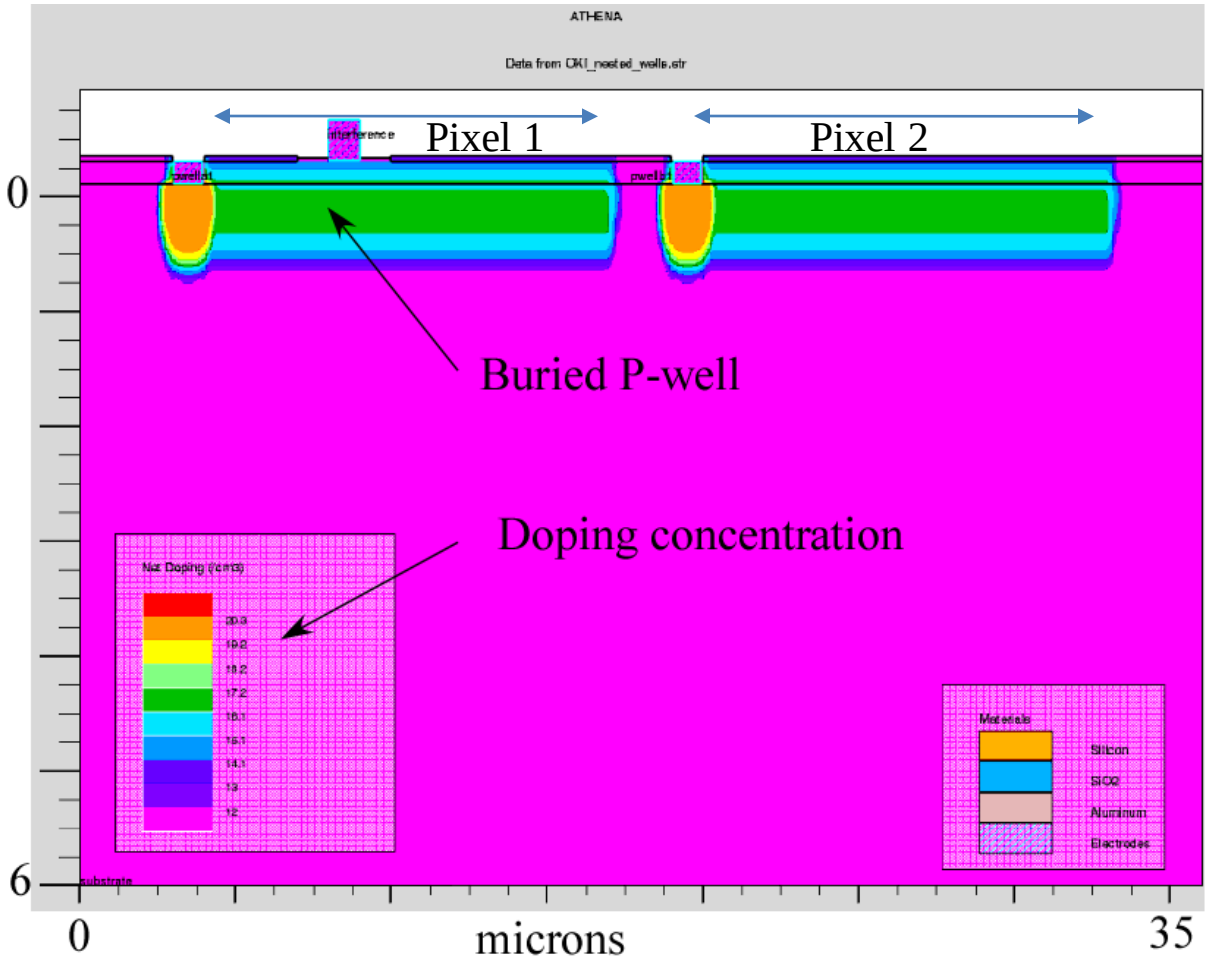
The distribution of the diode contacts affects the back gate potential which changes transistor Vt



Charge is injected through the BOX by transistors or metal traces on or near the top of the BOX. The charge is collected by the offending pixel, neighbor pixels, and the backside contact. 1 um x 1 um of material on top of a 200 nm BOX with a 1 v swing injects 1035 electrons into the substrate. The amount collected by a P+ implant is dependent on the location of the injection point.

MAMBO 3

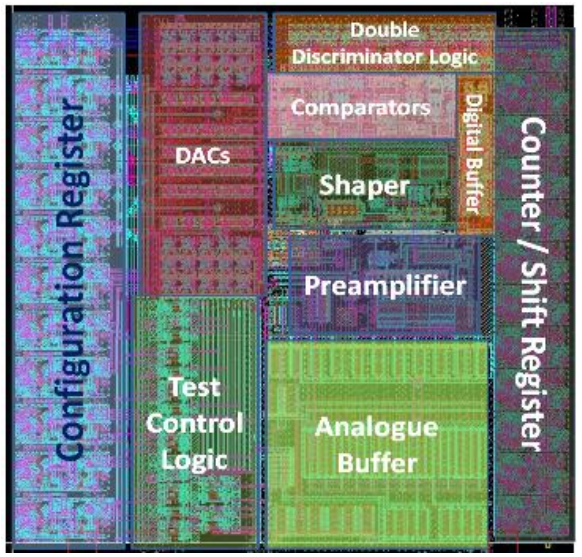
- After evaluating various designs from the MAMBO2 run, it was decided to add a buried P-well to the next process run to completely eliminate the back gate effect and to provide better shape of E-field in the detector region.
- Although this would be useful for peripheral circuits, the BPW would not help the charge injection problem associated with the MAMBO designs.



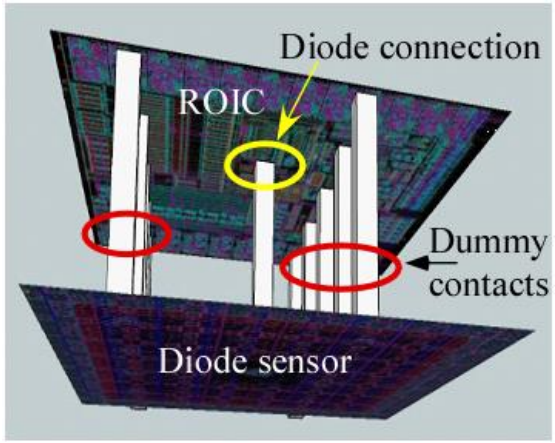
Buried P-well concept for back gate control

MAMBO 3

- MAMBO 3 was therefore designed as a two separate chips (ROIC and sensor in the same SOI process) which would then be 3D bonded together using the T-micro chip to chip assembly process.
- MAMBO3 is 44 x 44 array of 100 um pixels [3]
  - Design expanded to include two discriminators to form window comparator
  - each pixel has ~950 transistors
  - introduced trimming capabilities for leveling out offsets
  - Lowered overall gain of circuit
  - Circuitry for individual pixel testing added.



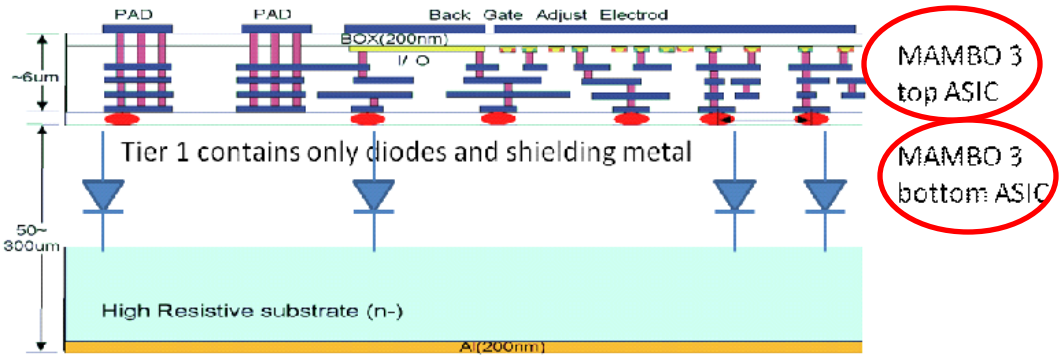
Single pixel electronics layout

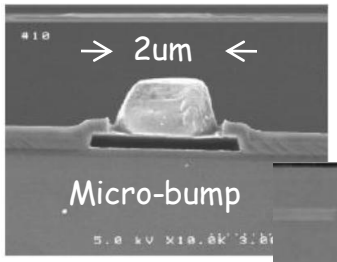


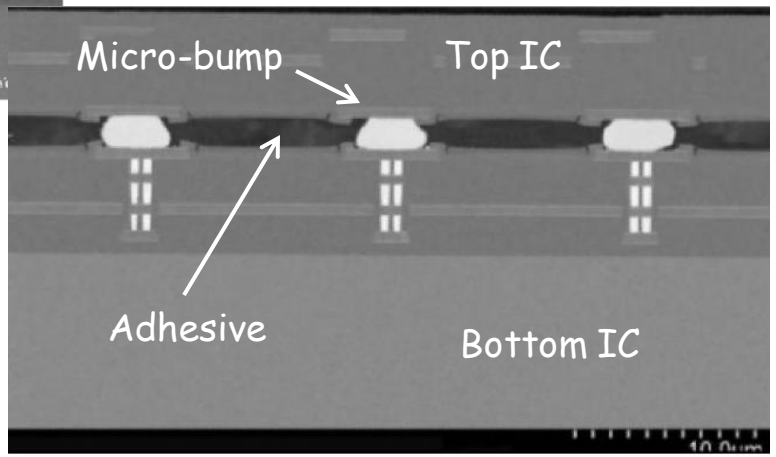
3D assembly for MAMBO3

MAMBO 3

- Goals
  - **Explore 3D assembly techniques with T-micro**
  - Diodes of same size as pixel to obtain uniform field in the active sensor volume and avoid potential pockets by using BPW.
  - Add shielding on detector layer to minimize charge injection
  - Possibility of changing gated diode voltage to improve diode separation
- T-micro assembly [4]
  - Small Au-In contacts used to make electrical connections and add mechanical strength to form a temporary face to face bond.
  - Permanent bond made by injection of adhesive between parts (wafer to wafer or die to die)
  - Thin ROIC to 6 um and add back metal pads and metal shield.
- MAMBO 3 due back mid October

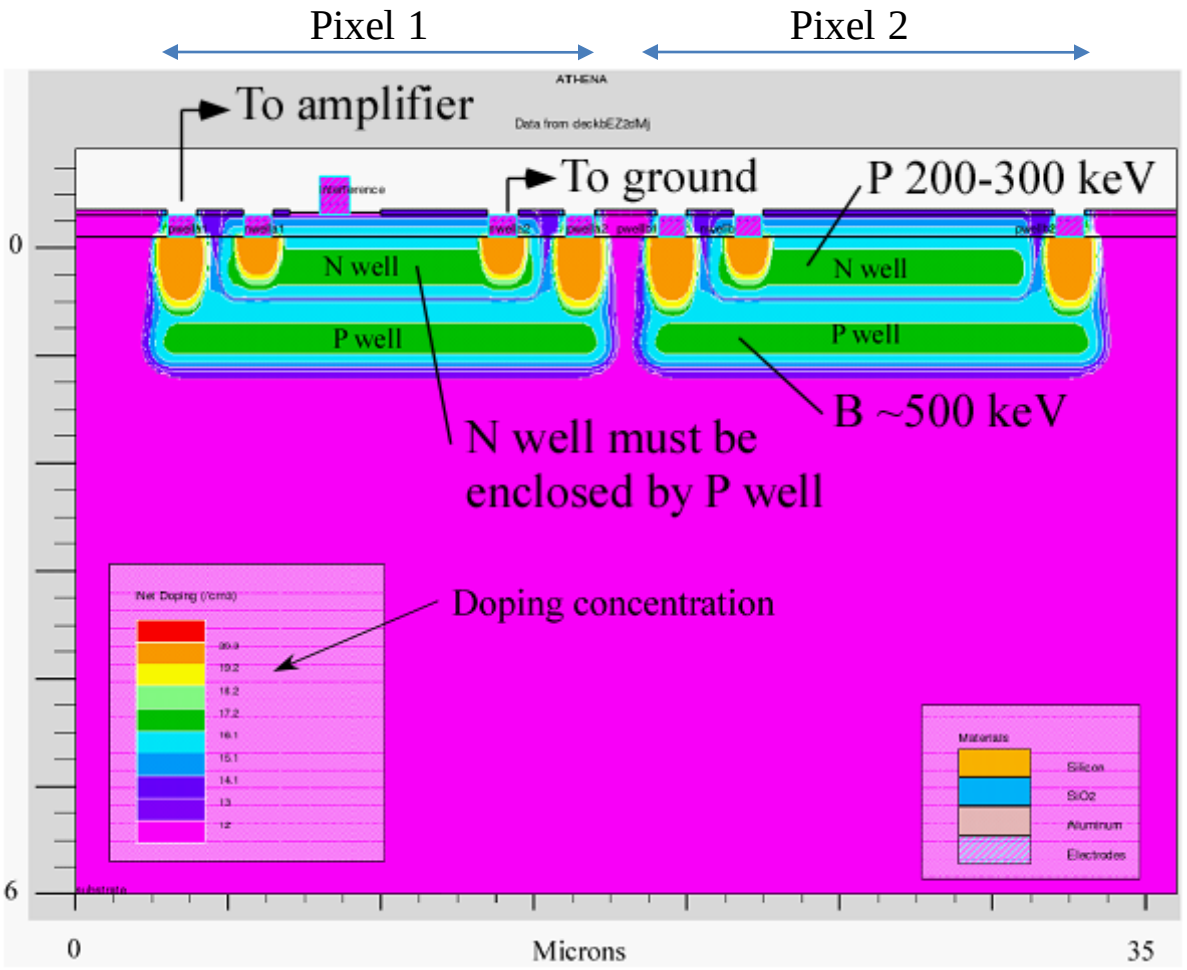






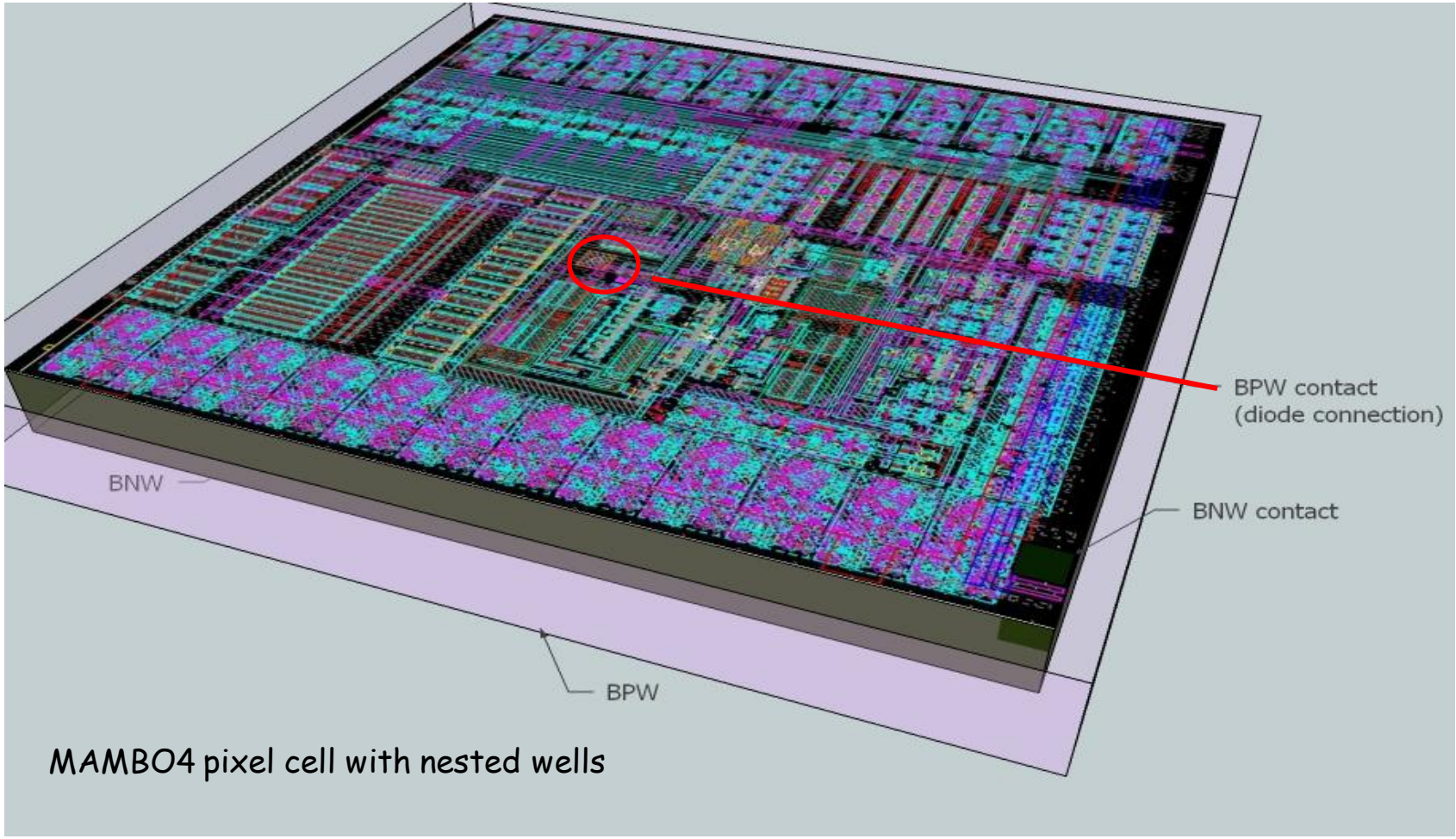
MAMBO 4

- Fermilab postulated some process enhancements and has worked closely with the OKI foundry to find optimal conditions for implementing nested wells into the OKI process
- Fermilab converted the MAMBO 3 design back into a single chip SOI design (MAMBO4)
- MAMBO4 – 41 x 42 pixel array
  - Addition of the nested wells should completely remove any coupling from the CMOS circuitry into the diodes in the substrate
  - Current pixel cell with added individual pixel testing capability is 105 x 105 um
    - Pixel size easily reduced to 75 x 75 um and 1 pf capacitance by removing individual pixel testing
  - The preamplifier and shaper designs had to be modified to accommodate a larger input capacitance.
- Chip is in fabrication



Silvaco simulation of nested wells

MAMBO4

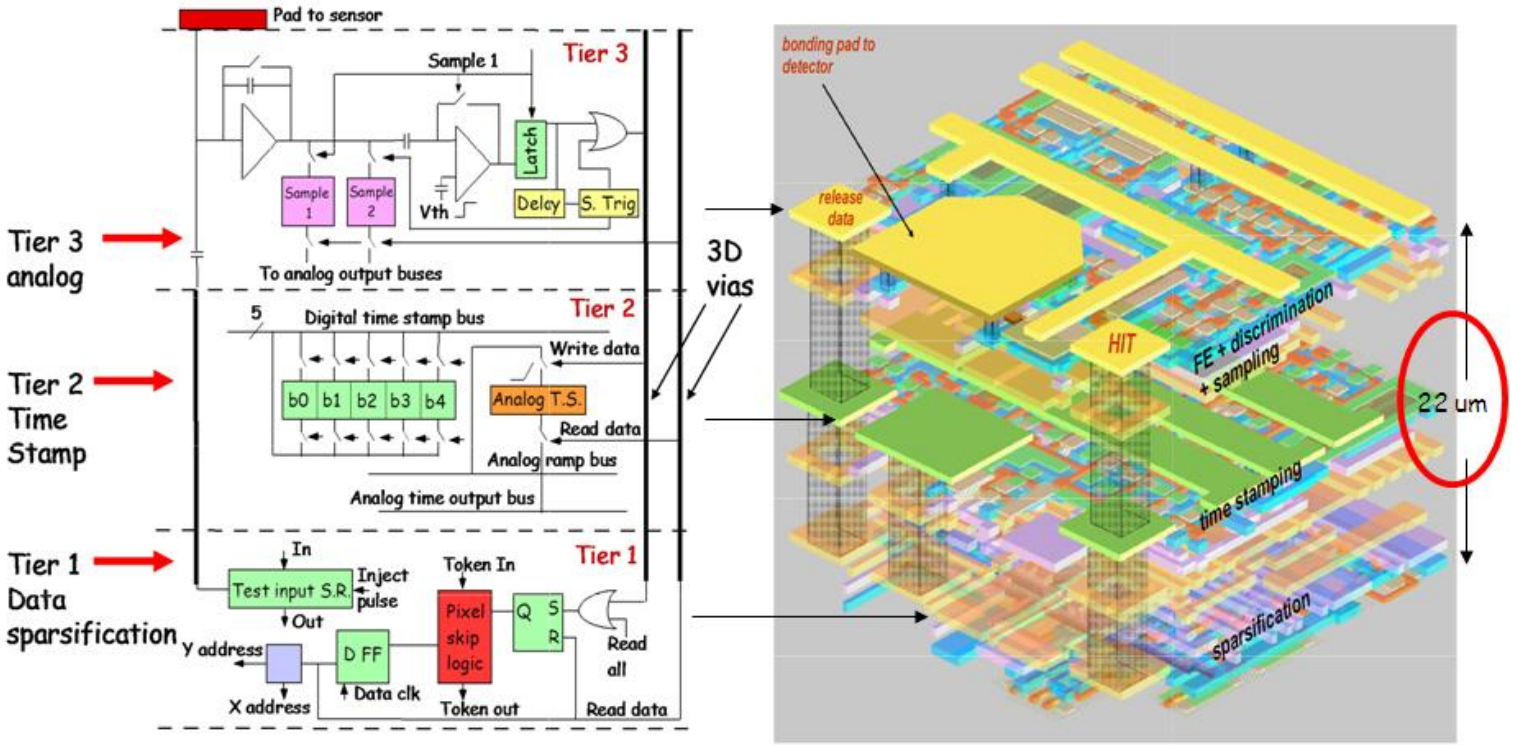


MAMBO4 pixel cell with nested wells

VIP1

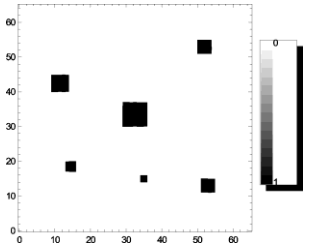
- The VIP1 chip is a demonstrator 3D ROIC for the ILC Vertex Detector. [5]
  - Designed in 2006 for MIT LL SOI process
  - Received and tested in 2008
  - Has 3 tiers
  - Sensor to be bonded separately
  - 180 nm process

- Features
  - Readout between ILC bunch trains
  - High speed data sparsification included
  - Analog output available
  - Digital (5 bit) and analog time stamping
  - Test input for every pixel
  - 4096 array with 20 um pixels

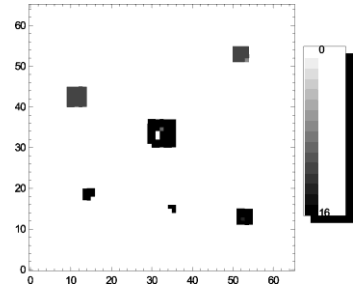


VIP1 Test Results and Problems

- The functionality of the chip was established:
  - Threshold scan
  - Input test charge scan
  - Propagation of the readout token scan
  - Data sparsification works
  - Measured fixed pattern and temporal noise
- No apparent problems with 3D vias
- Very poor yield with chips from two runs (2/20)
  - Much tuning required, only 1 fully functional.
  - Processing far from transistor models
  - High leakage currents affecting various circuits
  - Poor current mirrors
  - High leakage hurt performance of dynamic FFs
  - Possible trace opens and short
  - Transistor characteristics (Vt) changed after bonding

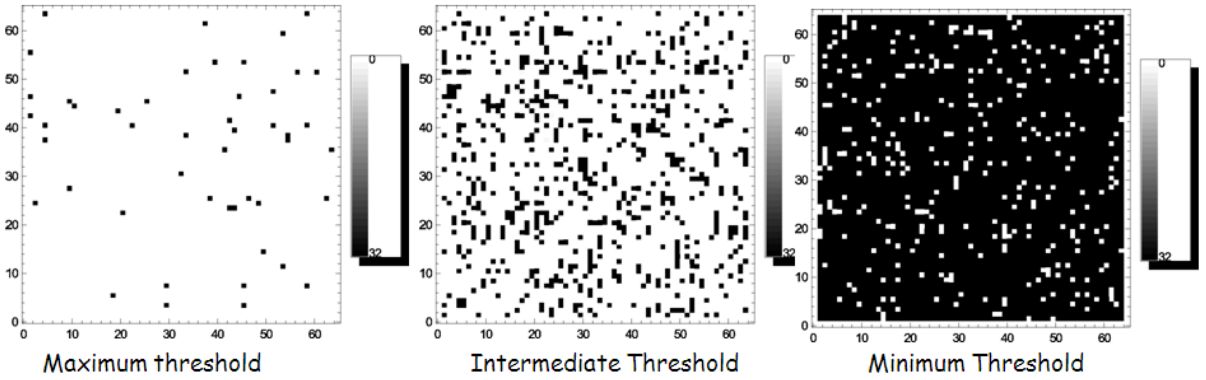


Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal



Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition – 8 times injection)

Data readout out using data sparsification scheme.

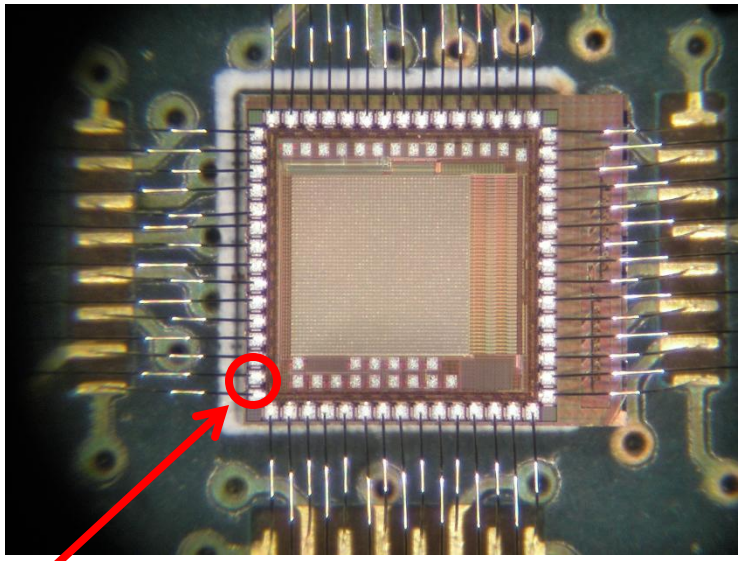


Note:
Same signal injected into all pixels

VIP2a

- Goals
  - **Improve performance**
  - **Improve yield**
  - No big architecture changes to allow for accurate performance comparison
- Timeline
  - Submitted Oct 2008
  - Received August 2010
- VIP2a features (150 nm)
  - Different power and grounding scheme (tied between tiers in pixels)
  - Redundant vias (Not TSVs)
  - Wider traces and trace spacing (x1.2)
  - Increased transistor sizes (Wmin*2, Lmin*3)
  - 48 x 48 array of 28 x 28 um pixels
  - Seven bit digital time stamp instead of 5
  - Redesigned current mirrors (use all separate devices instead of inter-digitated devices)
  - Removed dynamic logic due to leakage problems
  - Increased pull up strength on address lines to correct for possible leakage problems (selectable strenght)
  - Added diagnostics
  - Changed charge injection scheme

- Known processing problems
  - Processing problems occurred on each of the 3 tiers requiring several back up lots to be processed (Note not a production line)
  - tier3 to tier2 alignment exceeded our target value by 0.5um (VIP2a 3Dvia landing pads on tier2 (T2_BM1) were increased from 2.5 to 3.0um)
  - Tiers separated at bond pads on some chips during wire bonding

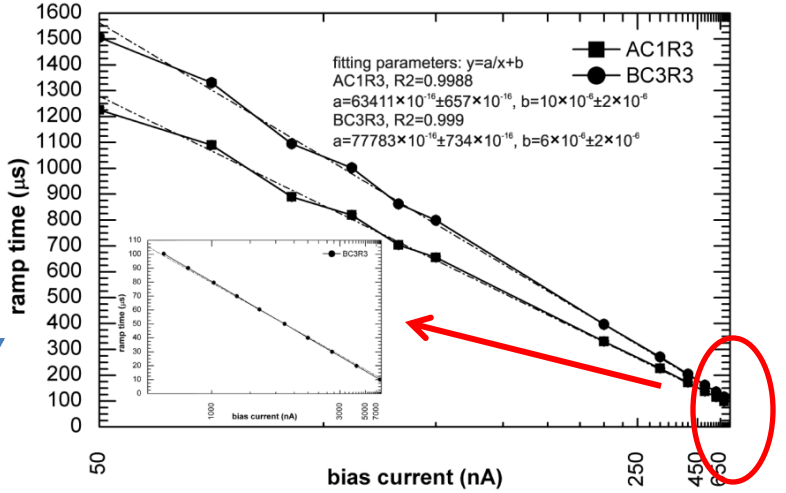


VIP2a

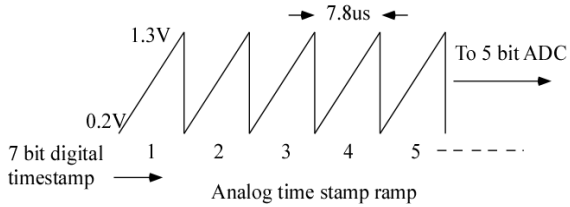
Lifting of two pads on two chips

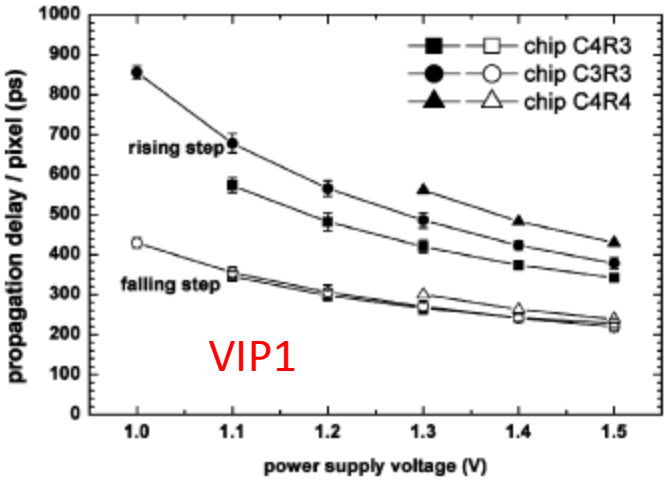
VIP2a

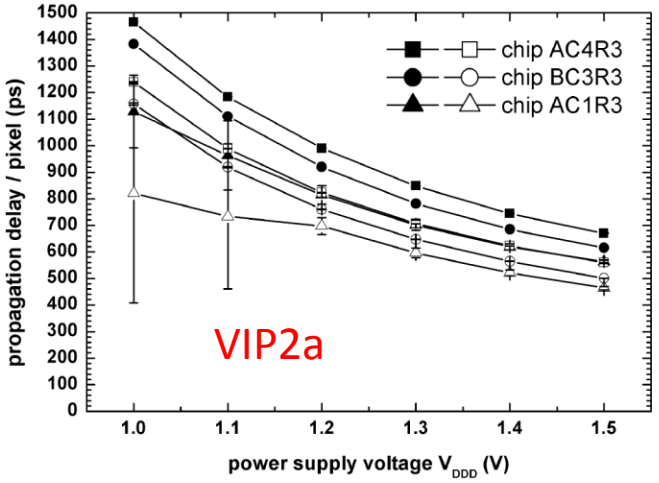
- After 1 week of testing it is noted that the yield and performance are significantly improved in VIP2a.
  - In VIP1 the analog time stamp did not work due to high leakage currents
  - The analog time stamp, based on a voltage ramp and S&H, works well in VIP2a
    - Excellent linearity (no droop) from 10 us to 1 ms
    - Can be used in conjunction with digital time stamp to achieve equivalent 12 bit time resolution (less than 1 usec in 1 msec)
  - Sparsification token propagation works over wider voltage range and on many more chips than on VIP1
  - Token propagation time is higher in VIP2a due to larger transistor sizes
  - Sparsification test mode works
  - Found protection diodes no longer leak



12 bit Time stamping



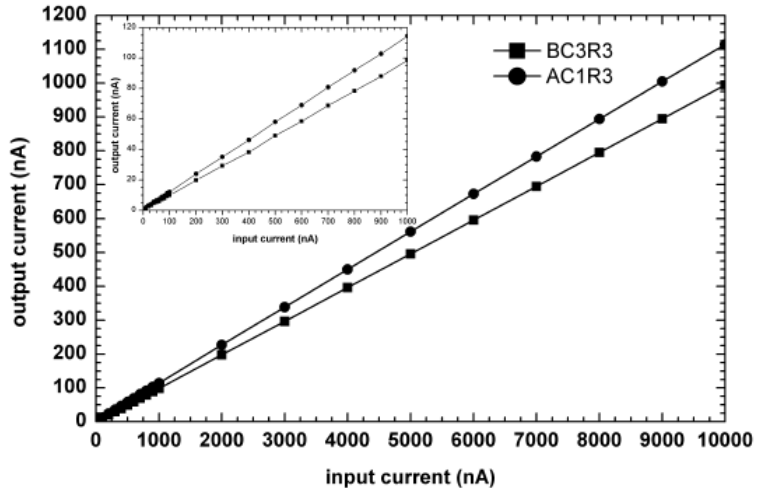




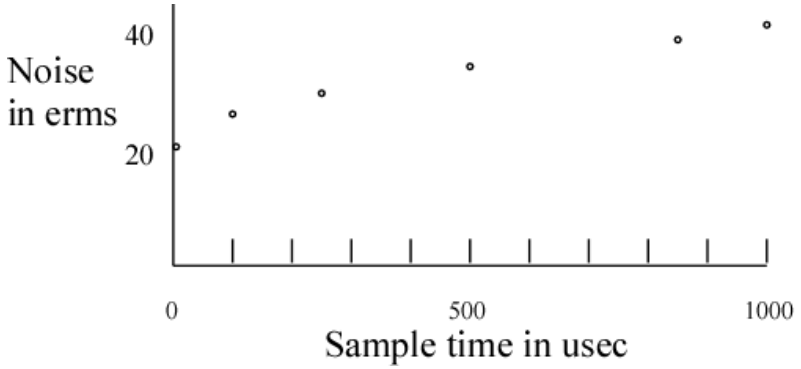
Token propagation delay per pixel for different chips at different power supply voltages

VIP2a

- Current Mirrors
  - VIP1 current mirrors on a chip and from chip to chip varied widely (nonlinear and incorrect current ratios)
  - VIP2a current mirrors are well matched – may be due to improved layout techniques
- Single pixel noise measurement
  - Comprised of amplifier noise and S/H noise in quadrature
  - 20erms @ 20 fF input capacitance (DCS with differential analog output, 1 us sample time, Tr=120 ns, Ib=0.5uA, Cs=100fF)
  - Noise @ max sample time ~ 40 e
  - Ideal S/N for 50 um detector = 50x80/40 = 100/1
  - Gain ~ 200 mV/fC
  - Noise from pixel array operation TBD.

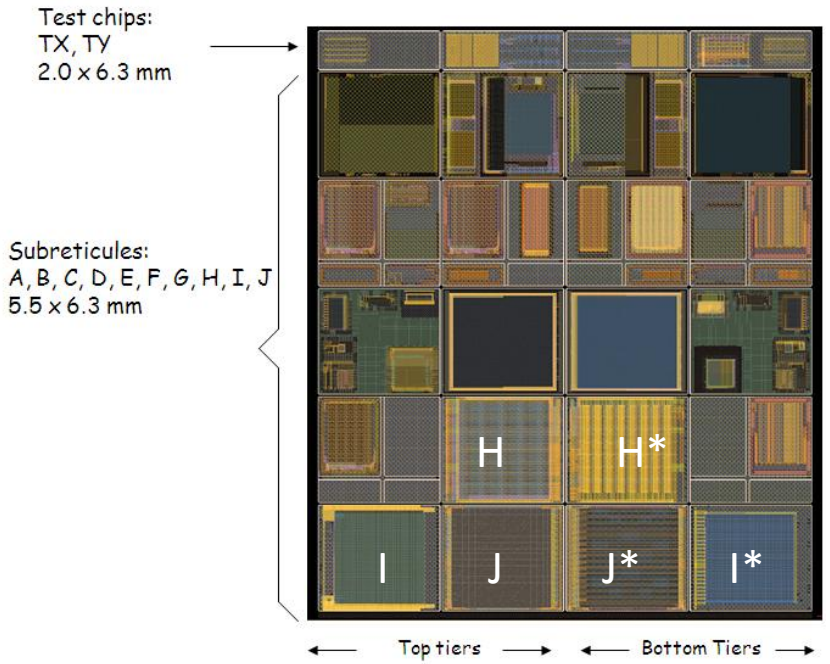


Current mirrors on 2 chips with good matching



Tezzaron/Chartered Chips

- Consortium established in late 2008 with
  - 15 members
  - 5 countries
  - Others have joined
- Initial designs for MPW run completed in May 2009
  - 2 tier 3D chip
  - Single mask set
  - Chartered 130 nm CMOS
- Numerous problems were encountered with designs, software tools at Tezzaron, shifting Chartered requirements, etc.
- MPW frame accepted by Chartered in March 2010
- Waiting for chips
- Delay appears related to Global/Chartered decision to move some equipment from prototype line, where 3D wafers are done, to the production line due to increase production demands.
- Fermilab chips H, I, J
- Plans for next MWP run are in the works



H, H* - VICTR, used as a demonstrator for implementation of PT cut algorithm for track trigger in SCMS
I,I* - VIP2b, demonstrator chip for ILC vertex detector
J,J* - VIPIC demonstrator chip for X-ray Photon Correlation Spectroscopy

Future Outlook for Tezzaron/Chartered

- In June 2010, CMP/CMC/MOSIS partnered to offer a 3D-IC process
  - Based on Tezzaron Supercontact technology and Chartered/Global Foundries 130 nm CMOS process
  - 2 tier face to face bonded wafers
  - Top tier is thinned to expose TSVs and backside metal added for wire bonding
  - A design kit supporting 3D-IC design with standard cells and I/O libraries produced by CMP.
- Recent Developments for Future Runs
  - Chartered to stop TSVs on 8 inch 0.13 CMOS wafers for the foreseeable future
  - Chartered agrees to process wafers from FEOL through M4
  - Tezzaron will have SVTC add TSVs from M4 down into the substrate and complete the BEOL processing including the bond interface metalization
  - Implication is that space will need to be left open on M1-M4 for the vias to pass through.
  - Future potential benefit will be that wafers from other foundries can use the Tezzaron 3D process.

Summary

- Two different chips are currently in fabrication at OKI. MAMBO 3 will used primarily to evaluate the T-Micro 3D assembly process. The MAMBO 4 device will be used to evaluate a new nested well option.
- The second 3 tier device (VIP2a) from MIT LL has been delivered. Yield and performance have been improved from VIP1. Good results thus far. Further tests are continuing.
- A MPW run from the 3DIC Consortium is in process at Chartered. Commercial vendors have partnered to offer 3D runs using the Tezzaron process.
- Changes continue in the world of 3D electronics. Process improvements are being made. Although we have had some successes there is still much to learn as this field begins to mature.

References

- [1] G. Deptuch, Ray Yarema, *Monolithic Active Pixel Matrix with Binary Counters in an SOI Process*, 2007 International Image Sensor Workshop, Ogunquit, Maine June 7-10, 2007, pp. 98-101.
- [2] R. Yarema, G. Deptuch, *3D and SOI Integrated Circuit Design at Fermilab for HEP and Related Applications*, 2008 NSLS/CFN Users Meeting, Workshop on Detectors, Brookhaven National Laboratory, May 2008.
- [3] Farah Khalid, et. al., *Monolithic Active Pixel Matrix with Binary counters (MAMBO III) ASIC*, Submitted to Proceedings of Science August 2010.
- [4] Makoto Motoyoshi, *SOI Pixel Detector with Micro-bumps*, 2010 Workshop on Vertically Integrated Pixel Sensors, Pavia, Italy, April 2010
- [5] G. Deptuch, et. al., *A Vertically Integrated Pixel readout Device for the Vertex Detector at the International Linear Collider*, IEEE Trans. on Nuclear Science Vol. 57, No. 2, April 2010