



COST-EFFECTIVE FLIP CHIP ASSEMBLY AND INTERCONNECTION TECHNOLOGIES FOR LARGE AREA PIXEL SENSOR APPLICATIONS

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PIXEL 2010 Grindelwald, Switzerland
5th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging,
September 6–10, 2010

Outline

COST-EFFECTIVE FLIP CHIP ASSEMBLY AND INTERCONNECTION TECHNOLOGIES FOR LARGE AREA PIXELSENSOR APPLICATIONS

- Overview Hybridization Technologies
- Low Cost Bump Deposition – Solder Paste Printing in Dry Film Resist
- Chip2Wafer Assembly using Temporary Carrier System
- Summary and Outlook

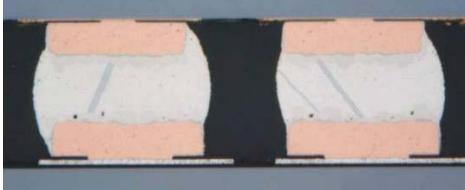
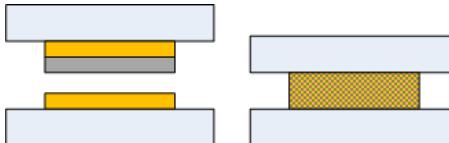
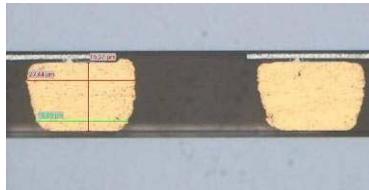
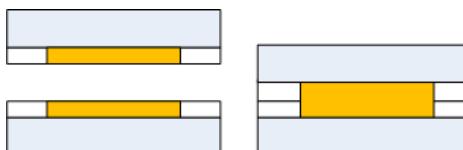
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Overview Hybridization Technologies

Technology		Deposition	Materials
Solder Bumping		<ul style="list-style-type: none">•Solder paste•Electroplating•Evaporation•Solder balls	<ul style="list-style-type: none">•Lead free: SnAg, SnAgCu•Lead cont.: SnPb•Low melt.: In, SnBi
IMC - Bonding		<ul style="list-style-type: none">•Electroplating	<ul style="list-style-type: none">•Cu -Sn IMC (SLID)
Thermo-compression		<ul style="list-style-type: none">•Electroplating•Stud Bumping•Evaporation	<ul style="list-style-type: none">•Au – Au•In-In
Metal-Metal Direct Bonding		<ul style="list-style-type: none">•Electroplating	<ul style="list-style-type: none">•Cu – Cu

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Hybridization Technologies

Cost drivers:

- Technology (process steps, tools, time, man power, ...)
 - Deposition
 - Assembly
 - Handling
 - Testing
- Material

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Number of Process Steps - Deposition

Electrodeposition of solder bumps

Sputtering plating base

Patterning of resist

electrodeposition

stripping of resist

stripping of plating base

reflow

Evaporation of solder bumps

Patterning of resist

Sputtering UBM

evaporation

stripping of resist (lift off)

reflow

Solder paste printing

UBM deposition
sputtering/eless/edepos.

Paste printing

reflow

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Number of Process Steps - Assembly

solder bump bonding (C2C)

Dicing of ROC and sensor

ROC pick and place onto sensor

reflow

Thermocompression bonding (C2C)

Dicing of ROC and sensor

ROC pick and place onto sensor
pressure/temperature

IMC bonding (C2W)

Dicing of ROC

ROCs pick and place on carrier wafer

Wafer to wafer bonding time/pressure/temperature

carrier wafer release from ROC side

Dicing of sensor wafer

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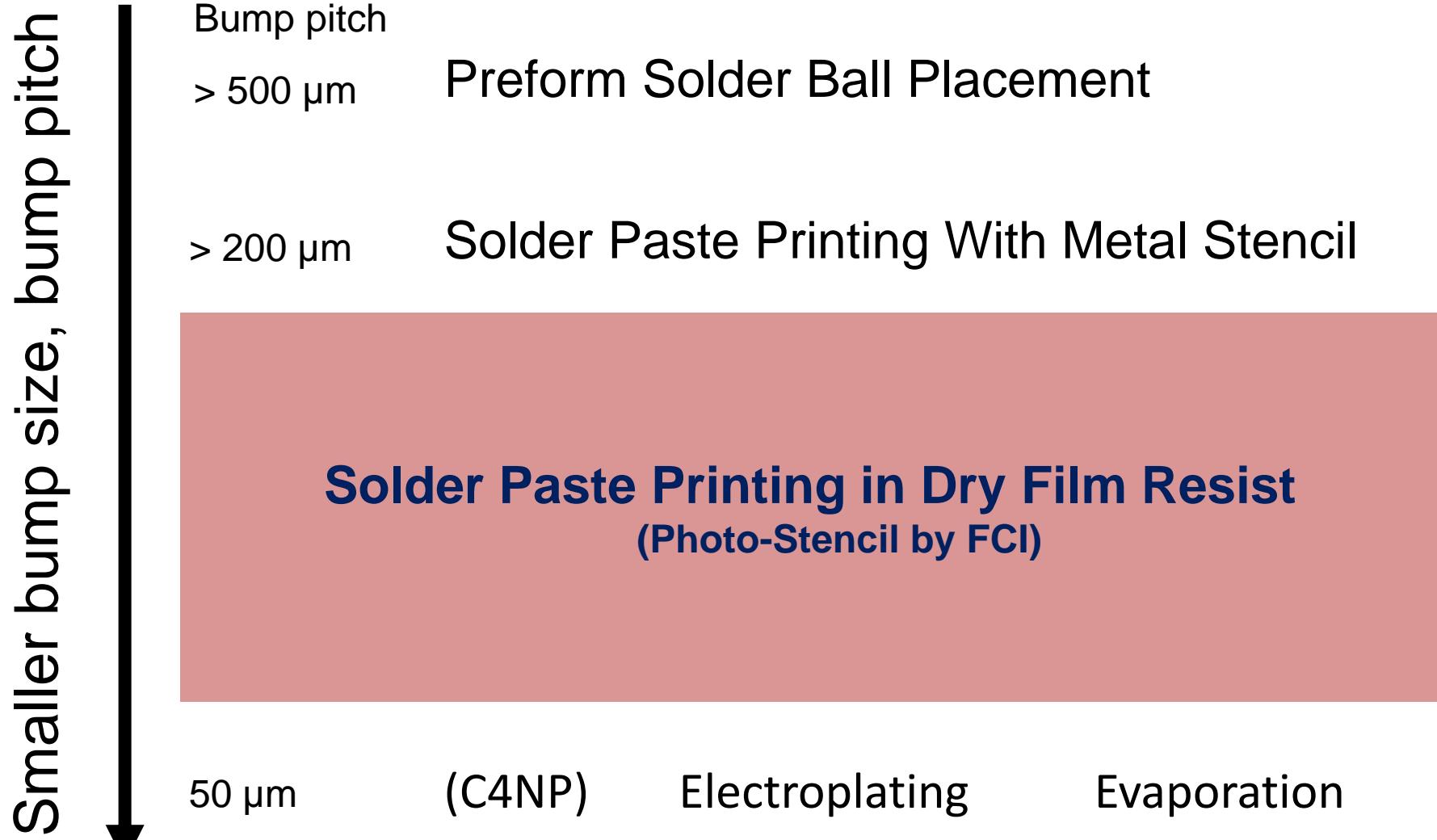
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Bump Deposition Technologies



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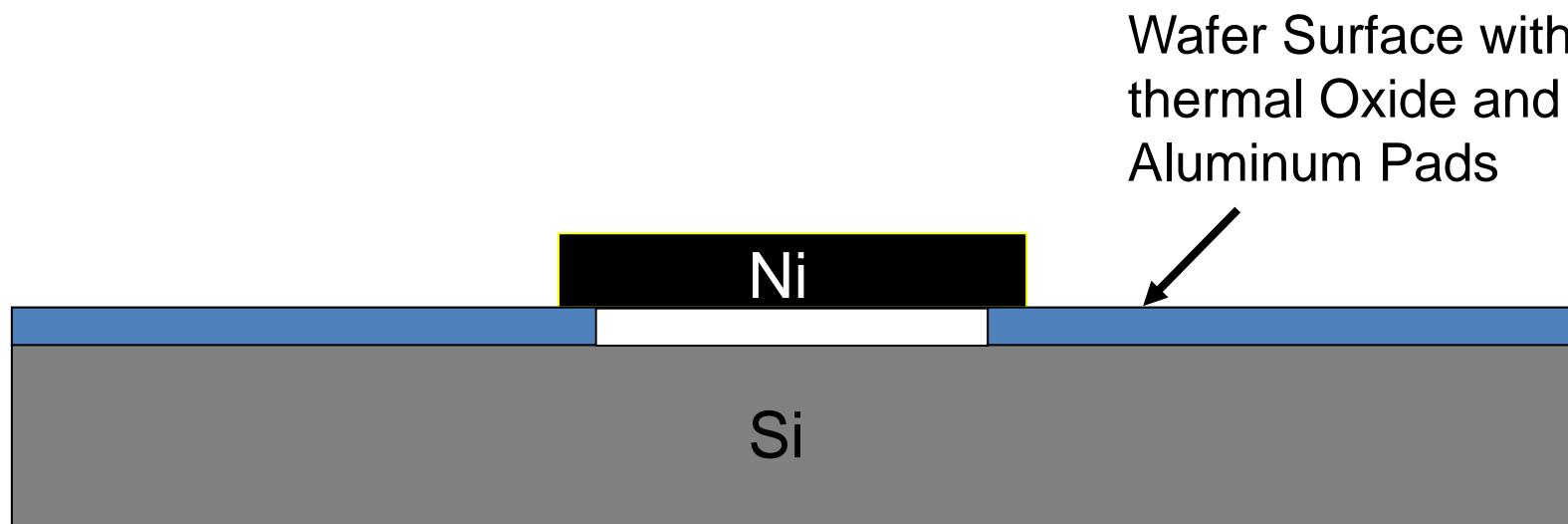
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Solder Paste Printing in Dry Film Resist

Process Flow

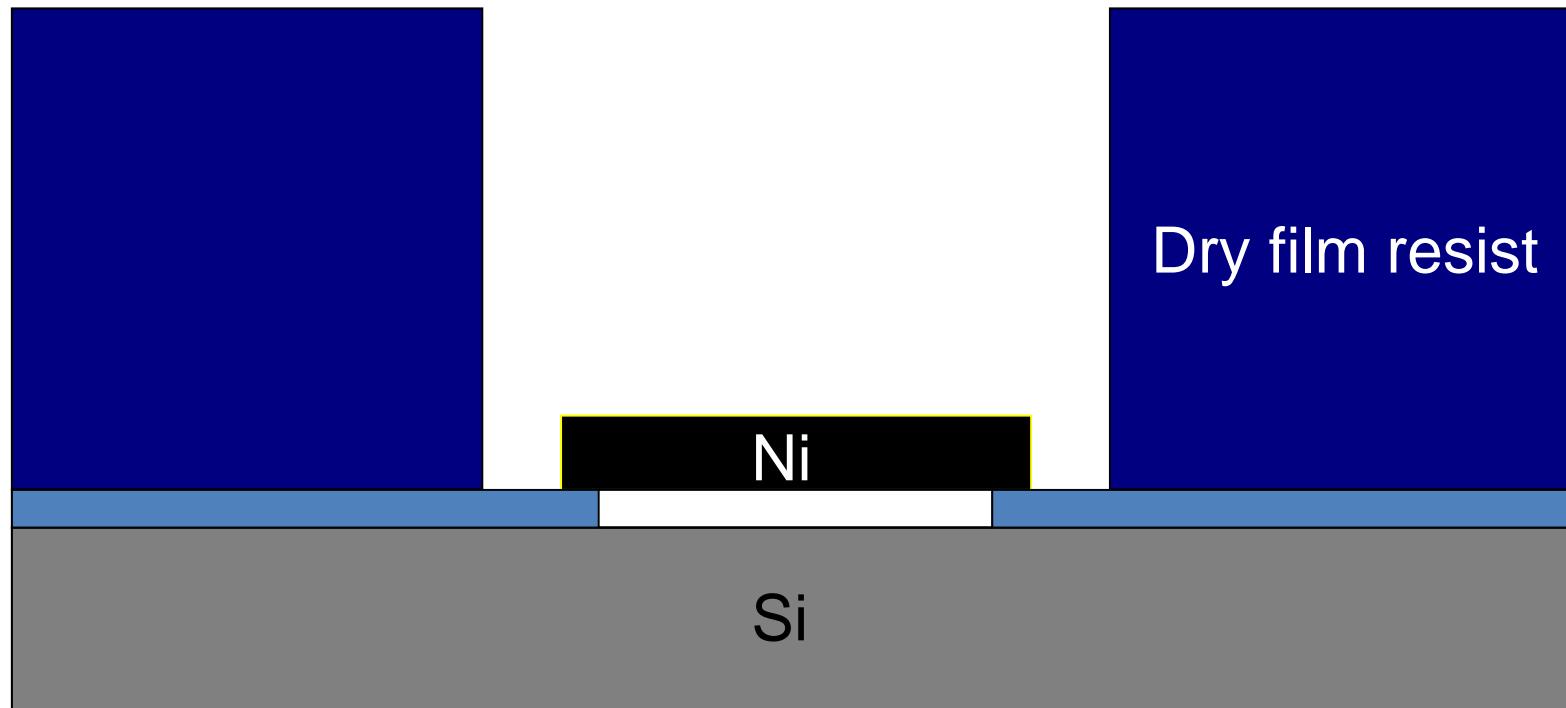
Step1: Providing an Under Bump Metalization (UBM)



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Solder Paste Printing in Dry Film Resist

Step2: Dry film lamination, exposure, development



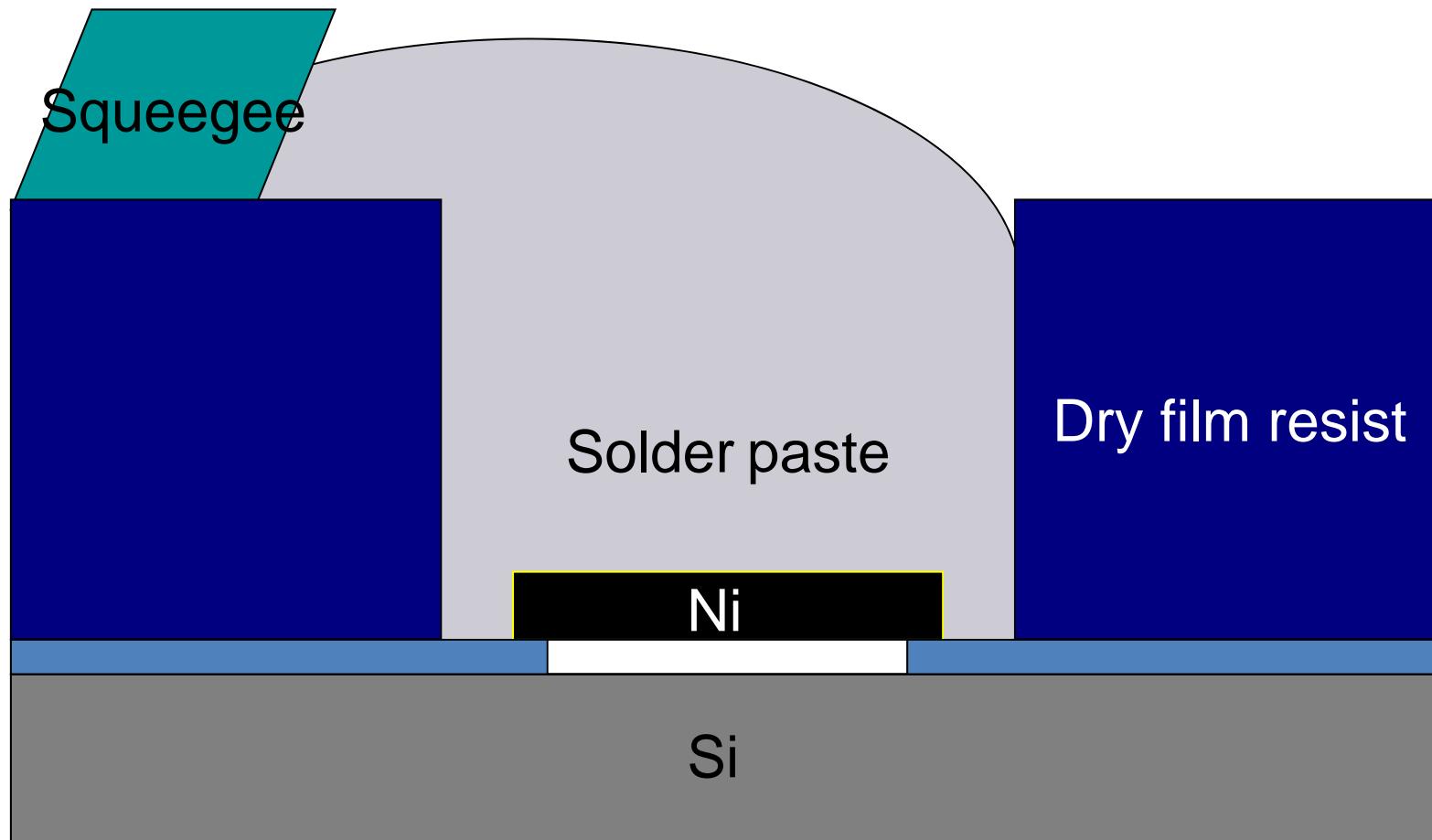
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Solder Paste Printing in Dry Film Resist

Step3: Paste printing



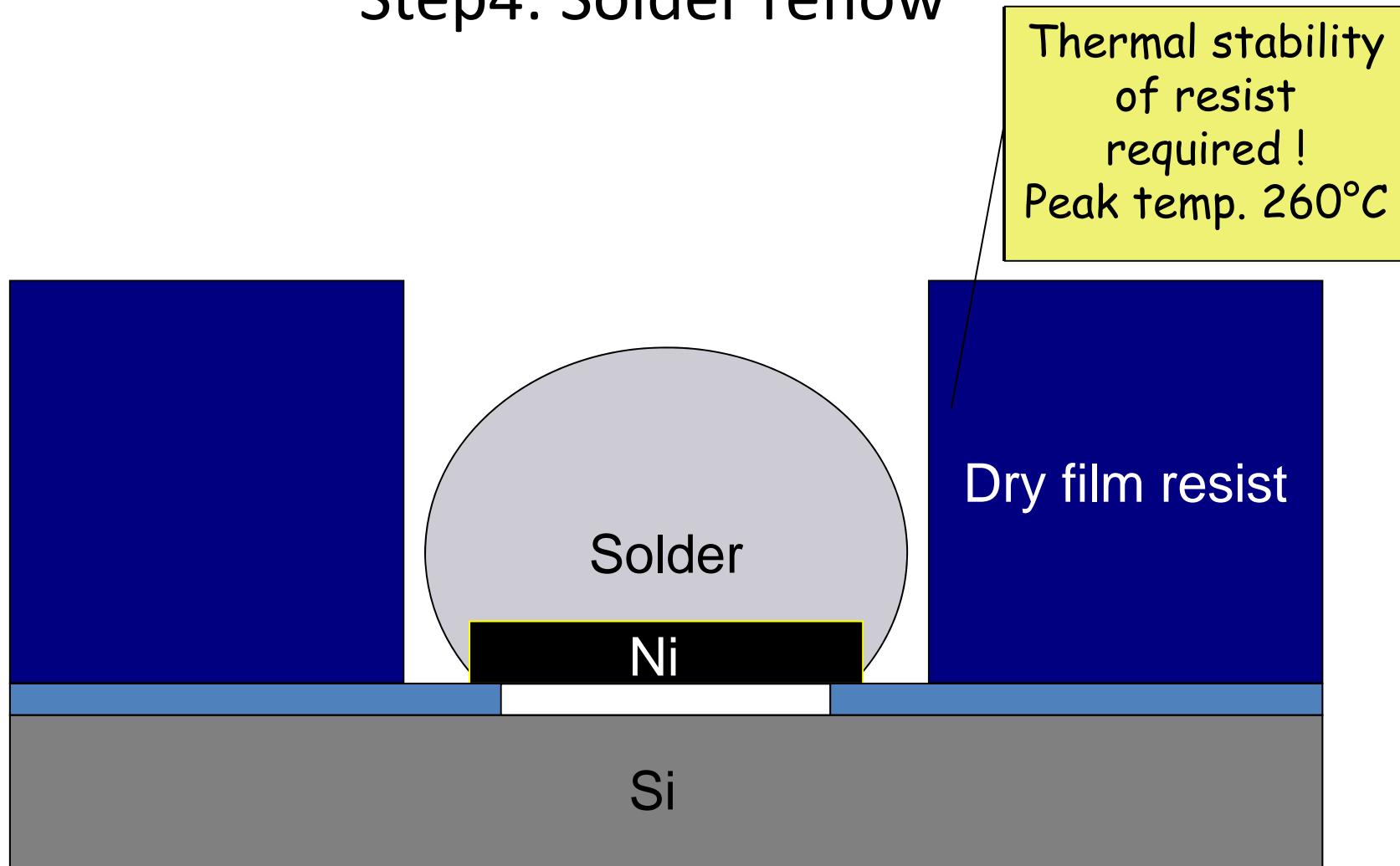
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Solder Paste Printing in Dry Film Resist

Step4: Solder reflow



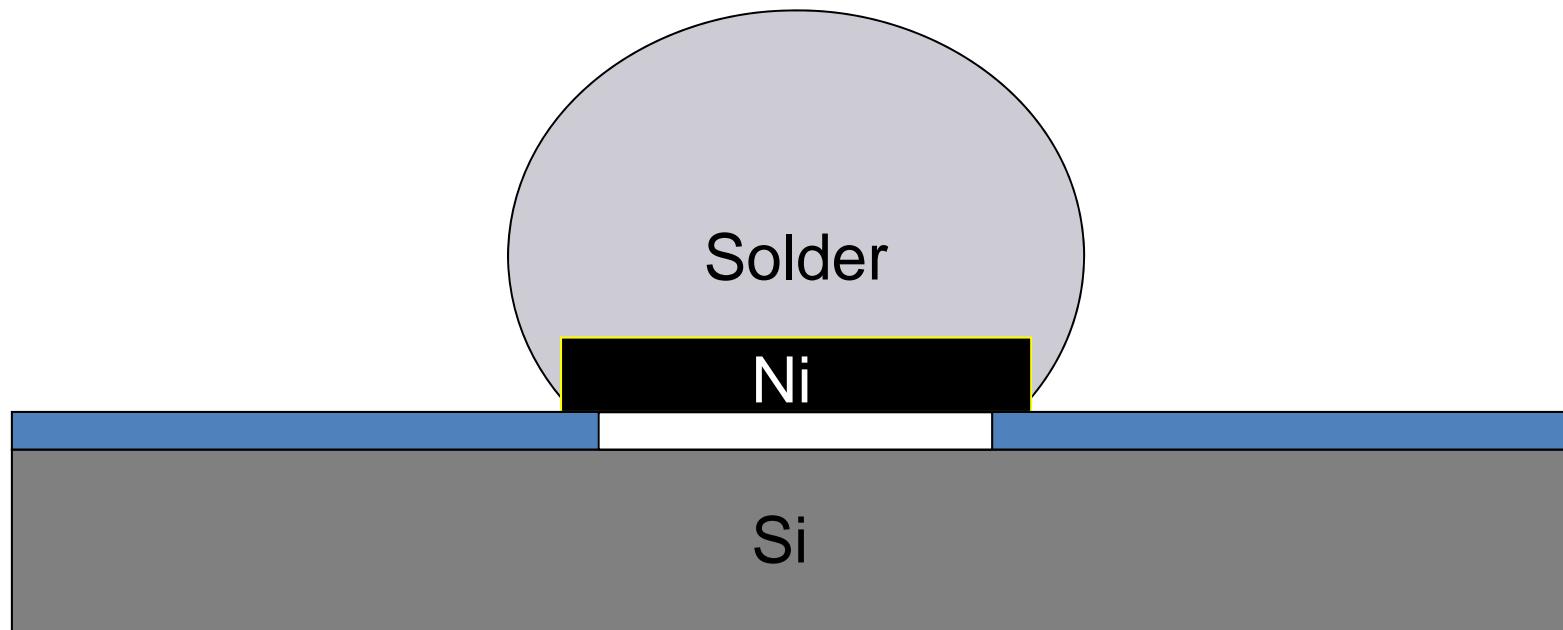
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Solder Paste Printing in Dry Film Resist

Bumped wafer



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Solder Paste Printing in Dry Film Resist

Technology Test Batch – Materials and tools

Solder paste:

- SnAgCu paste (type 5 + **6**) [10-25µm, **5-15µm**]
- PbSn paste (type 6 +**8**) [5-15µm, **2-8µm**]

Dry film resist:

- height 100µm, 75µm

Silicon wafer:

- Silicon wafer 200mm with Ni/Au UBM test pattern

Tools used:

- MicroControl Laminator Leonardo
- Suss MicroTec MA200 / Spray developer in Suss ACS200 cluster
- DEK paste printer / Heraeus reflow oven

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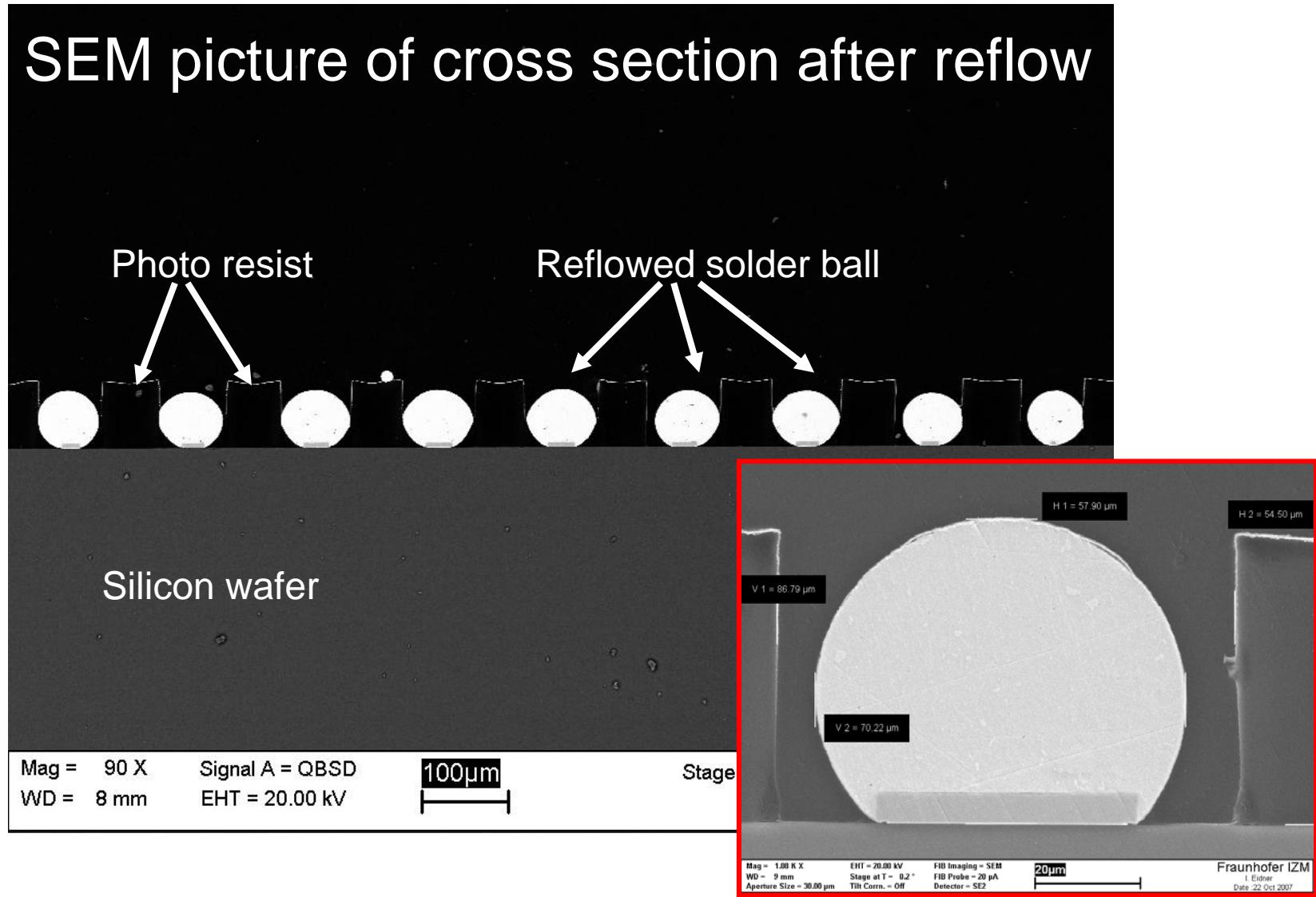
Solder Paste Printing in Dry Film Resist



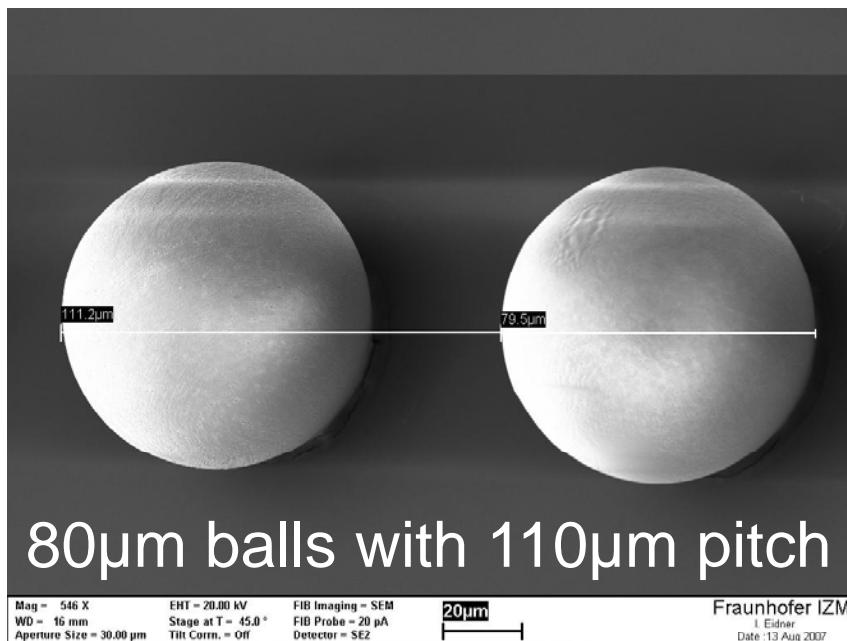
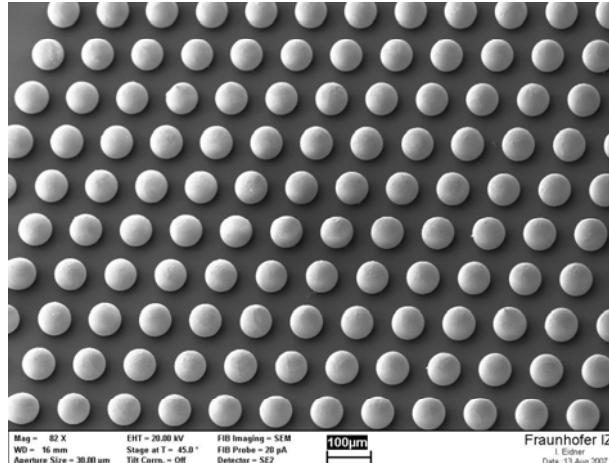
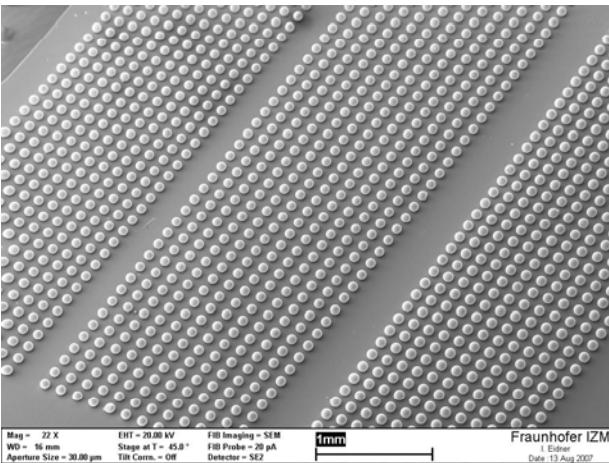
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Solder Paste Printing in Dry Film Resist

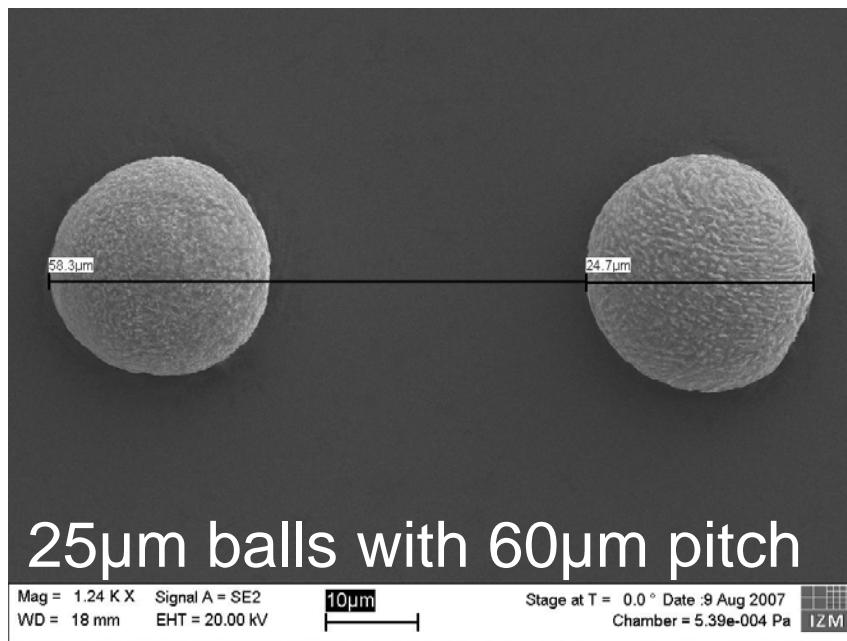
SEM picture of cross section after reflow



Solder Paste Printing in Dry Film Resist



80μm balls with 110μm pitch



25μm balls with 60μm pitch

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Chip To Wafer Flip Chip Assembly

C2W Assembly Process Evaluation

- Chip to wafer assembly of FE-I4 size ROCs using a high throughput Pick&Place Tool
- Pick and place alignment accuracy for 20 μm and 60 μm pad/bump size
- Reduction of flip chip pick and place alignment time (modified alignment marks)
- module release from temporary carrier (automation)

Karl Suss FC150



- Accuracy: $\pm 1 \mu\text{m}$ at 3σ
- cycle time: ~2 min. per die
- maximum die size: 2" x 2"
- maximum substrate size: 6" x 6"
- heating profiles from top and bottom possible
- minimum alignment mark size: 20 μm

Panasonic FCB3

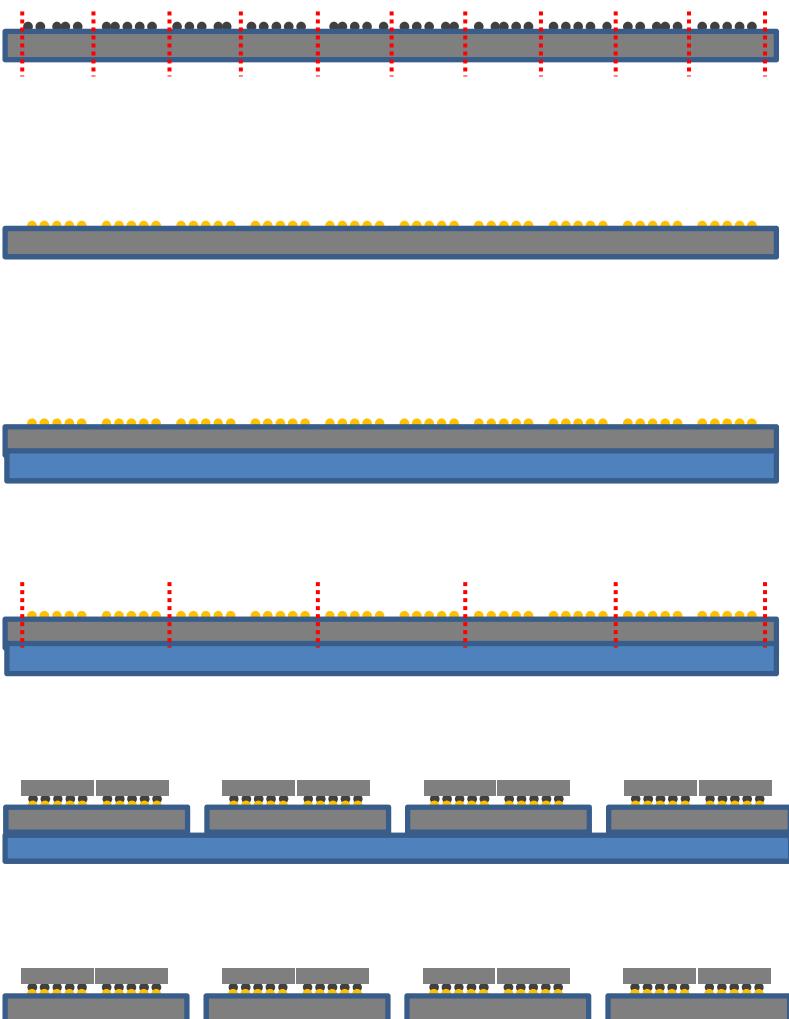


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Chip to Wafer Assembly – Technology Testbatch



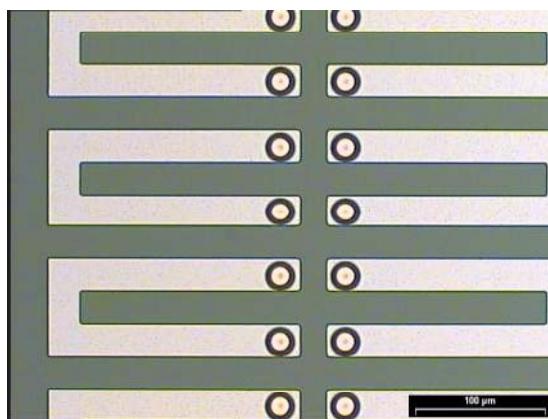
- SnAg bump deposition on 200mm FE-I4 daisy chain test chip wafer
- Solderable pad metal deposition on 150mm sensor daisy chain wafer
- mounting of the sensor wafer onto carrierwafer
- Sensor wafer dicing
- FE-ROC flip chip assembly at wafer level
- Module release from carrier wafer

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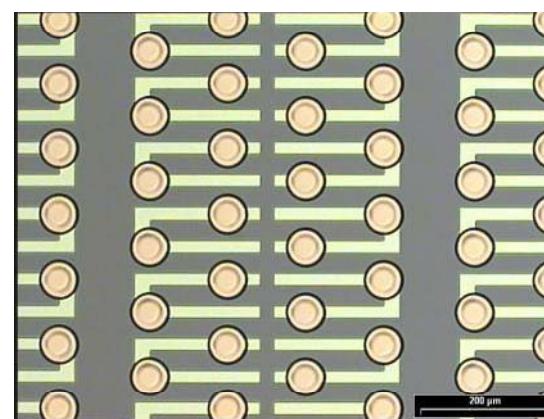


150mm Sensor Daisy Chain Wafer

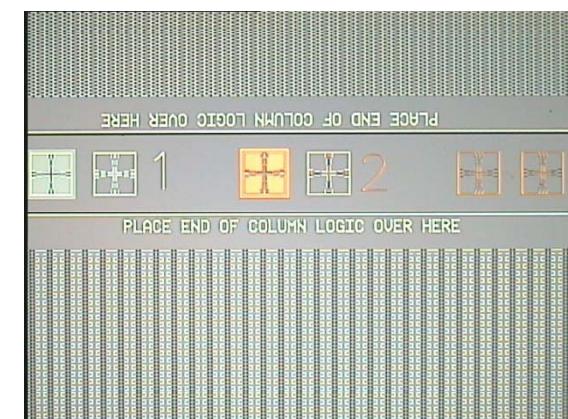
- FE-I4 Double-Chip Tiles
- FE-I4 Quad-Chip Tiles
- Pad size 20 μ m, 60 μ m
- Pad pitch 50 μ m, 100 μ m, stacked



Pad size 20 μ m, pitch 50 μ m



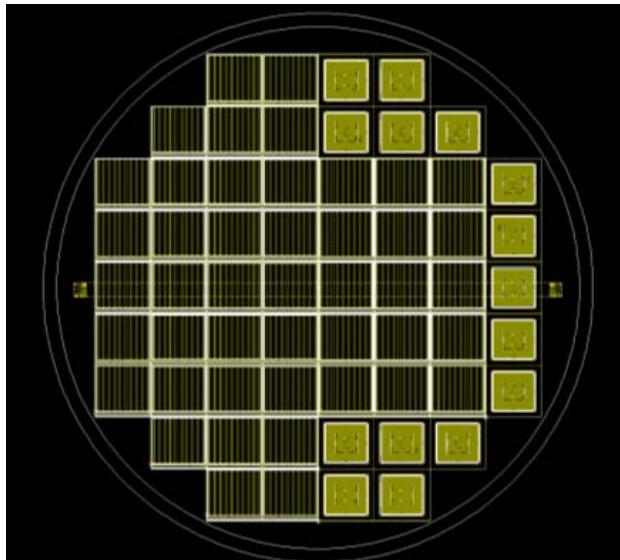
Pad size 60 μ m,
pitch 100 μ m, stacked



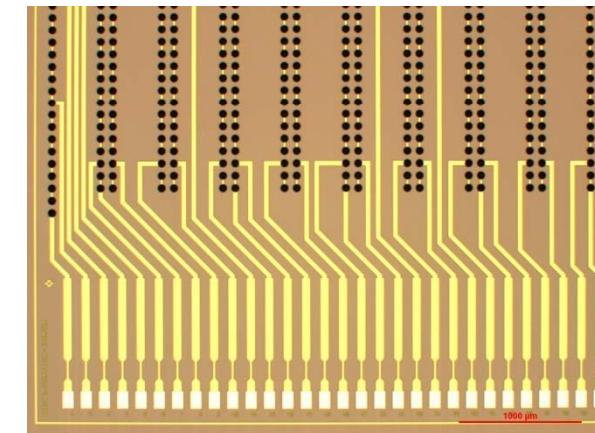
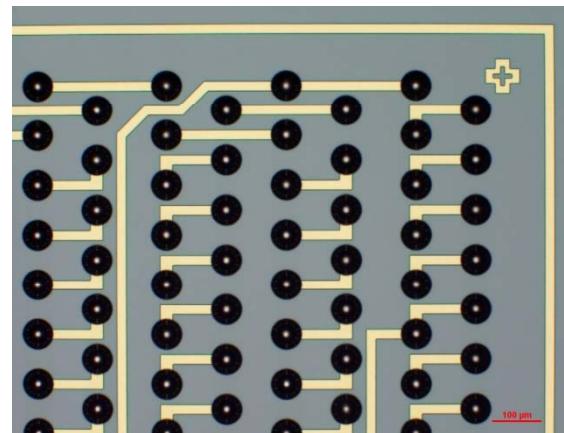
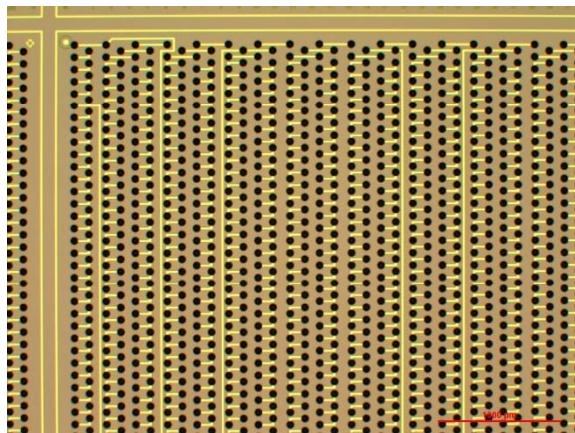
End of column logic overlap area

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200mm Daisy Chain Wafer – ATLAS FE-I4 size Chips



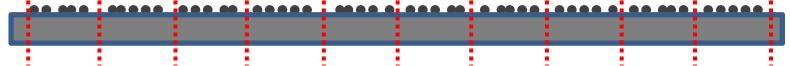
- FE-I4 size daisy chain test chips
- FE-I3 sensor fan out test chips (used by University of Dortmund)
- bump size 20 μ m, 60 μ m
- bump pitch 50 μ m, 100 μ m, stacked



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- SnAg bump deposition on 200mm FE-I4 Daisy Chain Testchipwafer



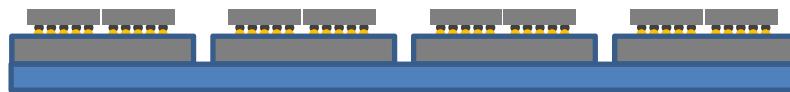
- Solderable pad metal deposition on 150mm sensor daisy chain wafer



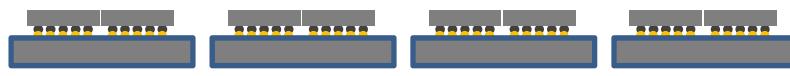
- mounting of the sensor wafer onto carrierwafer



- Sensor wafer dicing



- FE-ROC flip chip assembly at wafer level



- Module release from carrier wafer

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Summary:

- Overview on hybridization technologies with focus on costs
- solder paste printing in dry film resist – cost effective solder deposition
- test batch for low cost assembly technology – chip to wafer bump bonding using temporary carrier concept

Outlook:

- evaluation of solder paste printing in dry film resist on several wafer designs
- Process evaluation for high volume assembly technology:
 - Assembly tests and characterization
 - Module release from temporary carrier (automation)
 - Electrical characterization – daisy chain measurement

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Thank You !

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