A novel SOI pixel detector with depleted substrate

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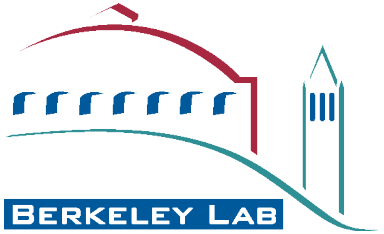
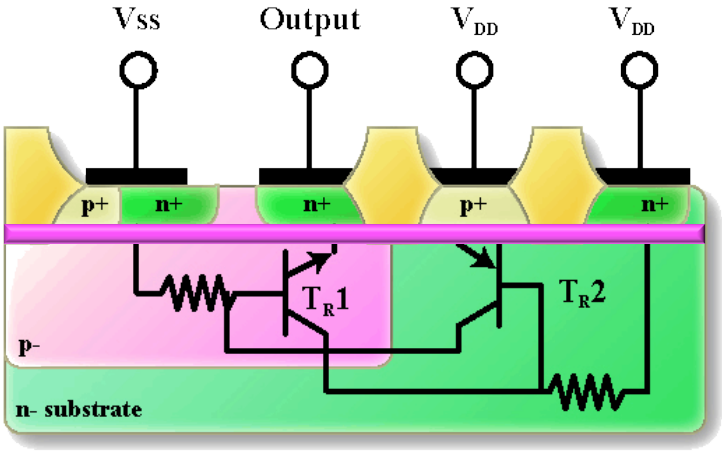
[4]CERN, Geneva, CH

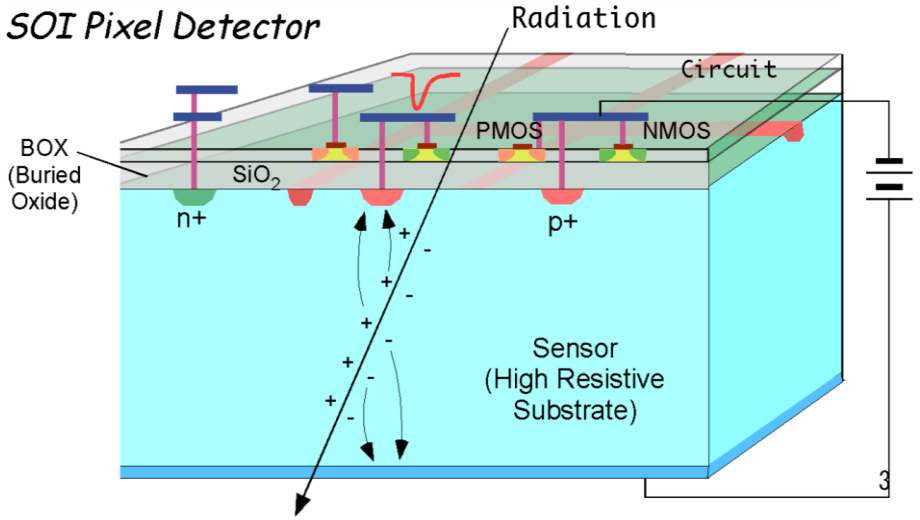


Some SOI basics

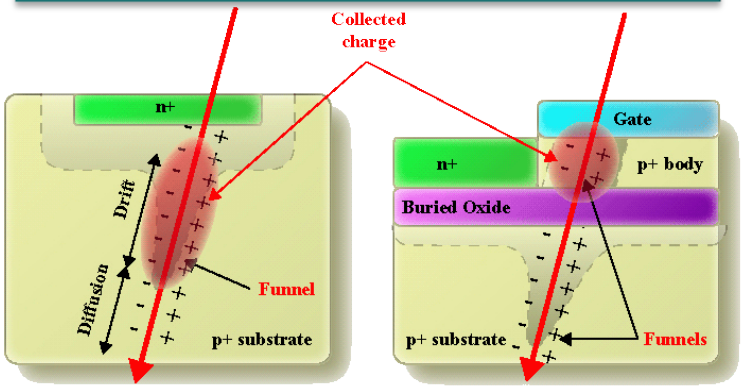
- SOI technology integrates CMOS electronics on top of a Buried Oxide (SOI), ensuring full dielectric isolation, small active volume and low junction capacitance: *latch-up immune, low power, high speed designs are thus favoured*
- 0.15-0.20 µm Fully-Depleted (FD) SOI processes from OKI, Japan allow contacting a high-resistivity (700 Ω/cm) substrate through the BOX for pixel implanting and substrate reverse bias
- Possibility for small pitch pixel sensors with high density, full CMOS readout electronics integrated in the same device → *SOI Monolithic Pixel Sensors*

40 nm silicon layer isolated from the bulk by the SiO_2 layer -> No PNPN parasitic structs.

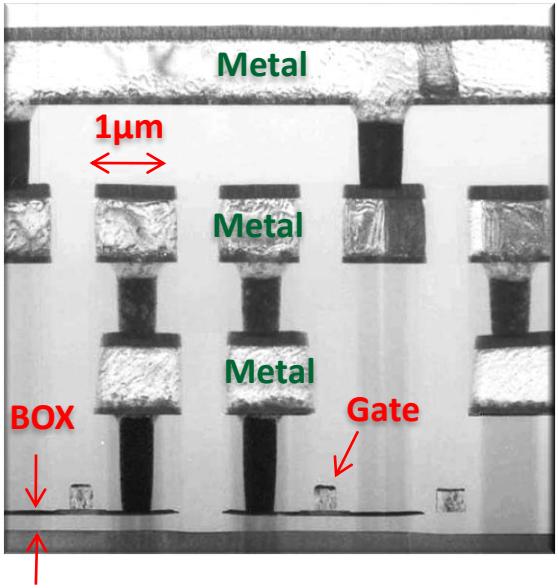




Small charge generation into the active area of the transistor, lower sensitivity to SEE.

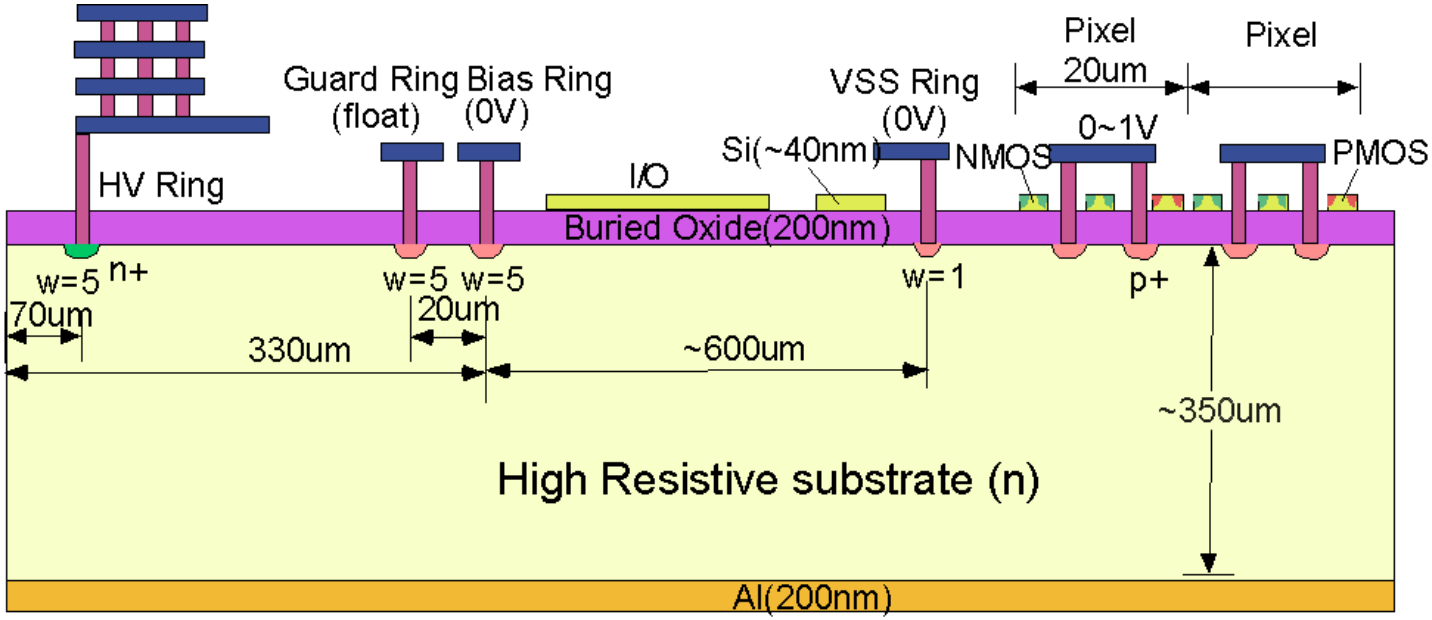


OKI SOI process



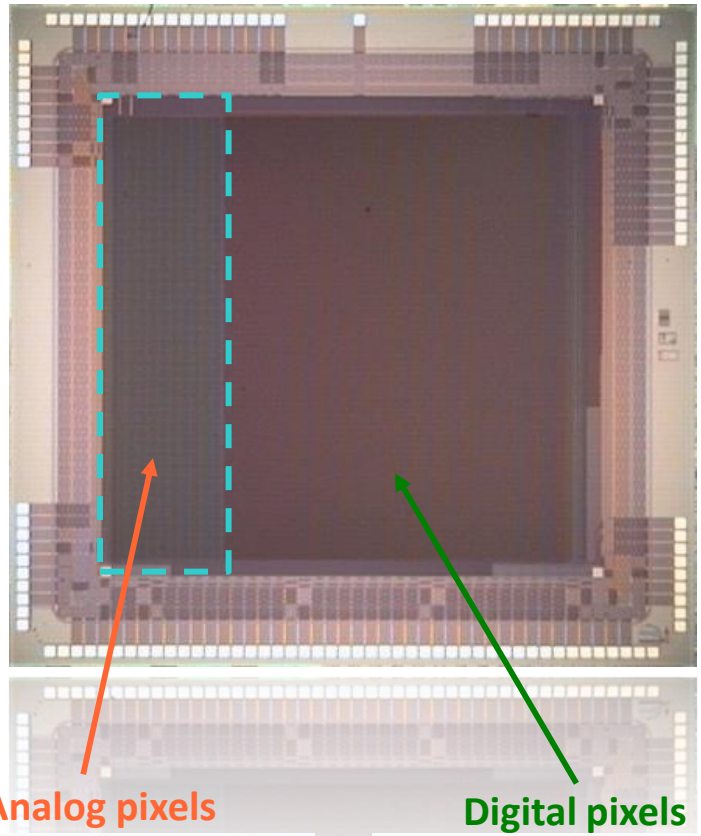
OKI 0.15 µm SOI process

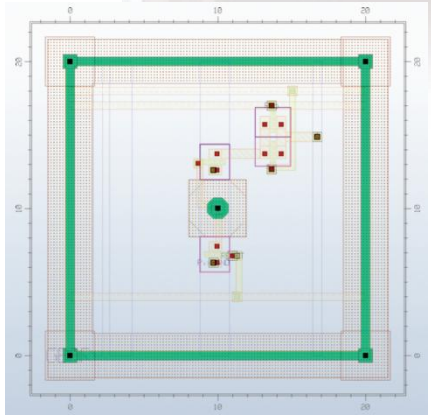
Process:	OKI 0.15µm fully-depleted SOI CMOS process, 1 Poly, 5 Metal	
SOI wafer:	Wafer Diameter: 150 mm, Top Si : Cz, ~18 Ω-cm, p-type, 40 nm thick fully depleted	Buried Oxide: 200 nm thick Handle wafer: Cz 700 Ω-cm, 650 µm thick (SOITEC ion cut)
Backside:	Thinned to 350 µm, plated with Al (200 nm).	

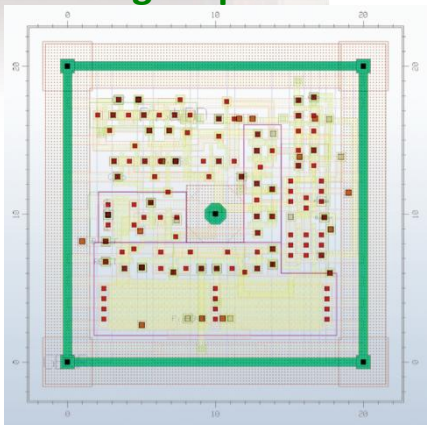


(This figure is not to scale)

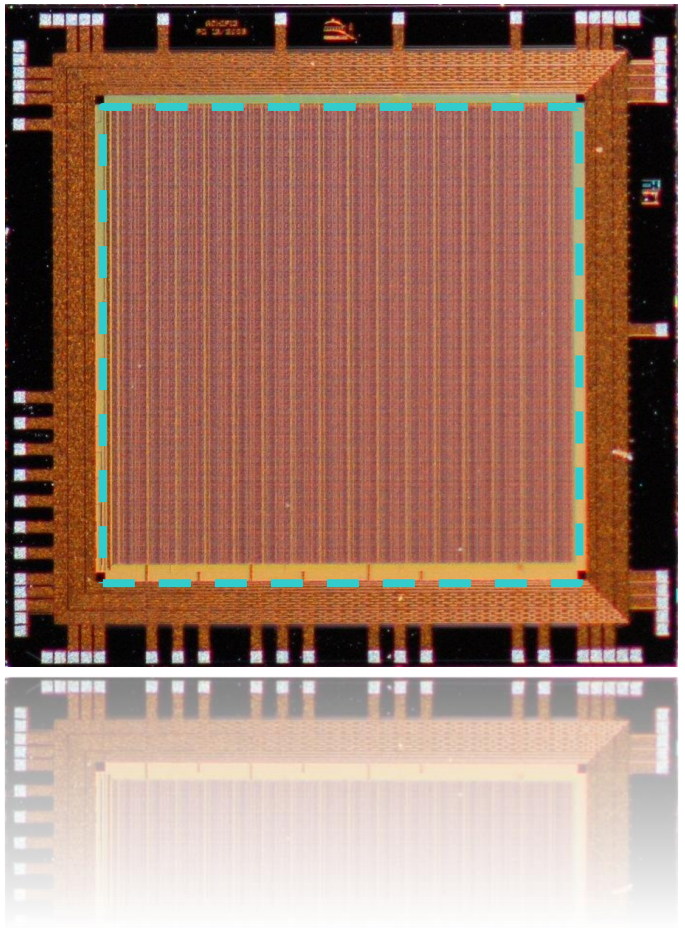
SOI 1







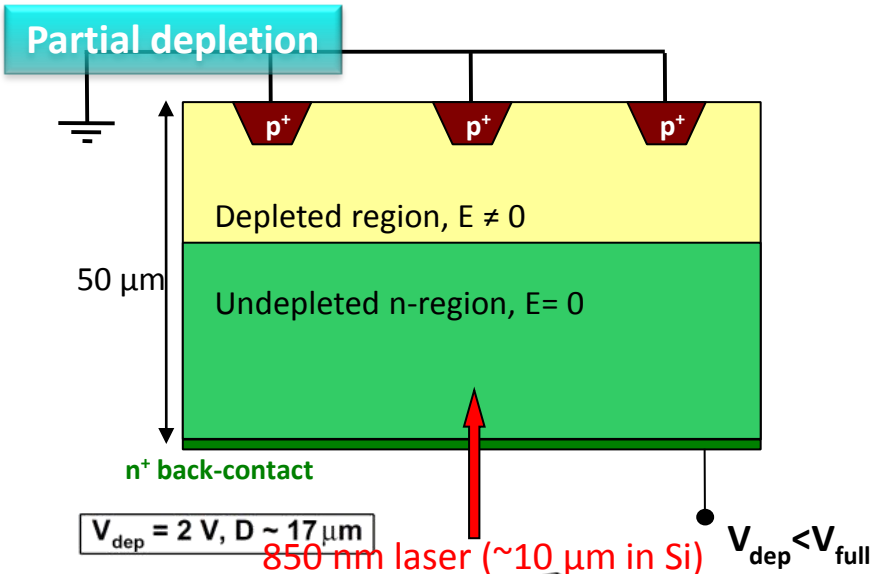
SOI *Imager* 1

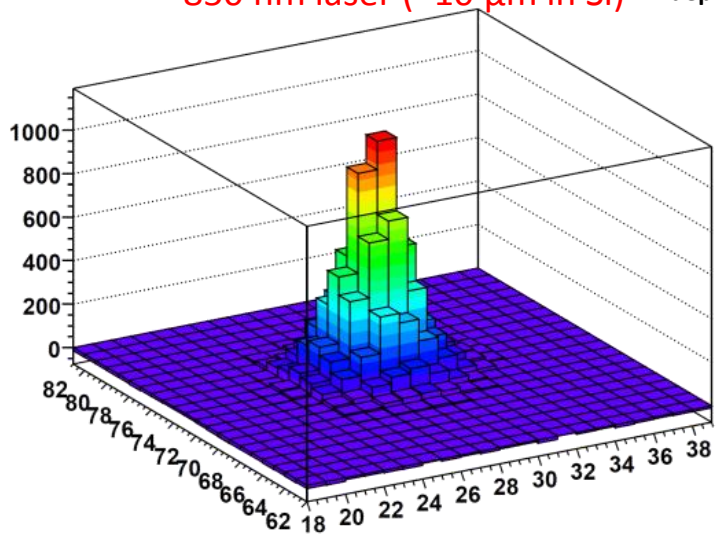


- OKI 0.20 µm FD-SOI process, 5x5 mm^2 area, 256x256 analog pixels, 13.75 µm pitch
- 4 parallel analog outputs, readout up to 50 MHz, 2-3 kframes/s

Charge diffusion measurements with 850 nm laser on a thinned chip

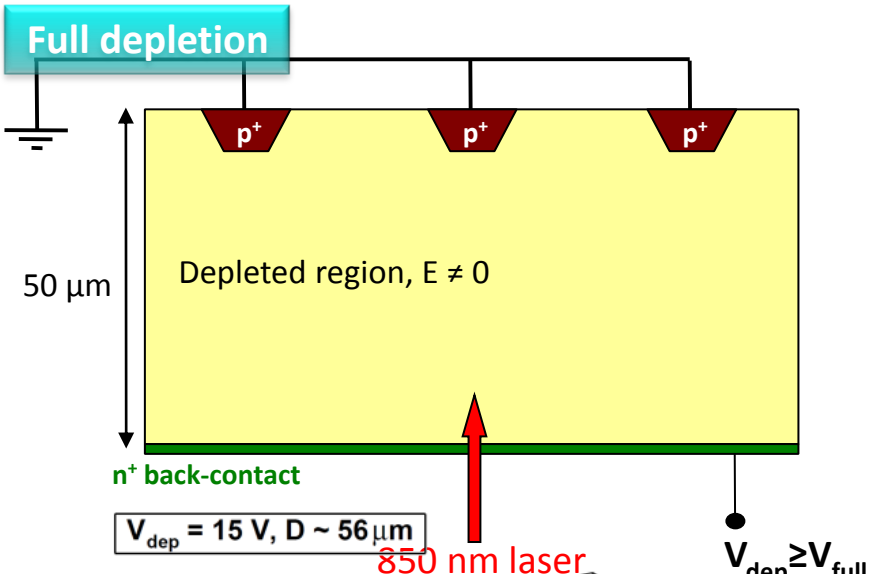
Partial depletion

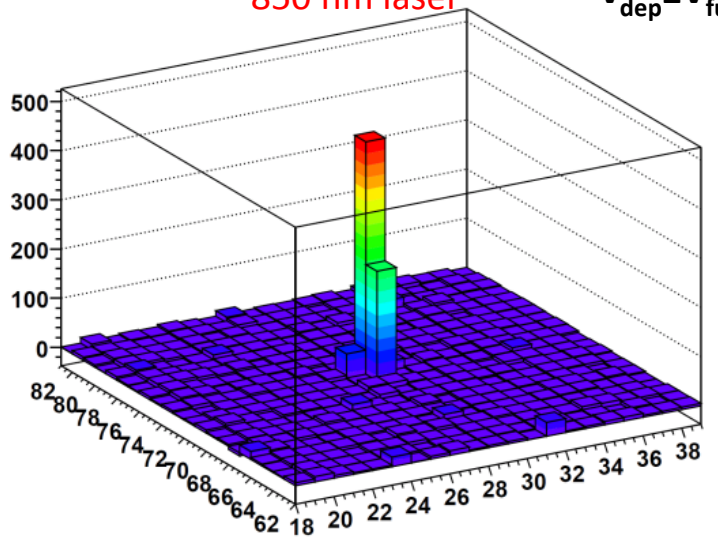




Large diffusion component in the undepleted silicon, large PSF

Full depletion

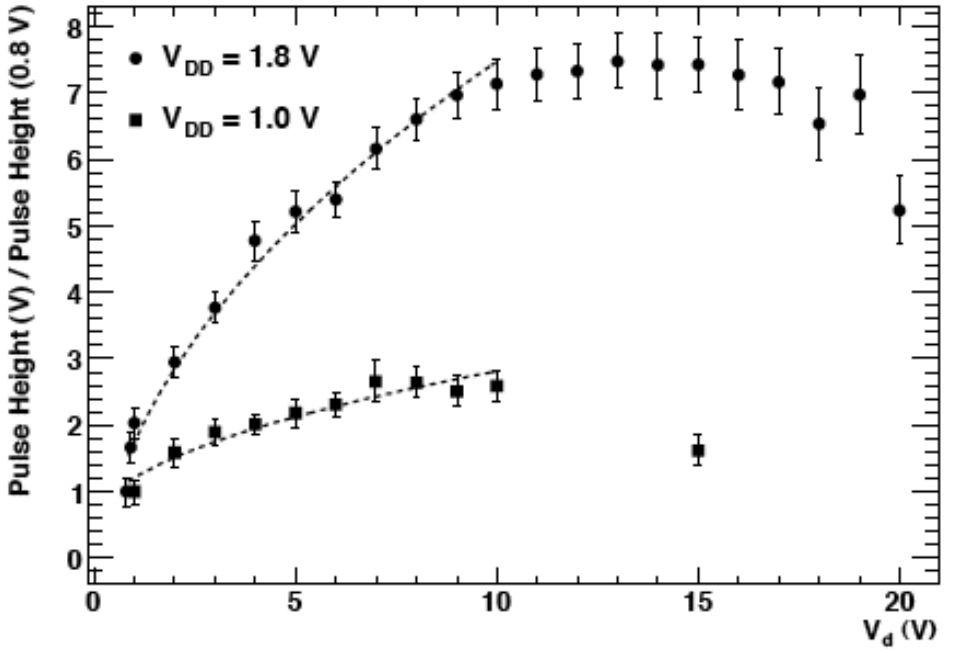


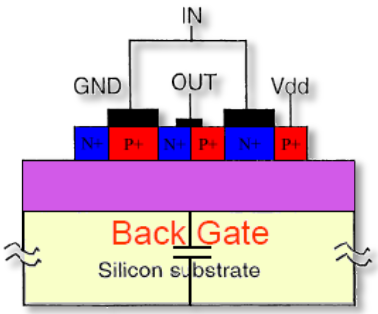


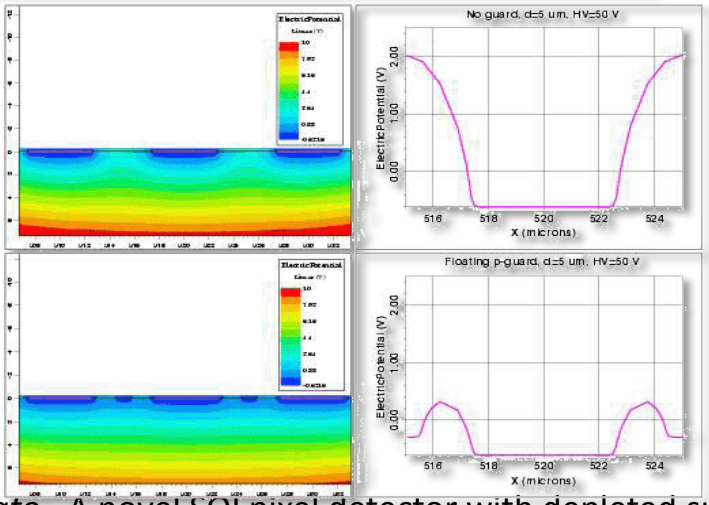
Charge collection dominated by drift, smaller PSF and faster collection time

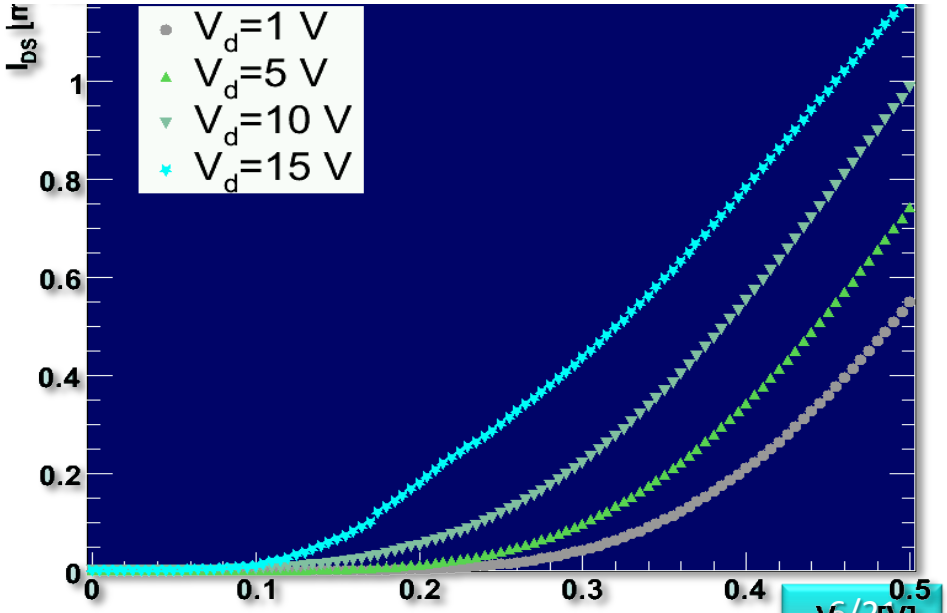
Back-gating effect on both SOI and SOI imager chip

- The high field in the depleted substrate causes back-gating of the CMOS electronics on top of the BOX
- Test of single transistors vs. depletion voltage: shift in the threshold voltage with increasing substrate voltage
- Significant effect observed in single transistor tests: expect analog section functional only for $V_{dep} < 20$ V
- Floating pguard structures around each pixel to keep potential low and limit back-gate effects on MOSFETs

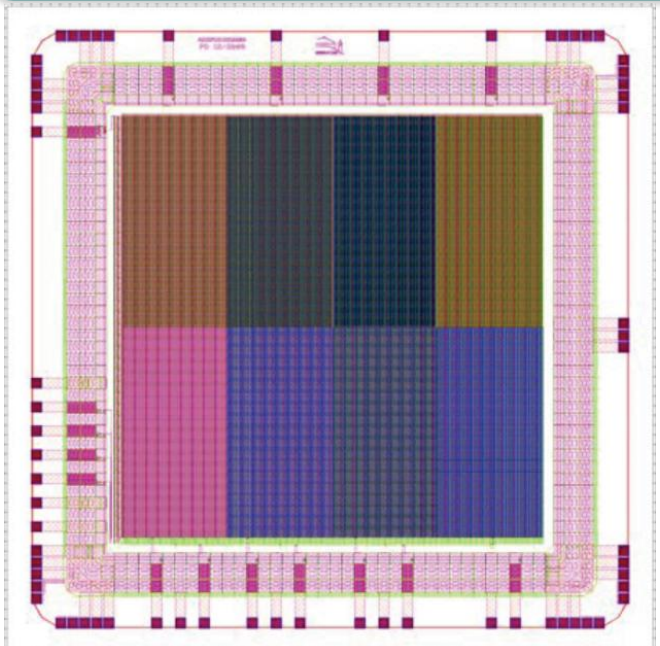




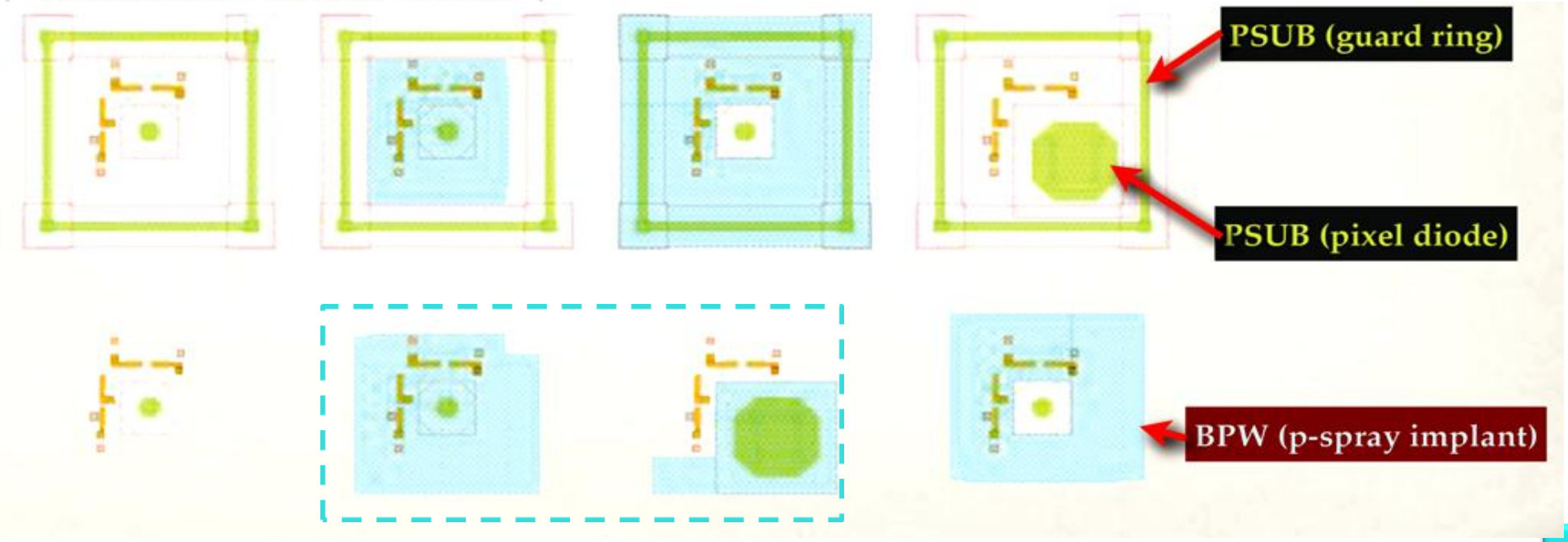




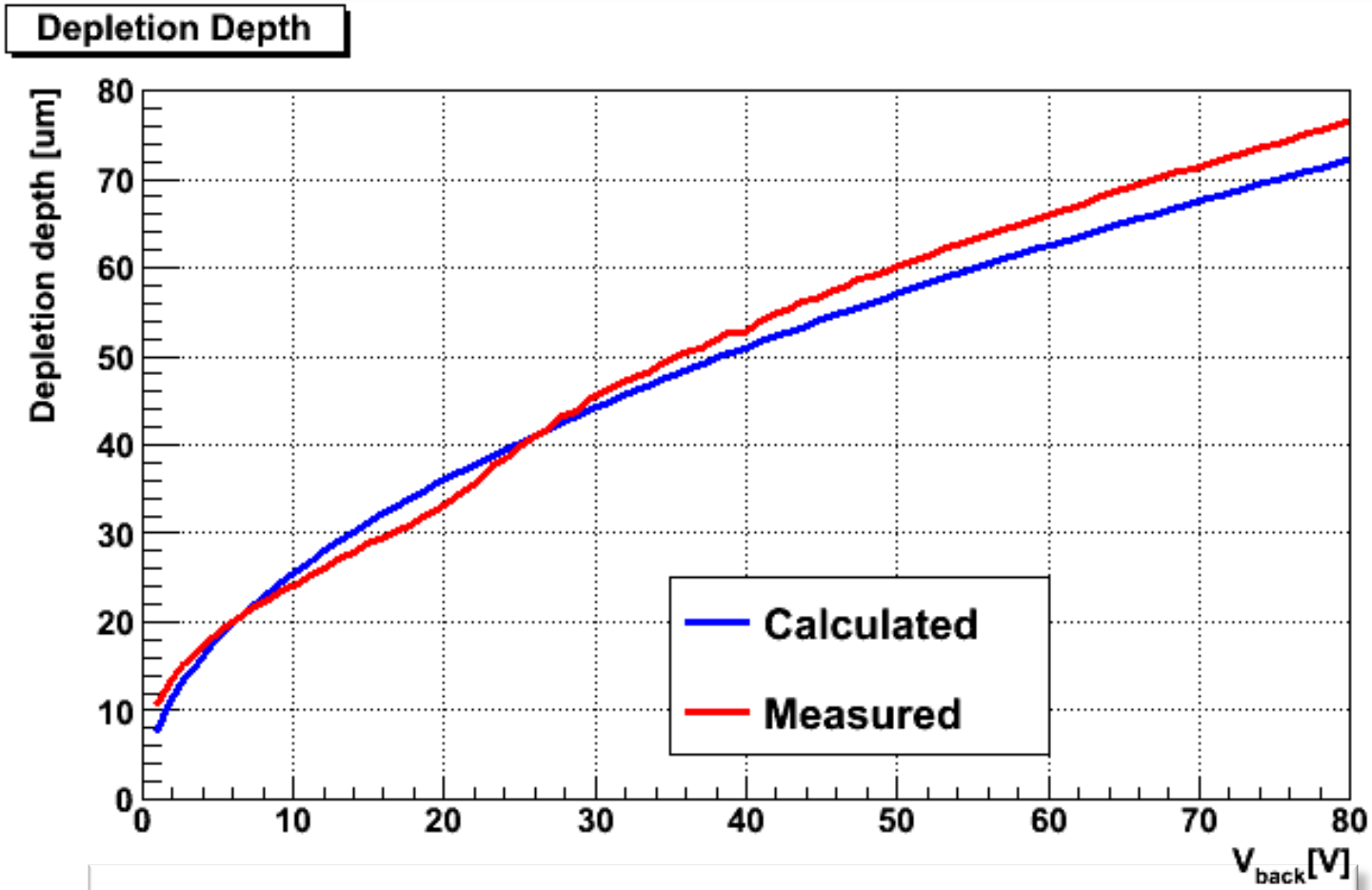
SOI *Imager 2*



- Improved version specifically designed to survive back-gating
- OKI 0.20 µm FD-SOI process, 5x5 mm^2 area, 256x256 analog 3T pixels, 13.75 µm pitch, 1.8 V operation, 8 different pixel flavours
- R&D version of 2009 LDRD-SOI-Imager prototype, exploring different pixel layouts and use of light p-doped implant (Buried P Well, *BPW*) vs pixel guard-ring (See Y. Arai talk).
- Is the BPW effective in containing back-gating?
- Can we avoid the floating guard-ring around the pixel (space)?



Actual depletion depth



- We measured depletion thickness by *C-V measurements* of the substrate, using the pixel guard-ring grid as electrode
- At first we had no agreement with resistivity data provided by company, then the company gave us new values which match near perfectly with our measurements.

- Measured depletion depth from C_j

$$W_{meas} = \varepsilon_S \cdot \frac{A}{C_j}$$

A: detector area
ε_S: silicon permittivity

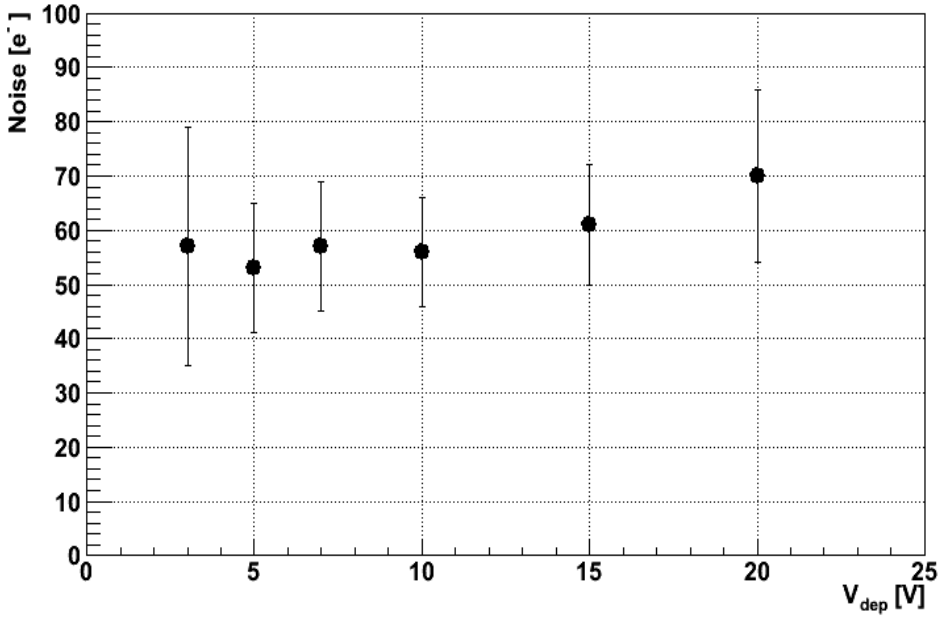
- Calculated depletion depth from the nominal resistivity (ρ = ***200*** $\Omega\cdot$cm $\leftrightarrow$ $N_B = 2\times10^{13}cm^{-3}$)

$$W_{calc} = \sqrt{2\varepsilon_S(V_{bi} - V_{back})\rho\mu_n} = \sqrt{\frac{2\varepsilon_S(V_{bi} - V_{back})}{qN_B}}$$

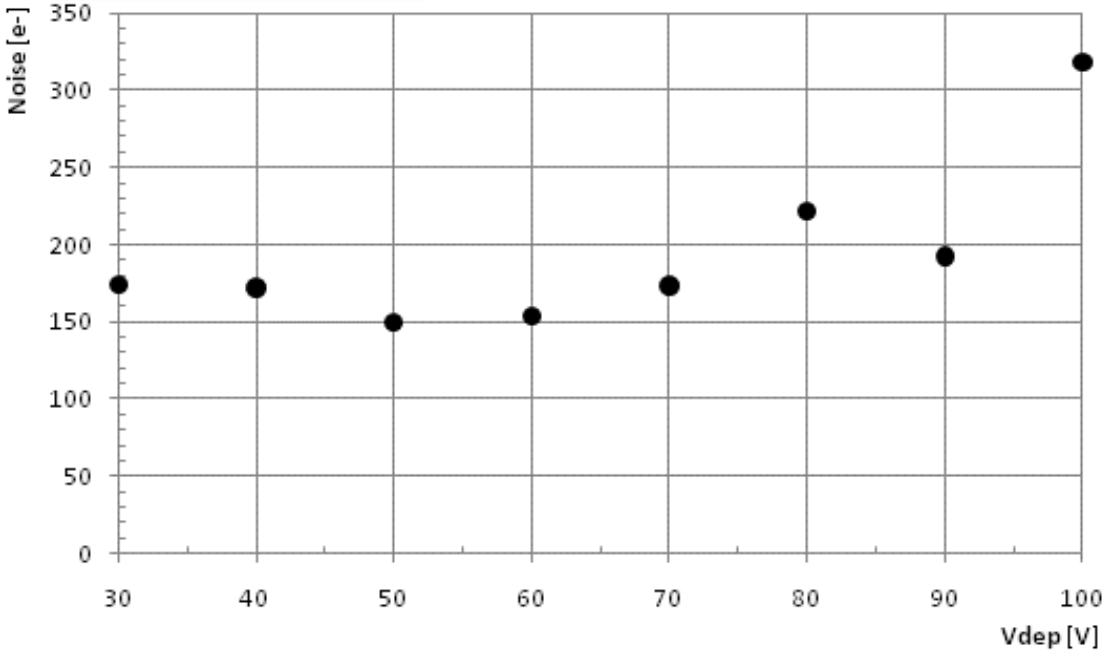
μ_n: electron mobility
ε_S: silicon permittivity
V_{bi} = V built-in
N_B = doping

Noise

SOI Imager 1 noise

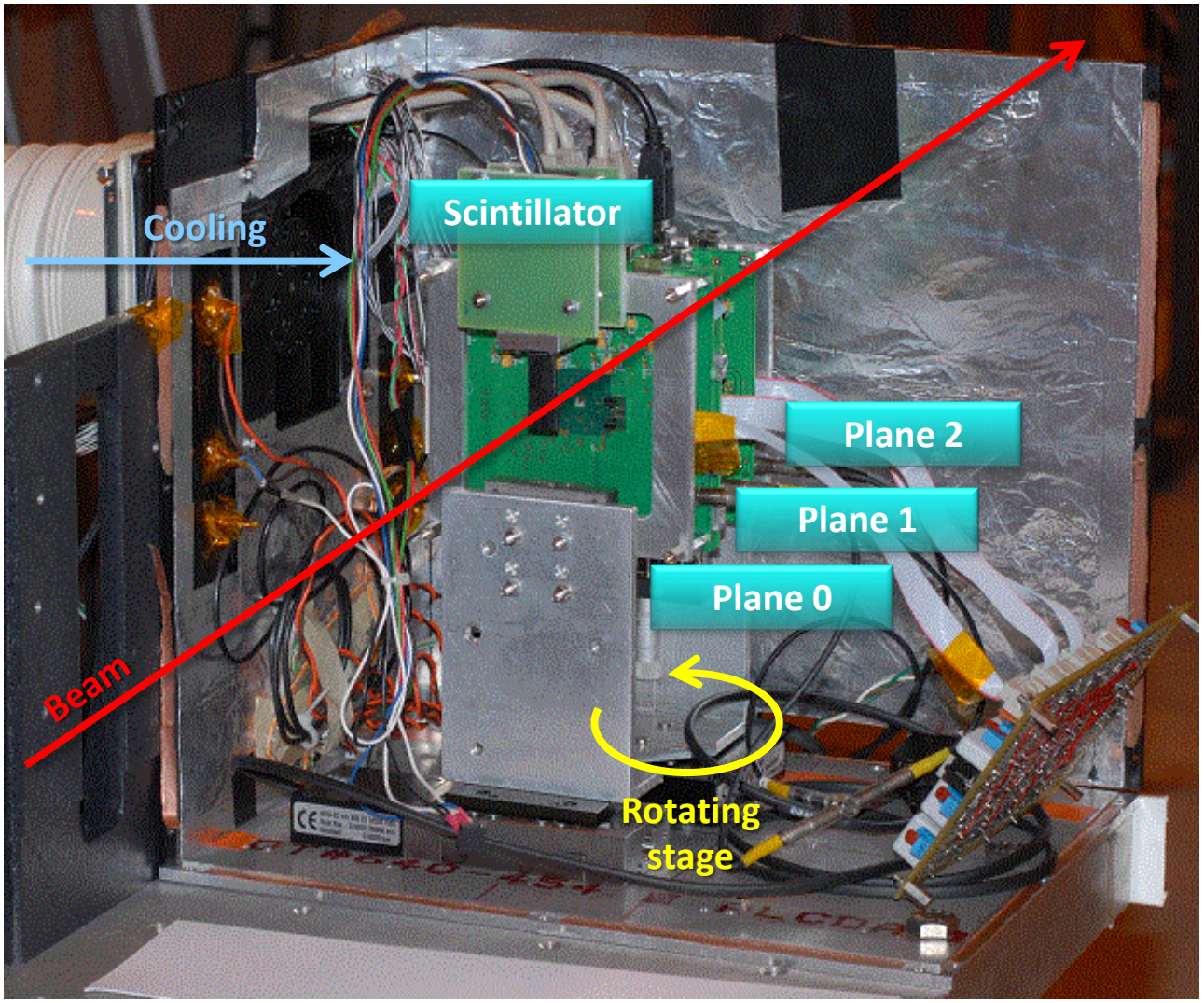


SOI Imager 2 noise



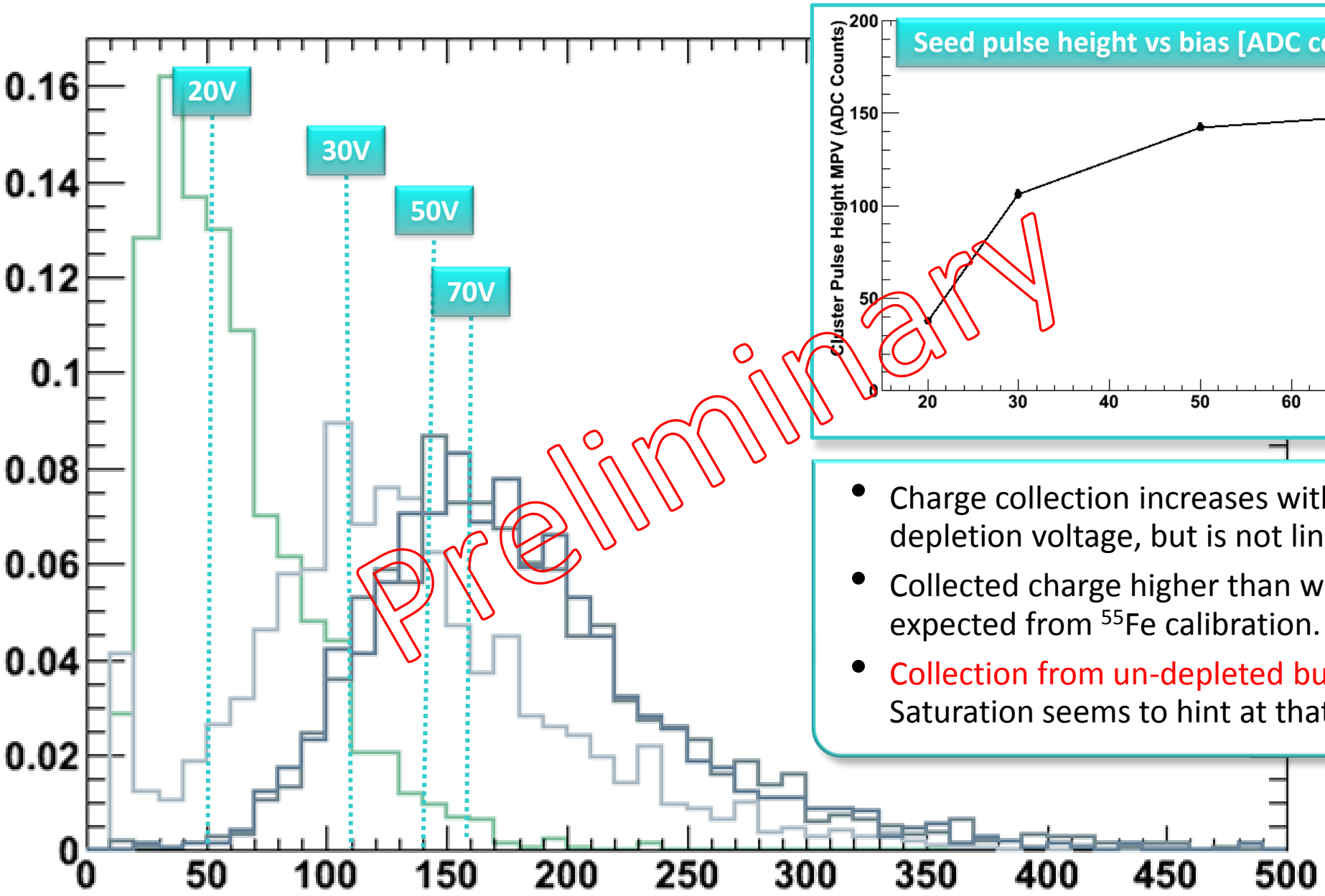
- Noise measured with the ^{55}Fe peak at *room temperature*.
- Noise much better with first run substrate batch (SOI Imager 1), but process is identical for both chip. Second batch shows much higher leakage current, so we think is just a quality issue with that batch.
- Tighter control over substrate should fix the issue in the future.

Test beam with 200 GeV π



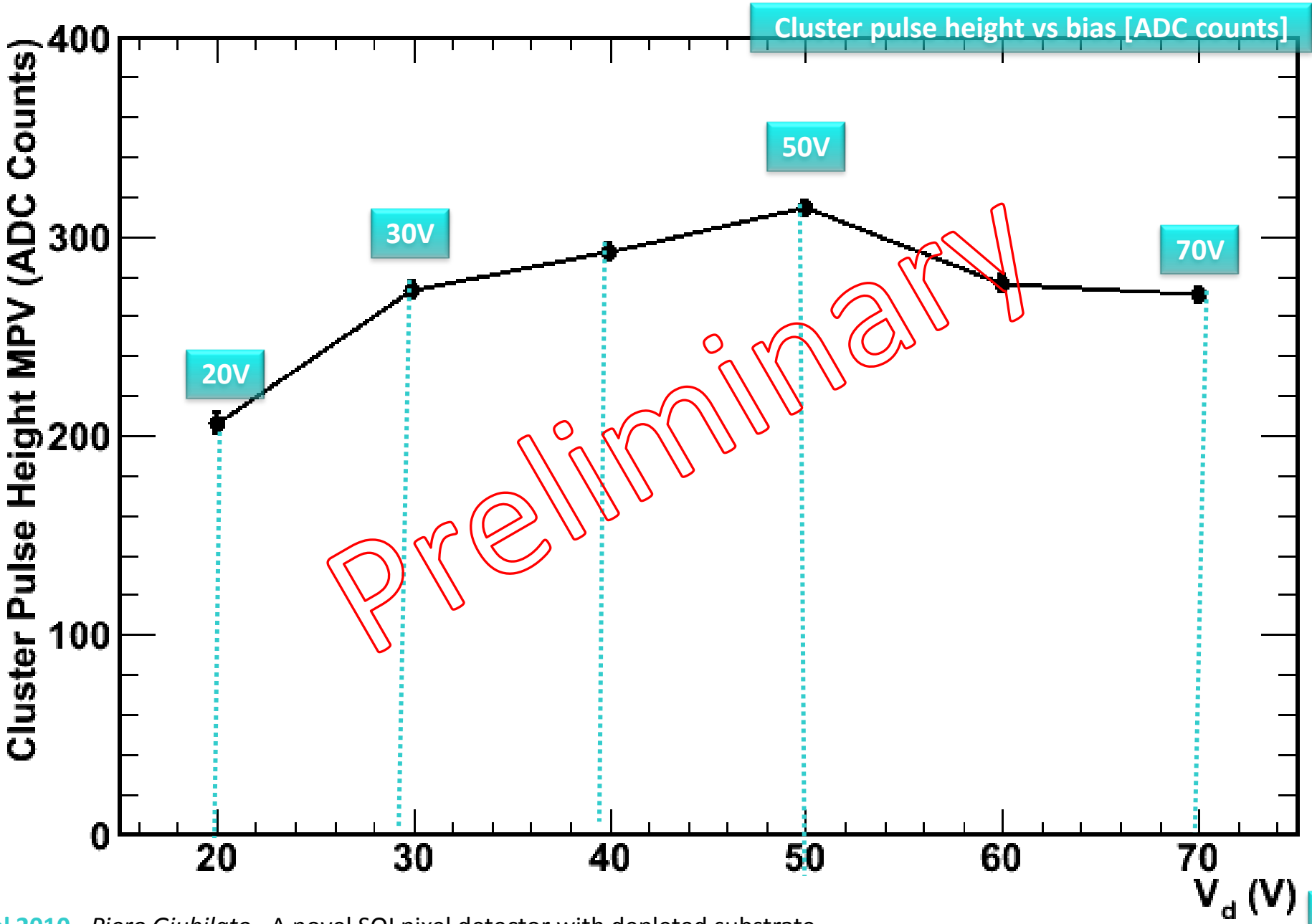
- Detectors arranged in one cemented "doublet" (9 mm spaced) and one rotating plane (33 mm spaced).
- The doublet is optically aligned with a better than 50 μm precision → easy and precise coincidence cuts in cluster recognition.
- Single plane can be rotated up to 20° for slanted tracks and cluster studies.
- Temperature is maintained around 20° by cool air flow and continuously monitored.

Test beam results – seeds height



- Charge collection increases with the depletion voltage, but is not linear.
- Collected charge higher than what expected from ^{55}Fe calibration.
- Collection from un-depleted bulk? Saturation seems to hint at that.

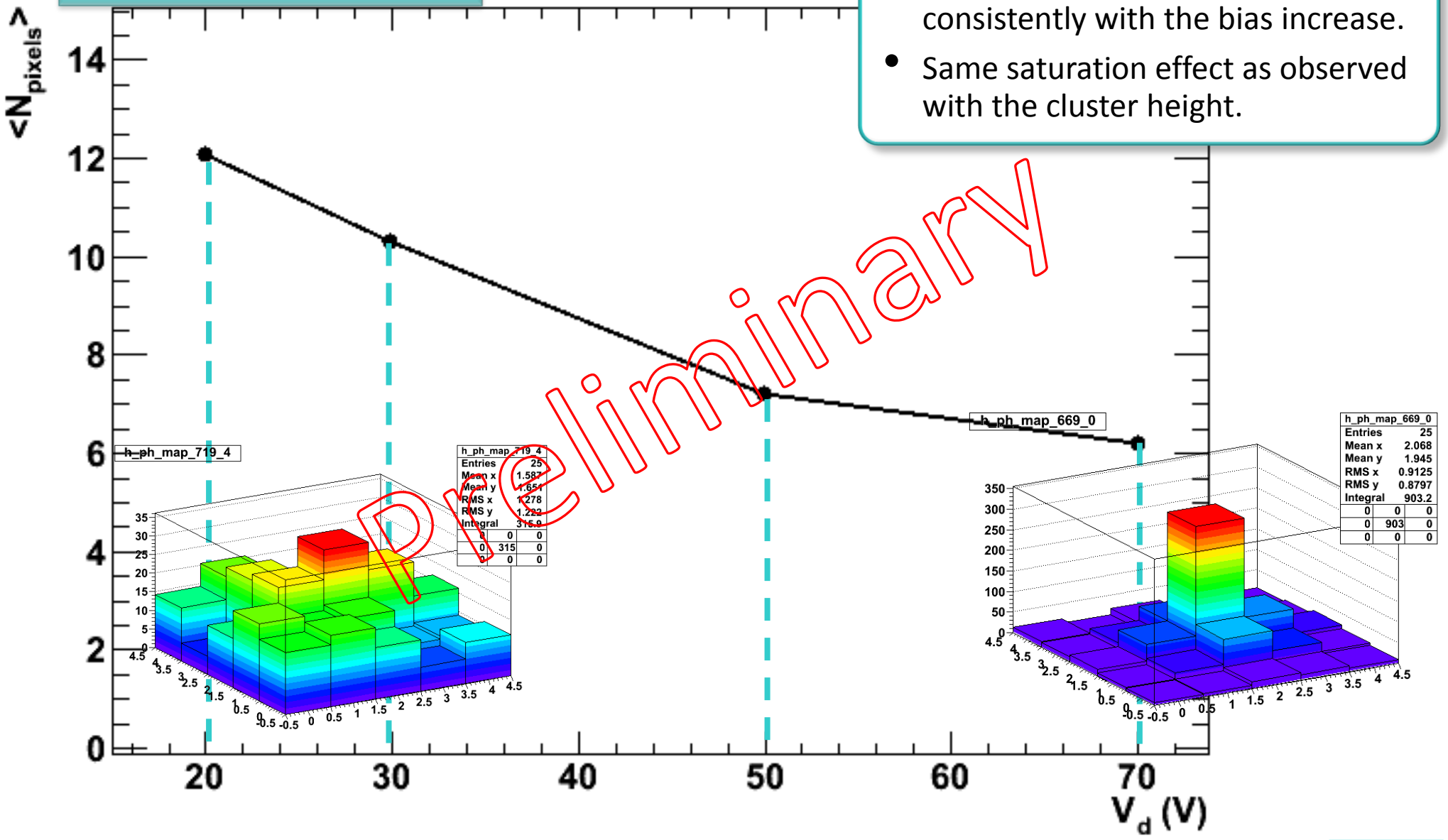
Test beam results – cluster pulse height



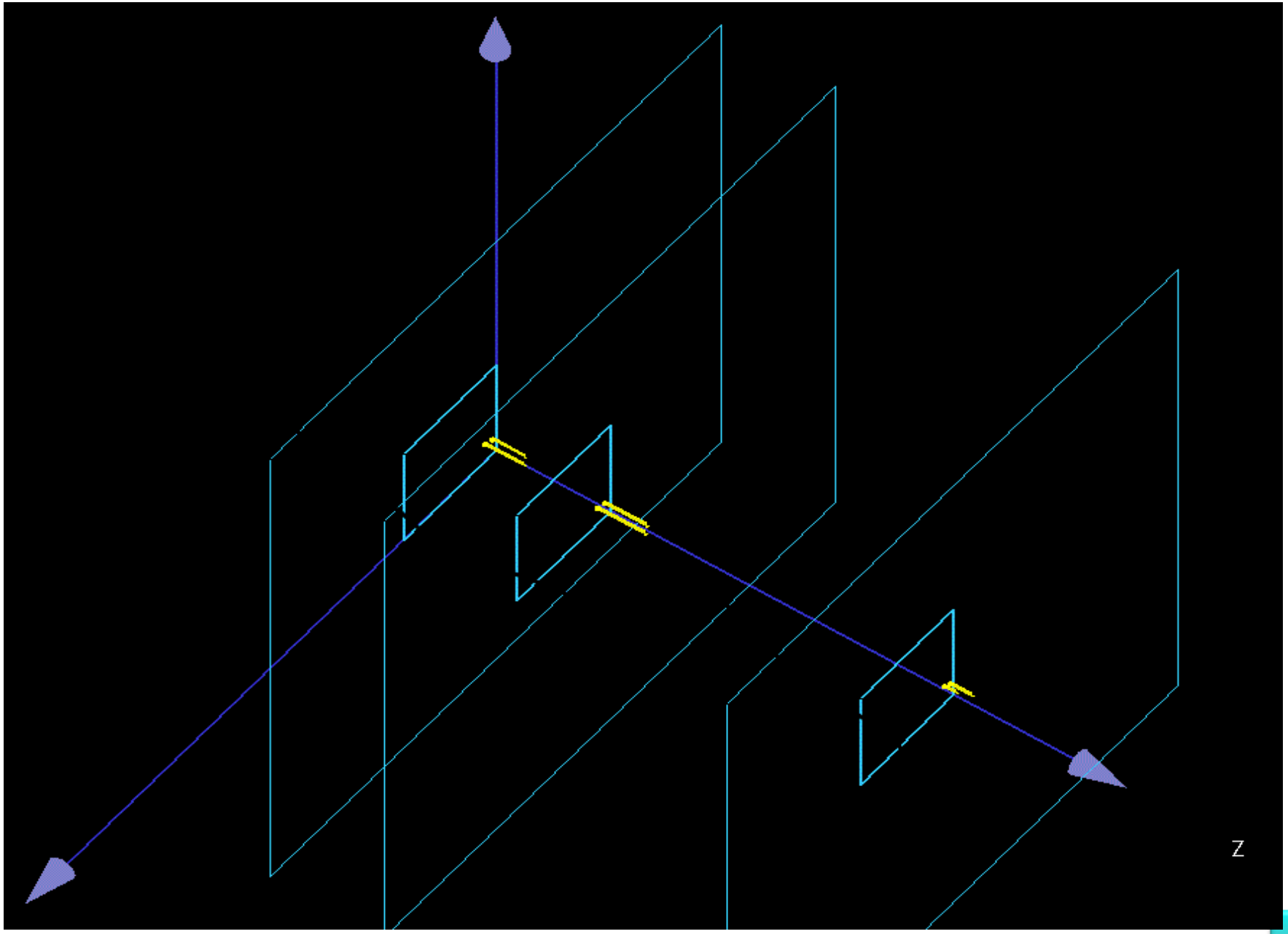
Test beam results – cluster multiplicity

Cluster multiplicity [pixels]

- Cluster multiplicity decreases consistently with the bias increase.
- Same saturation effect as observed with the cluster height.

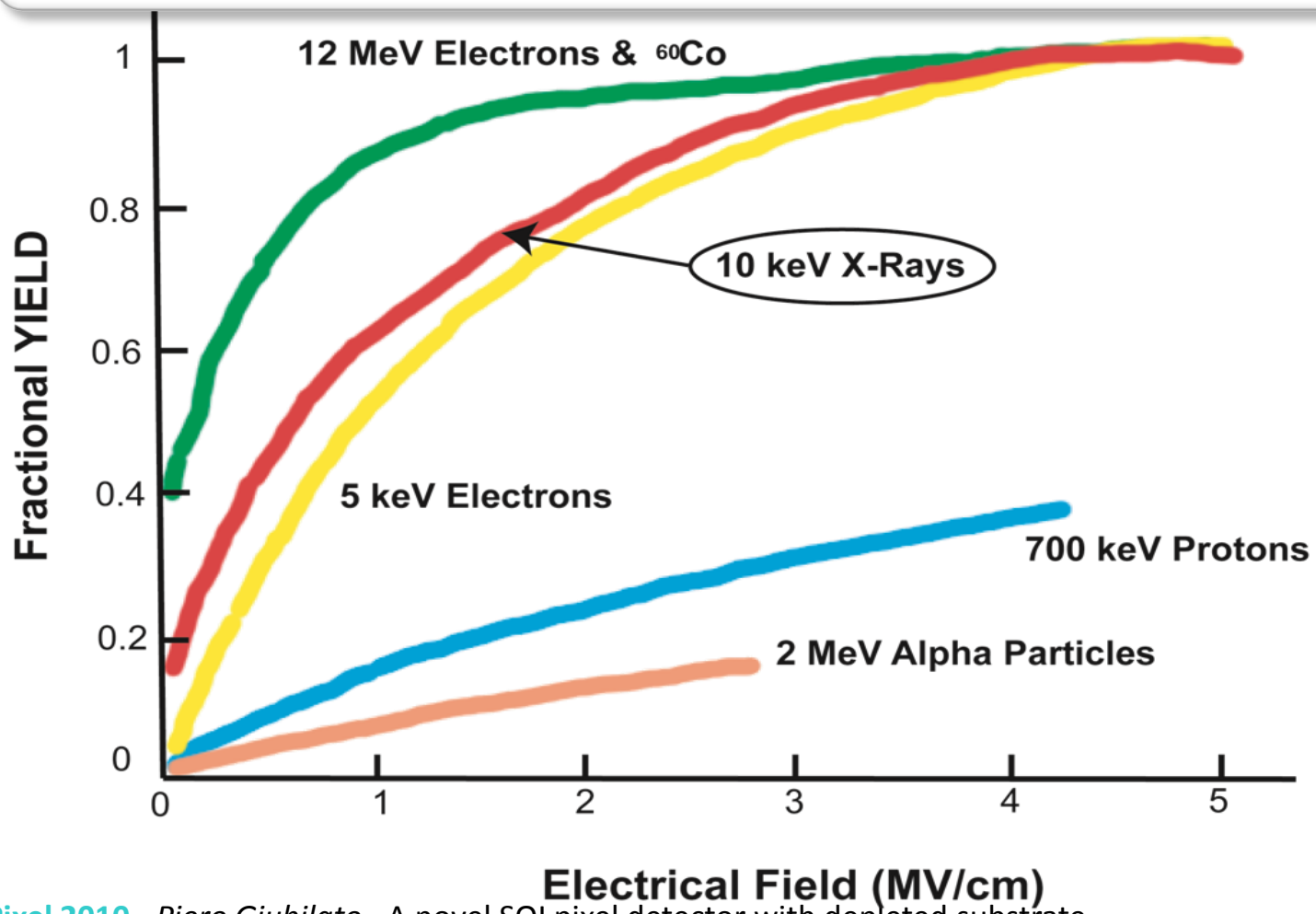


Test beam results – 3 planes tracking



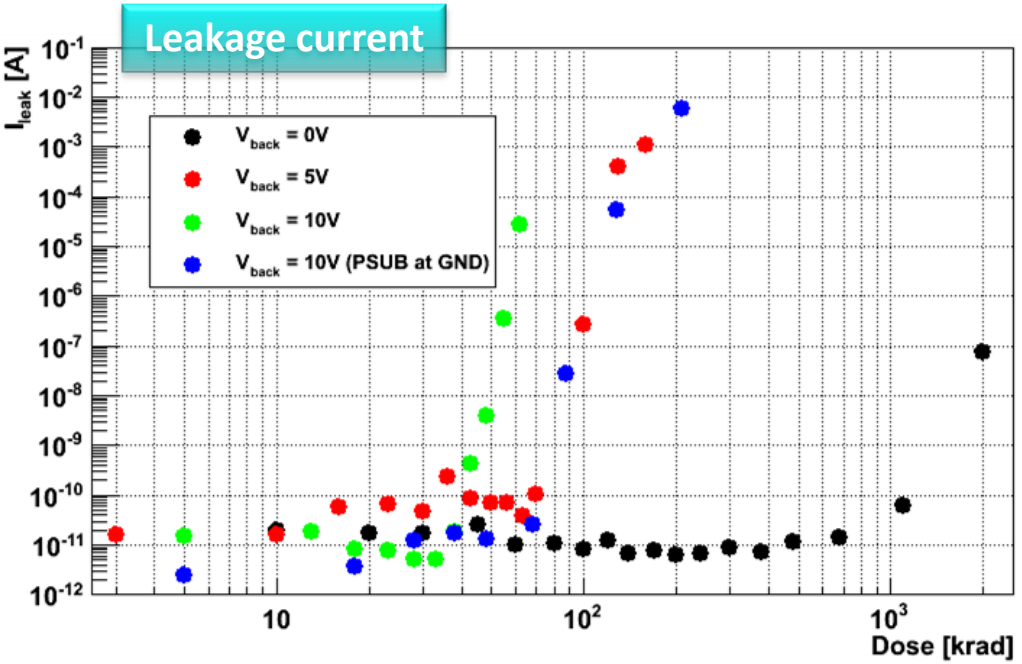
Total dose – fractional yield

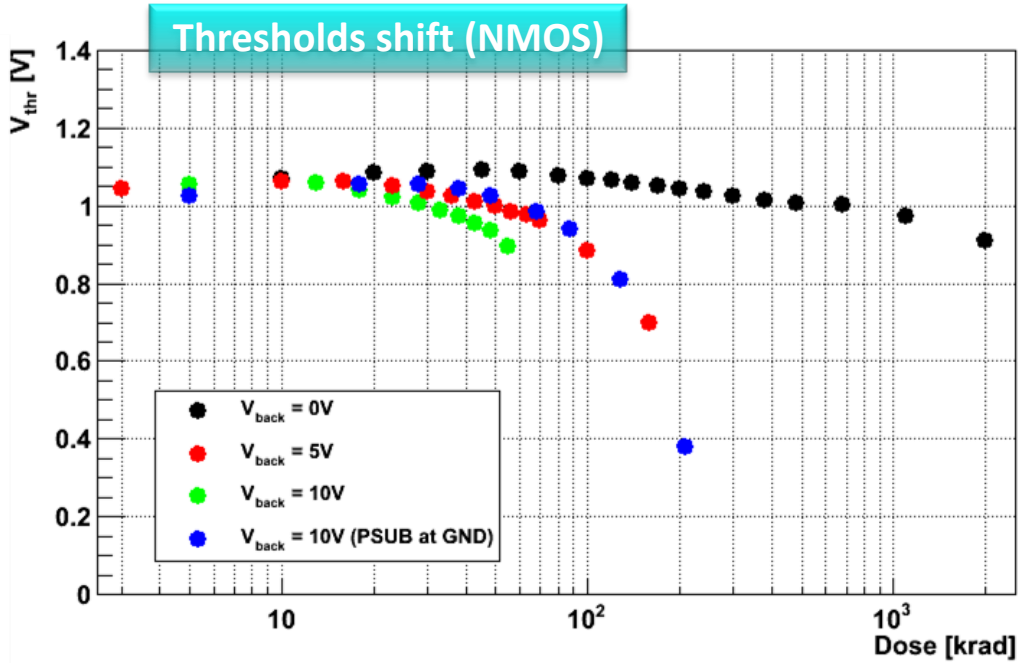
- In SOI technology, the thick buried oxide is expected to be sensitive to ionizing doses, which lead to positive charge trapping and consequently to an increase of the top-gate leakage current.
- This effect is even larger for depleted structures: the strong electrical field across the BOX splits the electron-holes pair generated by ionizing radiation, reducing the recombination yield. This greatly increases the amount positive charge which is trapped throughout the BOX → leakage current.



- The number of electron-hole pairs escaping recombination (fractional yield) strongly depends on the bias given to the substrate.
- It also depends on the stopping power of the incident particle (the lower the ionization density, the lower the recombination probability).

Total dose (10 keV XRay)– leakage current and thresholds shifts





The PSUB guard-ring tied at GND during irradiation indeed limits the electrical field through the BOX and improves the radiation hardness of the device.

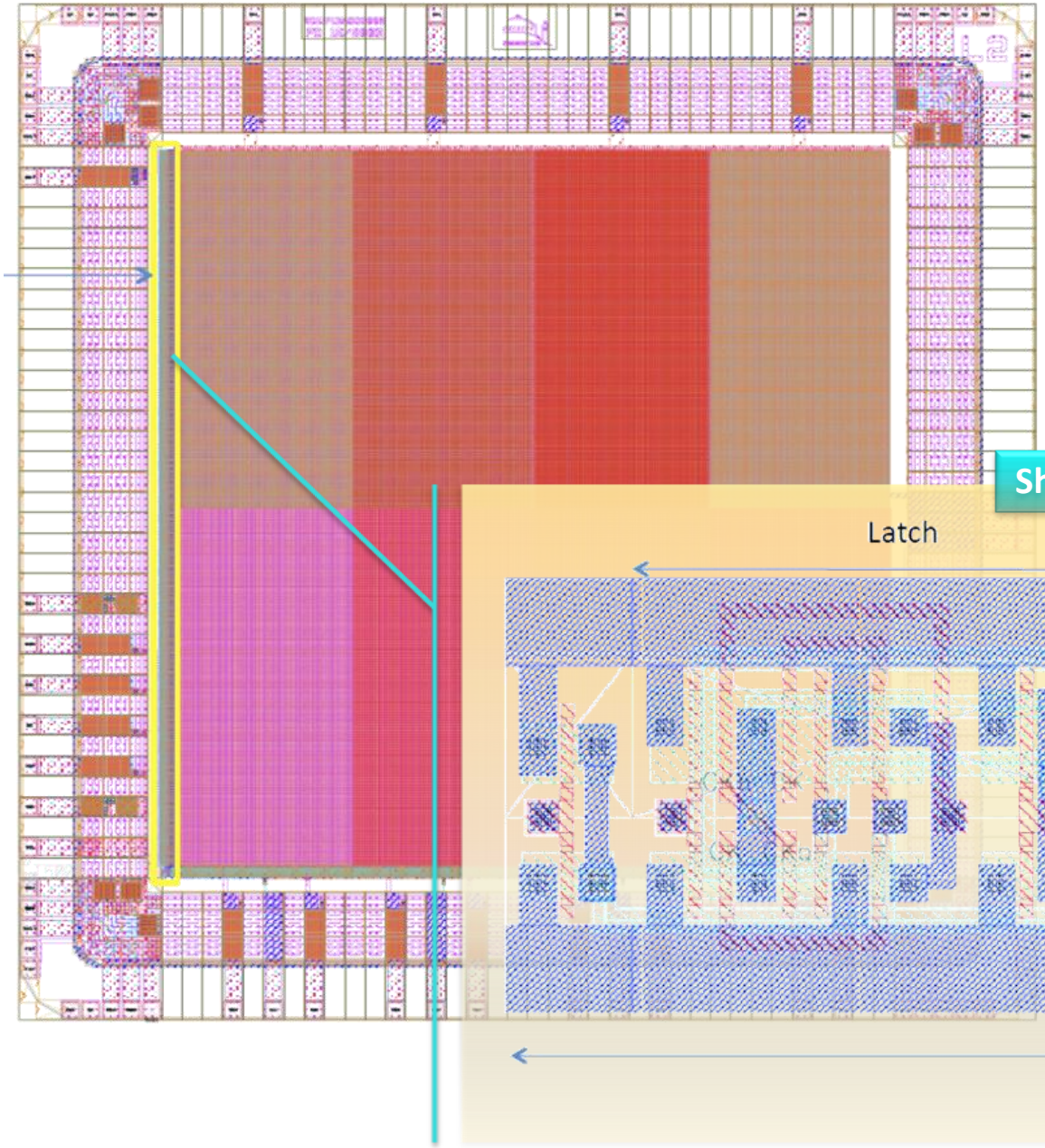
For V_{back} = 0V (no fractional yield) the transistor is still working properly up to doses of ~1Mrad

Provided to keep low the voltage under the BOX, technology can tolerate dose level up to ~1Mrad

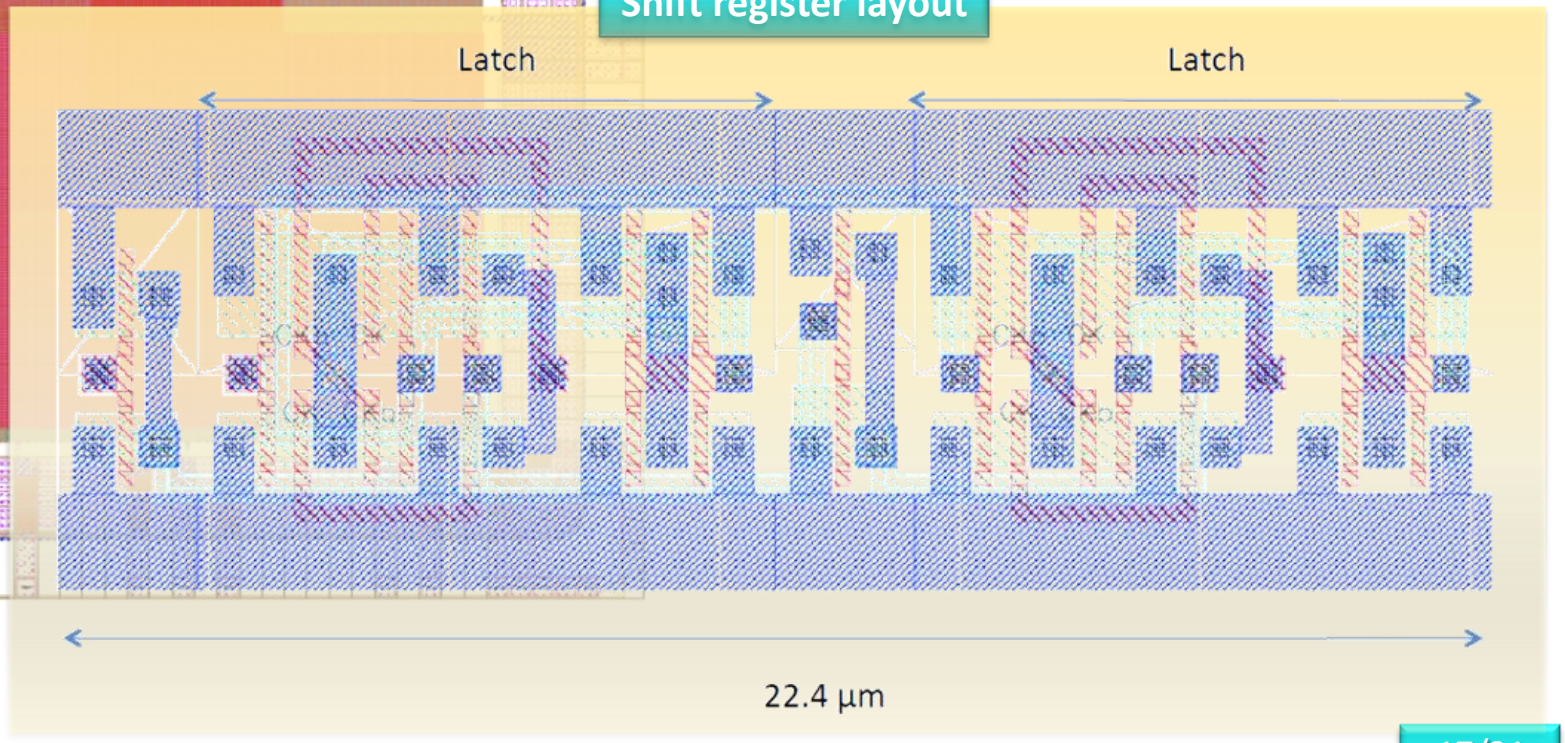
But this is exactly what the BPW provide → we need to test!

Single Event Upset (SEU) measurement

- We tested the technology for SEU sensitivity.
- Periphery row-selection shift register has been used to check for bit-flip through a dedicated test pad.
- Mind: the design is not hardened in any special way against SEU.



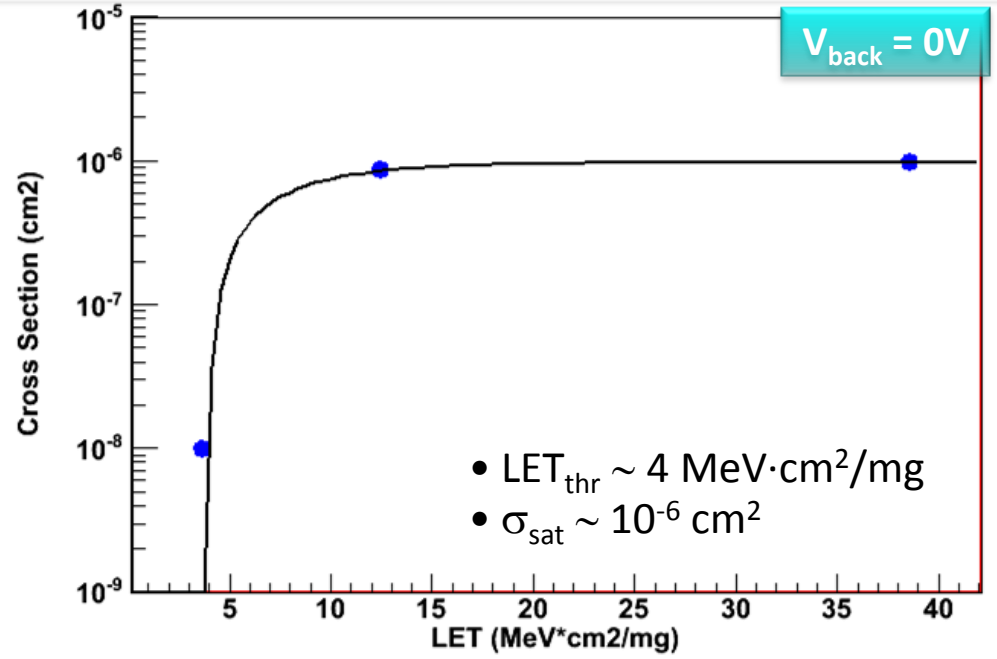
Shift register layout

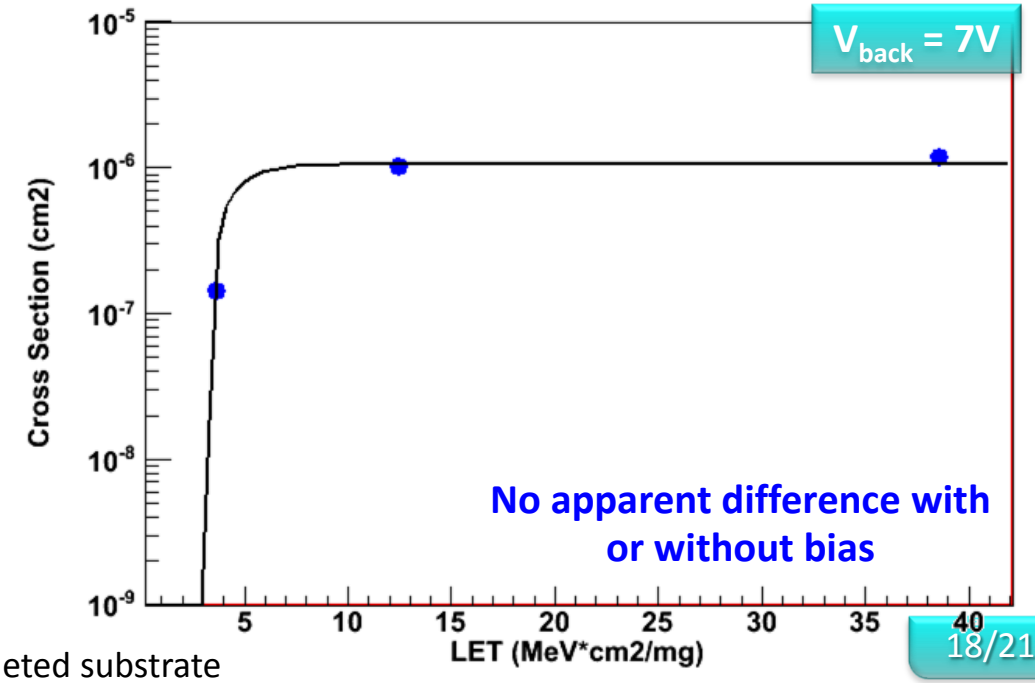


SEU - global cross section

- Single Event Upset (SEU) study performed at the **SIRAD irradiation facility,** LNL, Italy.
- A known logical pattern is written in and read back from the row selection shift register through dedicated pads during irradiation. Differences between the loaded and read-back pattern highlight a SEU occurred in the cells.
- Irradiation performed with three different ion species and, for each ion beam, for two substrate bias conditions (V_{back} = 0V - 7V).

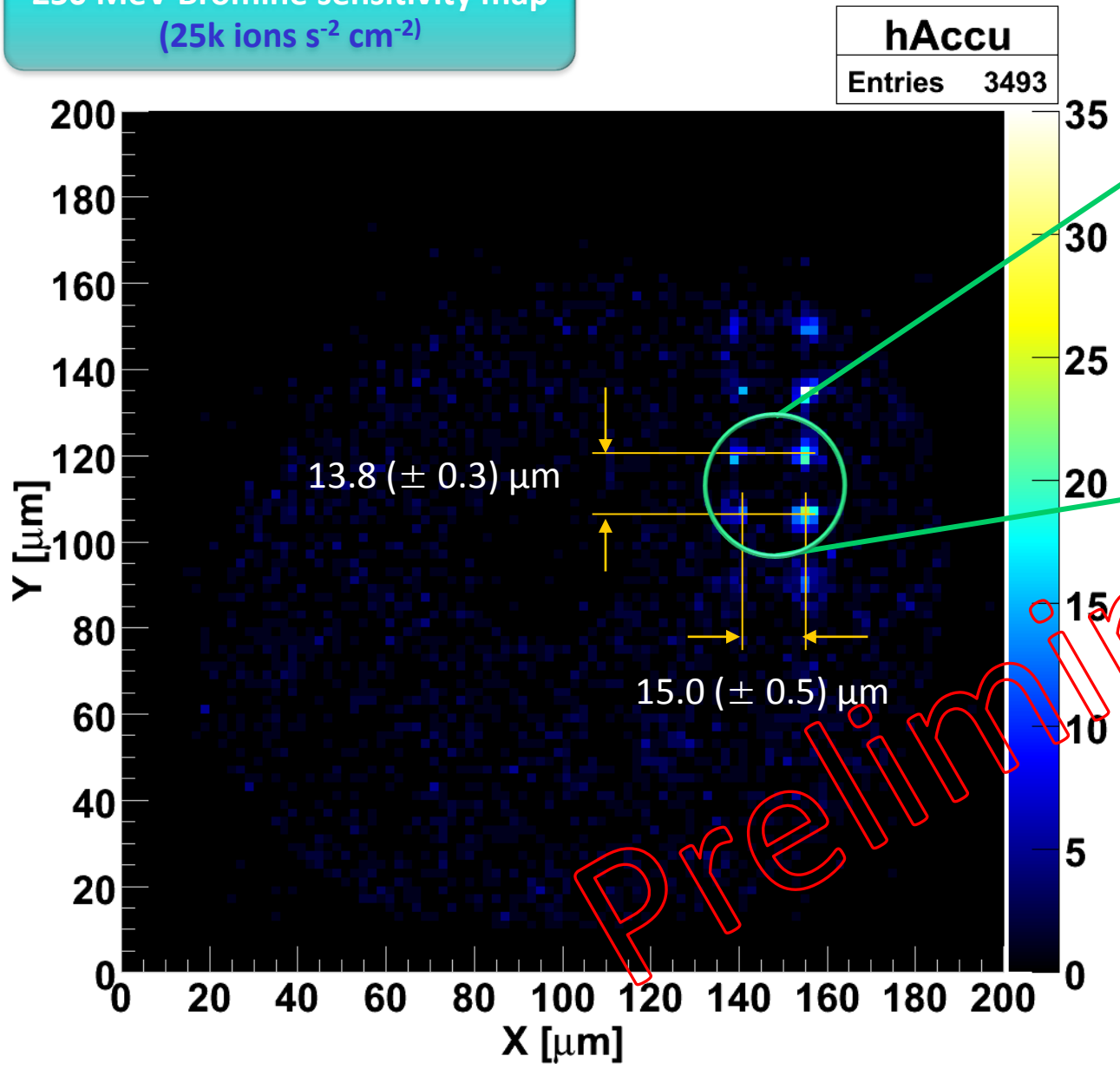
Ion	Energy [MeV]	LET in Si [Mev cm^2 mg^{-1}]
^{19}Fe	118	3.67
^{35}Cl	170	12.5
^{79}Br	240	38.6

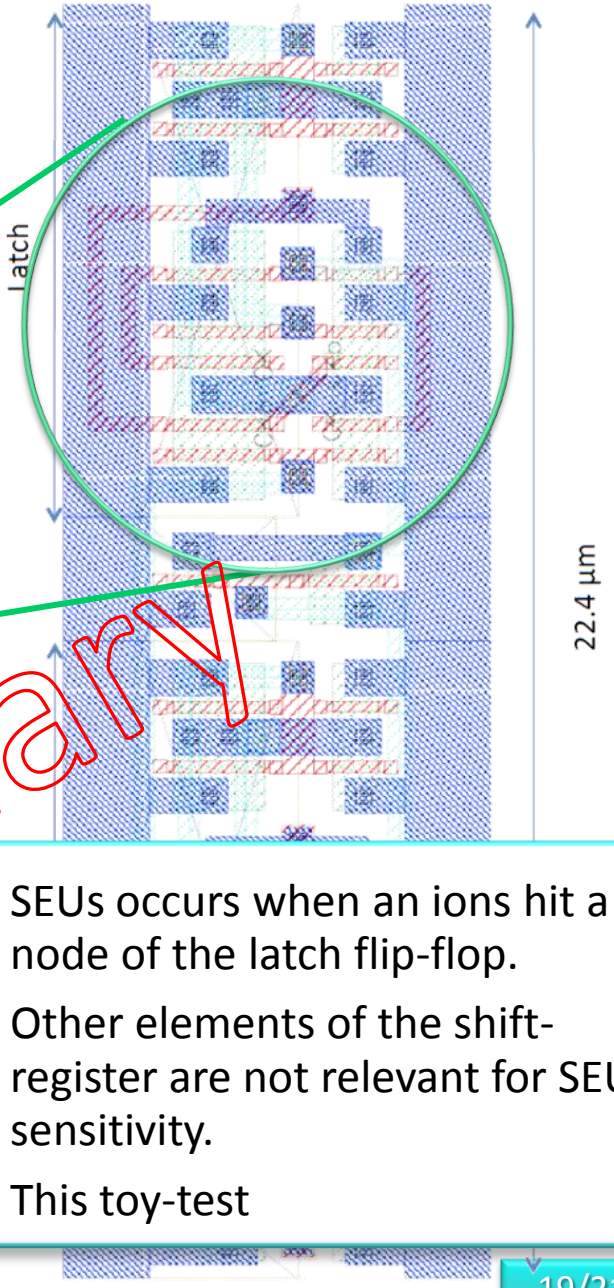




SEU - μmapping first results

250 MeV Bromine sensitivity map (25k ions s^{-2} cm^{-2})

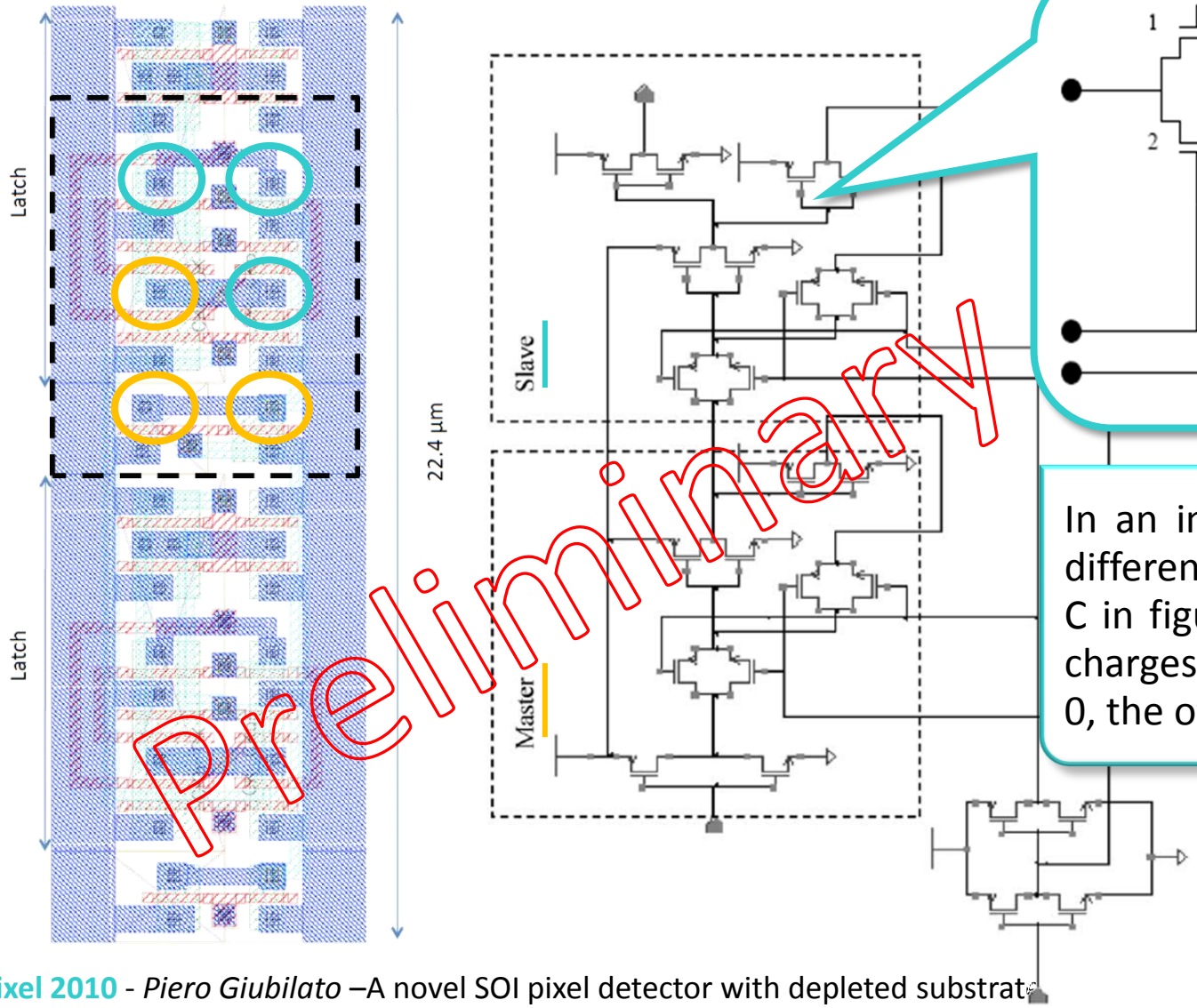


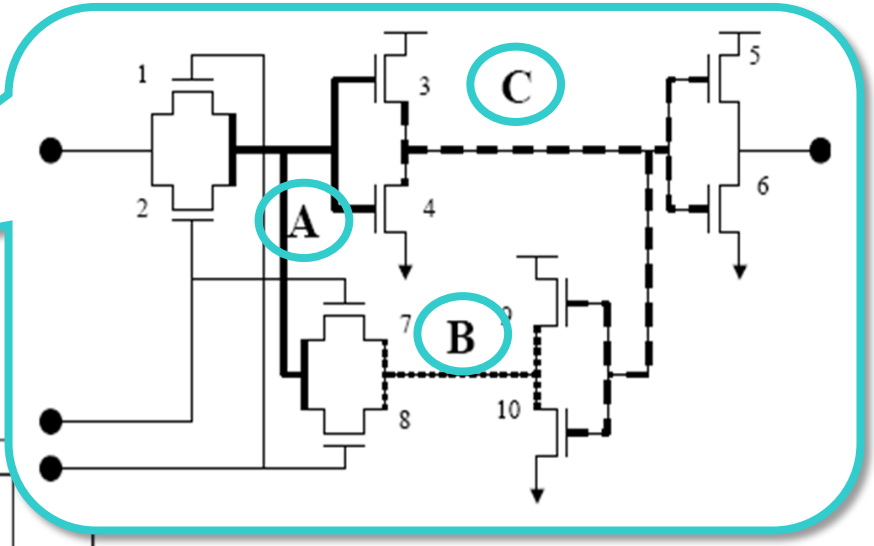


- SEUs occurs when an ions hit a node of the latch flip-flop.
- Other elements of the shift-register are not relevant for SEU sensitivity.
- This toy-test

SEU - μmapping, what we see

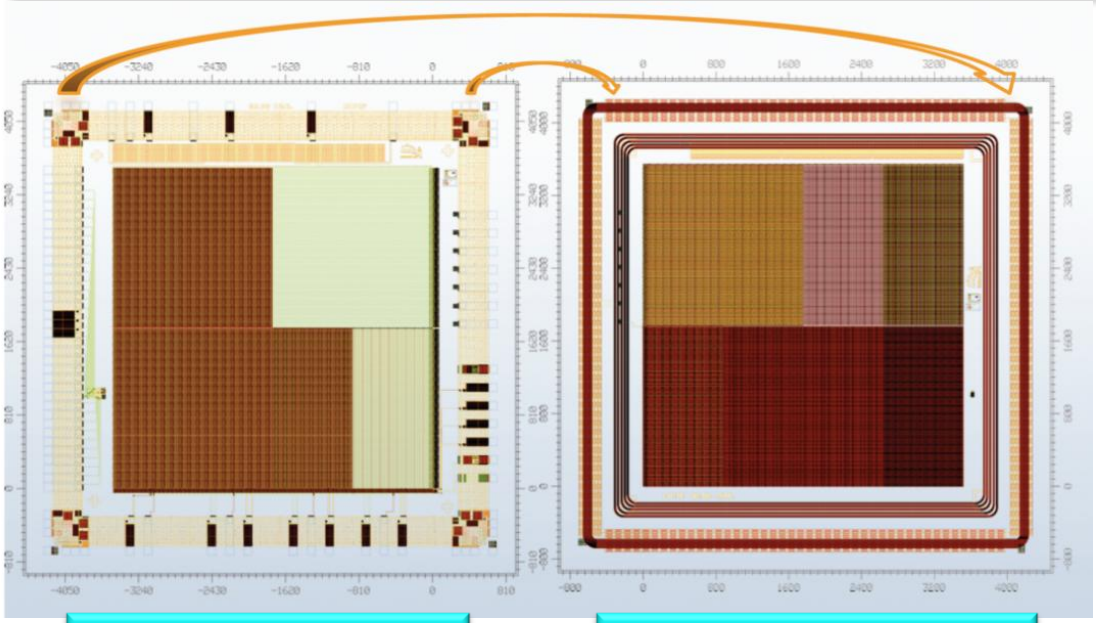
SEUs can be induced in both master and slave sections of each type of DFF, depending on whether the clock is high or low. Both master and slave of the DFF are two cross-coupled inverters with two transmission switches.





In an inverter structure we can find 3 different nodes sensible to SEUs (A, B e C in figure). Each node has two critical charges, one for the state transition 1–0, the other for 0–1.

Waiting in the pipeline… SOI-3D

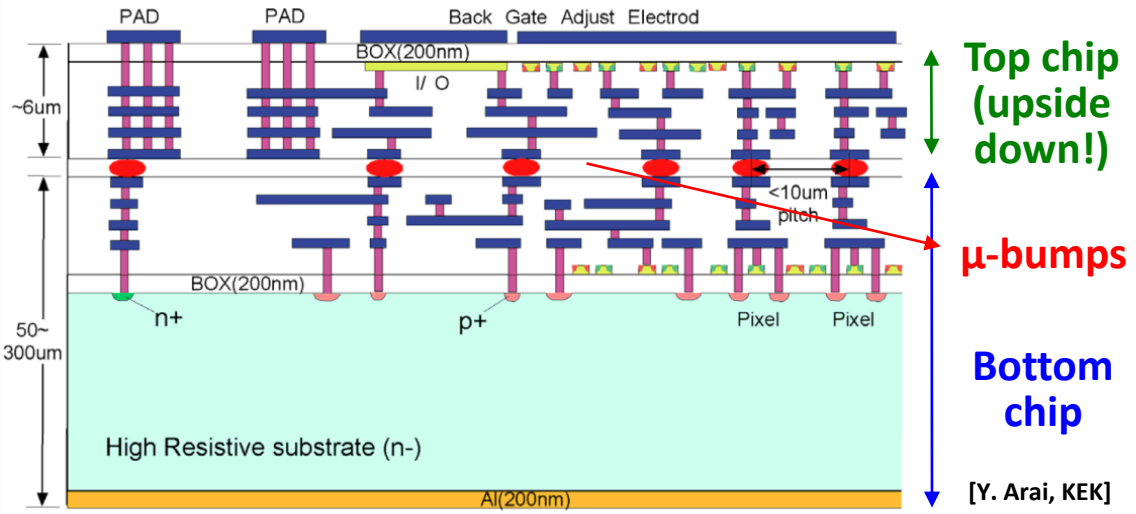


Top chip (readout)

Bottom chip (sensor)

- OKI 0.20 µm FD-SOI process (submitted 2009)
- Sensor chip with graded p-type guard-rings
- Readout chip to be wafer-bonded on top (ZyCube process)
- 256×256 analog pixels, 13.75 µm pitch, 4 parallel outputs
- 8 different pixel types, several test structures for process and interconnection evaluation

- 3D vertical integration process allows higher integration, improved radiation tolerance and lower power dissipation
- Vertical integration performed with ZyCube µ-bump bonding (~5 µm) technique
- After chip stacking, Si etching and pad lithography on back of top chip
- Process under way, chips waiting...

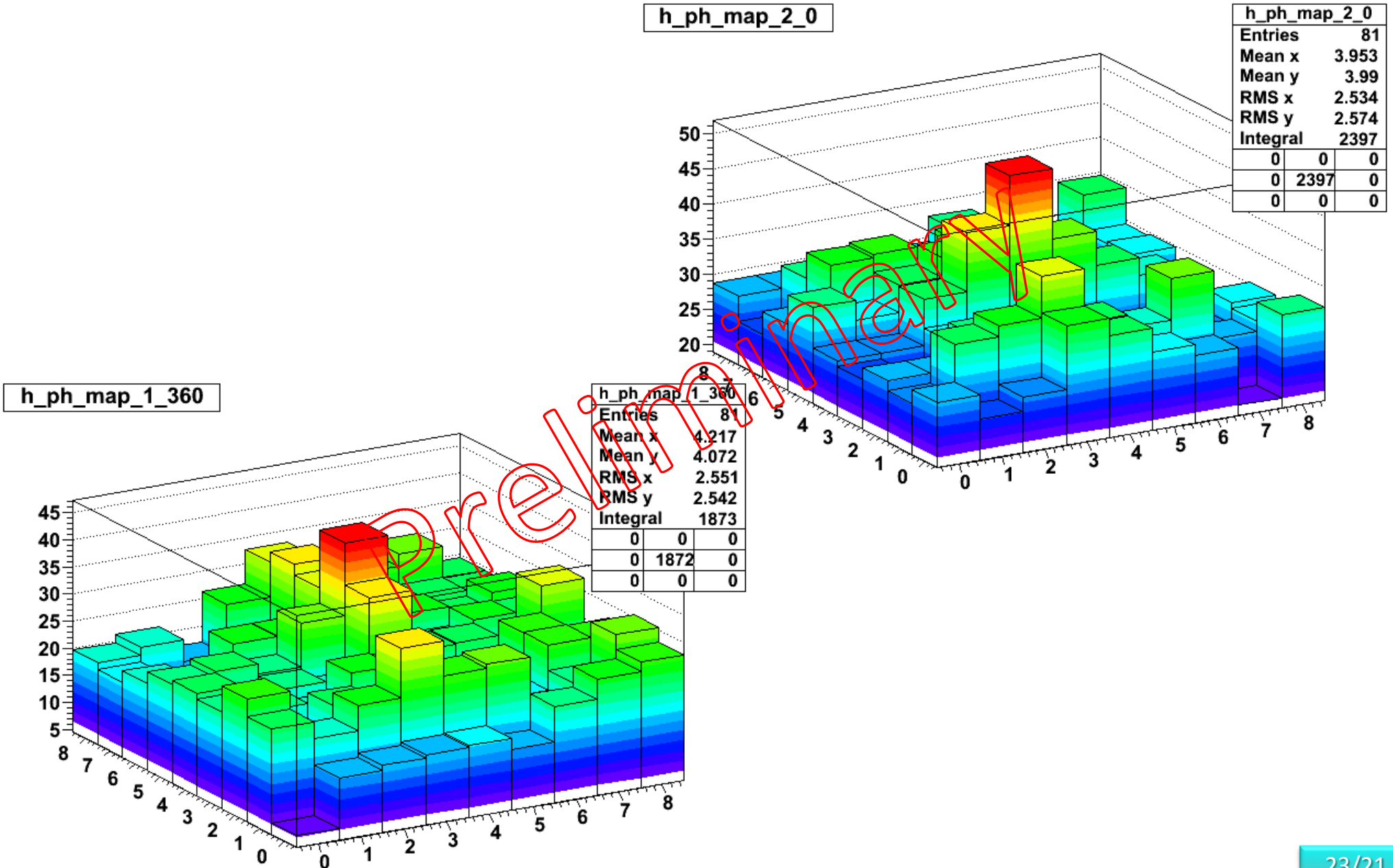


Conclusions

- Detectors play well in test beam
- It seems possible to improve radiation tolerance for total dose up to 1 Mrad
- PBW implant works well, freeing room (when compared to traditional guard ring) for more transistors to be packed in a single pixel

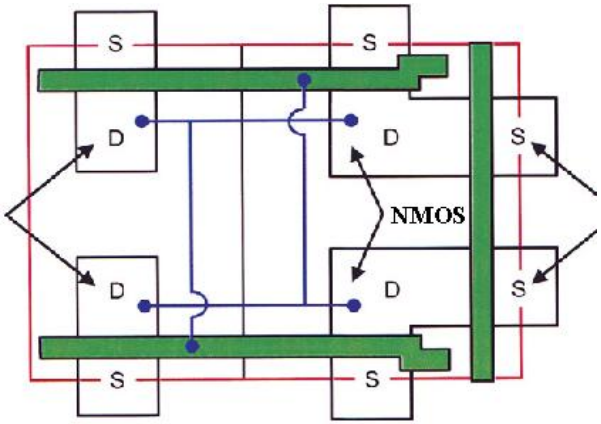
- Still waiting for the 3D chip…
- With an established pixel structure, we have to plan for a complete chip with some realistic features like periphery memory, ADCs, time-stamping… (not necessarily together on the same chip!)
- SEU tolerance still an issue for any application where it is a concern, needs to be investigated and in case addressed in future designs.

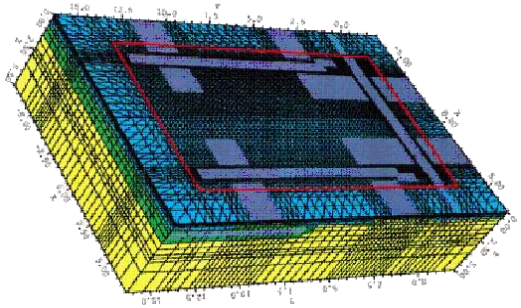
Test beam results – cluster shapes



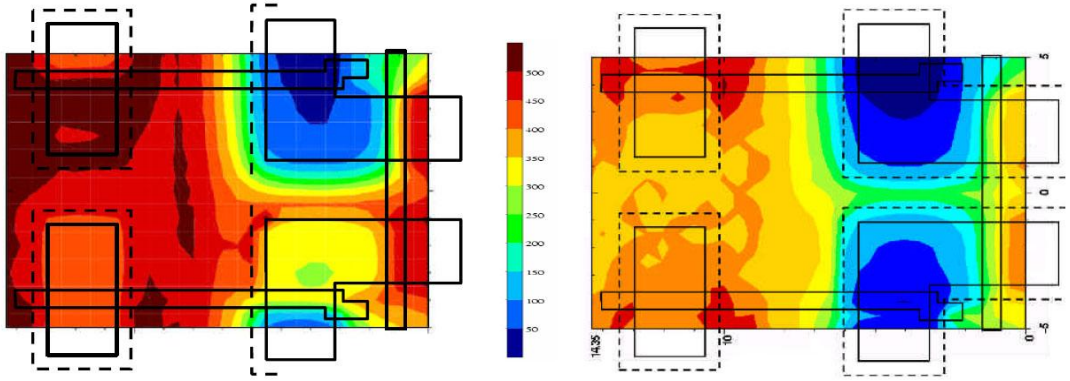
Look at this famous example:

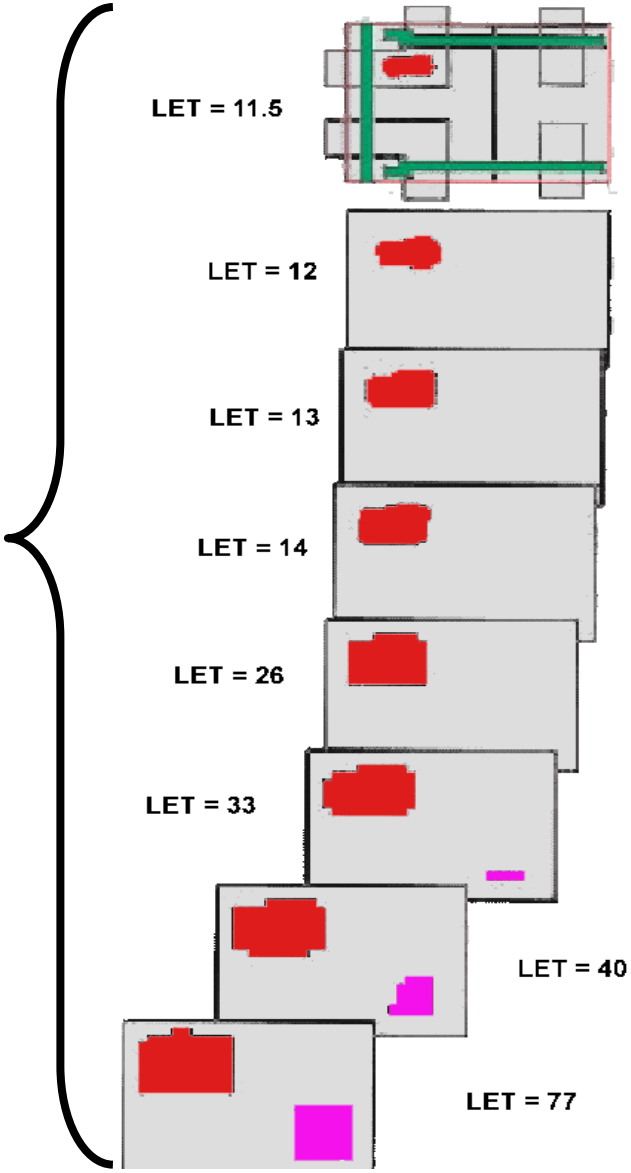
- By increasing the impinging ion energies is possible to discover that some areas of the device become sensible to radiation only over a precise LET threshold.
- These sensible areas are precisely defined inside the device volume, and every one has its own LET threshold level.





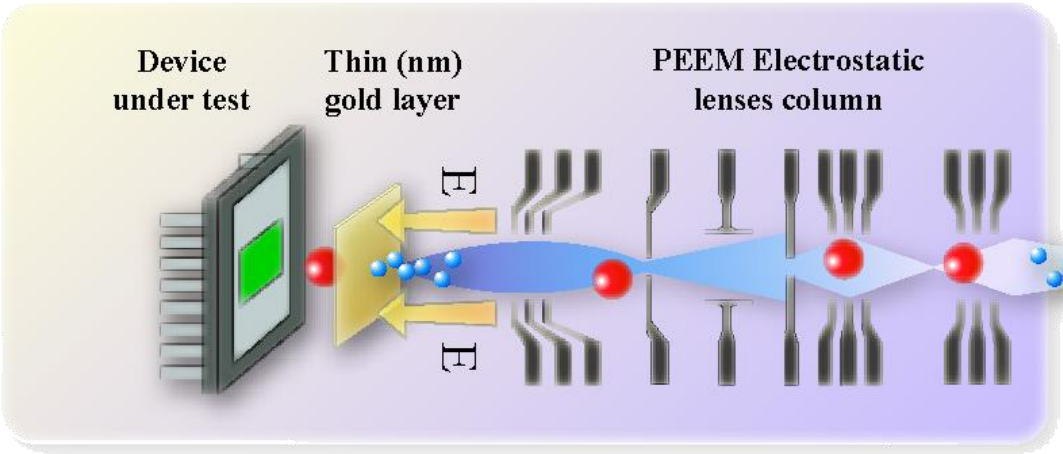
CMOS 256K SRAM
Unit cell SEU simulation
(9 days on 32 nodes SIBERIA)



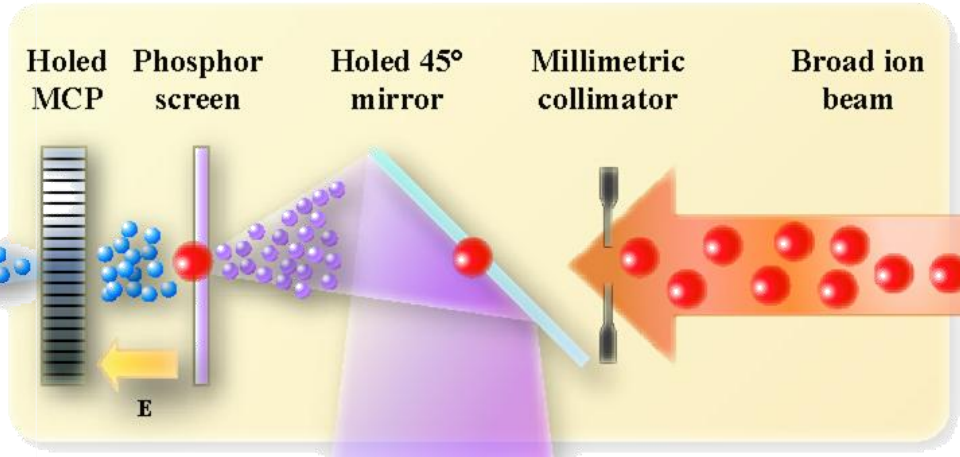


The IEEM technique for SEU μmapping

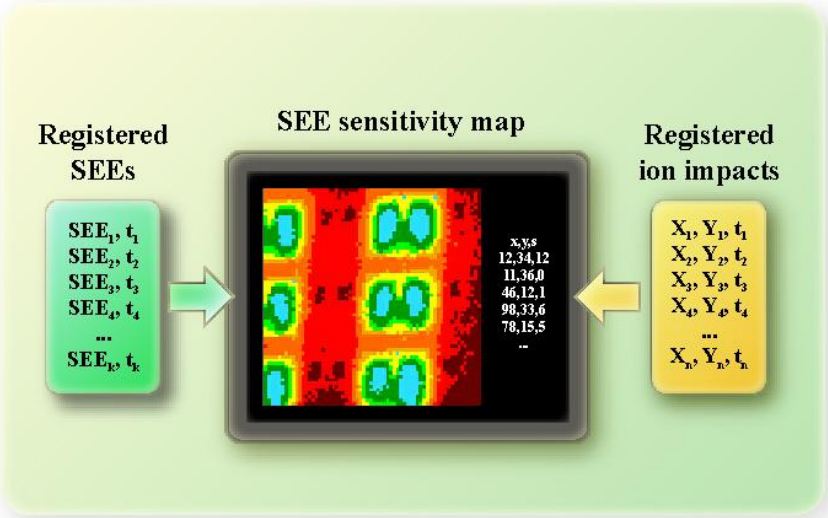
1 Electrons imaging



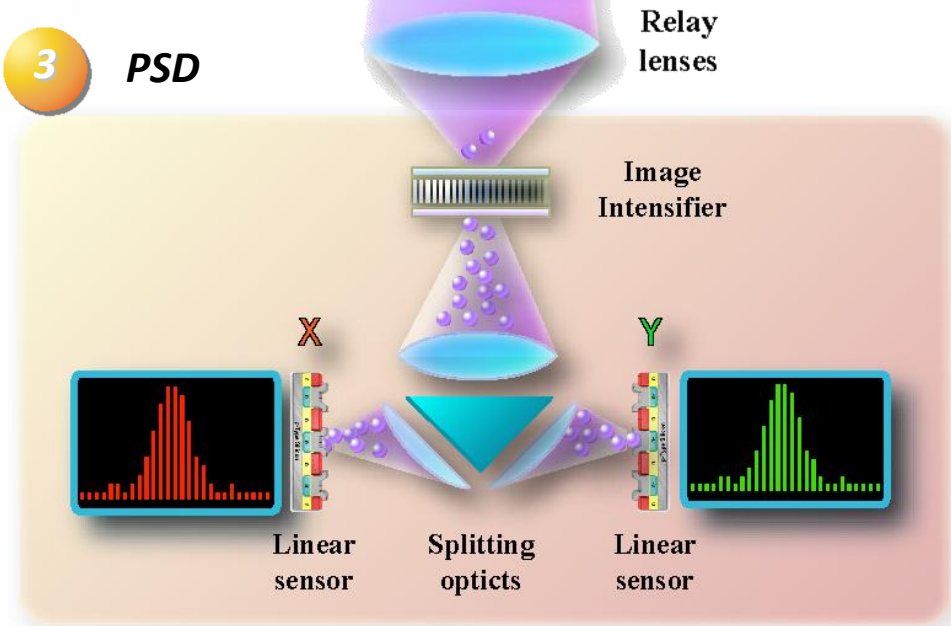
2 Electrons to photons



4 Data acquisition



3 PSD



The IEEM system for SEU μmapping