# Thin Pixel Development for the SuperB Silicon Vertex Tracker

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*on behalf of SuperB group*

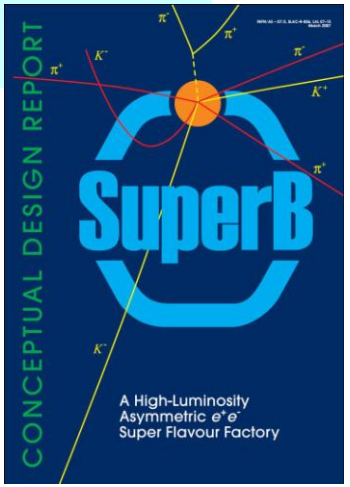
# Outline

- The SuperB Project
- The Silicon Vertex Tracker
- Layer0 Options for Technical Design Report
  - Deep N-Well CMOS MAPS
  - Hybrid Pixels
- Exploiting Vertical Integration for Layer0
- Conclusions

# The SuperB Project

- The physics case for a high luminosity B Factory is clearly established.
  - Flavour physics is rich, promises sensitivity to New Physics … but large statistics (50-100 $ab^{-1}$) is needed
- First generation of B-Factories (PEP-II and KEKB) exceeded their design goals ($\mathscr{L}$~1.2-1.7 x$10^{34}$ $cm^{-2}$ $s^{-1}$ , integrated 1.2 $ab^{-1}$) but an upgrade of ~2 orders of magnitude in $\mathscr{L}$ is needed to get 50$ab^{-1}$ .
- Increasing Luminosity by brute-force (higher currents) is expensive and difficult
  - wall plug power and detector background explosion
  - effective limitation around 5x$10^{35}$ $cm^{-2}$ $s^{-1}$
- The SuperB italian accelerator concept allows to reach $\mathscr{L}$=$10^{36}$ $cm^{-2}$ $s^{-1}$ with moderate beam current (2A) using very small beam size (~1/100 of present B-Factories beams exploiting the ILC R&D on damping rings & final focus) with the help of the Crab Waist scheme at the IP to keep the beams small & stable after collision (verified with tests on Dafne)
- This approach allows to (re-) use parts of existing detectors and machine components.

# The SuperB Process

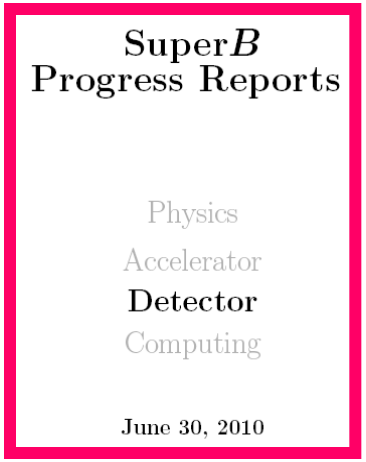



- SuperB Conceptual Design Report published in 2007
- All scientific reviews are positive. Presented to CERN Council and approved for preparatory phase.
- Growing international interest and participation with formal international collaboration being formed. Project structure defined.

➔ MOUs signed with France, Russia and SLAC and a letter of support from Canada.

- Technical Design Report phase approved by INFN in 2009
- R&D is proceeding on various items (eg. SVT Layer0)
- Intermediate Progress Report published this summer
  - http://arxiv.org/abs/1007.4241

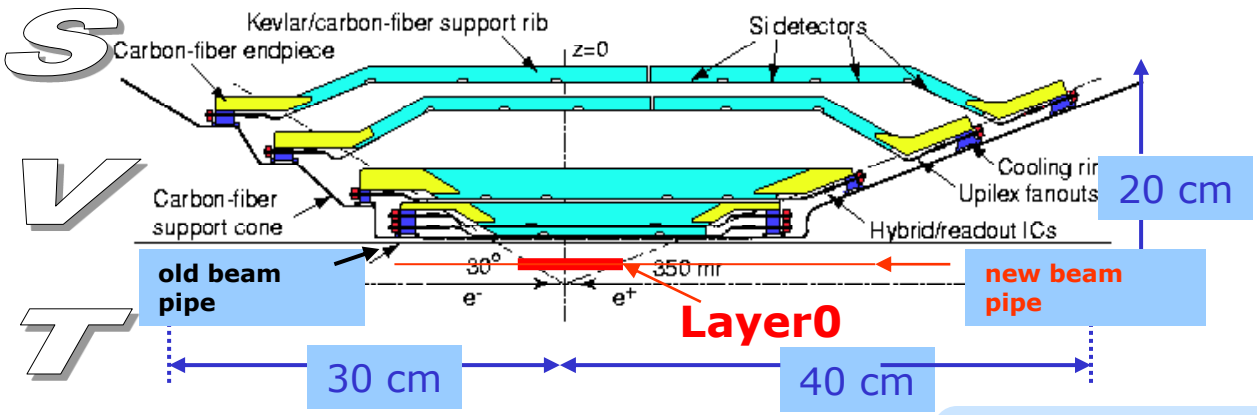
➔ SuperB inserted as first project in the National Research Plan by the Italian Research Ministry




## NEXT STEPS

- Government approval expected very soon
- Technical Design Report: summer 2011
- Operation by 2015.

# The SuperB Silicon Vertex Tracker

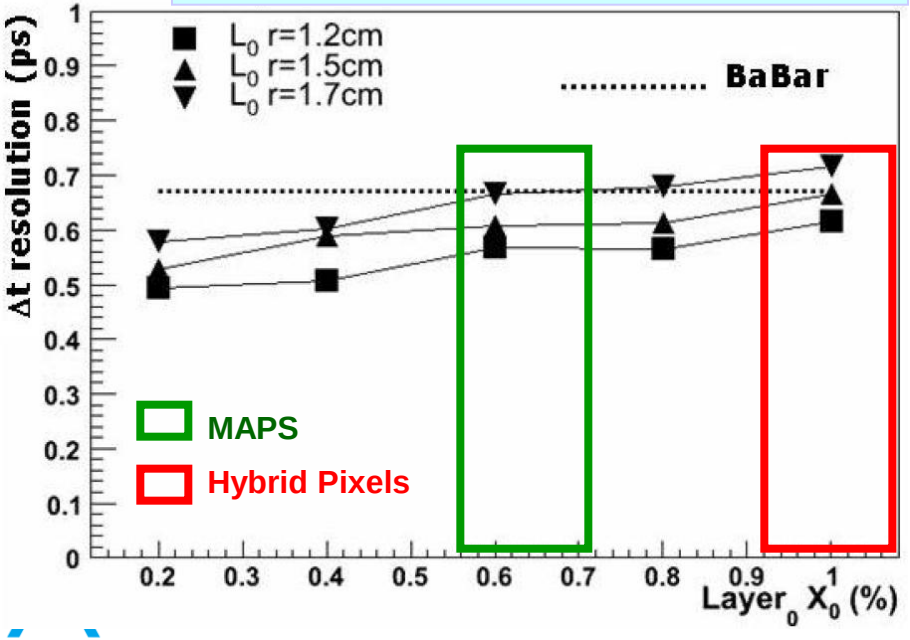



**BaBar SVT**

- 5 Layers of double-sided Si strip sensor
- Low-mass design. ($P_t$ < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15μm at normal incidence

SuperB SVT based on Babar SVT design for R>3cm. BUT:

B→π π decay mode, βγ=0.28, beam pipe X/X0=0.42%, hit resolution =10 μm




1) reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) requires an improved vertex resolution (~factor 2)
   - Layer0 very close to IP (@1.5 cm) with low material budget (<1% $X_0$) and fine granularity (50 μm pitch)
   - Layer0 area 100 $cm^2$

2) bkg levels depend steeply on radius
   - Layer0 needs to be fast and rad hard (>20x5 MHz/$cm^2$, >3x5 MRad/yr)

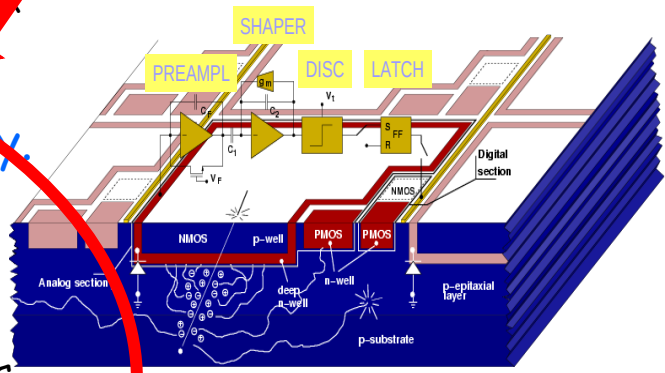
# SuperB SVT Layer 0 technology options

- Striplets option: mature technology, not so robust

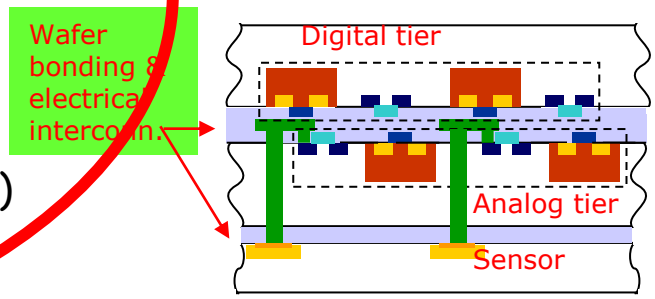
## 2D MAPS and 3D pixels are the two most advanced options considered for Layer0 upgrade:


- Reduction of front-end pitch to 50x50 μm²
- → Produced and tested FE prototype chip with 50x50 μm² pitch & fast data push readout (already developed for DNW MAPS) - (4k pixels, ST 130 nm)

- CMOS MAPS option: new & challenging technology.
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-INFN Collaboration) on
    - Deep N-well devices 50x50μm² with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS (4k pixels) successfully tested with beams.

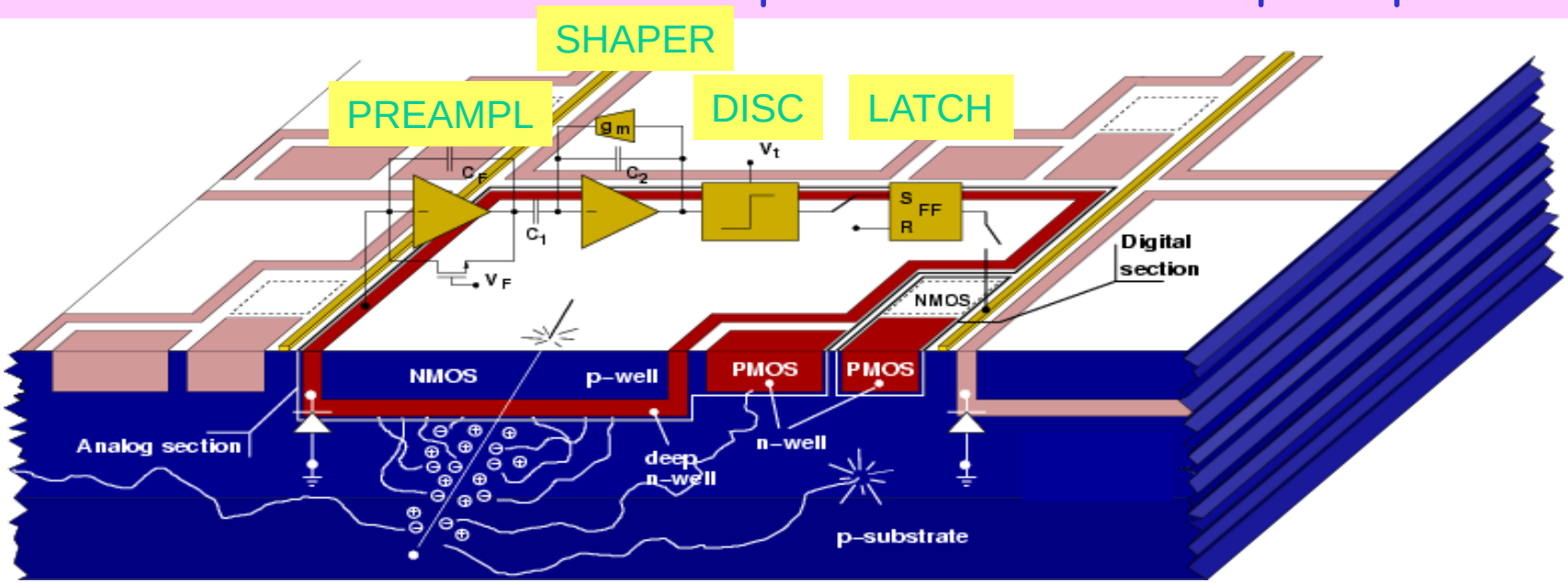



- Thin pixels with Vertical Integration: **reduction of material and improved performance.**
  - Two options are being pursued (VIPIX – INFN Collab.)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor



# Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential




A classical optimum signal processing chain for capacitive detectors can be implemented at pixel level:

- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss due to competitive N-wells where PMOSFETs are located
- Need to keep the fill factor (DNW/tot N-well ) as high as possible: ~ 90% in our design.

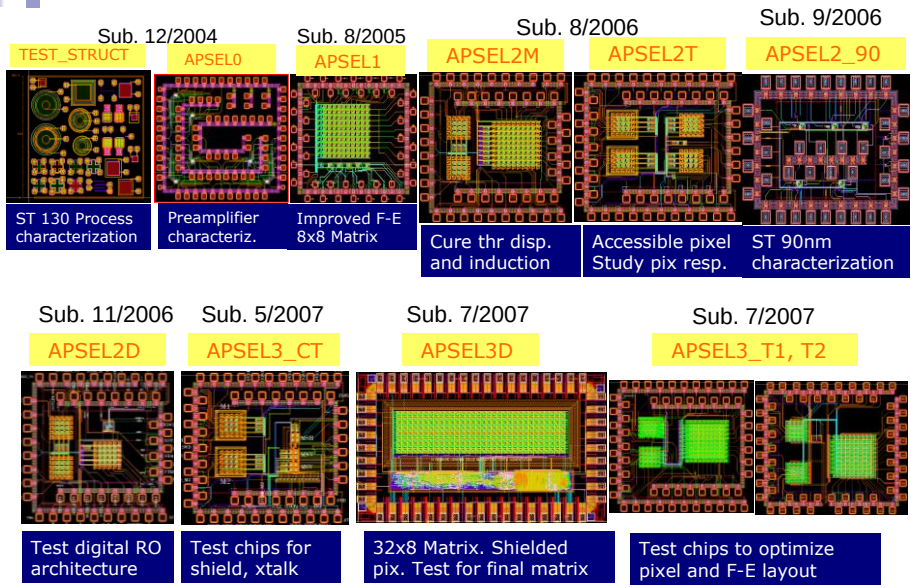
# DNW MAPS R&D

SLIM5 Co

**IC group contribution:**
- Pavia (PV)-Bergamo(BG) analog front-end
- Pisa(PI)-PV-BG in pixel digital logic
- Bologna-PI digital readout architecture

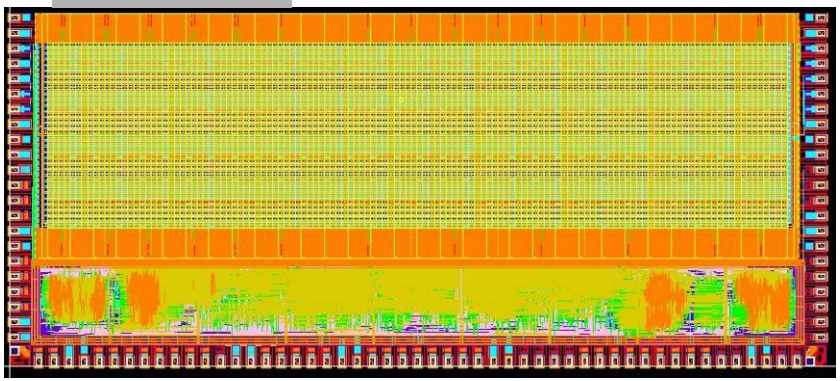
- **Implemented in ST 130 nm process**
- Proof of principle (APSEL0-2)
  - first prototypes realized in 130 nm triple-well ST-Micro CMOS process
- APSEL3
  - 32x8 matrix with sparsified readout
  - Pixel cell optimization (50x50 um$^2$)
    - Increase S/N (15→30)
    - reduce power dissipation x2
- **APSEL4D**: 4K(32x128) 50x50 μm$^2$ matrix
  - data-driven sparsified readout + timestamp
  - Pixel cell & matrix implemented with full custom design and layout
  - Sparsifying logic synthetized in std-cell from VHDL model
  - Periphery inlcudes a "dummy matrix" used as digital matrix emulator
- **Beam tests:**
  - 2008 - APSEL4D MAPS matrix + striplets
  - 2009 - MAPS structures with analog output & irrdiated devices
- **Radiation tests:**
  - Irradiation with $^{60}$Co γ up to 10MRad
  - Irradiation with neutrons under way

## Submitted MAPS Chips






APSEL4D sub 11/2007- rec 3/2008

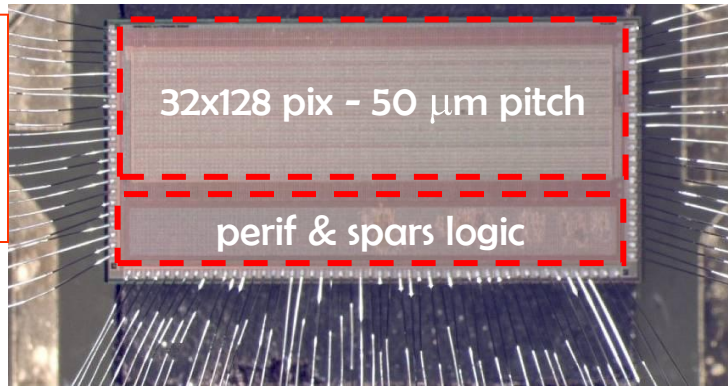


32x128 4k pixel matrix for beam test

# APSEL4D

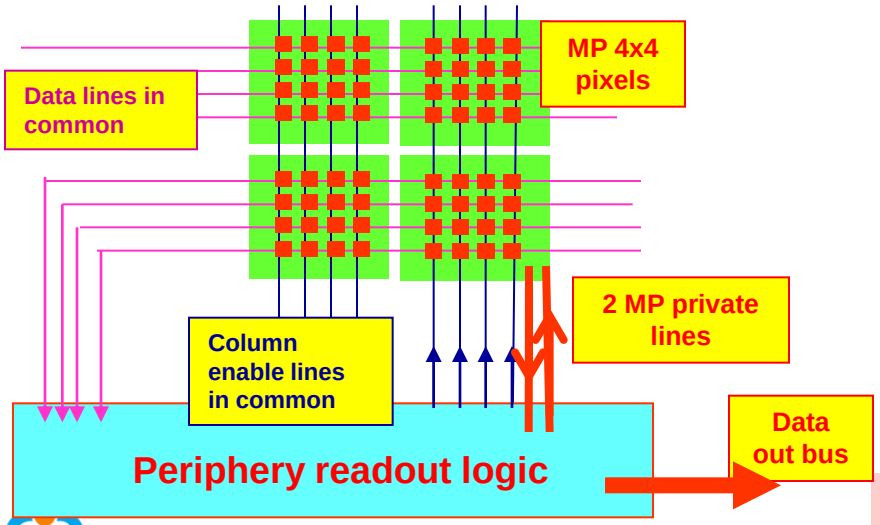
In the active sensor area we minimized:

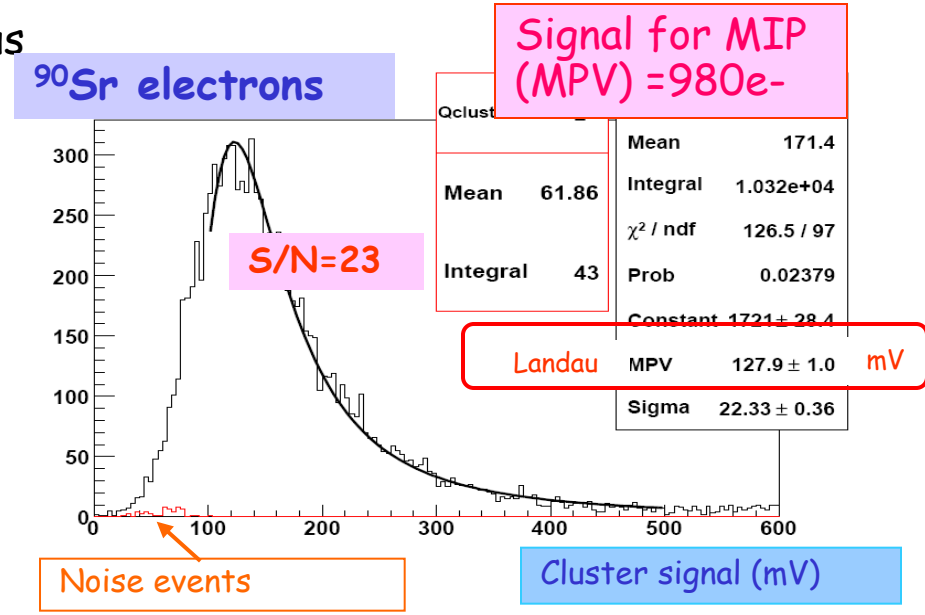
- logical blocks with PMOS to reduce the area of competitive n-wells
- digital lines for point to point connections to allow scalability of the architecture with matrix dimensions




- 4K(32x128) 50x50 μm² matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:
  - Register hit MP & store timestamp
  - Enable MP readout
  - Receive, sparsify, format data to output bus

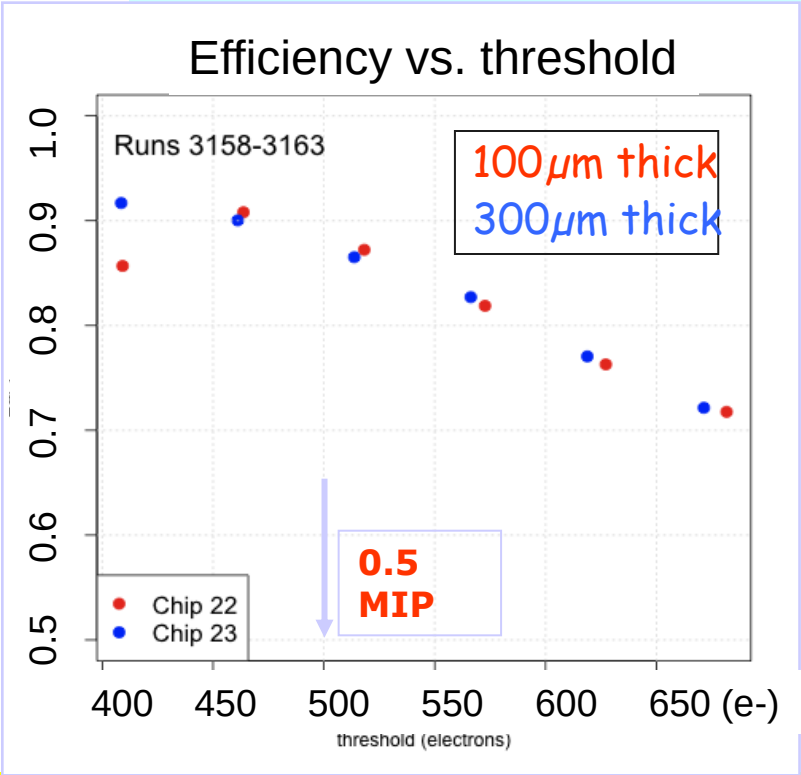
- S/N ~ 20 with power consumption ~ 30 μW/ch




Threshold dispersion = 60 e-  Gain = 860 mV/fC

# DNW MAPS Hit Efficiency measured in a CERN beam test (APSEL4D)

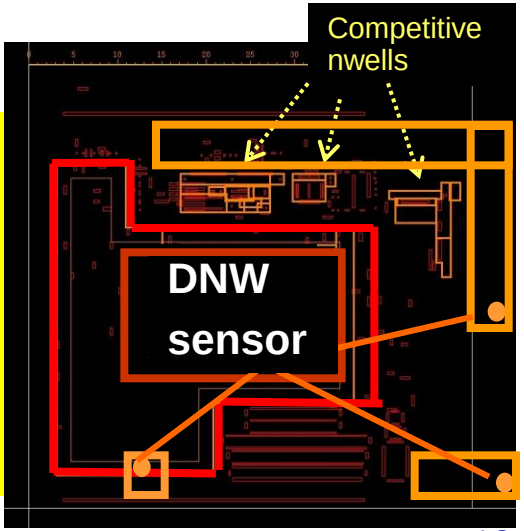



Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

- MAPS hit efficiency up to 92 % @ 400 e- thr.
- 300 and 100 μm thick chips give similar results
- Intrinsic resolution ~ 14 μm compatible with digital readout.

- Test Beam results in: *S. Bettarini, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.08.026*

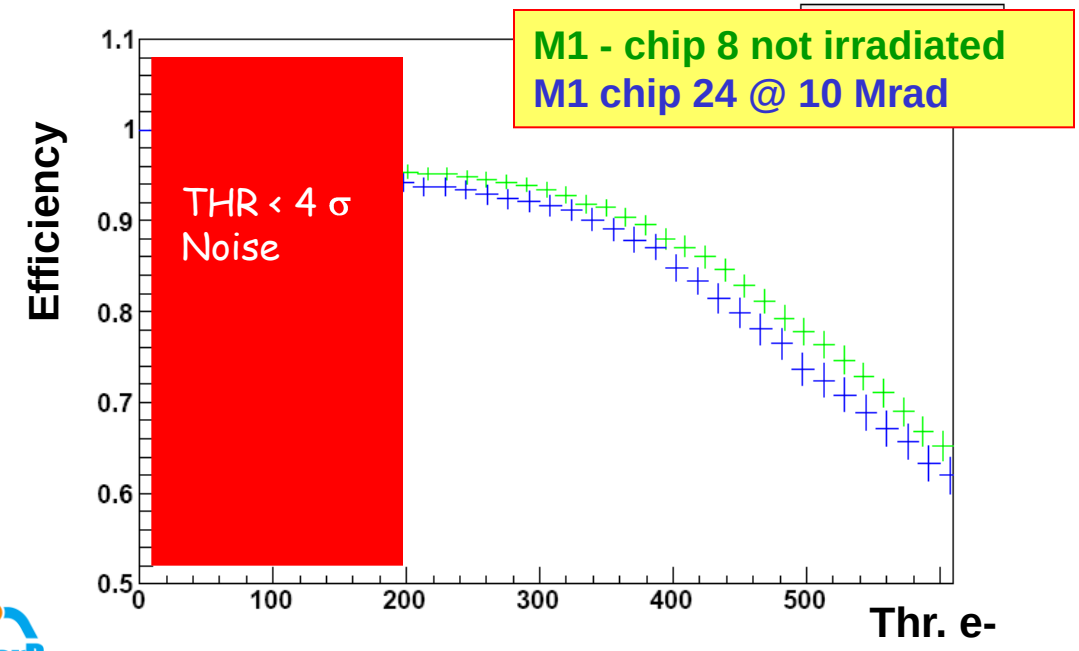
- Competitive N-wells (PMOS) in pixel cell steal charge reducing the hit efficiency: fill factor (DNW/tot N-well) ~ 90 %
  - **2D MAPS**: efficiency can improves adding multiple collecting electrodes around competitive nwells, even better using a quadruple well process (INMAPS being considered).
  - **3D MAPS**: (2 tiers for sensor&analog + digital) fill factor and efficiency can improves significantly.

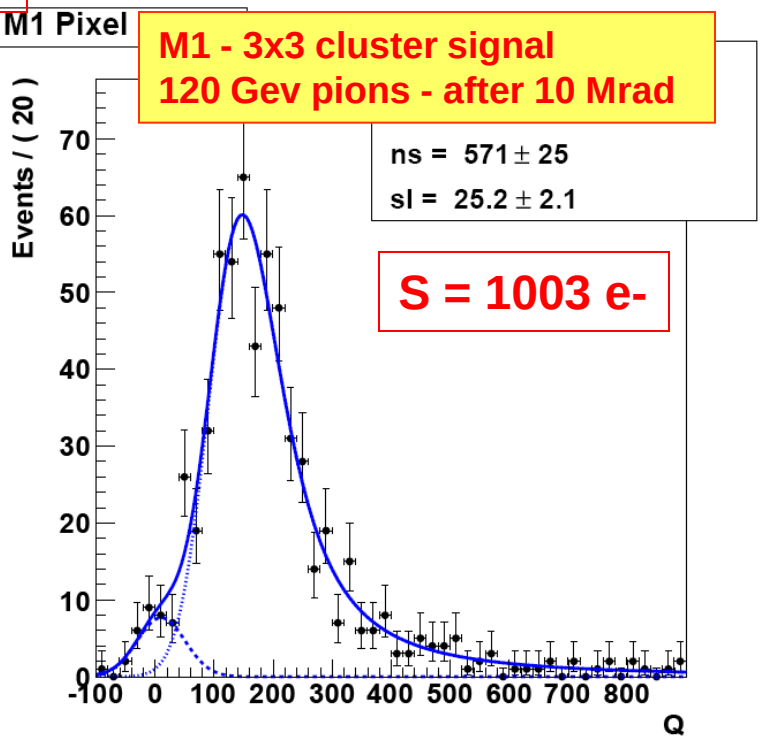


# Tesbeam with irradiated MAPS - 2009

Results for MAPS (3x3 matrix) with analog output (pre/post irrad. 10 Mrad $^{60}Co$ $\gamma$ )

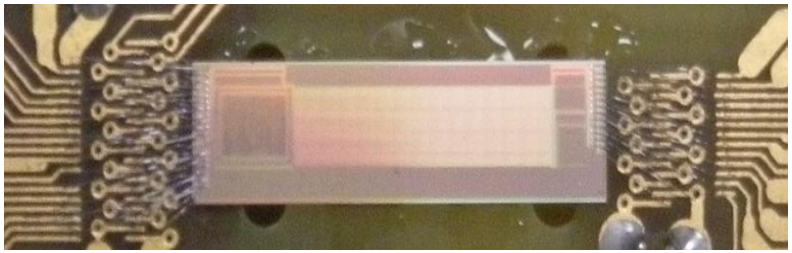
- Qcluster ~1040 e- for M1 (930 e- for M2)
- S/N~15-20 depending on the electrode geometry
- Efficiency~90% for both M1,2 in agreement with the measurements on digital MAPS
- Modest reduction in collected charge and efficiency in chip irradiated up to 10 Mrad
  - ENC increased by ~35%

# Hybrid Pixel R&D

- Prototype Front-end chip for hybrid pixel tested before sensor connection
  - ST 130 nm process (single tier)
  - 32x128 pixels, 50x50 μm pitch.



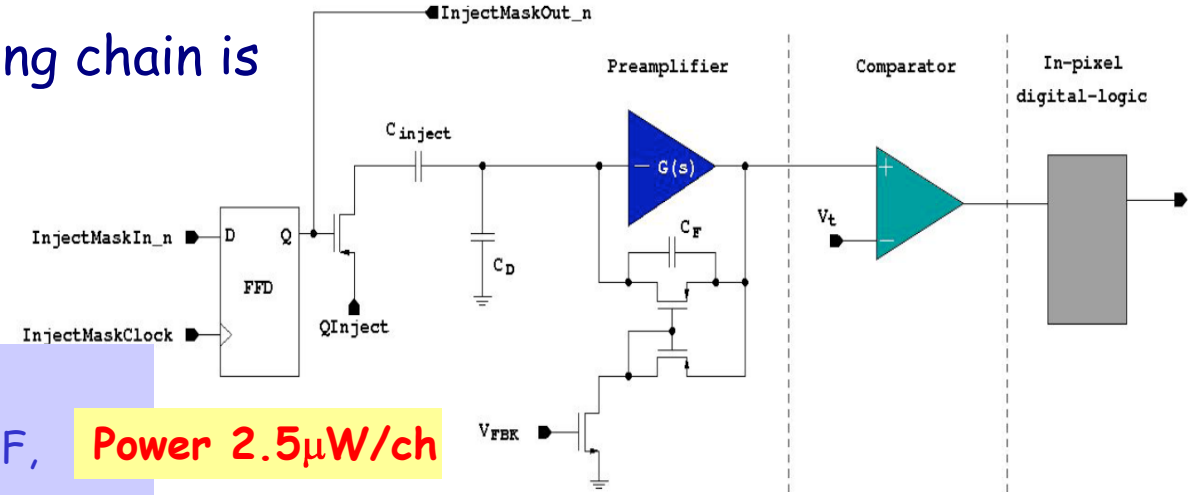
- Use data push readout architecture developed for MAPS chip, now optimized with target rate (100 MHz/cm2) for full chip size (~1.3 cm2)
- VHDL simulation: readout efficiency > 98% @ 60 MHz RDclock
- Space time coordinates with time granularity 0.2-5.0 μs (BCO clock)

- Pixel sensor matrix ready and characterized (FBK-IRST)
- N-on-N: P-spray isolation on n-side, p implant on the back side
- Wafer thickness: 200 μm (FZ, HR Si)

- Bump bonding with the FE chip with IZM Berlin under way
  → characterization with beams for the TDR preparation.

# FE chip for Hybrid Pixels – First Results

- A classical signal processing chain is implemented (no shaper)
  - ➔ Chip comparator threshold
  - ➔ in-pixel charge inj. circuit




❑ Post layout simulation:
- ENC: 150 e- @ $C_D$= 100 fF,
  120 e- without sensor
- Thr. Dispersion: 350 e-
- Gain: 45 mV/fC

**Power 2.5μW/ch**

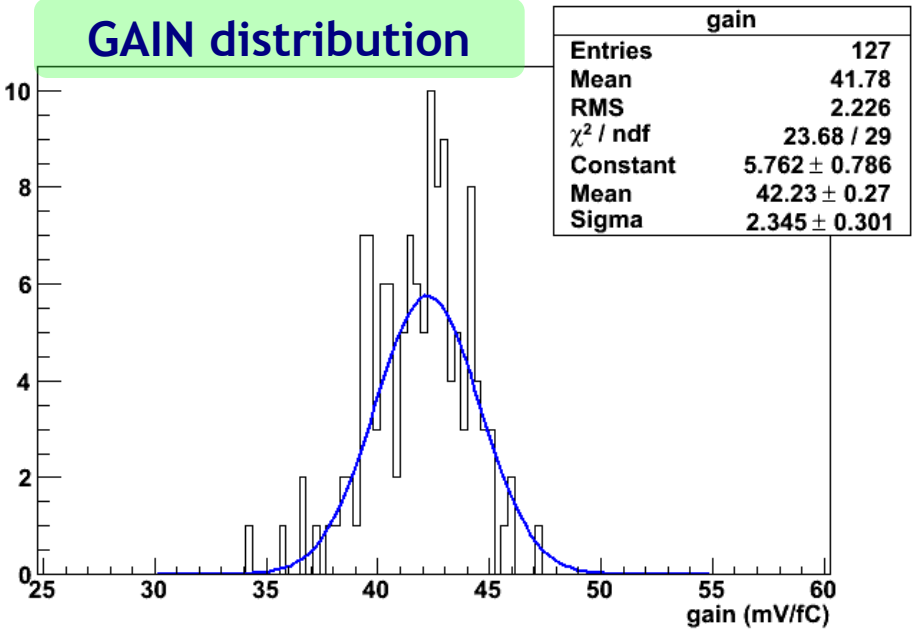
❑ Preliminary tests encouraging:

Noise scan (turn on curve)
- ENC: 70 e- without sensor
- Thr. Dispersion: 490 e-
  - pixel thr. tuning in next design!

Threshold scan with charge injection:
- Gain: 42 mV/fC (~5% dispersion)

- Further tests with sensor in Oct.

**GAIN distribution**

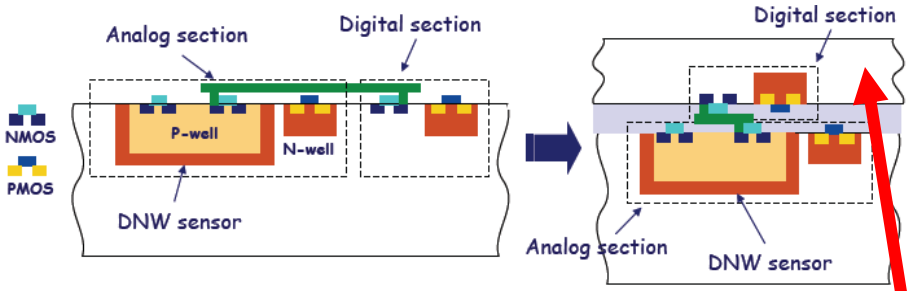


# Vertical Integration (3D) technology options for the SuperB Layer0

INFN - VIPIX collaboration

## from 2D to 3D MAPS

- ✓ less PMOS in the sensor layer
  - ➔ improved collection efficiency
- ✓ more room for in-pixel logic
  - ➔ improved readout architecture

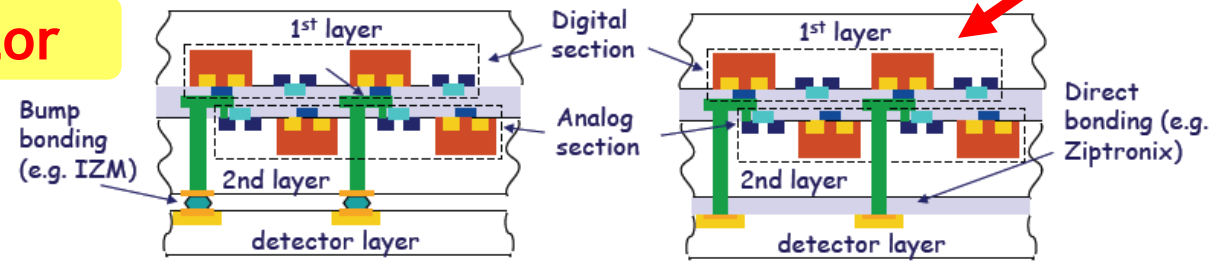



**Same architecture will be implemented in 3D MAPS and 3D FE chip for Hybrid pixel**

- ✓ **Tier 1:** sensor + analog front-end + part of the discriminator
- ✓ **Tier 2:** part of the discriminator + digital front-end + peripheral readout electronics

## 3D Hybrid Pixel detector

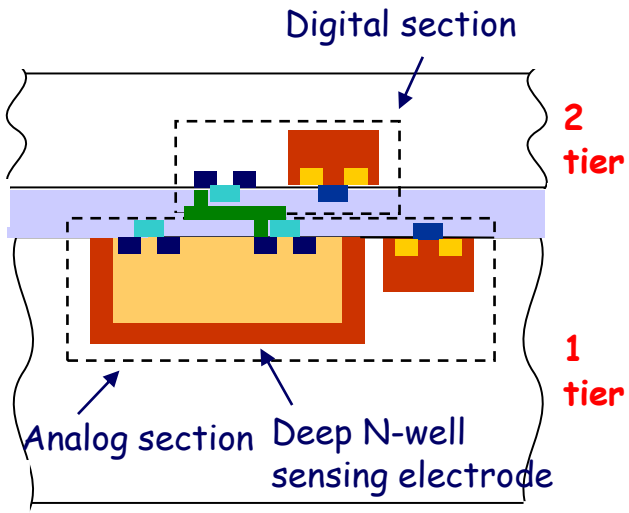
- ✓ high resistivity sensor
  - ➔ larger signal
  - ➔ better trade off between S/N and dissipated power
  - ➔ radiation hard

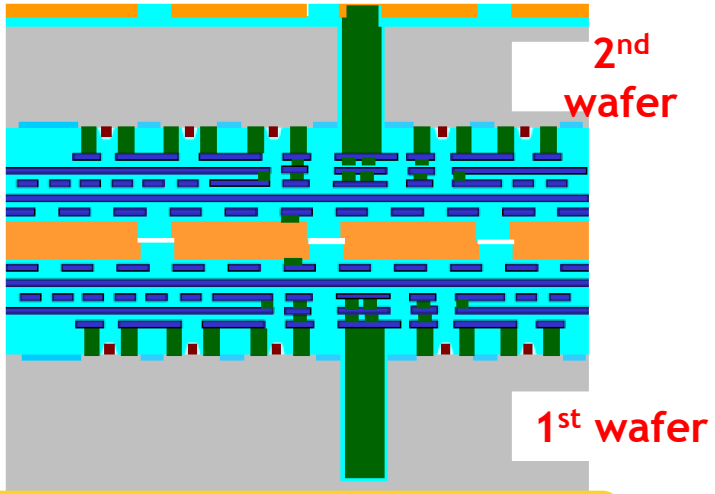



✓ **3D front end chip:** (2 tiers=more room for in-pixel logic) to be connected to high res. sensor with more (bump bonding) or less (direct bonding) standard technique

# The first 3D CMOS MAPS in the APSEL family

**3D MAPS**




Chartered/Tezzaron technology (Fermilab MPW run)

• first APSEL-like DNW MAPS (2 tiers) realized within the 3DIC Consortium to explore the 130 nm Chartered/Tezzaron process. Run still ongoing!

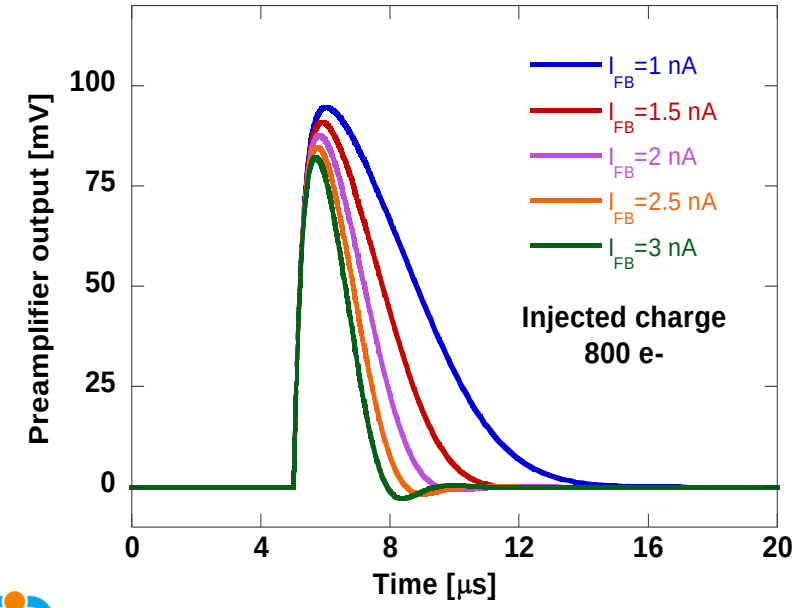
➔ Test structures → 3x3 analog matrix
- first optimization of analog cell and sensor layout for 3D version

➔8x32 MAPS matrix with APSEL4D readout architecture
- data-driven sparsified readout + timestamp; MacroPixel based
- in next version improved architecture exploiting 3D (i.e. remove MacroPixel)

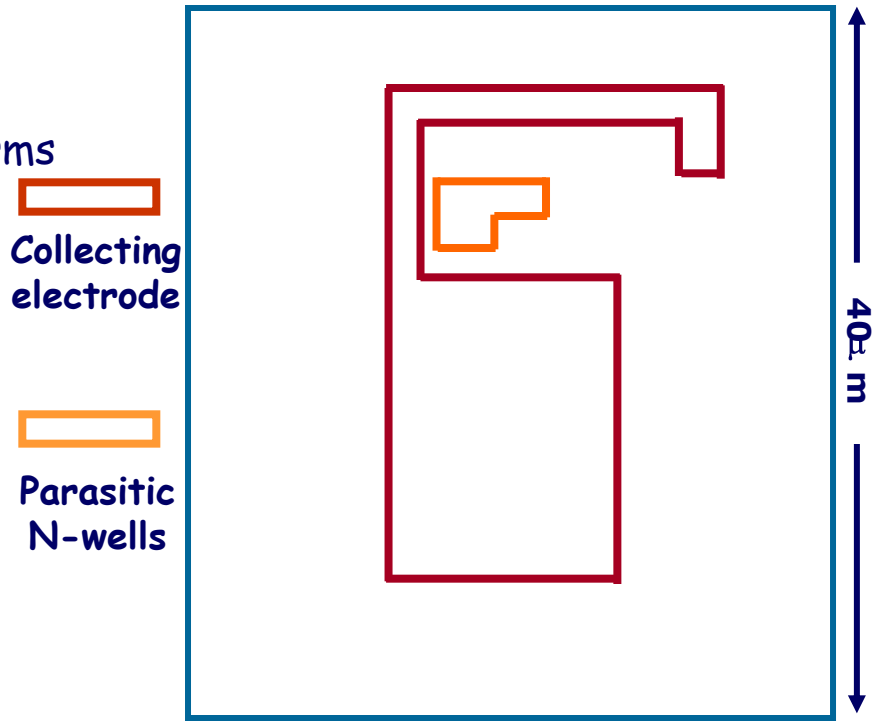
# Exploiting 3D integration: pixel pitch and sensor efficiency

## Main design features and simulation results

- W/L=30/0.3
- $C_D$=250 fF
- ~1 μs peaking time
- Charge sensitivity: 750 mV/fC
- Equivalent noise charge (ENC): 33 e rms
- Threshold dispersion: 40 e rms



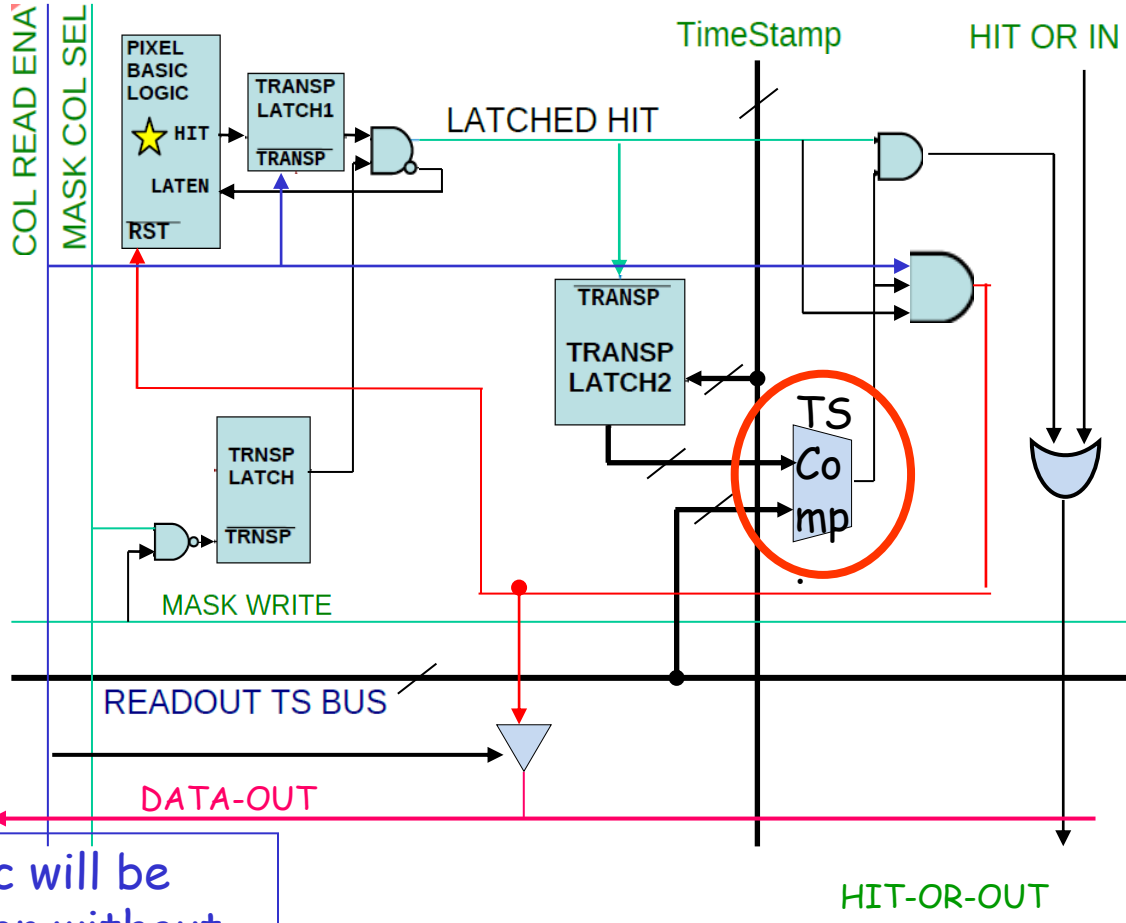

A three-dimensional technology makes it possible to significantly reduce the area of charge stealing N-wells → significant improvement in charge collection efficiency expected




**Sensor area: 346μm²**
**NW-PMOS area: 22μm²**
**Fill Factor: 0.94 (0.87 in the "2D" version)**

# Exploiting 3D integration for next submission: in-pixel logic with time-stamp latch for a time-ordered readout

- No Macropixel
- Timestamp (TS) is broadcast to pixels & pixel latches the current TS when is fired.
- Matrix readout is timestamp ordered
  - A readout TS enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that TS.
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit) is generated for pixels in the active column with hits associated to that TS




- This more complex in pixel logic will be implemented with 3D integration without reducing the pixel collection efficiency even improving the readout performance (*readout could be data push or triggered*)

VHDL simulation of the data push chip (100MHz/cm$^2$ input hit rate)

- Readout Effi > 99 % @ 50 MHz clock with timestamp of 200 ns.

# Conclusions & Perspectives

- The SuperB project is in good shape waiting for the government approval.
- Physics and background conditions set stringent requirements on the SuperB Layer0: thickness, readout speed, segmentation, rad resistance.
- The Layer0 baseline option for the TDR preparation (2011) is based on striplets sensors but an upgrade to thin pixel is foreseen for the full luminosity run (~ 2 years after t0).
- Technology options under development for Layer0 upgrade at full luminosity: DNW MAPS & hybrid pixel + vertical integration.
  - → A first DNW MAPS matrix with in-pixel sparsification and timestamp information fully characterized with beams with good results.
  - → A FE prototype chip for hybrid pixel (50x50$\mu m^2$ pitch, single tier) realized, tests ongoing.
- → Plan to exploit the vertical integration both for hybrid pixel (FE chip with 2 tiers + high res. sensor) and DNW MAPS with an expected improvement in performance.
  - First prototype 3D DNW MAPS in production to evaluate the Chartered/Tezzaron 130 nm process.
  - Larger DNW matrix and FE chip for high resistivity matrix will be submitted next year→ optimization to fully exploit 3D opportunities.

# backup

# The INFN VIPIX collaboration

## VIPIX - Vertically Integrated PIXels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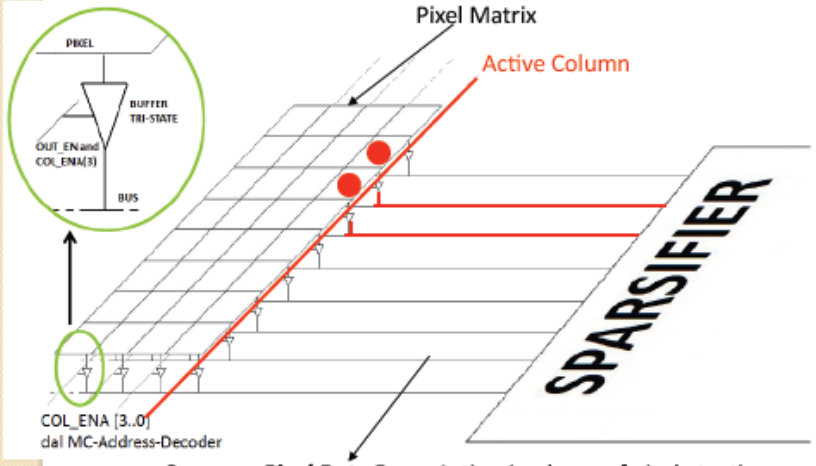
# FE Chip architecture

- Use data push readout architecture developed for MAPS chip, now optimized with target rate (100 MHz/cm2) for full chip size (~1.3 cm2)
- VHDL simulation: readout efficiency > 98% @ 60 MHz RDclock
- Space time coordinates with time granularity 0.2-5.0 us (BCO clock)

## Matrix overview

- Binary **pixels matrix**
- Column-wide **shared data-bus**
- **One column read per clock cycle**




**Common Pixel Data Bus** – Active 1 column of pixel at a time

- the per-column readout starts at the arrival of a BC which increase also the time counter
- for each column, each MP is read by a sparsifier
- informations are collected in barrels and then get out of the submatrix

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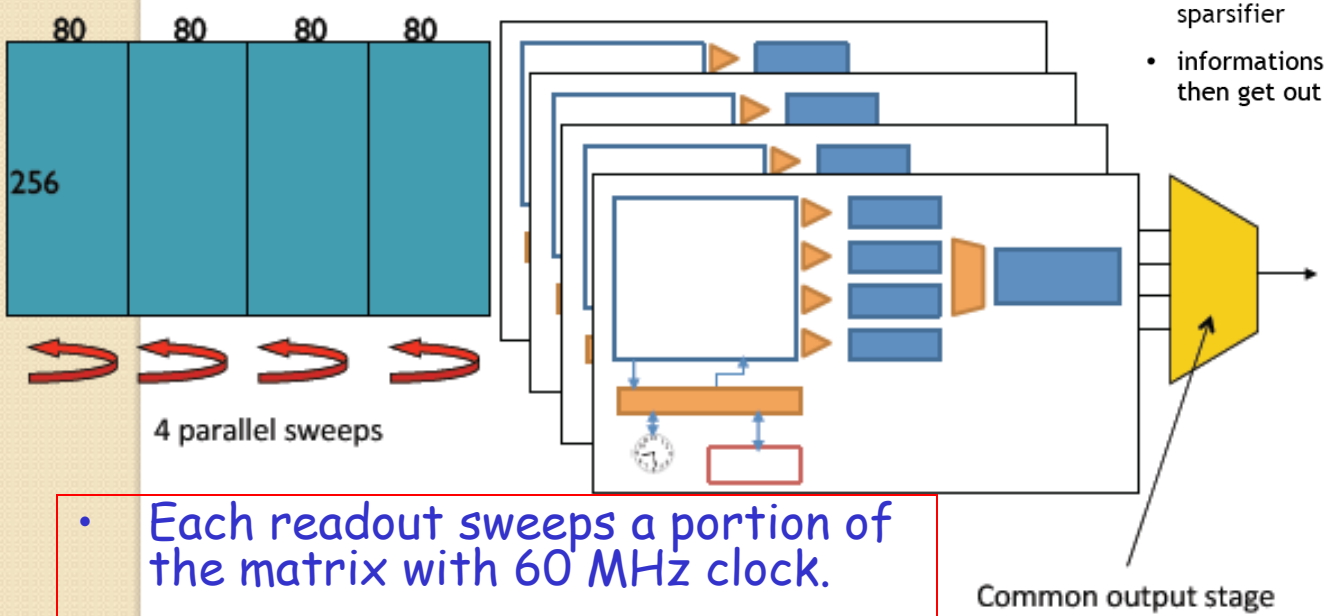
- Each sub-matrix scan has its own readout & scan logic
- All readout working in parallel
- Queuing output system




- Each readout sweeps a portion of the matrix with 60 MHz clock.

- Data from the final barrel are sent to a common bus with a faster clock ~ 160 MHz

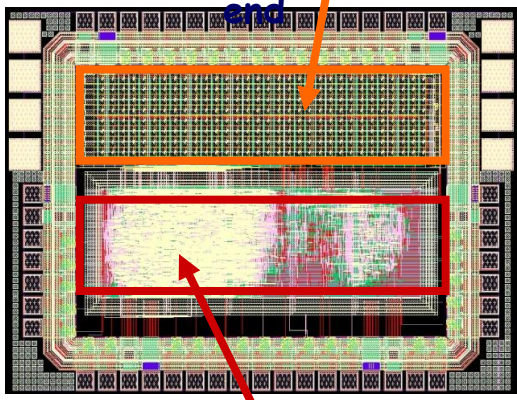
# Readout electronics in a 40 x 40 μm² 3D MAPS pixel cell

Sensing diode and charge sensitive preamplifier

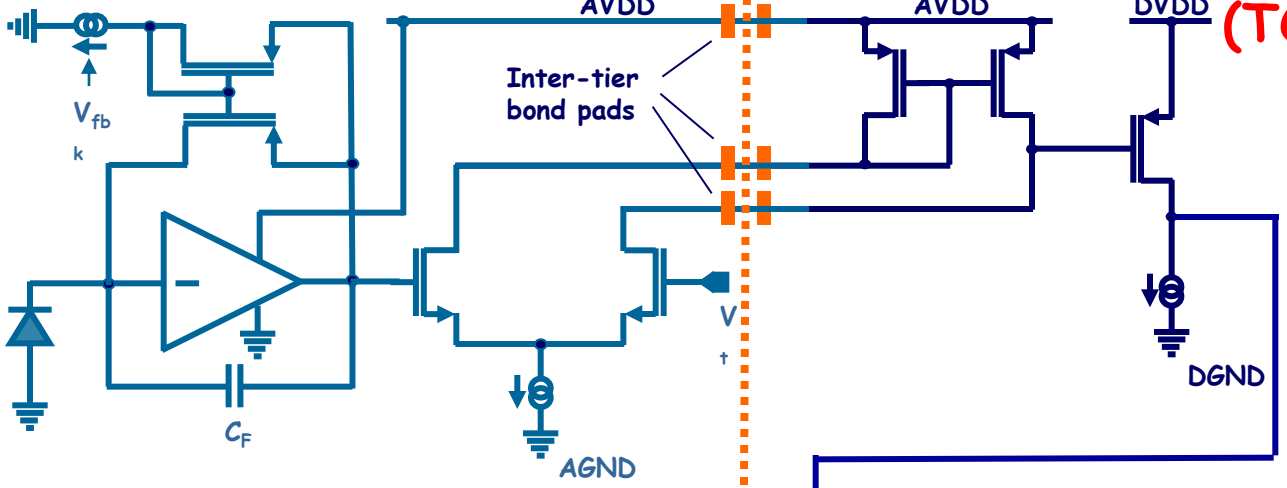
discriminator

TIER 2 (TOP)

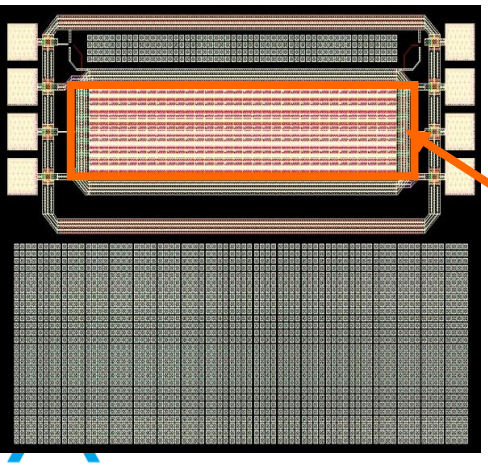
Pixel-level digital front end



Digital readout electronics




TIER 1 (BOTTOM)



8x32 pixel matrix

from the discriminator

## Pixel-level sparsification logic

3D integration removes layout constraints and will allow for an improved readout architecture (no macropixel) in future chips

# Exploiting 3D integration: readout architecture without MacroPixel

- The MacroPixel arrangement was adopted for 2D MAPS to reduce the pixel-level logic (limiting the area of competitive N-wells) and the digital switching lines running above pixel columns

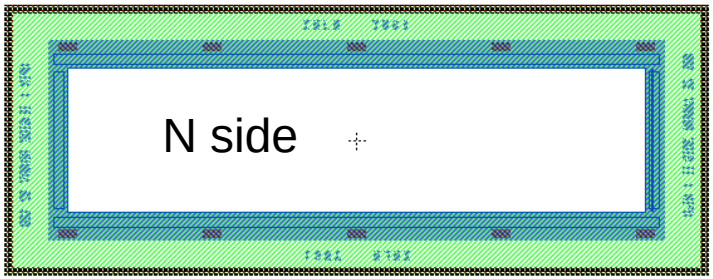
- Reasons to eliminate the MacroPixel architecture:
  - **The routing of private lines (FastOR, Latch Enable) scales with matrix column dimension**
  - **Inefficiency due to dead time (freezed MP) depends on MP dimensions**
  - **Not-fired MP columns of fired MPs are also scanned (time consuming) by the sparsification logic**

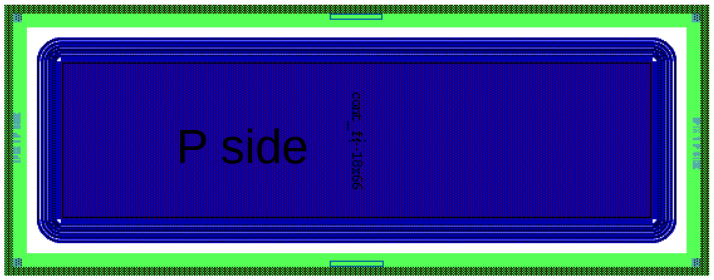
- Matrix readout speed can increase, also carrying along a readout logic simplification

- Removing the MacroPixel and implementing timestamp latching at the pixel level appears possible with 3D integration, without reducing the pixel efficiency

# Pixel Sensor Matrix

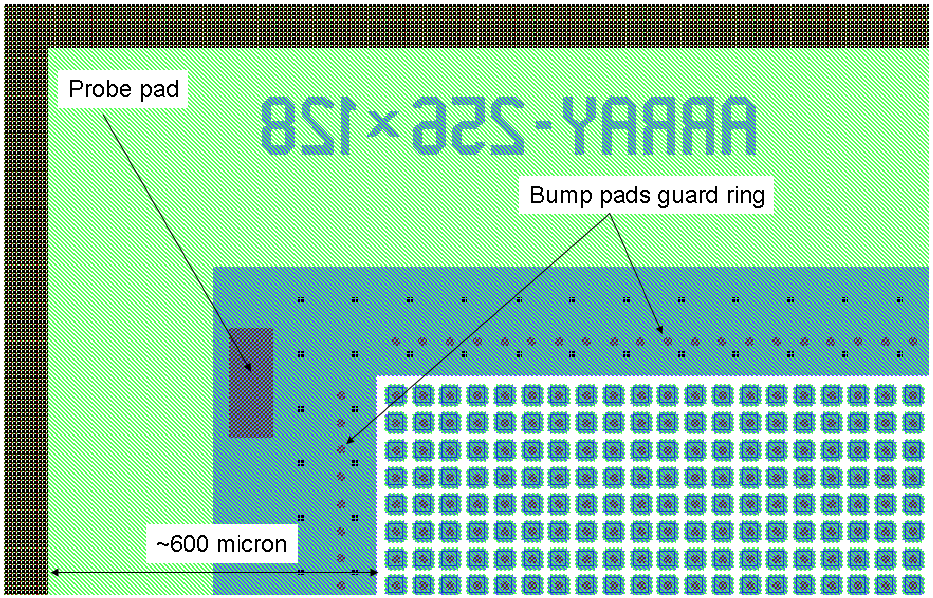
- Layout of the sensor wafer almost completed:
  - Several matrix sizes 32x128 → 256x128 (for multichip assembly)
  - N-on-N: P-spray isolation on n-side, p implant on the back side
- Wafer thickness: 200 μm (FZ, HR Si)
- Pixel capacitance (~ 20 fF) is dominated by the bump bond capacitance ~ 80 fF
- Termination structures:
  - Large GR on the pixel side
  - Multiguards on the bias side





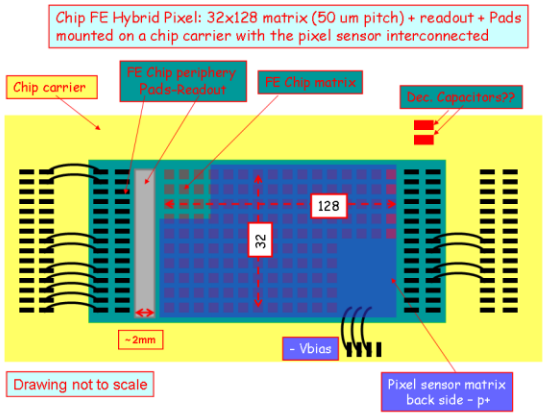

## Sensor corner, pixel size



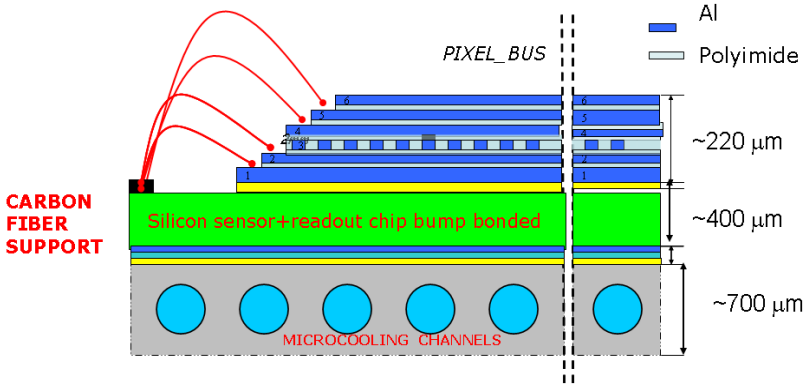
# Plans for Hybrid Pixel (II)

PAD on test chip positioned to allow single chip on carrier test but also production of a multichip pixel module:

- 3 chips + pixel sensor matrix + Al bus + support with integrated cooling.

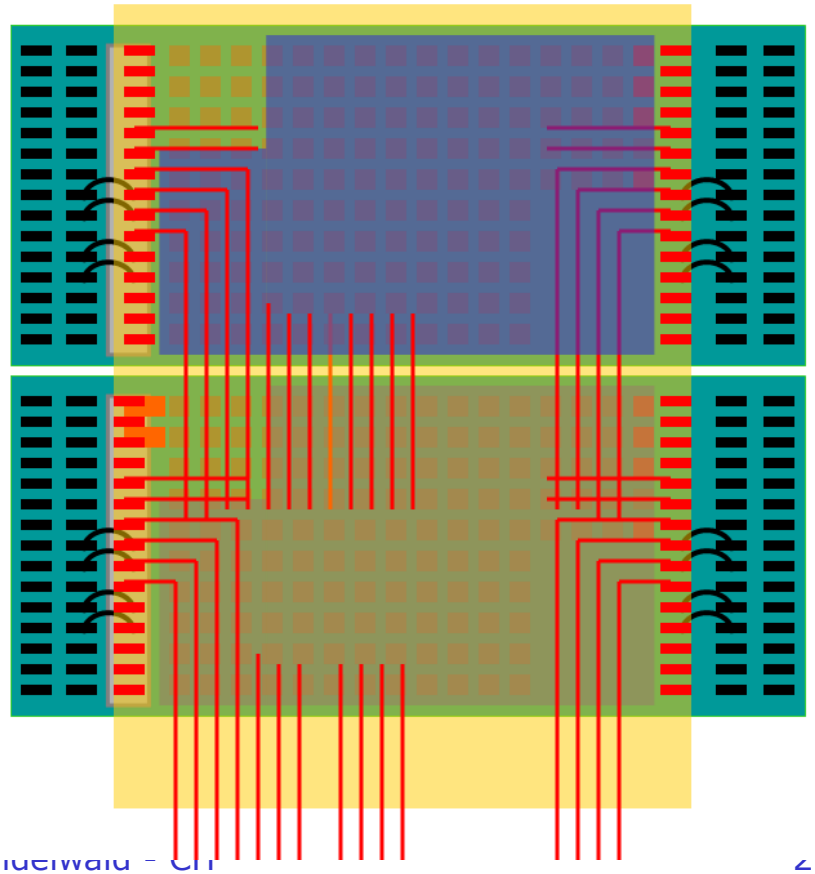



Layer0 module cross section



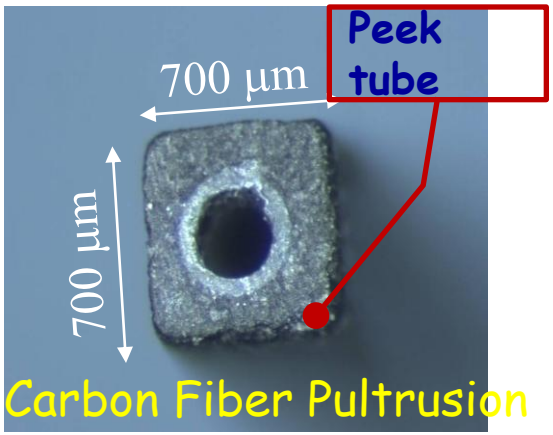

Note: drawing not to scale

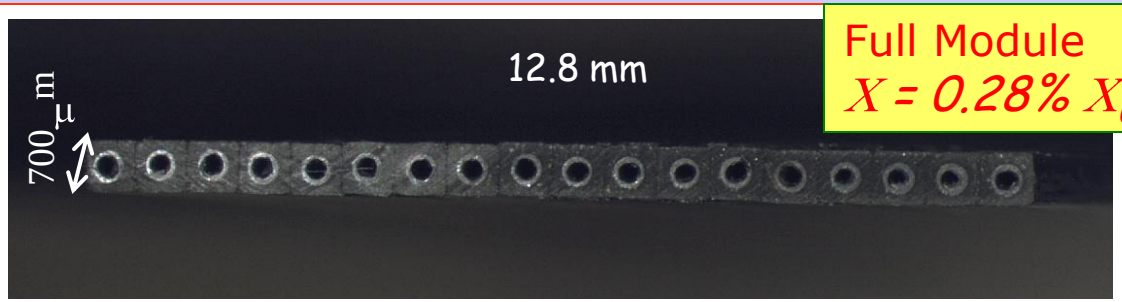
Pixel module 2 or more chips + sensor and Al pixel bus.



# Light pixel module support & cooling

- Light support with integrated cooling needed for pixel module: P~2W/cm$^2$
- Carbon Fiber support with microchannel for coolant fluid developed in Pisa:
  - Total support/cooling thickness = 0.28 % $X_0$ full module, 0.15% $X_0$ net module
- Thermo-hydraulic measurements in TFD Lab: results within specs

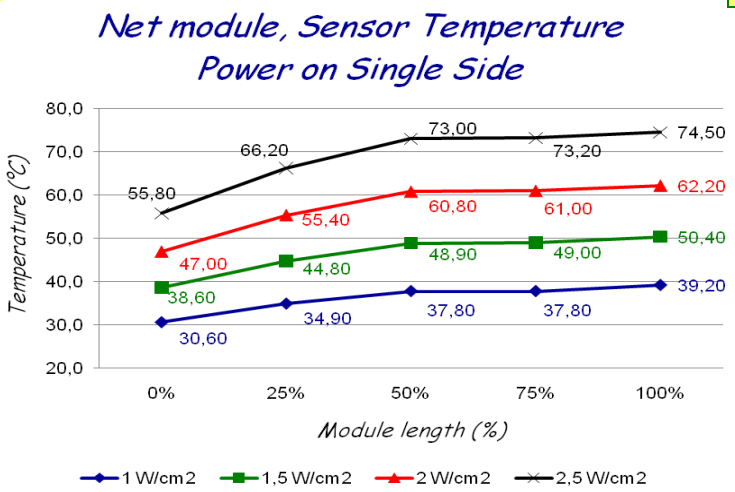


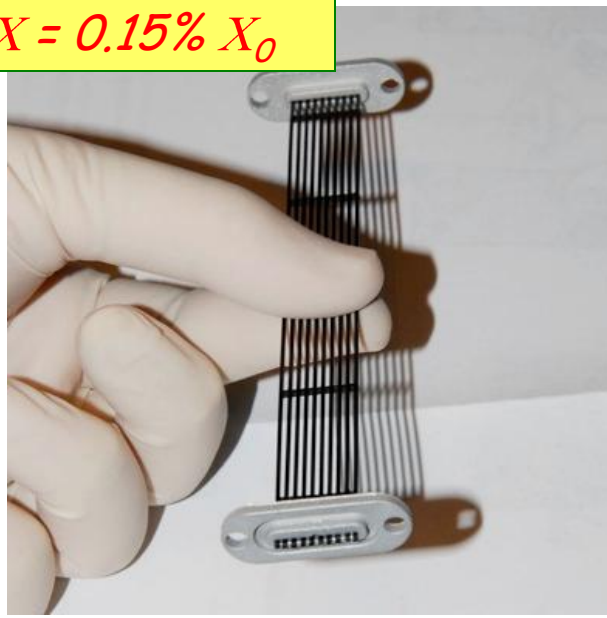




Full Module
$X = 0.28\% X_0$

Net Module
$X = 0.15\% X_0$

Full module support with microchannels glued toghether



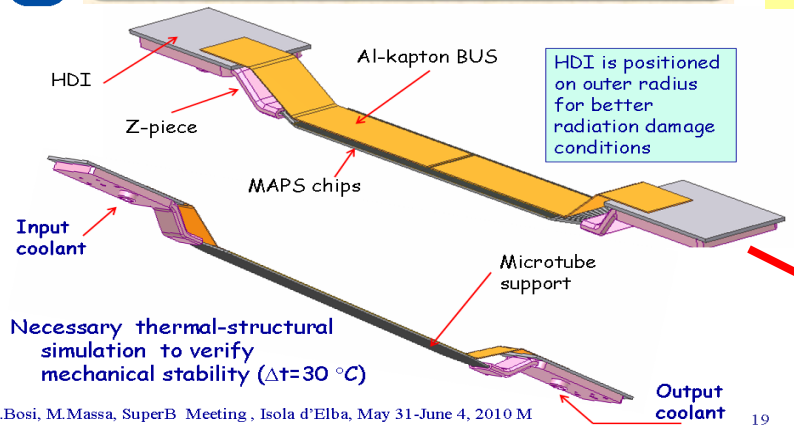



# SVT Mechanics

- Good progress on mechanical beam pipe design & integration of Layer0 modules on cooled flanges
- Next: conceptual design for quick removal of Layer0

**F.Bosi-M.Massa**

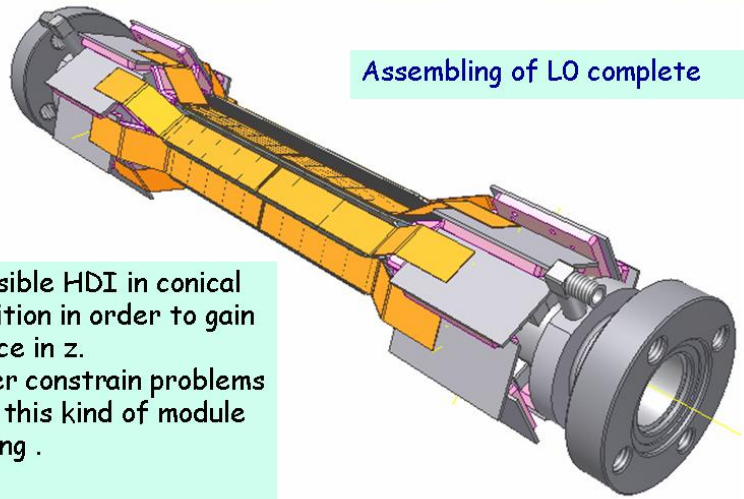
## MAPS L0 module Design




Necessary thermal-structural simulation to verify mechanical stability ($\Delta t$=30 °C)

F.Bosi, M.Massa, SuperB Meeting , Isola d'Elba, May 31-June 4, 2010 M 19

## L0 on Be pipe Design



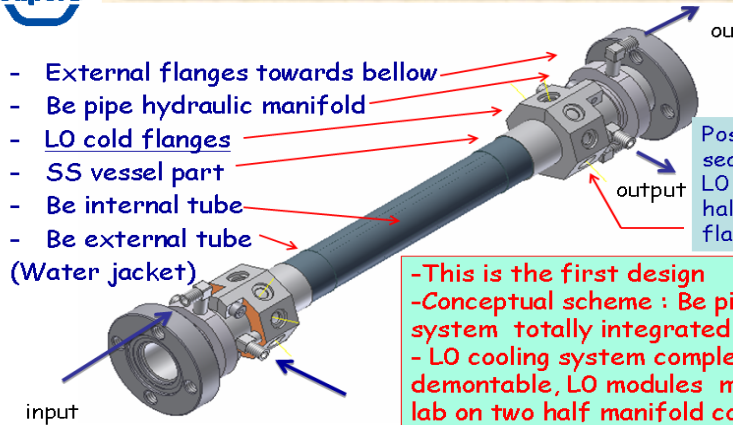
Assembling of L0 complete

Possible HDI in conical position in order to gain space in z.
Over constrain problems for this kind of module fixing .

F.Bosi, M.Massa, SuperB Meeting , Isola d'Elba, May 31-June 4, 2010 M 33

## Be pipe Design

- External flanges towards bellow
- Be pipe hydraulic manifold
- L0 cold flanges
- SS vessel part
- Be internal tube
- Be external tube (Water jacket)




Positioning and sealing of Z-piece L0 modules on the half manifold cold flanges

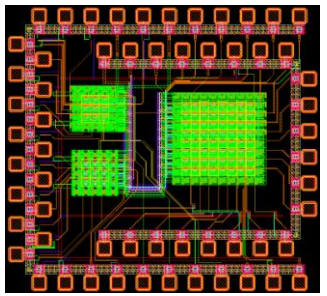
-This is the first design
-Conceptual scheme : Be pipe cooling system totally integrated.
- L0 cooling system completely demontable, L0 modules mounted in lab on two half manifold cold-flanges, positioned and fixed on rigid SS part on the B.P.

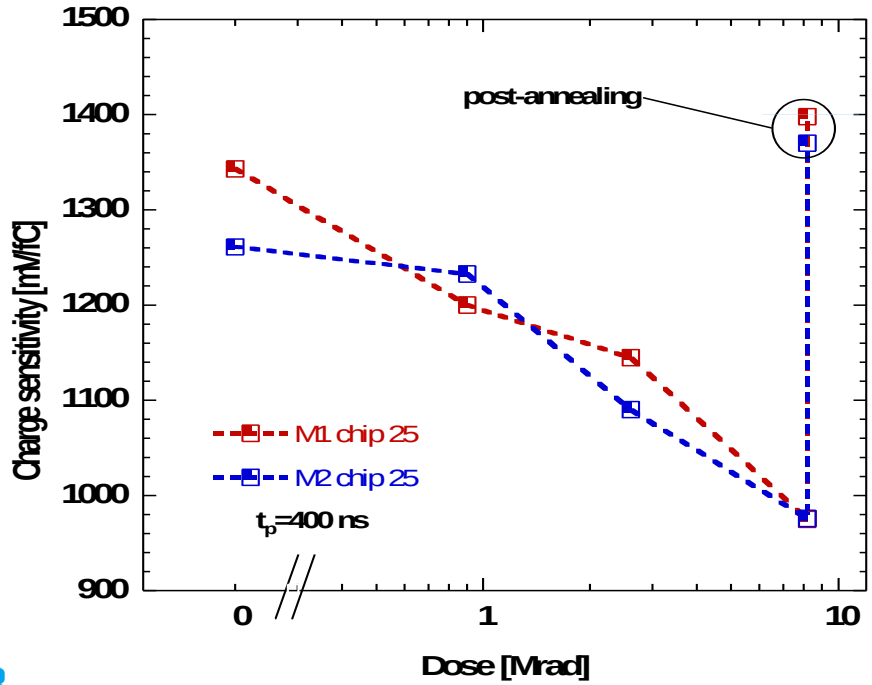
F.Bosi, M.Massa, SuperB Meeting , Isola d'Elba

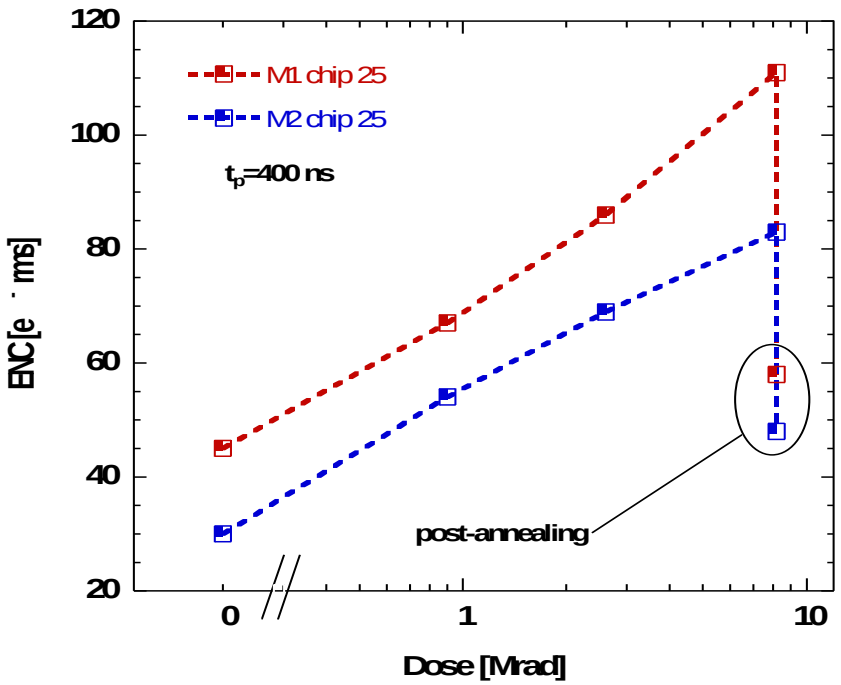
# Radiation tolerance of DNW MAPS

- Irradiation with $^{60}Co$ $\gamma$-ray up to ~ 10 Mrad
- Gain reduction ~ 3%/MRad
- Noise increase ~ 15%/MRad
- Significant recovery after 100°C/168h annealing cycle
  - Noise increase ~ +33% @ 10 MRad
- Charge collection efficiency under test
- Next step investigate bulk damage

Apsel3T1 test chip
($t_p$=200, 400 ns)

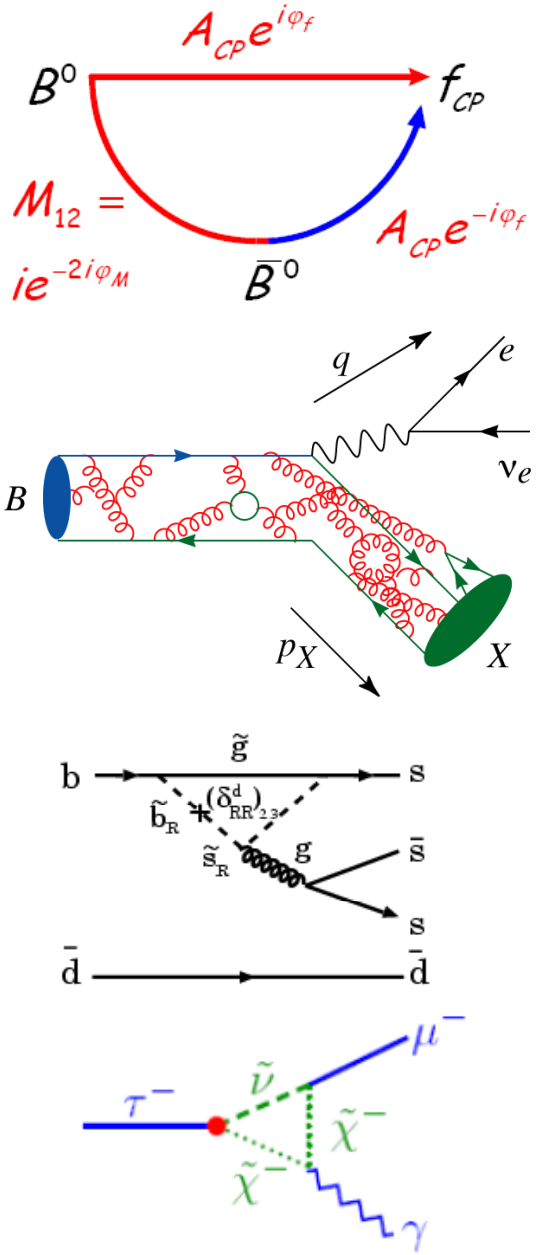




# Why flavour physics

1. Explore the origin of CP violation
   - Key element for understanding the matter content of our present universe
   - Established in the B meson in 2001
   - Direct CPV established in B mesons in 2004
2. Precisely measure parameters of the standard model
   - For example the elements of the CKM quark mixing matrix
   - Disentangle the complicated interplay between weak processes and strong interaction effects
3. Search for the effects of physics beyond the standard model in loop diagrams
   - Potentially large effects on rates of rare decays, time dependent asymmetries, lepton flavour violation, …
   - Sensitive even to large New Physics scale, as well as to phases and size of NP coupling constants



# Very high luminosity

Ways to increase luminosity by two order of magnitude:

KEKB:
- High currents
- Small damping time
- Short bunches
- Crab cavities for head-on collisions

- Large RF power
- High order modes
- High backgrounds

**Brute-force method not approved. Now investigating "the Italian approach"**

SuperB:
- Very small emittance (ILC-DR)
- Small β* at IP
- Large Piwinski angle
- Crab waist technique
- Currents similar to present ones

- Small collision area
- No parasitic crossing
- No synchro-betatron resonances
- Moderate backgrounds

**Reuse many PEP-II components**

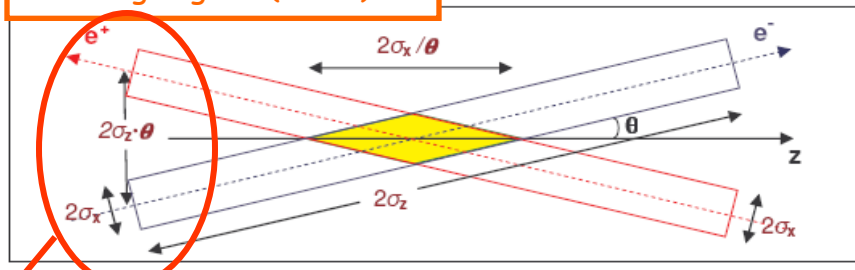
# Italian approach for a SuperB @ $10^{36}$

$$L \approx f_{coll} \frac{N_{e-} N_{e+}}{4\pi\sigma_y \left( \sigma_x \oplus \sigma_z tg\vartheta \right)}$$

## To make a long/complicated story short:

- Luminosity depends on beam currents ($\propto N$) and collision area ($\propto$ beam sizes $\sigma$ )
  - Machine people like to express beam size with transverse emittance $\varepsilon = \pi\sigma\sigma'$ and amplitude function $\beta = \sigma/\sigma'$ : $\sigma = (\varepsilon\beta)^{1/2}$

Holds for collisions with a crossing angle $\theta$ (KEKB)



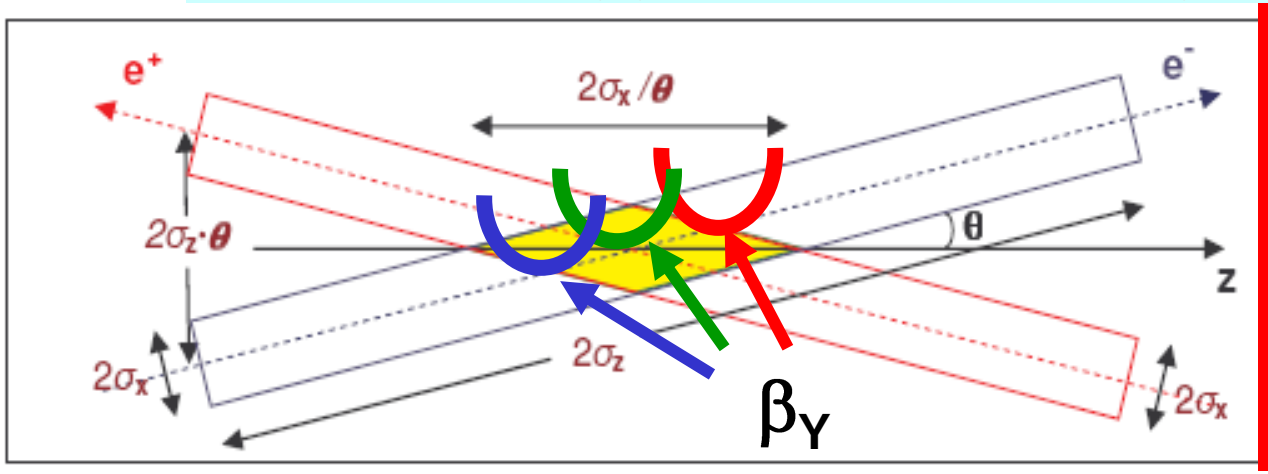

## How to reach high Luminosity:

- SuperKEKB approach: increase the currents (squeeze moderately the beams)
  - wall power and detector background explosion
  - effective limitation around $5 \times 10^{35} cm^{-2} s^{-1}$
- SuperB approach: low currents (2A), squeeze the beams and keep them small after collisions:
  - Ultra-low emittance (ILC-DR like)
  - Very small $\beta$ at IP
  - Large Piwinski angle: $\Phi = tg(\theta)\sigma_z/\sigma_x$
    - With large $\theta$ (17 mrad) and small $\sigma_x$ (4μm)
    - e- e+ bunches well separated after IP ($\sigma_z$ =6mm)
  - "Crab Waist" scheme
    - also improves Lumi by a factor ~2

Reduce $\sigma_y$ from 3 μm(KEK) to 0.035 μm→ ~L(KEK) x 100

Reduce beam beam effects and preserve the low emittance
This new IP scheme tested succesfully in DAΦNE.

# Italian approach for a SuperB @ $10^{36}$




**y waist can be moved along z with a sextupole on both sides of IP at proper phase**

**"Crab Waist"**

## How to reach high Luminosity:

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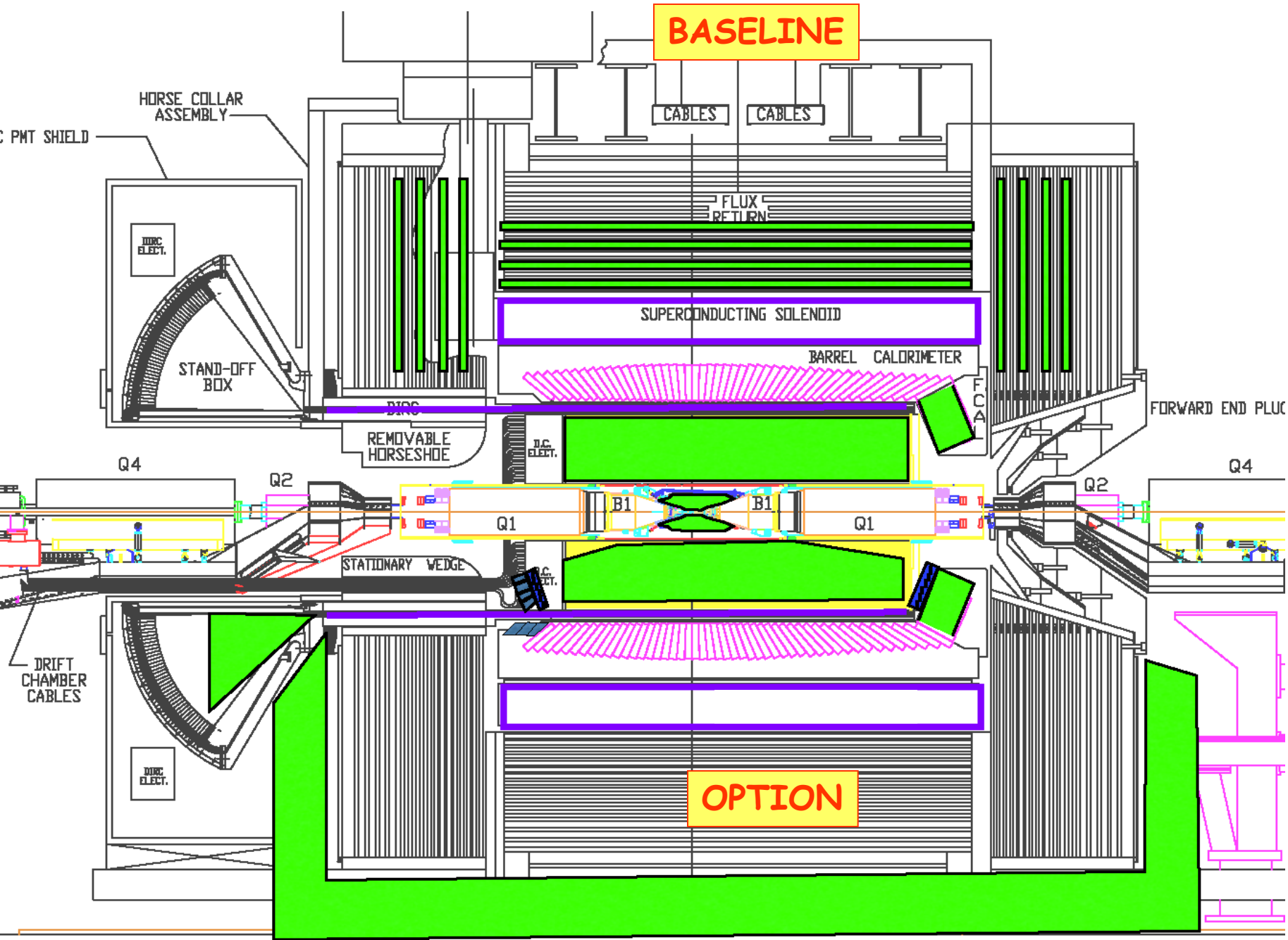
  - "Crab Waist" scheme
    - also improves Lumi by a factor ~2

Reduce beam beam effects and preserve the low emittance
This new IP scheme tested succesfully in DAΦNE.

# Detector Concept

- Babar and Belle designs have proven to be very effective for B-Factory physics
  - Follow the same ideas for SuperB detector
  - Try to reuse same components as much as possible
- Main issues
  - Machine backgrounds – somewhat larger than in Babar/Belle
  - Beam energy asymmetry – a bit smaller
  - Strong interaction with machine design
- A SuperB detector is possible with today's technology
  - Baseline is reusing large (expensive) parts of Babar
  - Quartz bars of the DIRC
  - Barrel EMC CsI(Tl) crystal and mechanical structure
  - Superconducting coil and flux return yoke.
- Some areas require moderate R&D and engineering developments to improve performance
  - Small beam pipe technology
  - Thin silicon pixel detector for first layer
  - Drift chamber CF mechanical structure, gas and cell size
  - Photon detection for DIRC quartz bars
  - Forward PID system (TOF or focusing RICH)
  - Forward calorimeter crystals (LSO)
  - Minos-style scintillator for Instrumented flux return
  - Electronics and trigger – need to revise Bfactory "½-track" trigger style
  - Computing – large data amount
- More details in:
  - www.pi.infn.it/SuperB/CDR - SuperB Conceptual Design Report
  - http://agenda.infn.it/categoryDisplay.py?categId=109 - SuperB Workshops

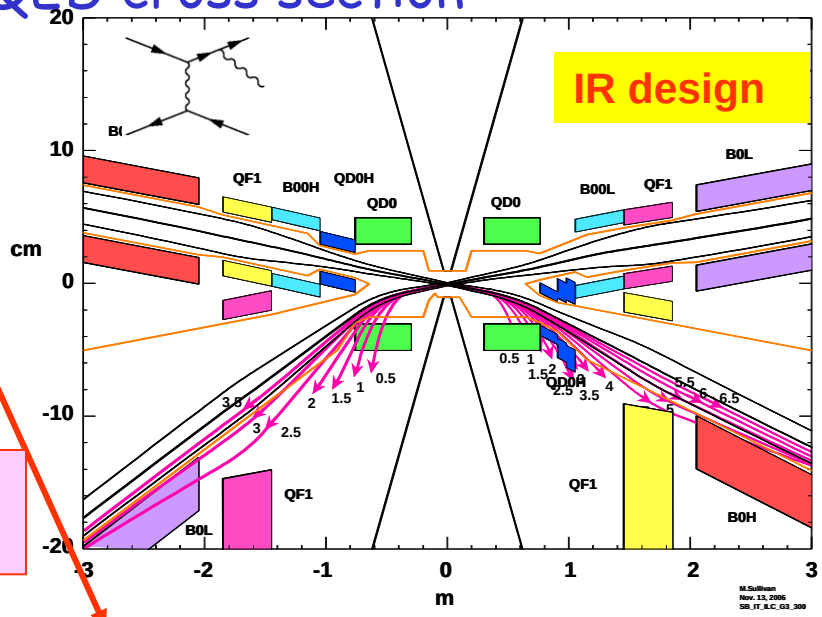
# Detector Layout - Reuse parts of Babar



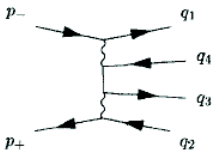
# Backgrounds @ SuperB

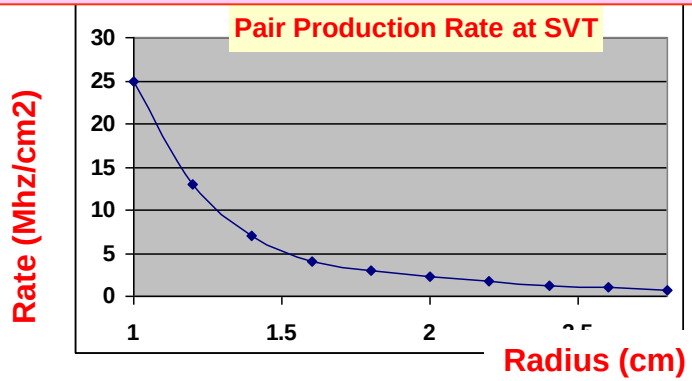
- Low currents (2A):
  - Beam-gas are not a problem (similar to BaBar)
  - SR fan can be shielded
- High luminosity → dominated by QED cross section

| | Cross section | Evt/bunch xing | Rate |
|---|---|---|---|
| Radiative Bhabha | ~340 mbarn ( Eγ/Ebeam > 1% ) | ~680 | 0.3THz |
| $e^+e^-$ pair production | ~7.3 mbarn | ~15 | 7GHz |
| Elastic Bhabha | O($10^{-5}$) mbarn (Det. acceptance) | ~20/Million | 10KHz |
| $\Upsilon(4S)$ | O($10^{-6}$) mbarn | ~2/million | 1 KHz |




Track rate reduced to ~5 MHz/cm² in Layer0
→ e+/e- have low energy and loop in the 1.5T B field.



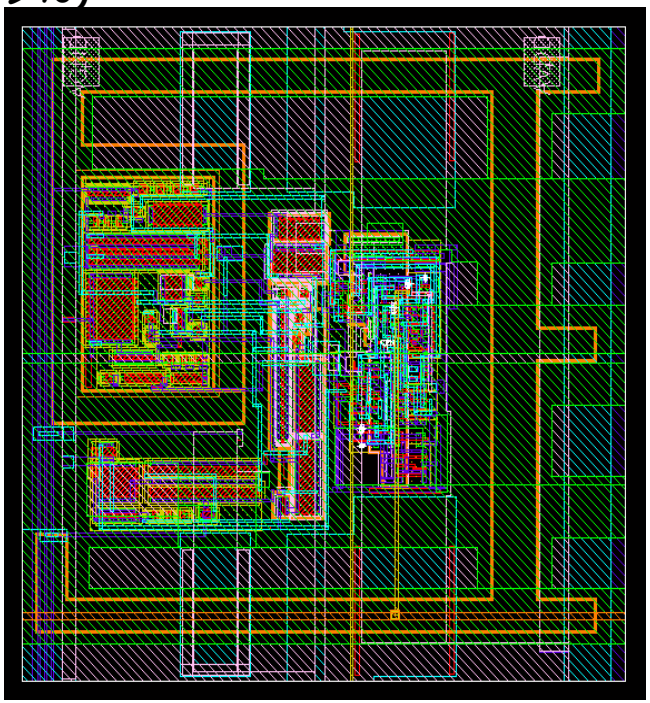



Rate reduced to ~ 100 kHz/cm2 @ SVT location with present IR design and proper shielding to prevent the produced shower from reaching the detector

# Optimization of sensor layout

- Small size prototype module with functionalities and cooling/mechanics close to SuperB specifications needs a **128x128 (or 320x80) MAPS chip (APSEL5D)** with 40μm x 40μm pixel cells
  - With respect to APSEL4D, scaling to larger matrix size dictates to remove the shaper stage to make room for additional macropixel private lines and to reduce the pixel pitch
  - Inside the pixel cell, sensor layout has to be changed to increase detection efficiency (→ 99%)

- Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- Optimized cell with satellite N-wells (right): efficiency ~ 99% from TCAD, promising results from laser tests



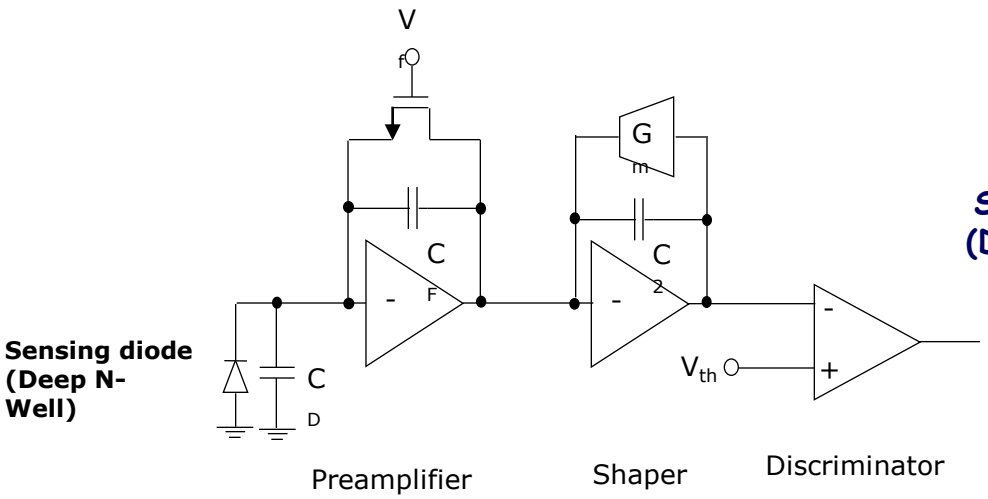
**Charge collecting electrode with annular shape**

**Sensor area: 480μm²**
**CNW-PMOS area: 70μm²**
**Fill Factor: 0.87**

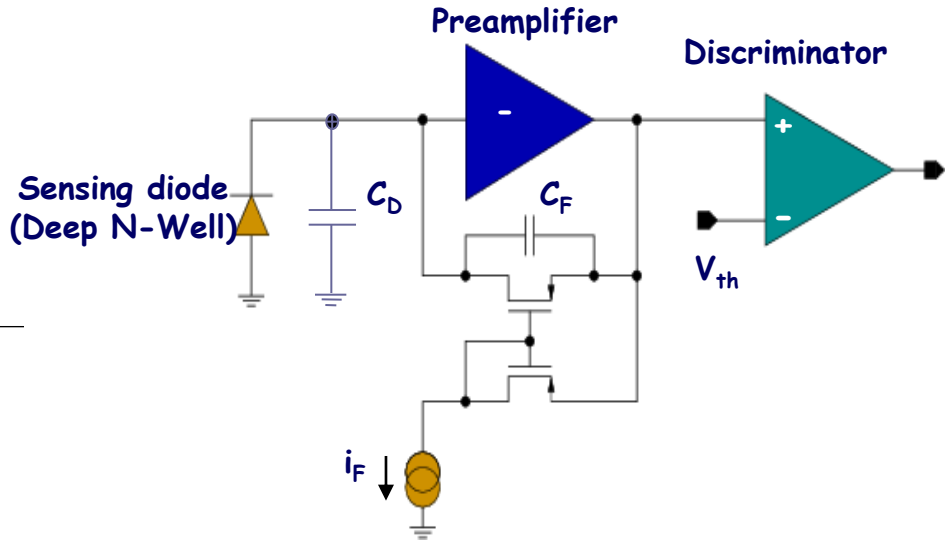
# The analog section in the pixel cell

- A new design ("shaperless" analog front-end) and layout (charge collecting electrode with satellite N-wells) of the pixel cell was successfully tested in small test structures (APSEL5T)

**APSEL4D**



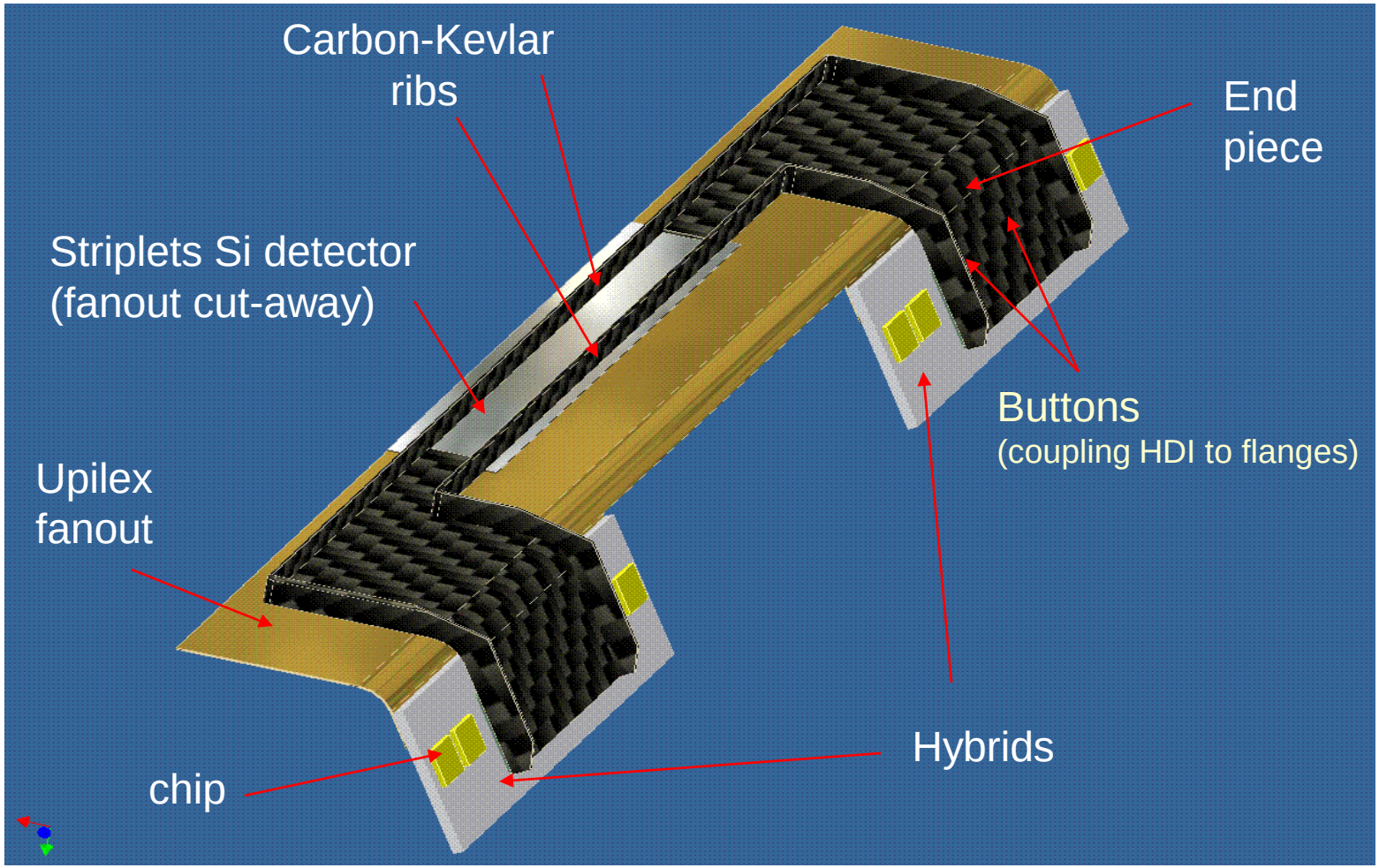

**APSEL5T**



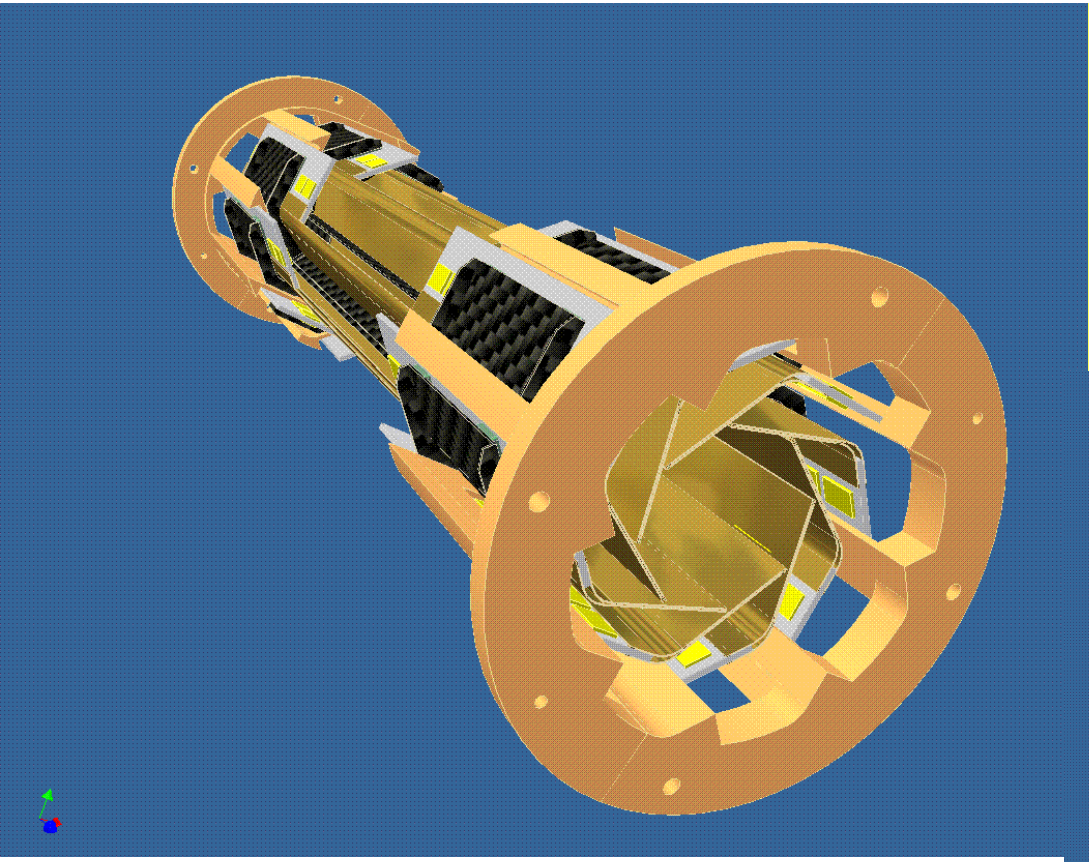

- Pixel cell: 50x50 $\mu m^2$
- Sensor capacitance: 400 fF
- Power dissipation 30 $\mu W$
- ENC = 60 e rms

- Pixel cell: 40x40 $\mu m^2$
- Sensor capacitance: 270 fF
- Power dissipation: 20 $\mu W$
- ENC: 55 e rms

# Module Layer0 (striplets): 3D-view

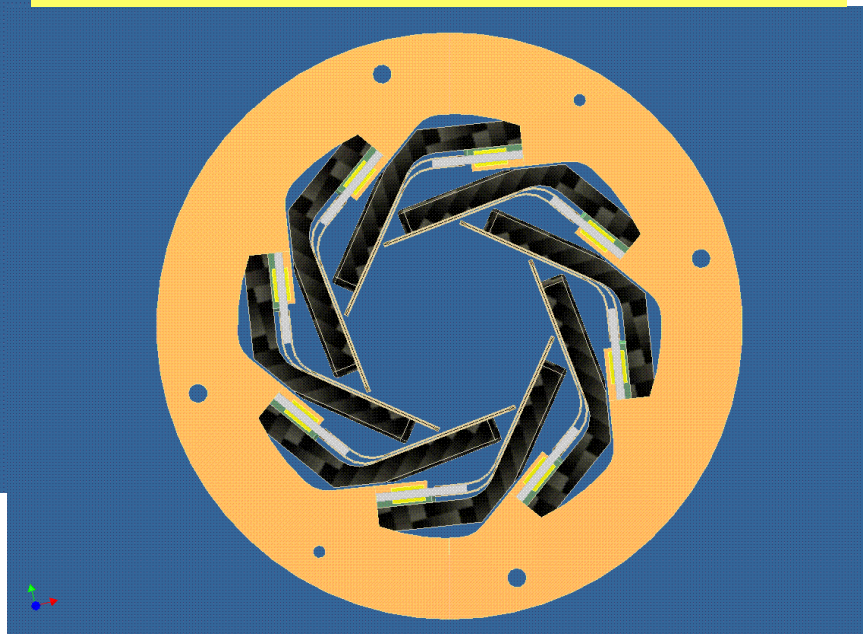


# Final Layer 0 (striplets) structure



3-D view

- Mechanical aspects worked out in some detail: from module assembling up to final mounting on the beam pipe.



r-$\phi$ cross section