UNIVERSITY OF LIVERPOOL

Pixel 2010

International Workshop on Semiconductor Pixel Detectors for Particles and Imaging

Grindelwald, Switzerland

Characterisation of “n-in-p” detectors for high radiation environment

I.Tsurin, University of Liverpool

Subject: design of planar silicon detectors for the Atlas upgrade (beneficial for the LHCb VeLo upgrade R&D)

- **Detector layout: readout implants, guard structure, cut edge**
- **Measurement instrumentation and methods**
- **Some results (before irradiation)**

September 6-10, 2010

Liverpool Expertise in Detector Development

Long tradition in making silicon detectors for HEP

SLHC challenges: Radiation Hardness

Detector technology (research with e2v)

Sensor layout (research with Micron Semiconductor)

Detector environment: cooling, HV, readout etc.

My subtask:

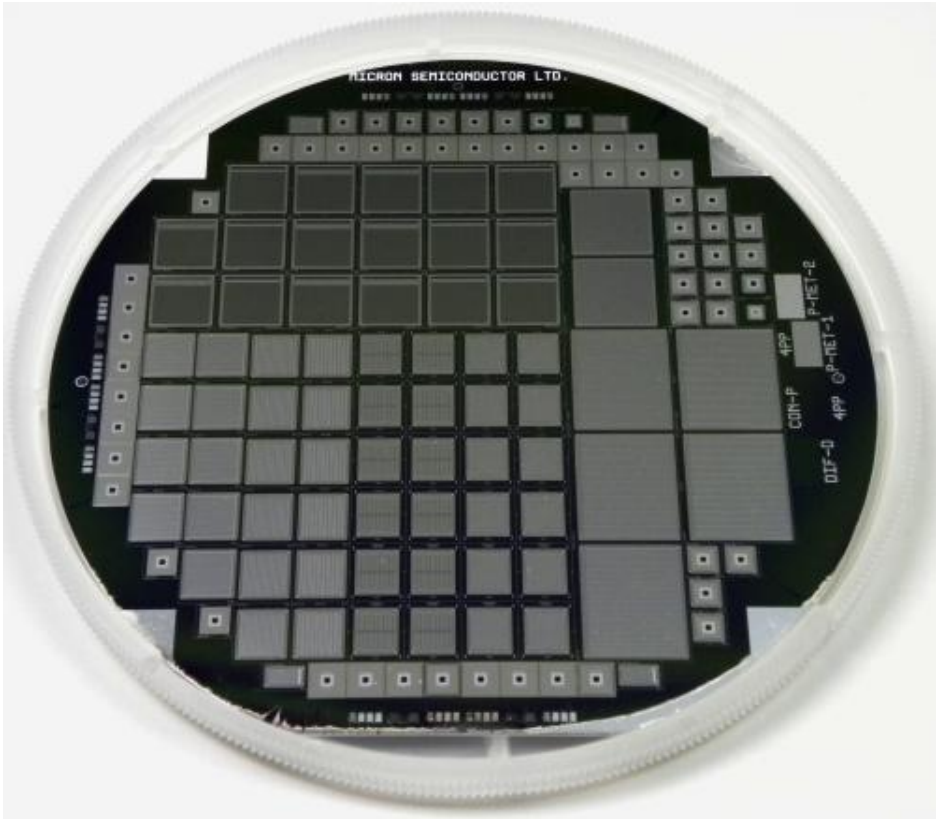
Mask design for the planar silicon pixel (and strip) detectors to be manufactured in the UK by e2v and Micron Semiconductor

To achieve good spatial resolution through efficient charge collection:

- HV performance (main focus in this work)
- Optimal implant geometry -> new RD50 wafer

Pixel Detector Programme in Liverpool

6” wafers 2800-2825 fabricated by Micron



in the double metal “n-in-p” FZ process

Strip detectors:
- **Polysilicon bias resistors**
- **Punch-through biasing**
- **Bias rail option**

Pixel detectors:

FE-I3, FE-I4, PSI-46, MPIX-II, APC, APR (interleaved pixels)

Pad detectors:

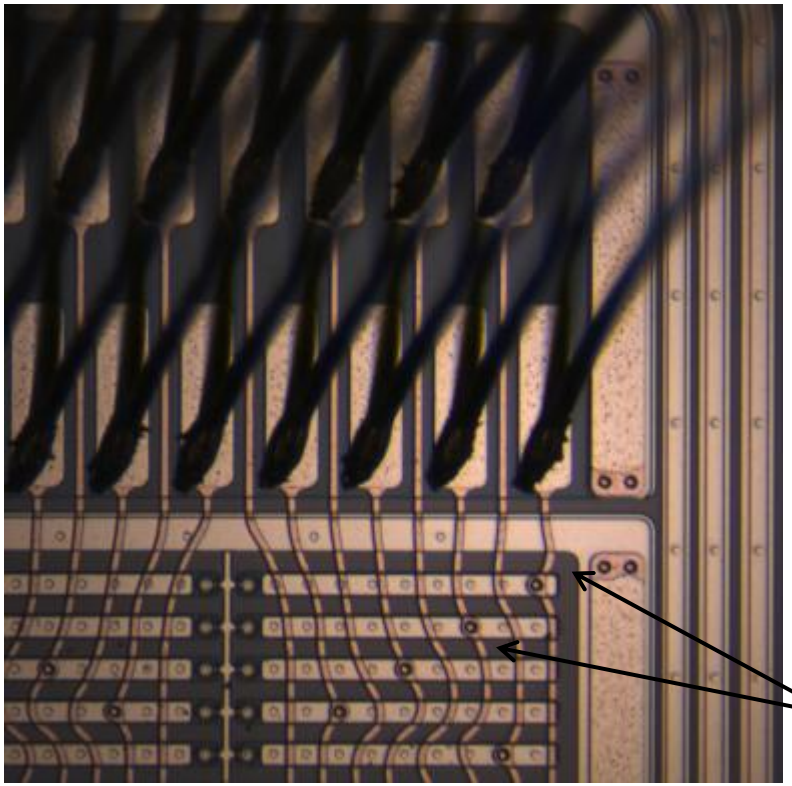
RD-50, PSI, MPI guard structures, Cut edge scenarios (8, 4, 2, 1 rings)

Test structures:
- **Process control, device modelling**

Pixel Detectors with Wire-bonded Readout

Working horse:
pixel sensors with interleaved readout implants connected to wire bond pads

Column-parallel / Row-parallel readout



Shuffled R/O channels to minimise the cross talk between connection lines

Pulse shape analysis
Cross-calibration of ToT

Fast "Cold" bonding to the readout for annealing studies

Re-use of bonding pads
No need to irradiate the readout
-> good data quality

Inter-"strip" resistance and capacitance measurements

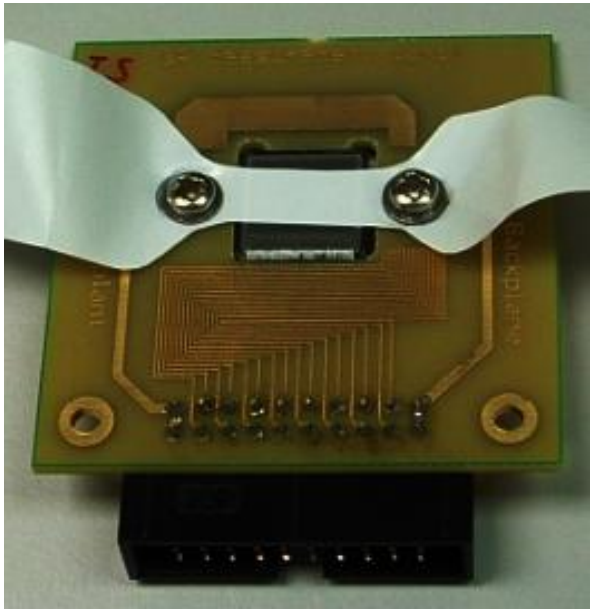
Measurement of the punch-through voltage of the biasing circuit

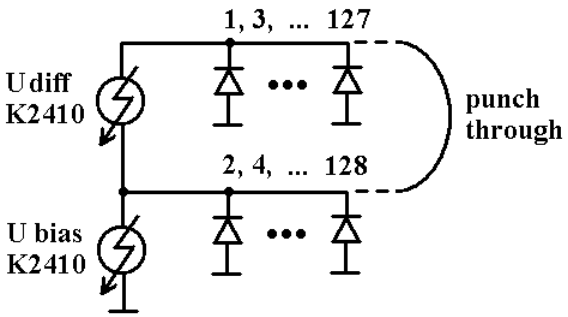
Readout Implants, part I (resistances)

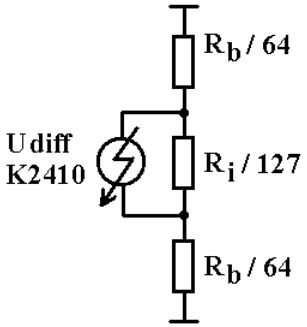
Sheet resistance ~400 Ohm/square (implant dose ~10^{14} cm^{-2})

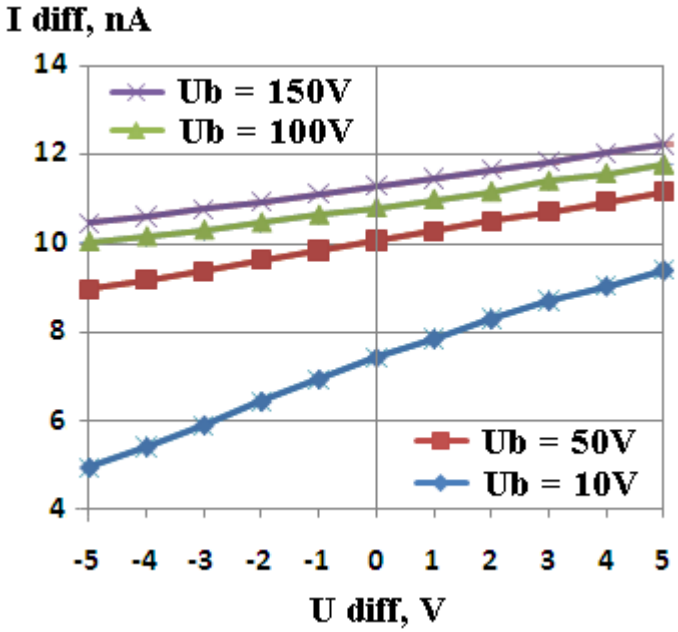
Inter-"strip" resistance ~1 TOhm/cm for 50 um pitch (see spare slides)

PCB for measurements of the punch through voltage, potentials on guard rings and characteristic inter-"strip" resistance and capacitance









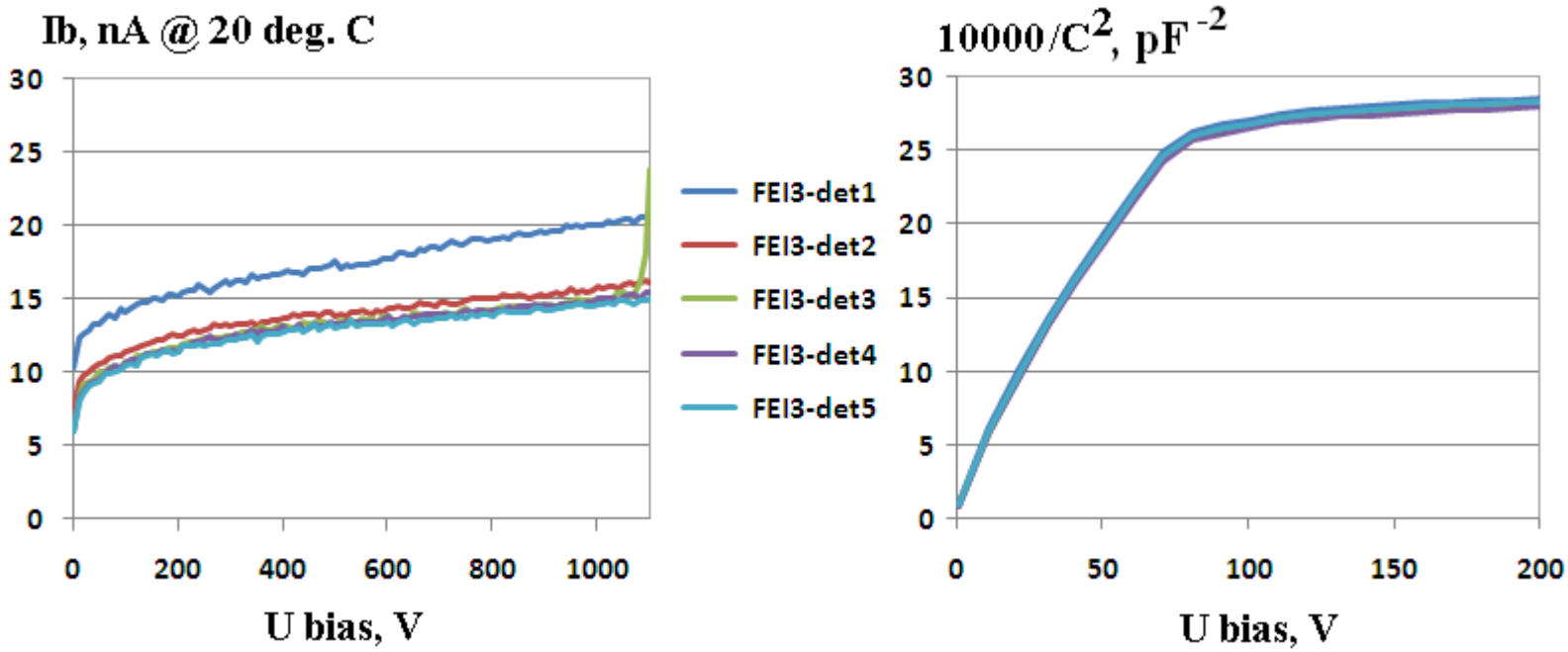
Sensor's substrate is attached to the heat sink for cooling by the air flow

Readout Implants, part II (capacitances)

Inter-"strip" capacitance ~0.5 pF/cm for 50 um pitch (see spare slides)

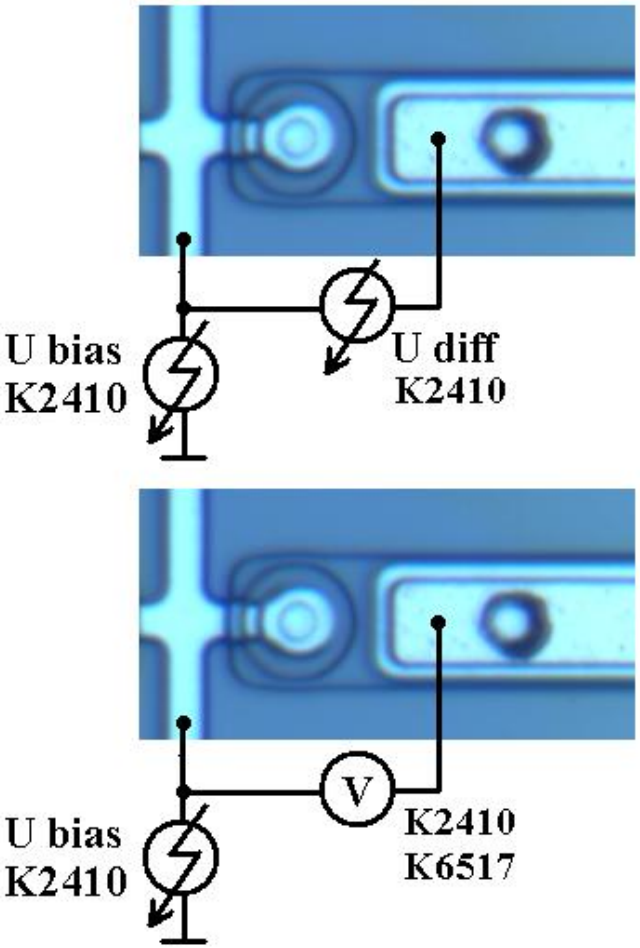
Capacitance to bulk ~1 pF/sq. mm at full depletion voltage (reduces when the bias network is powered, this effect depends on the sensor size; it is not quantified here)

IC(V) curves for the FE-I3 single chip sensors



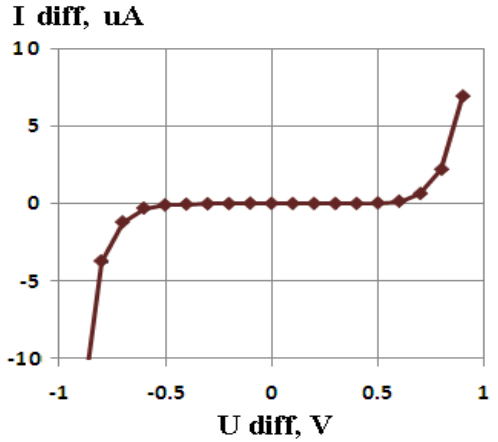
Full depletion voltage ~80 V (unirradiated, bulk resistivity ~15 kOhm.cm)

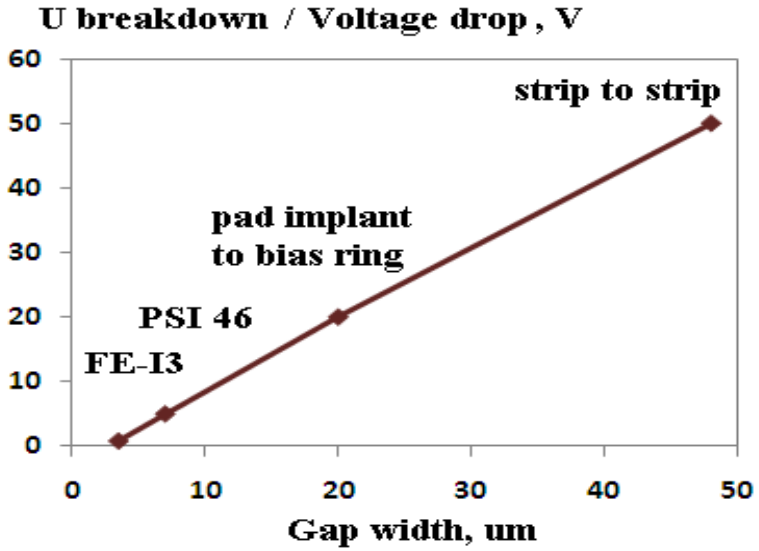
Readout Implants, part III (punch-through biasing)



Atlas pixel sensor

Punch-through gap = 3.5um



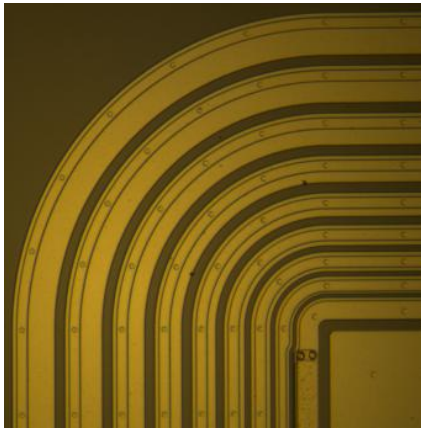


Punch-through voltage ~1 V/um -> the hybrid designer should pay attention to:

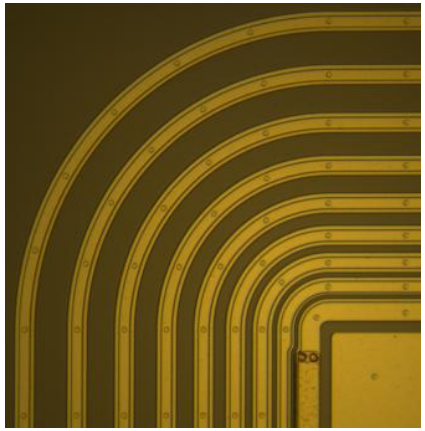
- **potential of the bias ring connected to ASIC (pixel shortening, chip breakdown)**
- **potential of the 1st GR connected to ASIC (chip breakdown)**

Guard Structures

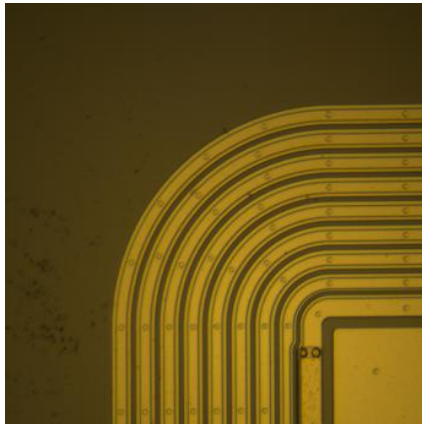
"RD-50"



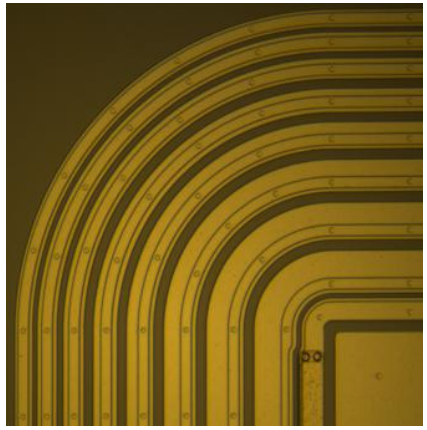
"PSI"



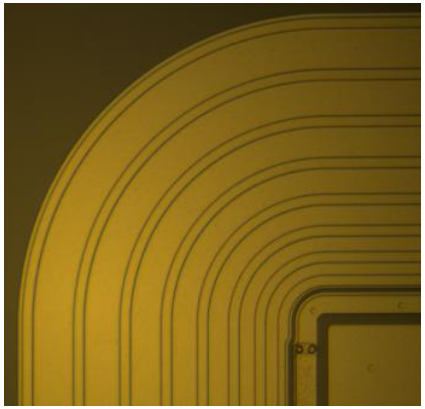
"MPI"



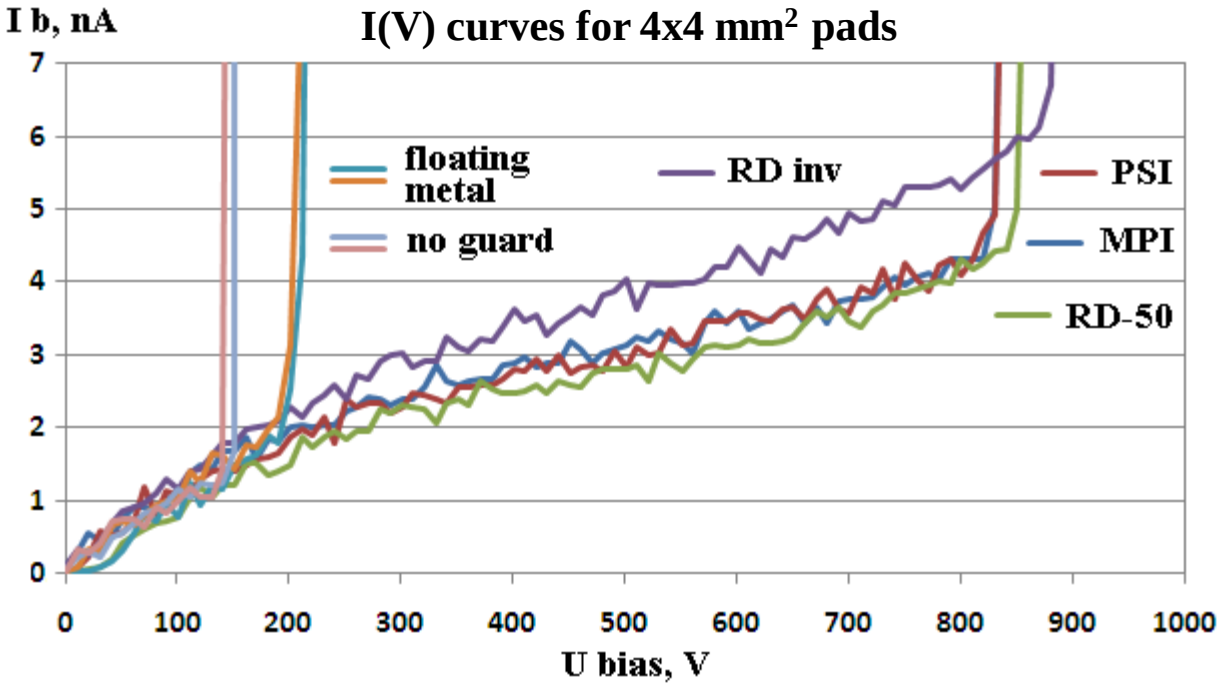
"RD-50"



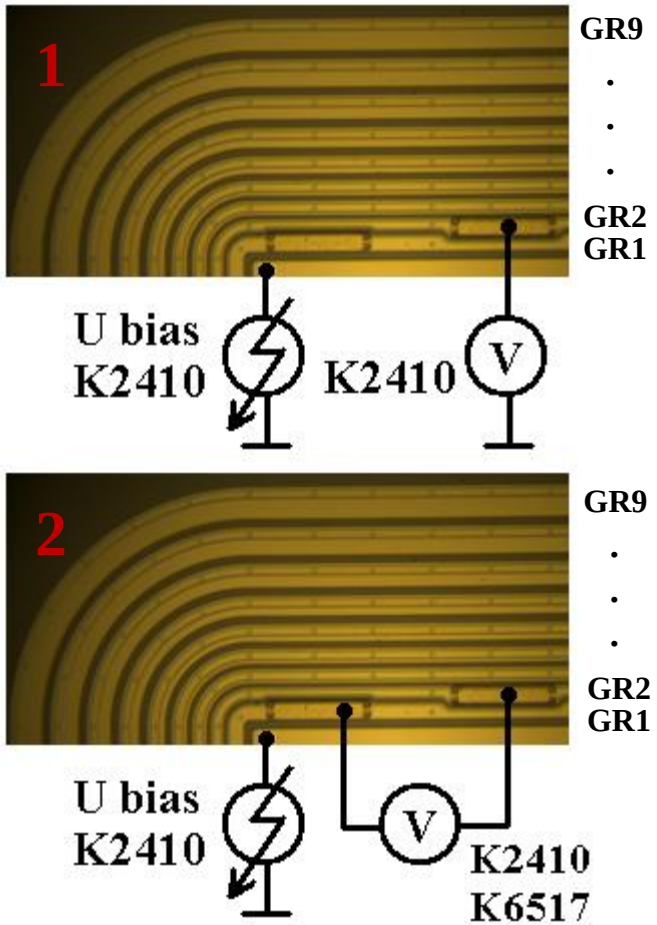
"Floating metal"



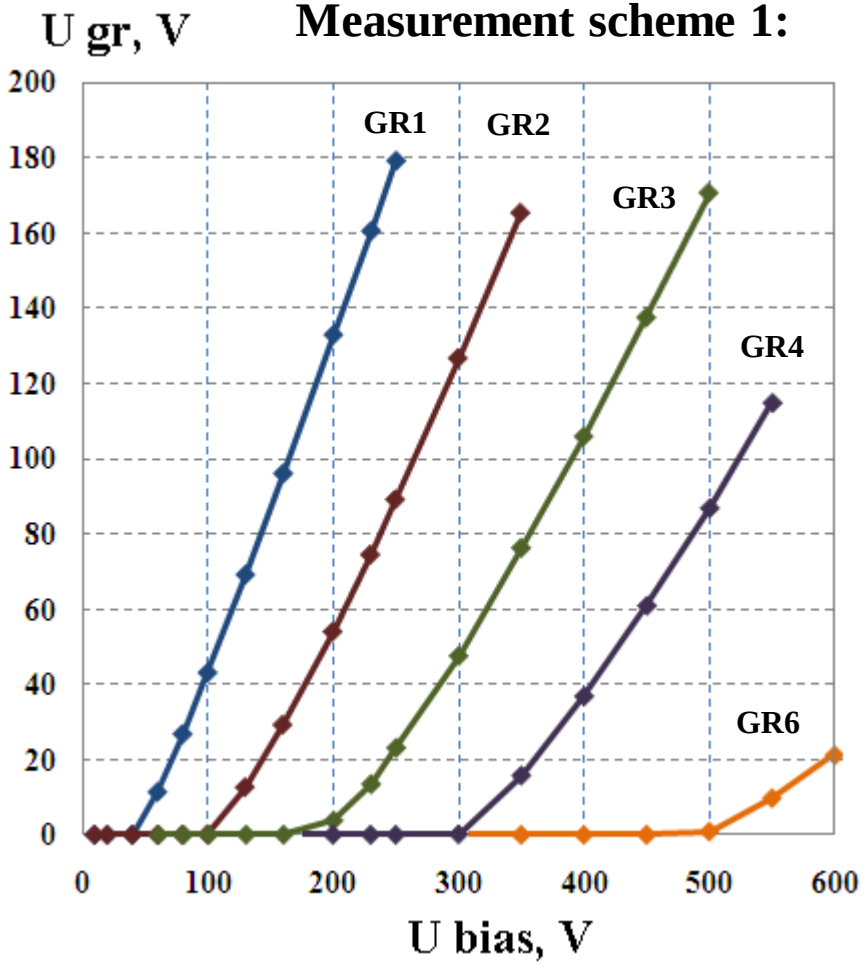
+ more geometries (new wafer)



Measurements of the Guard Ring Potentials



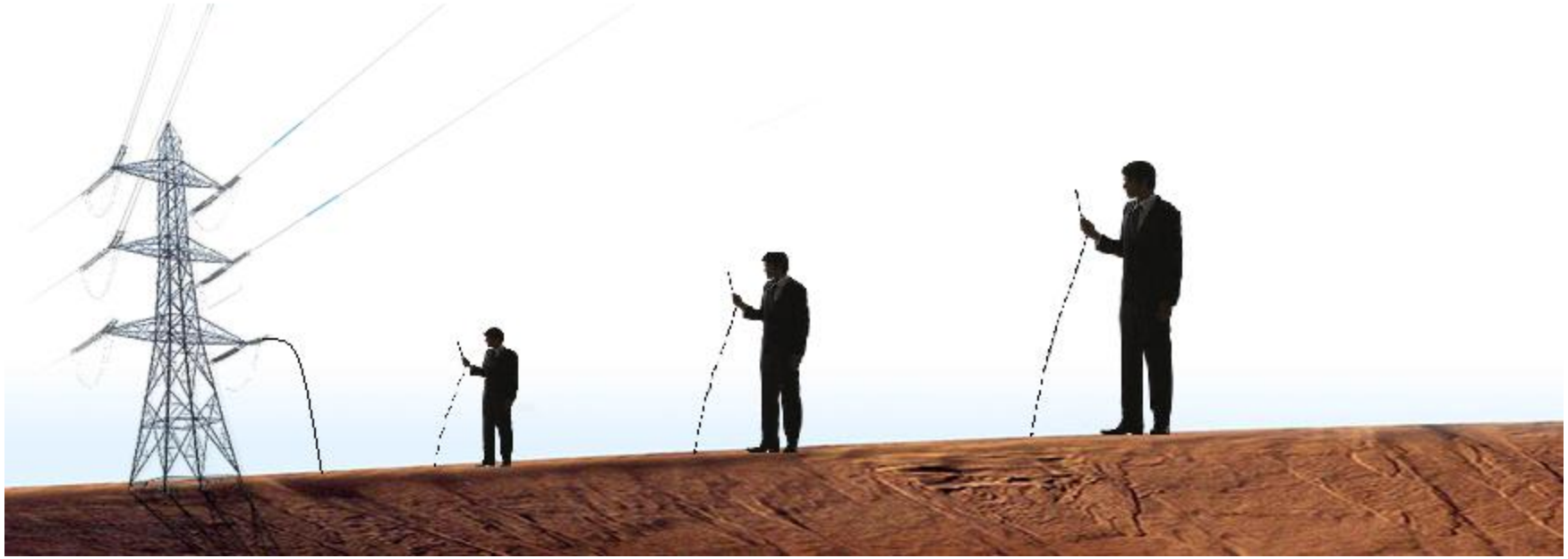
Measurement scheme 1:



GR has a substrate potential unless bulk depletion reaches it

Device modelling: guard structure is NOT a voltage divider !

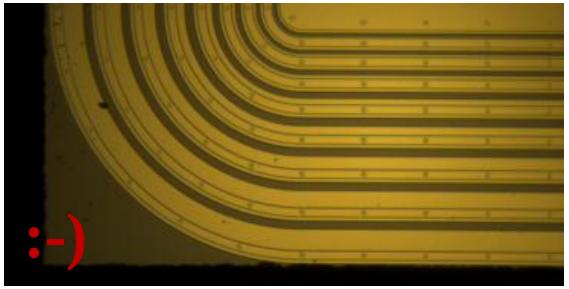
Measurements of the Guard Ring Potentials



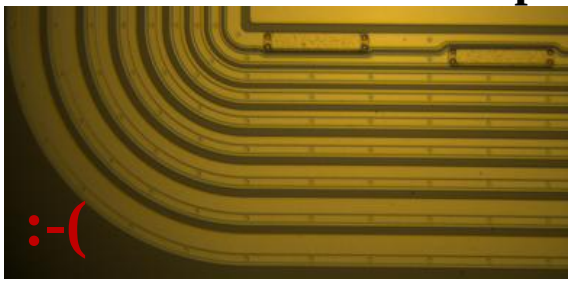
Interference with the Guard Structure

Probe pads

Straight implant and metal lines

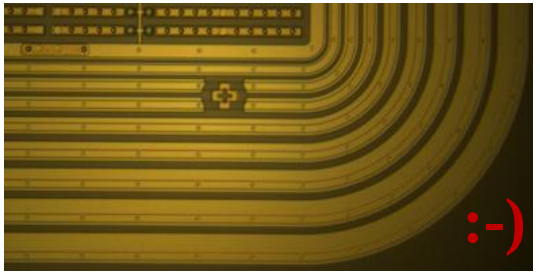


Thin and wide sections for pads

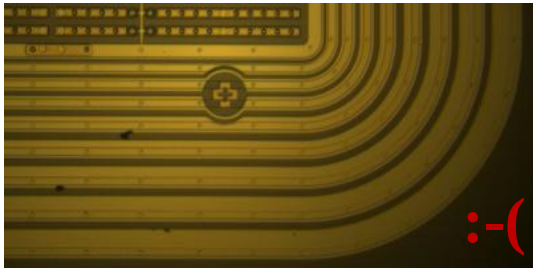


Alignment marks

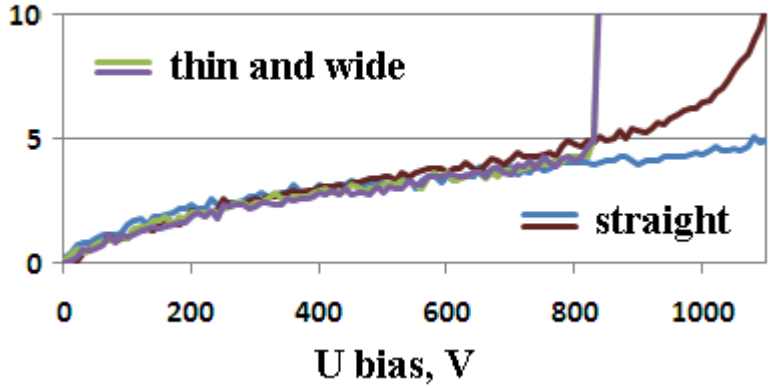
Straight implants, broken metal



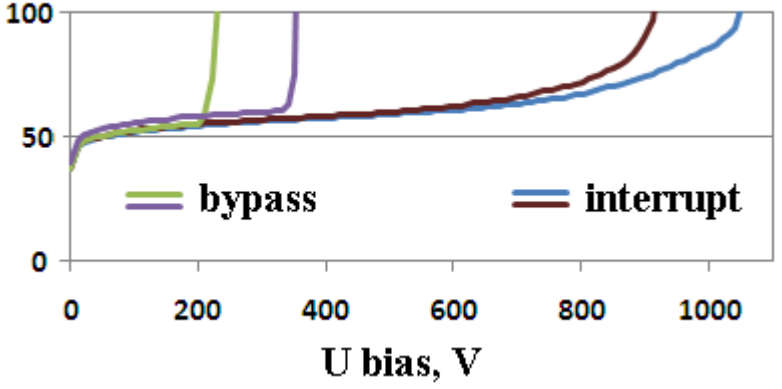
Thinned implants, metal bypass



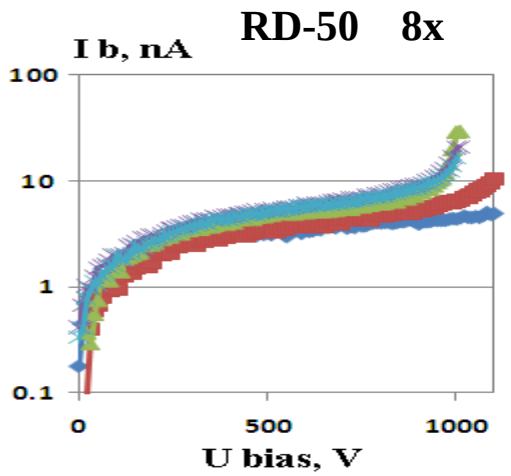
I b, nA I(V) curves for 4x4 mm² pads

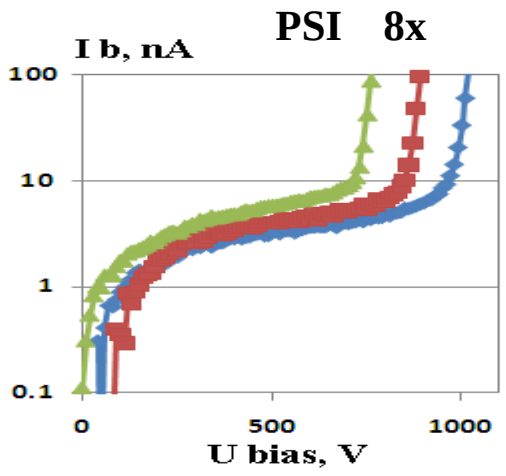


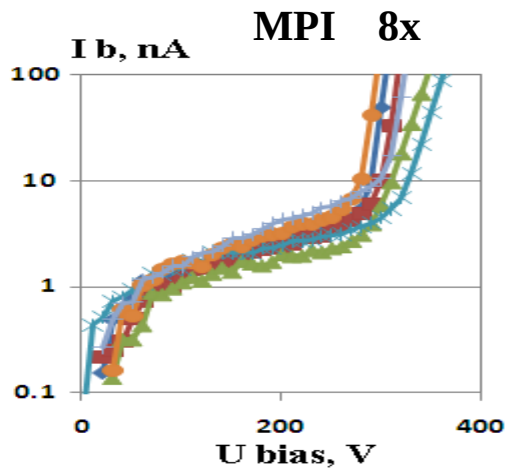
I b, nA I(V) curves for FE-I4 SC sensors

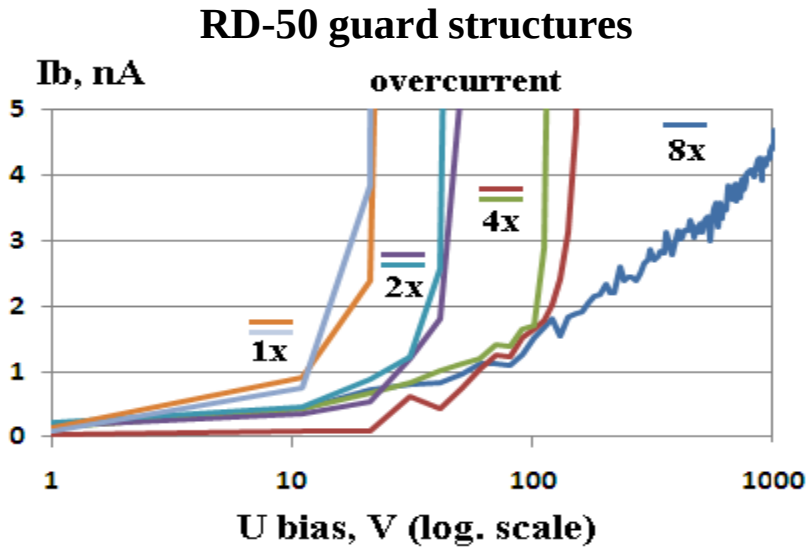


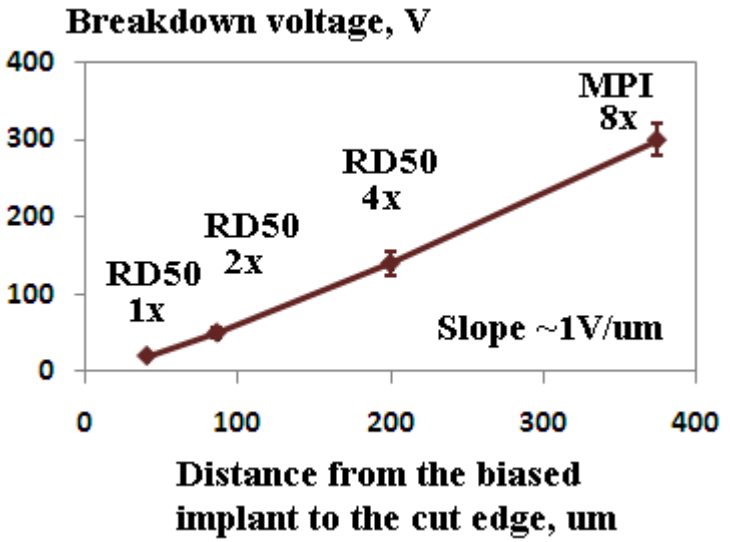
Cut Edge Studies







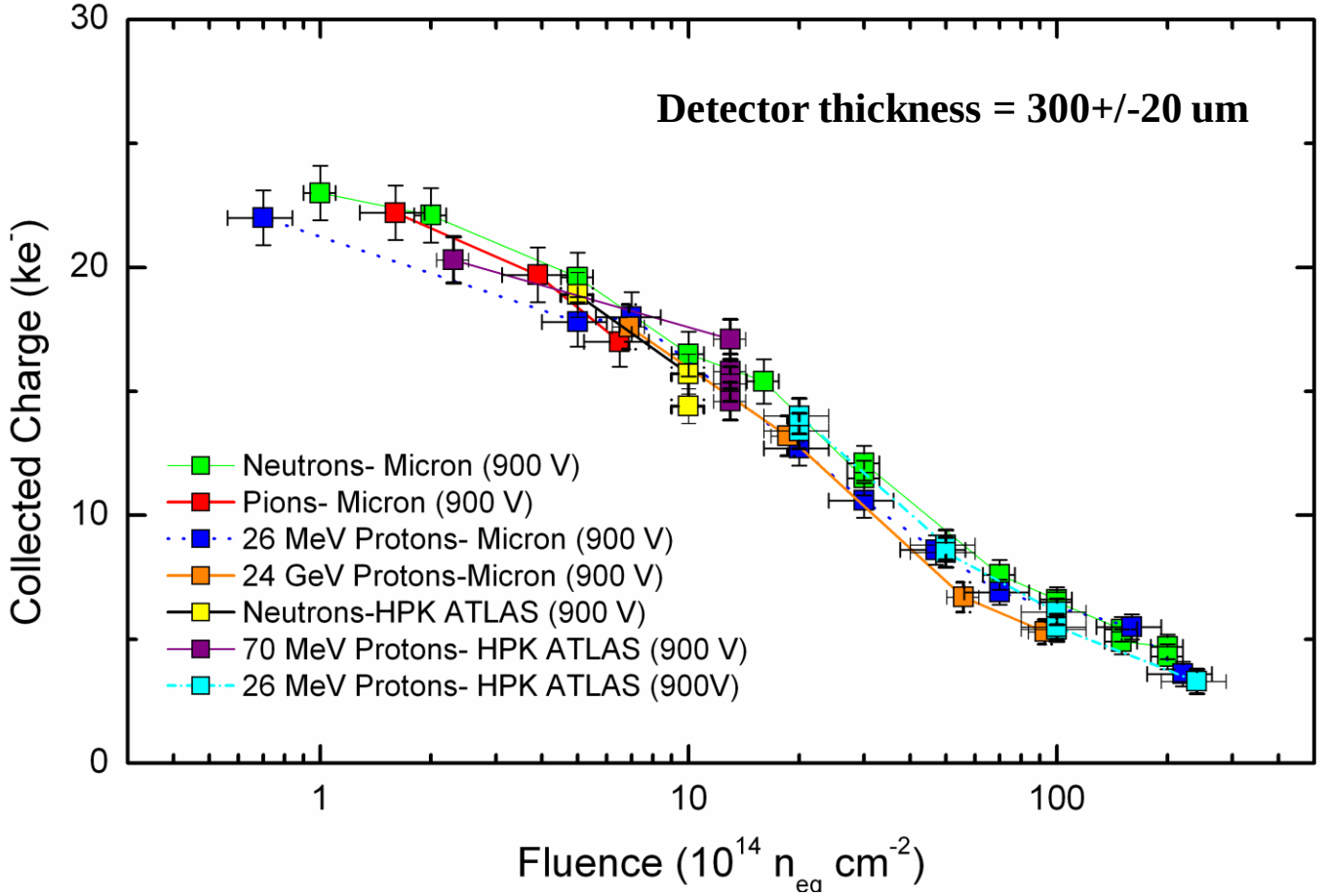




Breakdown condition: bulk depletion in the lateral direction reaches the cut edge

Charge Collection Measurements after High Radiation Doses

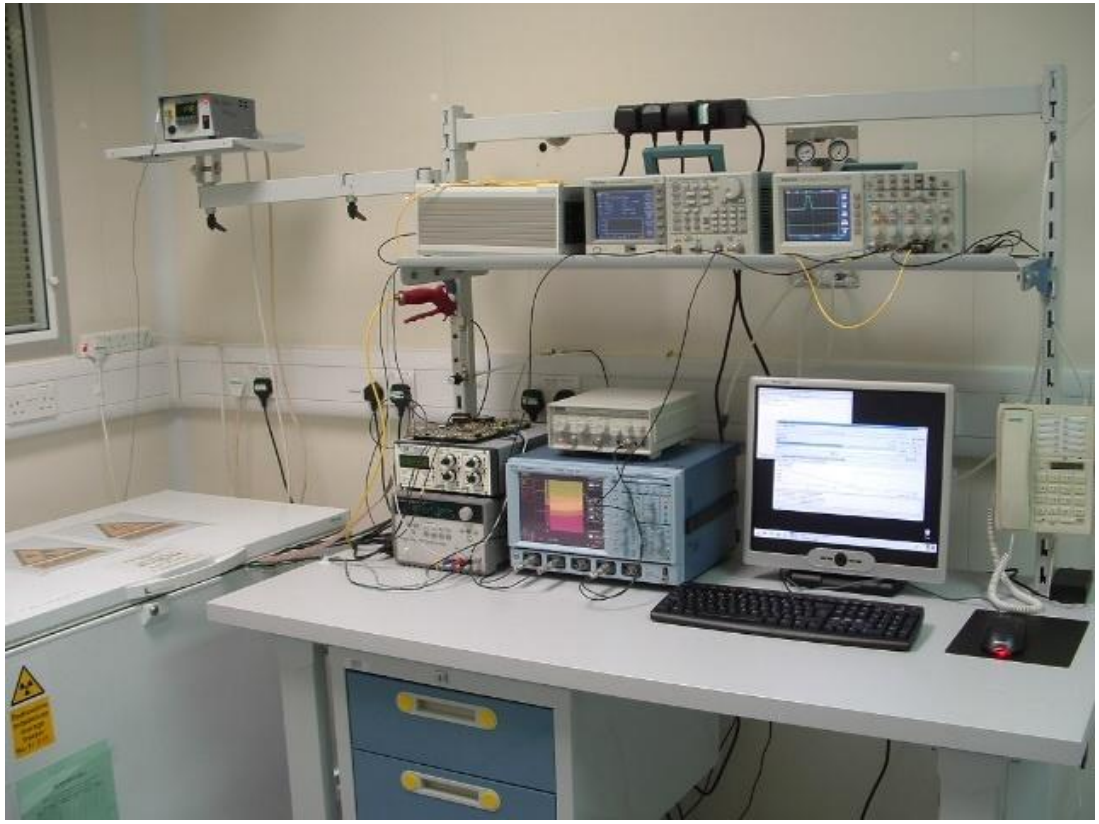
Measurements for the Micron n-in-p strip detectors using a data acquisition system based on the SCTA-128VG readout chip (40 MHz readout speed)



A. Affolder, et. al., NIMA (2010) doi.10.1016/j.nima.2010.02.187
K. Hara, et. al., NIMA (2010) doi.10.1016/j.nima.2010.04.090

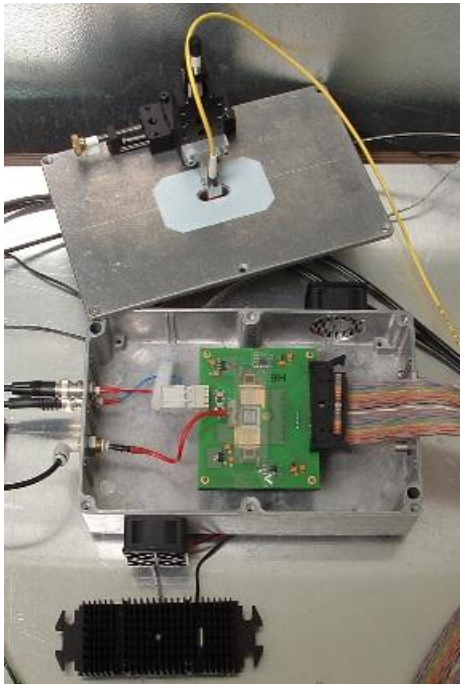
Alibava – a new Spectroscopy System

Analogue readout based on the Beetle V1.5 chip (40 MHz readout speed) Designed in collaboration with Barcelona and Valencia Universities



Cooling down to - 45 deg.C (ElCold EL11LT)

Signal generation with ^{90}Sr source or IR Laser (980/1060 nm) for charge collection & sharing studies

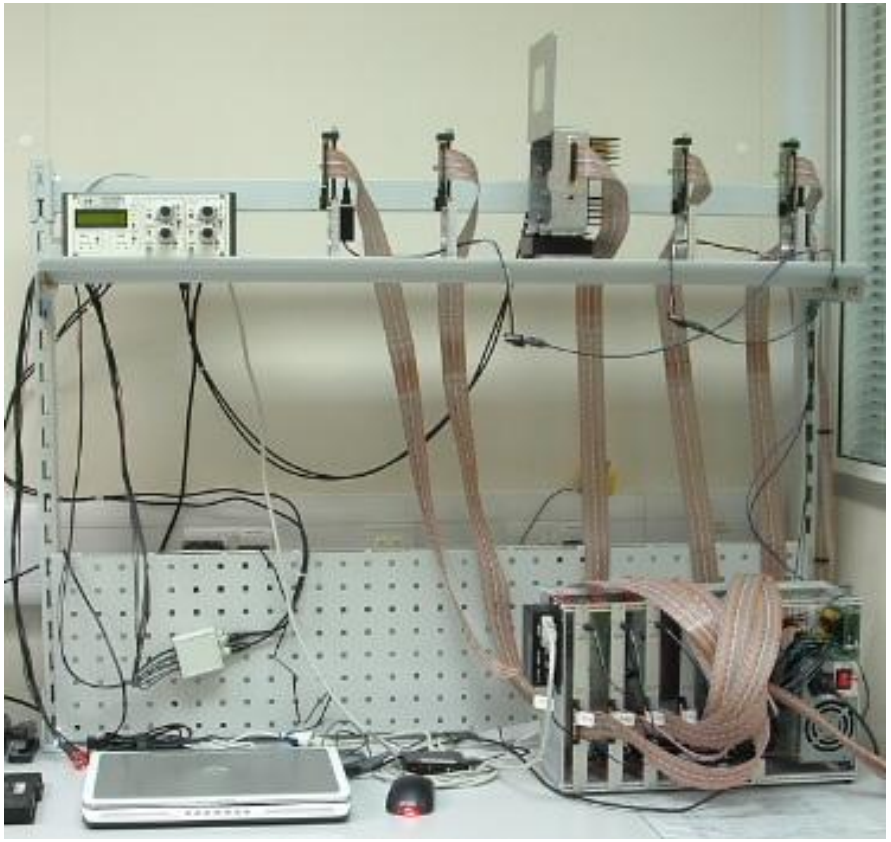


Coincidence trigger: layers of silicon pads or PMT assemblies

Beam Telescope

for the charge cluster analysis and spatial efficiency and resolution measurements.

Alibava readout of 4 XYT planes + up to 12 DUTs



DUT cooling (down to -25 deg. C) is based on a Peltier element for up to 200mW of the sensor's heating power

TDAQ is integrated as a master with the telescope for the device under test

PCB for studies of the irradiated pixel detectors. The chip + sensor assembly is detachable. The sensor is being cooled.

Summary

Design rules for a "safe" (in terms of HV) detector layout

Laboratory equipment:

- **2 "cold" probe stations (R&D and production)**
- **2 Alibava and 1 TDAQ spectroscopy systems**
- **Beam telescope**

Irradiation programme (24 GeV protons, 7×10^{15}, 1.5×10^{16} cm^{-2}), awaiting samples delivery from CERN

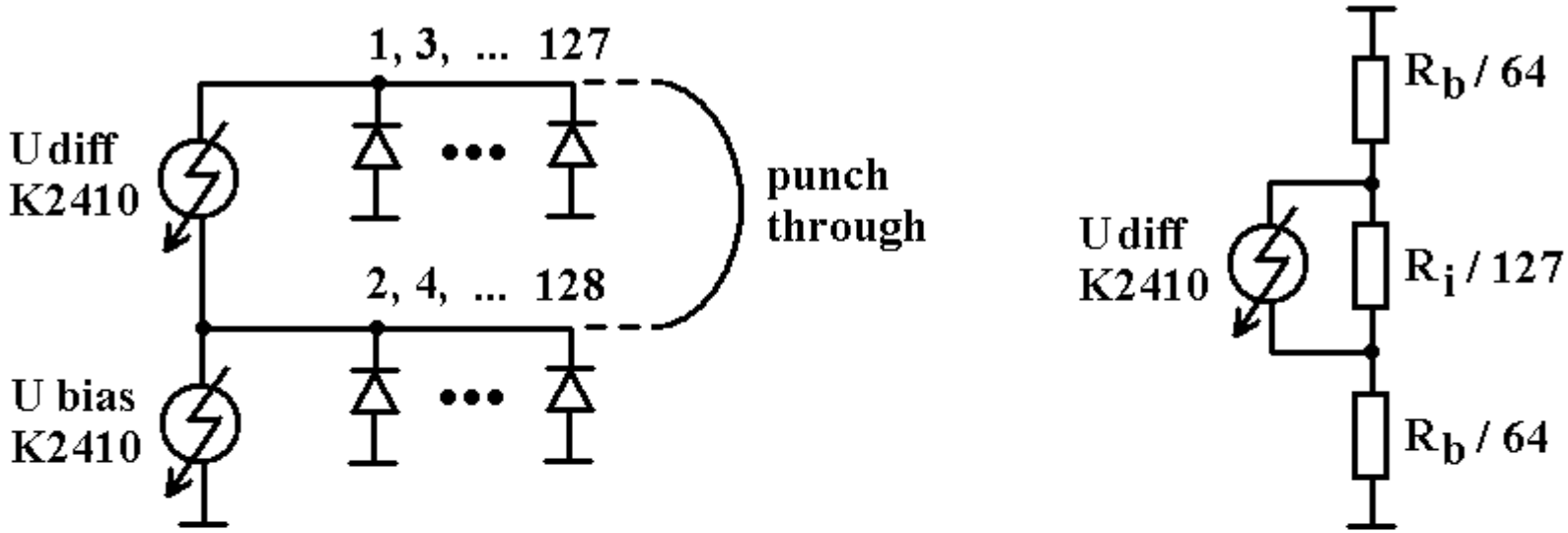
Atlas beam test at CERN (scheduled for July, postponed till October)

Acknowledgments

Many gratitudes to

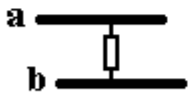
- **Gianluigi Casse for his patronage and patience**
- **Norbert Wermes for help with launching our pixel programme**
- **Ricardo Marco and Henry Brown for setting up the Alibava system**
- **Anthony Affolder and Valery Chmill for our discussions & co-work**
- **Micron Semiconductor Ltd for good detectors quality**

Spare Slide 1: Measurement of the Inter-“strip” Resistance



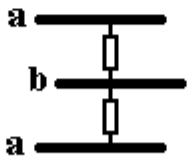
R_b (300 um depleted bulk) >> R_i

N strips = 2



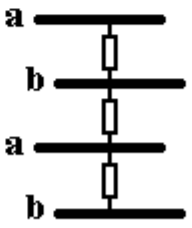
$R_{ab} = R_i$

N strips = 3



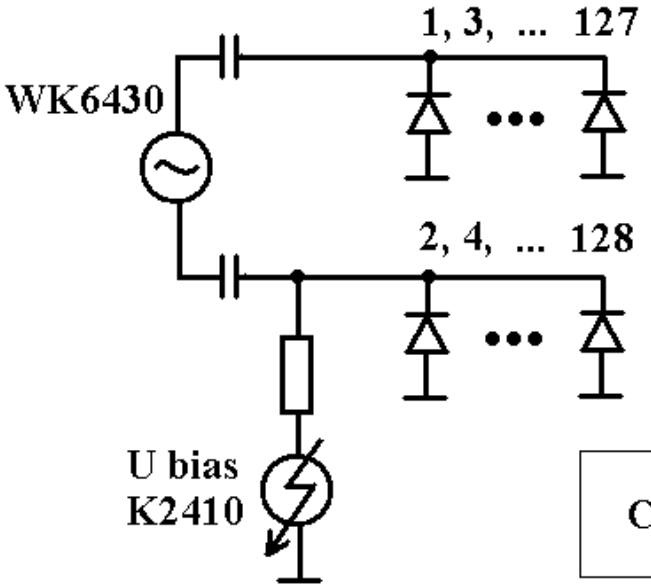
$R_{ab} = R_i / 2$

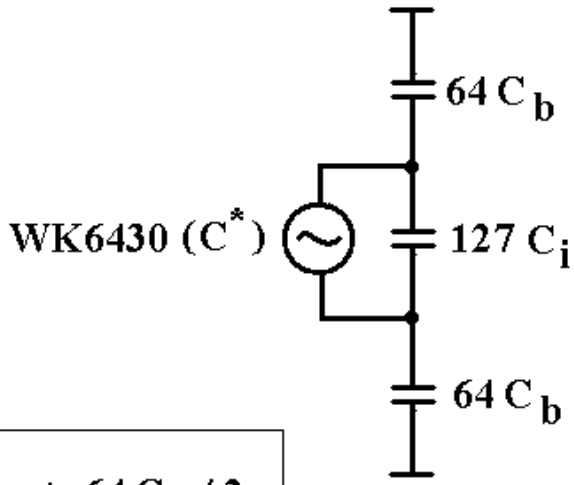
N strips = 4



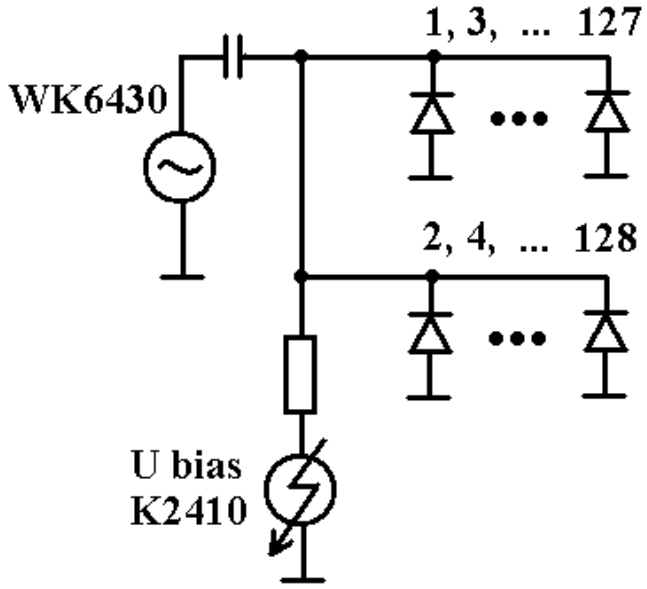
$R_{ab} = R_i / 3$

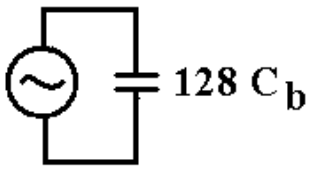
Spare Slide 2: Measurement of the Inter-“strip” Capacitance





$$C^{*} = 127\, C_i + 64\, C_b / 2$$





Spare Slide 3: Advantages of the “n-in-p” Technology

- **Variety of vendors, high yield**
- **Low manufacturing costs (3 masks for pixel sensors)**
- **Possibility of back-thinning for low material budget**
- **Easy mechanical handling of the backplane**
- **Can be operated under-depleted (not a case for the n-in-n detectors before their bulk type inversion)**
- **Low capacitive load for the readout compared to 3D**
- **Bulk type does not invert => simpler data analysis**

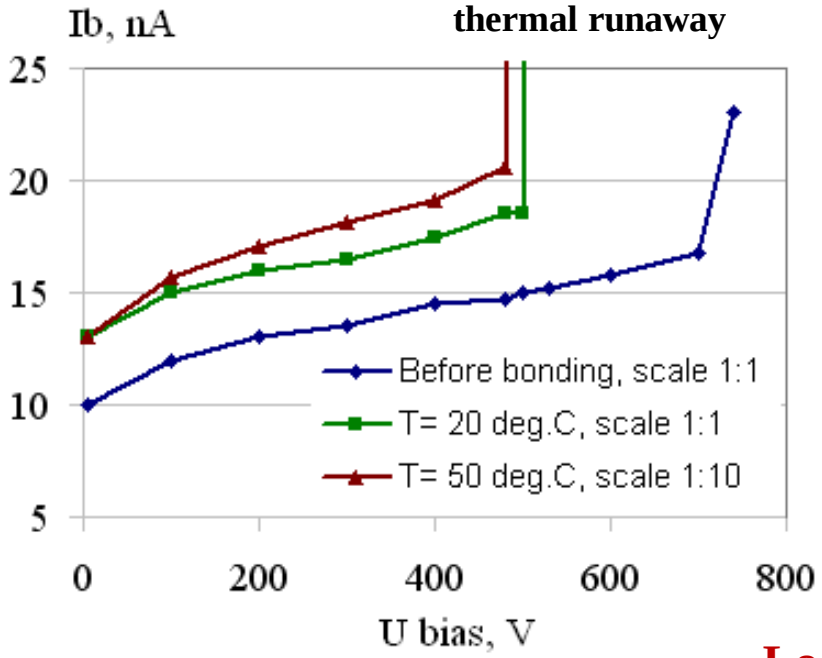
Potential Problems

- **HV discharge**

Spare Slide 4: Studies of Spark Conditions

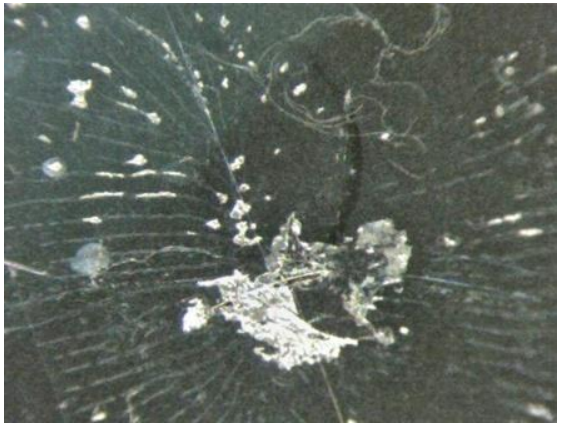
Dielectric strength of air = 3 MV/m (3V/um)

IV scans of the Atlas SC pixel sensor before assembly (blue) and after its bump bonding to the FE-I3 chip. The green line corresponds to unpowered ASIC (chip temperature = 20 deg.) and the red (scaled down by factor 10) shows IV during data taking when the chip heats to 50 degrees



The difference in Vbd before and after assembly is probably due to thermal / mechanical stress of the SC pixel sensor during its bump bonding to the R/O chip

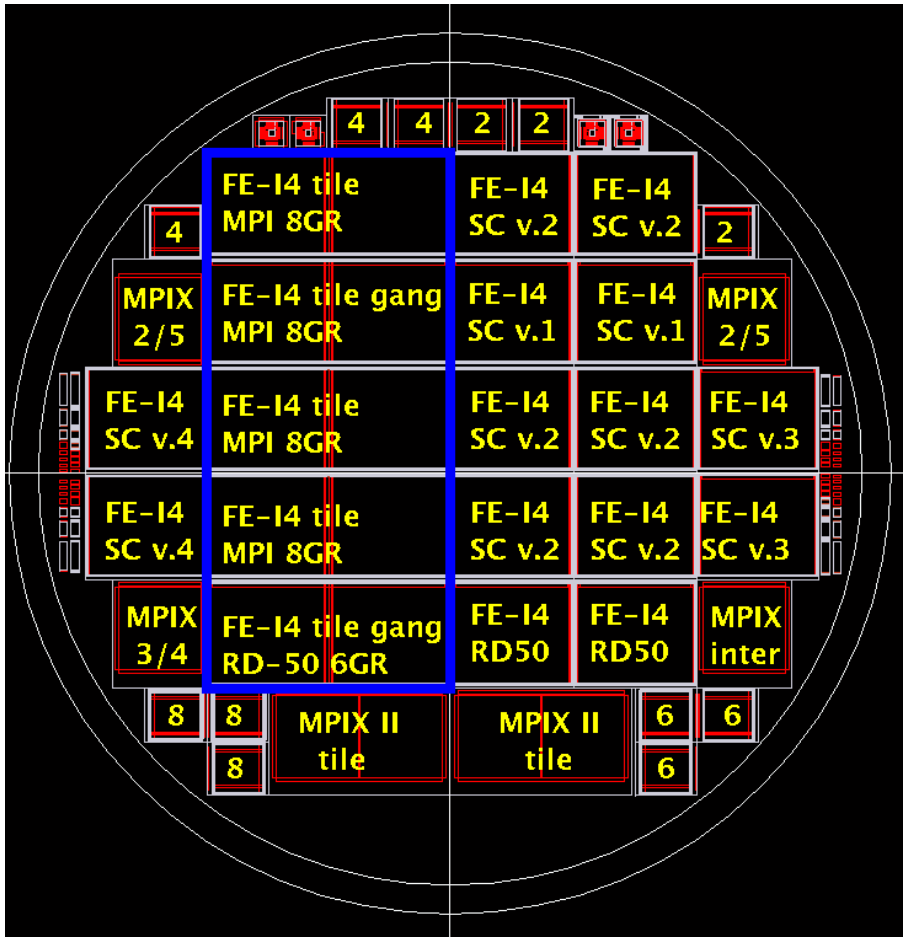
spot on the sensor's backplane



Looks OK, but there is no guarantee...

Spare Slide 5: new 6-inch Micron Pixel Wafer

n-in-p, single metal FZ process, 300um



There are plans to deliver n-in-n, and thinned wafers and 1 wafer with no capacitor oxide

5x FE-I4 tiles (2guard ring options, 250 um and 450 um)

14x FE-I4 SC (4 guard ring options, 450 um and 250 um)

12x FE-I3 SC (4 guard ring options, 40, 80, 200, 600 um)

2x Medipix-II tiles, 2x Medipix SC

4 diodes (process control, new GR)

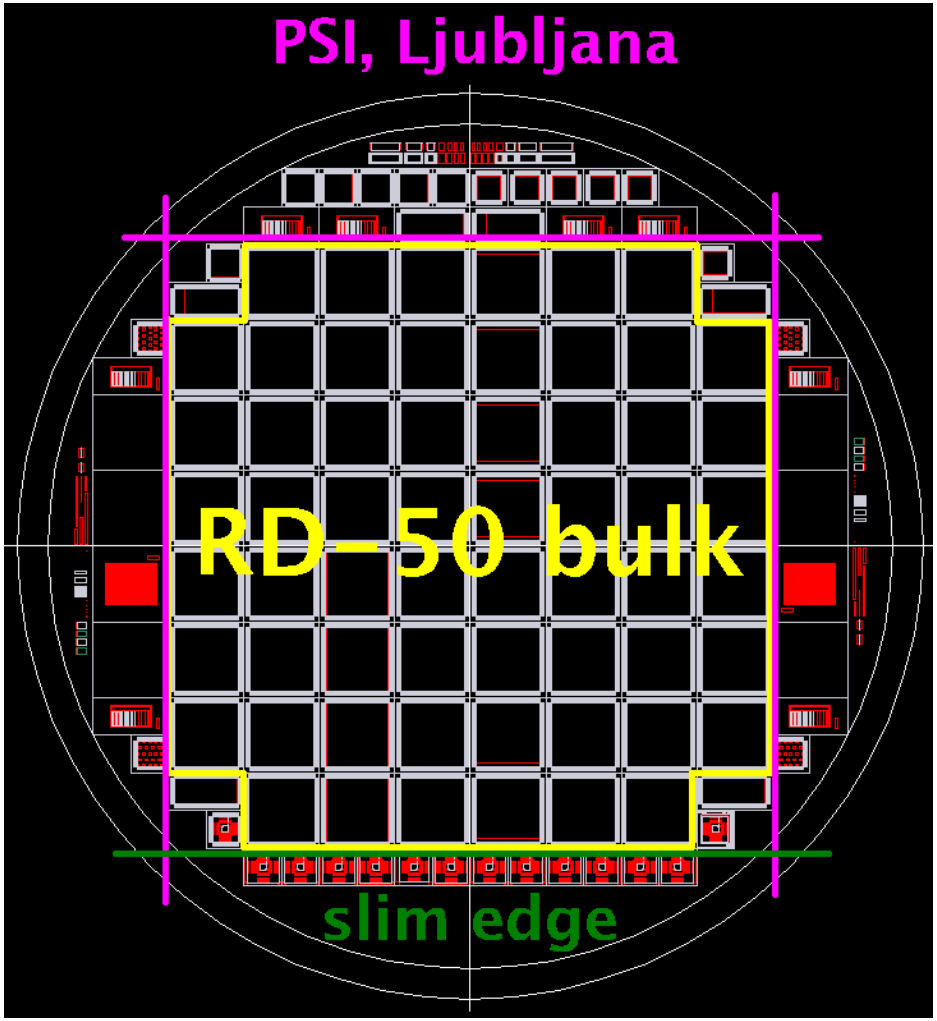
Test structures (transistor models, R, C, punch-through)

Delivery: 14.09 (first batch)

There is a room for 14x FE-I4 tiles (good homogeneity across the wafer)

Spare Slide 6: new 6-inch Micron RD-50 Wafer

n-in-p, single metal FZ process, 300um



Last call for submission

RD-50 bulk devices:

100 um, 80 um and 40 um pitch strip detectors with optional intermediated strips (biased and floating) and 3 different implant width for each type.

PSI and Ljubljana devices

Pad detectors for further slim edge studies (number of guard rings, GR implant width, via/trench contact)

Proposal of the RD-50 design depositary