A 130 nm ASIC prototype for the NA62 Gigatracker readout

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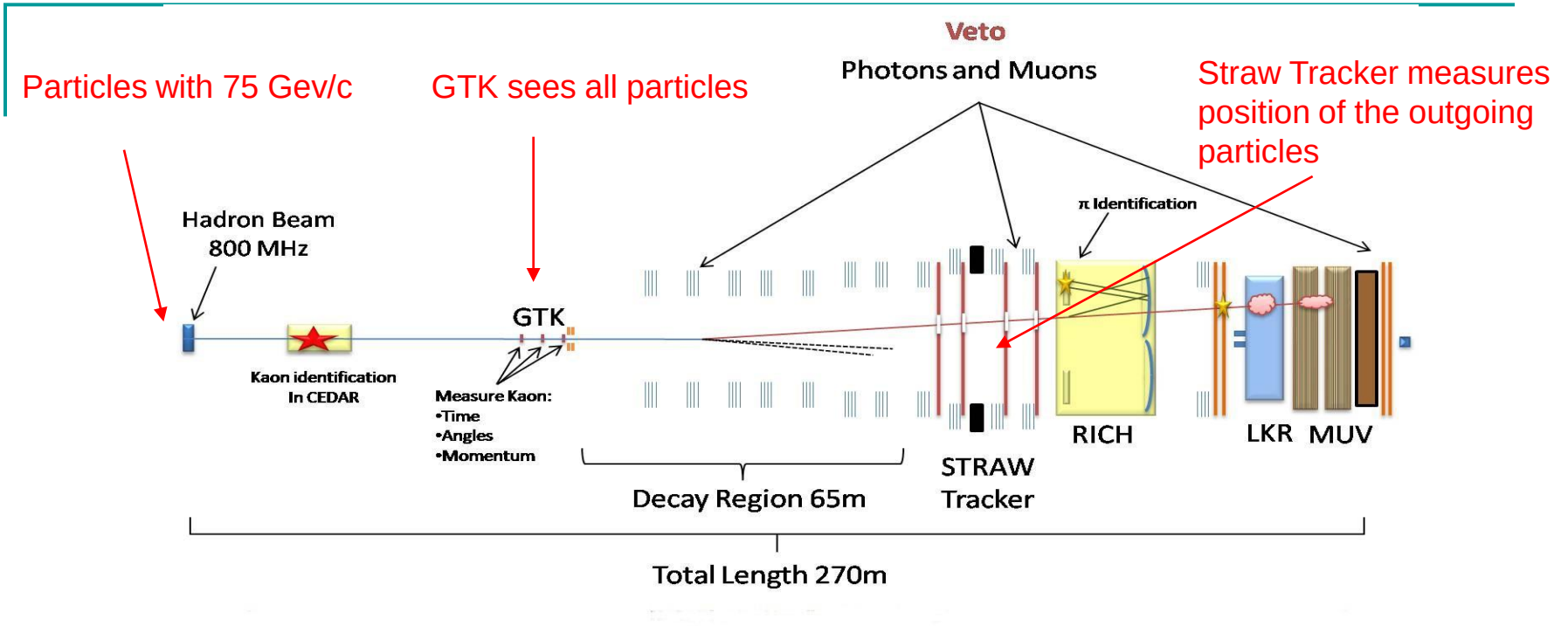
Outline

- Overview of the NA62 Gigatracker system
- Readout chip requirements
- Architecture of the TDC per Pixel (pTDC) readout chip (a different prototype called End of Column TDC[1] has been designed at CERN and it is now under test too)
- Test results
- Conclusions

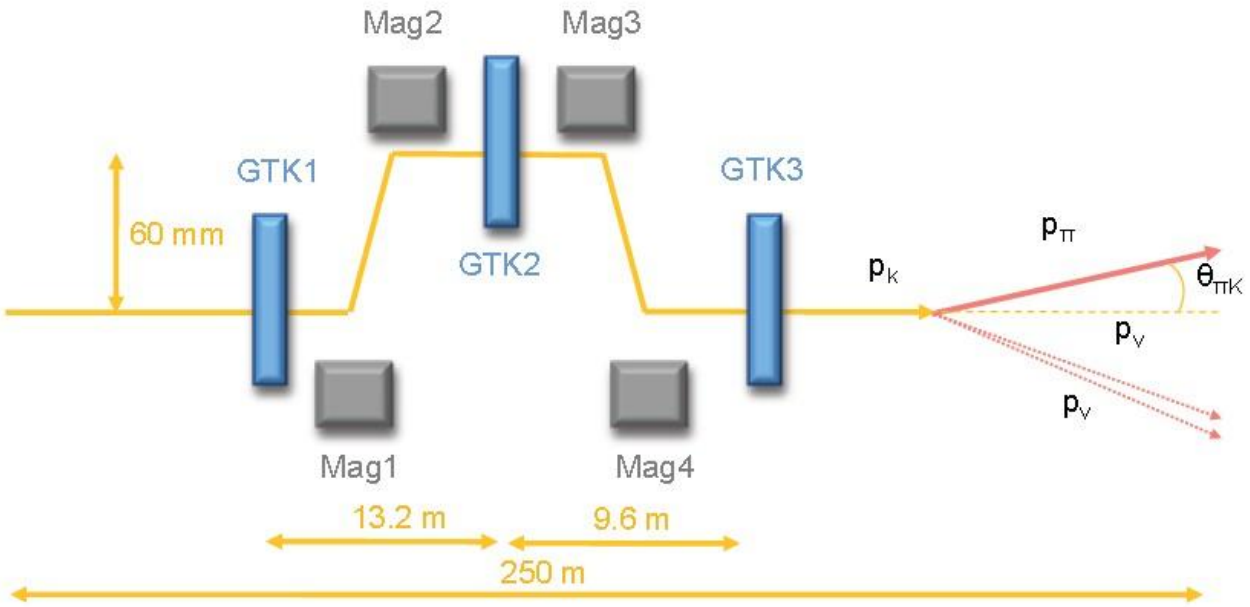
1. M. Noy et all, *The front end electronics of the NA62 Gigatracker: challenges, design and experimental measurements,* proceeding of 12th Topical Seminar on Innovative Particle and Radiation Detectors (IPRD10) in Nuclear Physics B.

NA62 experiment



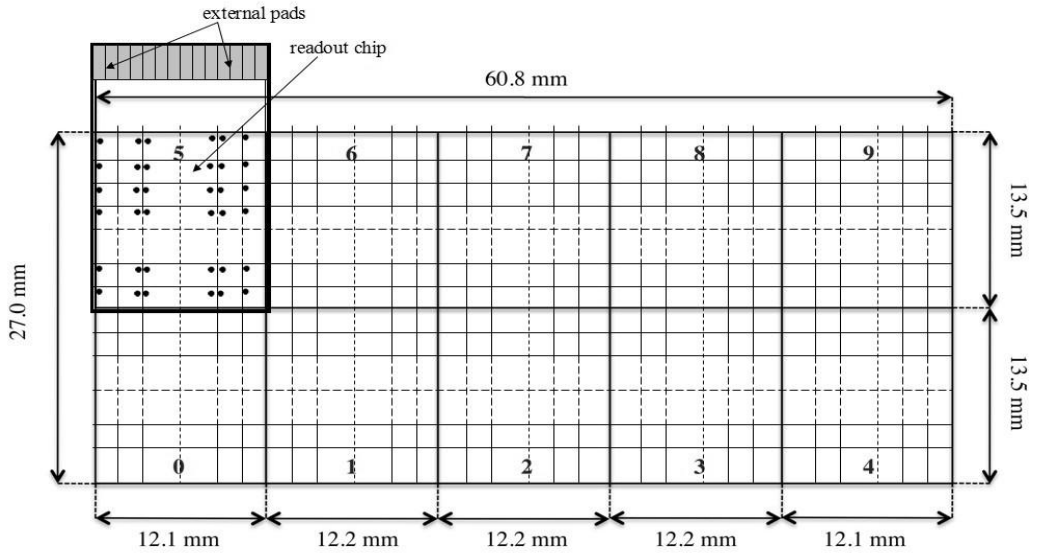
- The aim of NA62 at CERN SPS is to study the rare decay $K^+ \to \pi^+ \nu \bar{\nu}$
- The Gigatracker system provides momentum, time and direction of the incoming particles
- 20% of K^+ decays in the vacuum region, but only 10^{-11} is of interest
- Because of the high rate (800 MHz), in order to match tracks between GTK and Straw, the required time resolution is 150 ps rms per track

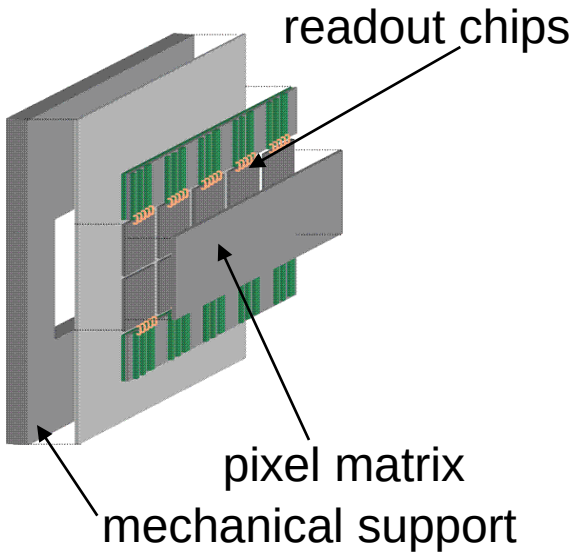
Gigatracker system



- Consists of three stations of hybrid silicon pixels sensors (p-in-n), operating in vacuum Each station covers an area of 60(X) x 27(Y) mm^2 and every pixel is 300 μm x 300 μm
- Beam intensity in the central area is 1.5 MHz/mm^2
- Required time resolution is 200 ps rms per station (150 ps rms for GTK). Spatial resolution is 150 μm rms (for GTK)
- Required material budget is 0.5% X_0 (sensor thickness 200 μm, readout chip thickness 150 μm)

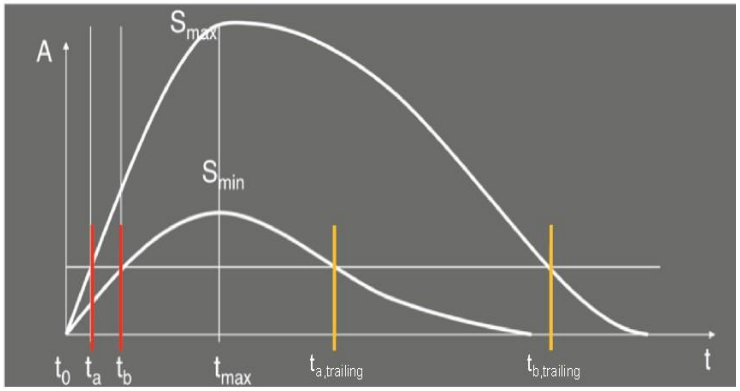
Readout chip requirements

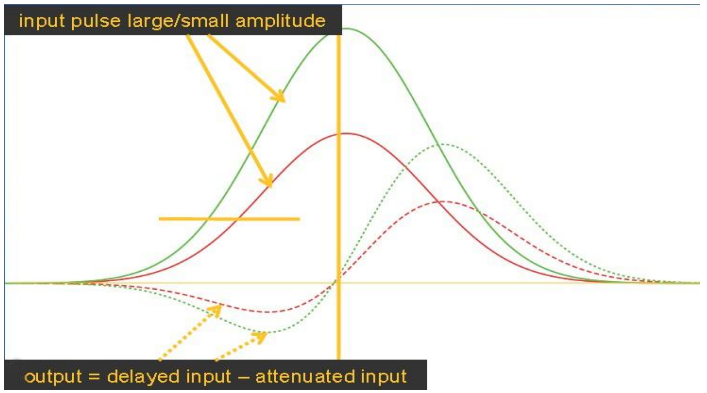




- Two rows of 5 readout chips (CMOS 130 nm) are bump-bonded to the sensor. Every chip reads a matrix of 45 x 40 pixels and has a size of 12 x 20 mm
- Maximum particles intensity per chip: 130 MHz
- Maximum particles intensity per pixel: 140 kHz
- Average data rate per chip: 4.2 Gb/s (6 Gb/s accounting for the fluctuations): the readout is trigger less
- Total dose in one year: 10^5 Gy: the system must be cooled below 5^0 C and replaced every 60 working days (one year of data taking)
- Power budget: lower than 2 W/cm^2 per chip (32 W per station)

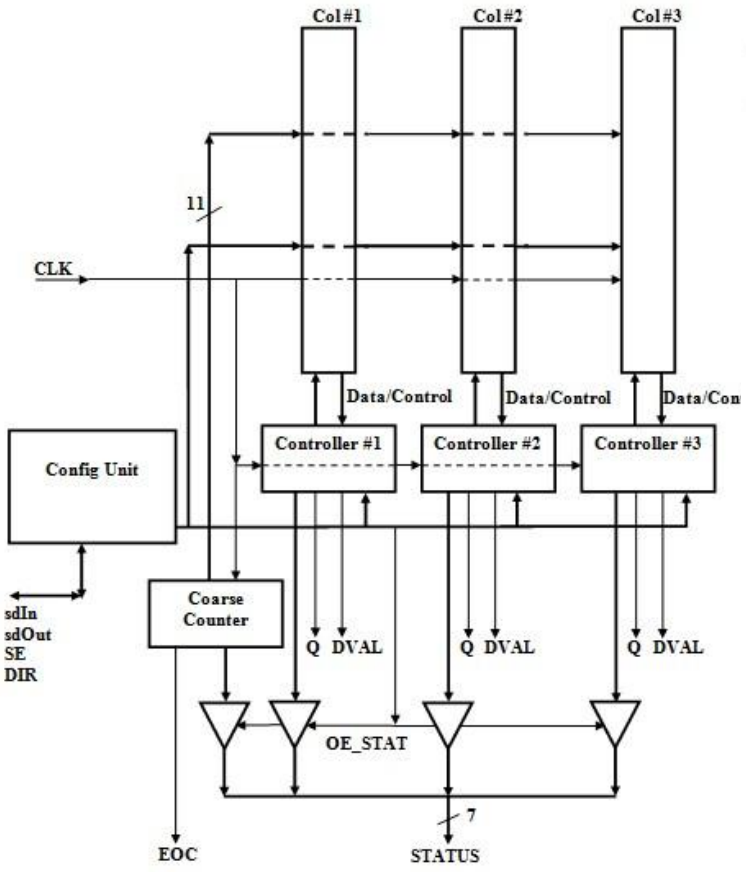
Time walk and time measurement

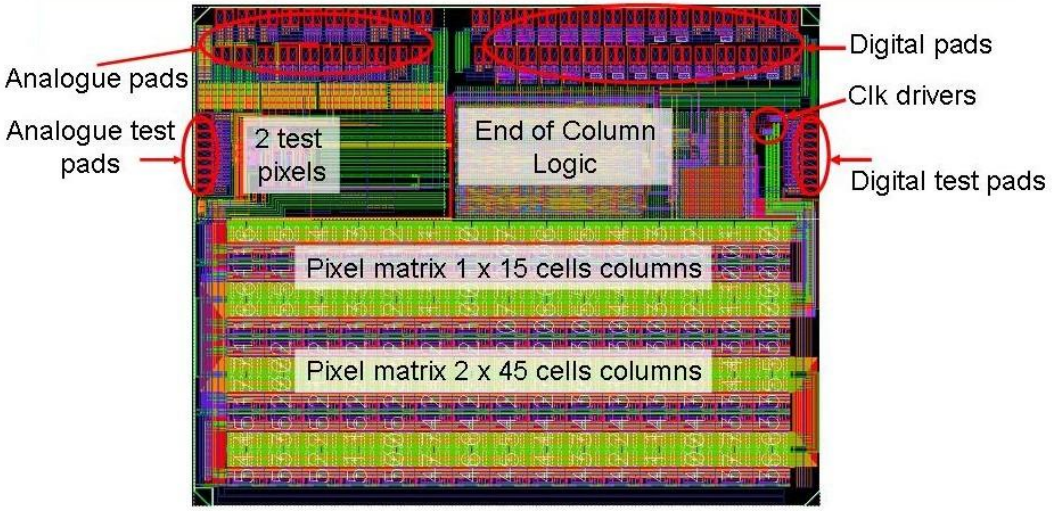




- With a dynamic range of the input signal between 5000 and 60000 e^- (avg. 15000 e^-) the time walk compensation is mandatory to achieve the required time resolution (~100 ps rms per chip)
- In the TDC per Pixel (pTDC) prototype the time walk correction is performed by a Constant Fraction Discriminator (CFD):
  - Complex analogue circuit
  - One measurement only for each hit
- The time measurement is the combination of a Course and a Fine time information. The first one is performed by a clock counter (160 MHz). The second one is obtained by a Time to Digital Converter (TDC) based on a Time to Amplitude Converter (TAC) circuit, implemented on each pixel

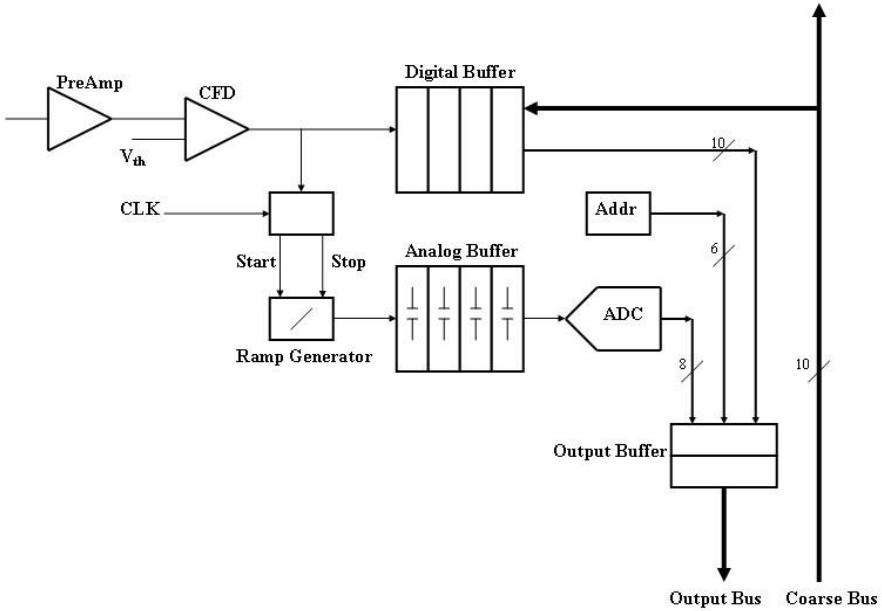
ASIC prototype architecture





- CMOS 130 nm DM
- Two 45-pixel columns and one 15-pixel column, fully equipped
- Three independent End of Column readout
- Two test pixels (only analogue)
- LVDS 2.5 V digital pads (except digital test pads, CMOS 1.2 V)

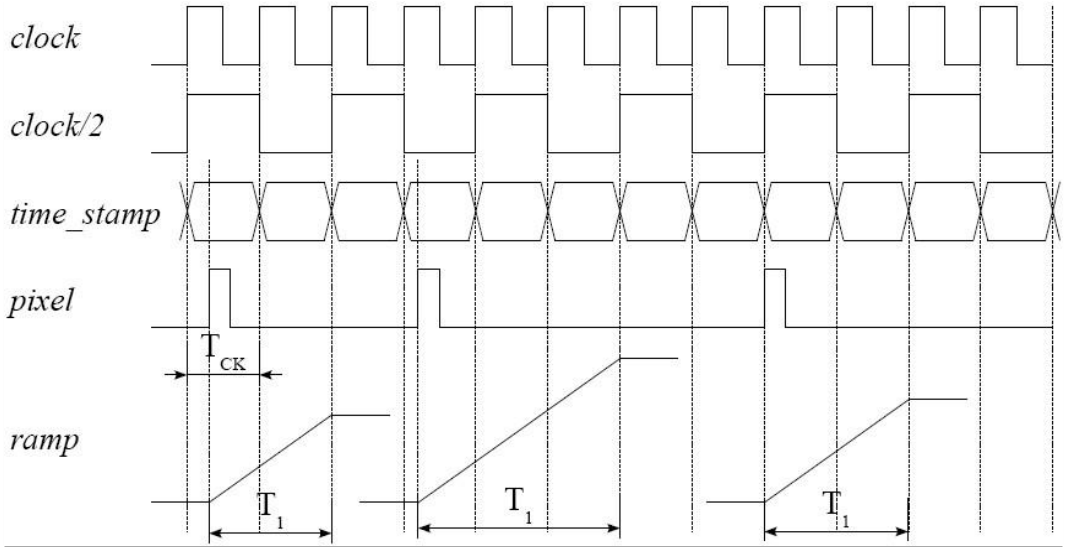
Analogue cell



- Time stamp is given by a 10-bit Gray counter distributed through the whole chip
- CLK freq. 160 MHz
- Preamplifier and CFD are differential in order to use the same chip with p-in-n or n-in-p sensors
- CFD output latch the counter content to define the Coarse Time

- CFD output start a ramp to charge a reference capacitor.
- To define the Fine Time a Wilkinson ADC converts the voltage, which is proportional to the time distance between signal and CLK
- The local derandomization is performed by a 4 level buffer placed before the A/D converter
- Coarse and Fine time information are grouped in the output buffer

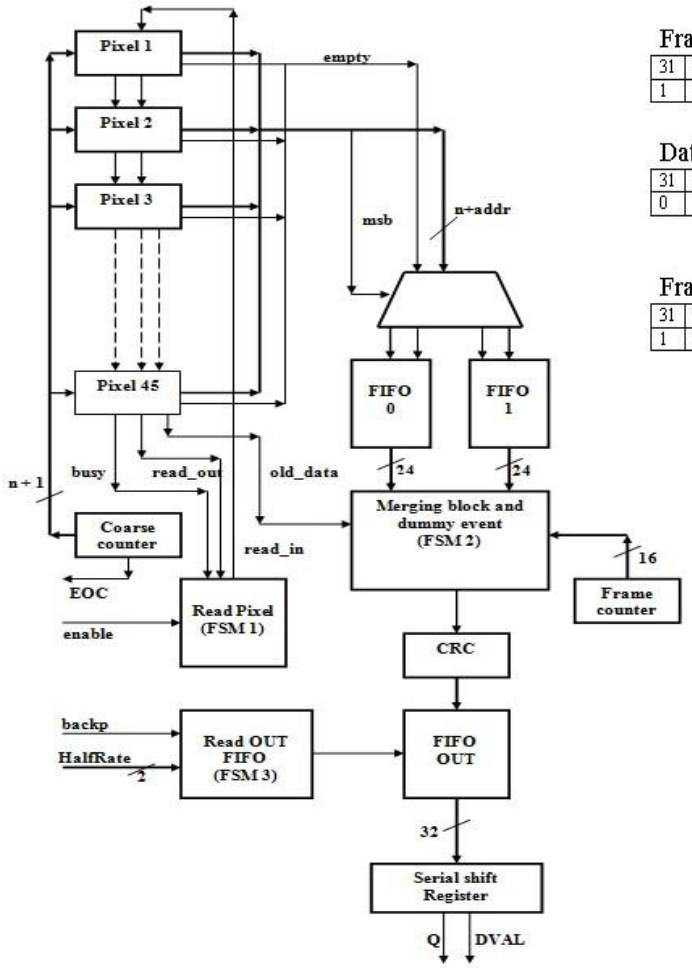
TDC behaviour



- With the clock frequency 160 MHz a 6-bit fine time should be enough to reach the 100 ps timing resolution
- Fine time is 8-bit encoded. Extra bits can be used for off line corrections
- To guarantee an adequate charging ramp length the half frequency clock is used

- The ramp has stopped on the first CLK rising edge after the CLK/2 falling edge
- The analogue to digital conversion is performed by the discharge of the reference capacitor with a current 64 times lower than the charging current. A clock counter measures the discharging time
- TDC resolution: 6.25 ns /64 = 97.65 ps
- The maximum conversion time is 64x3x6.25 ns = 1.2 μs => 192 clock cycles (7.5 bit)

End of column readout



Frame header

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1						Frame number																							

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				Column address				Pixel address						Coarse measure												Fine measure							

Frame trailer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0						Word counter								CRC-16															

- The digital output data are grouped in frames. Each frame is a whole turn of the Coarse counter (6.4 μs)
- Trailer contains the CRC-16 code ($X^{16}+X^{15}+X^{2}+1$) which guarantees an error coverage of 99.9984% with data length < 2^{15} bit (1024 words 32-bit long)

SEU aspects

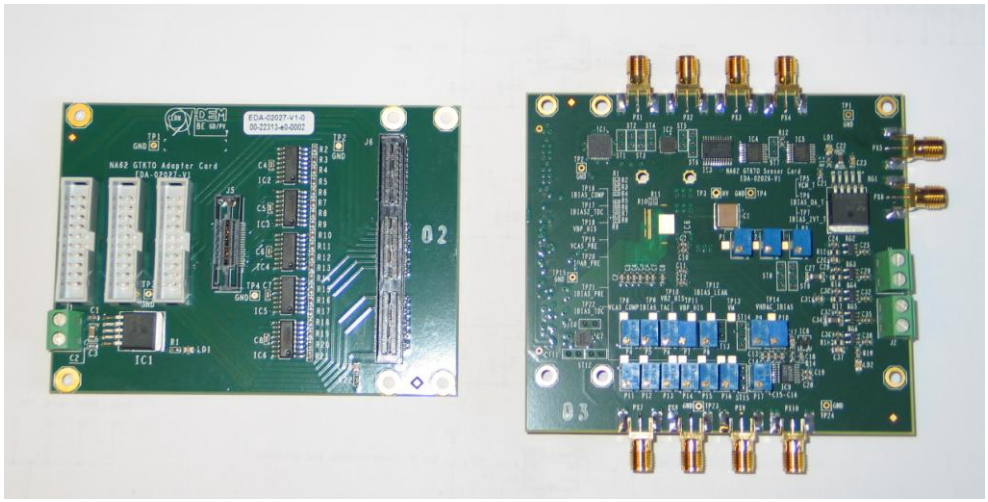
Bit position		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Encoded data bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8	d9	d10	d11	p16	d12	d13	d14	d15	
Parity bit coverage	p1	X		X		X		X		X		X		X		X		X		X		...
	p2		X	X			X	X			X	X			X	X			X	X		
	p4				X	X	X	X					X	X	X	X					X	
	p8								X	X	X	X	X	X	X	X						
	p16																X	X	X	X	X	

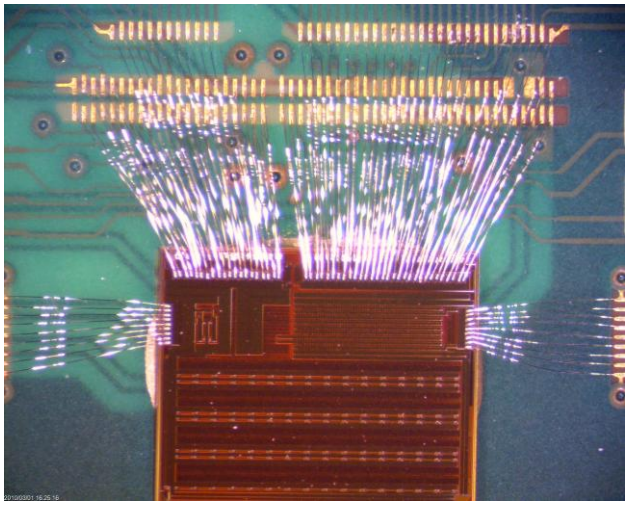
The sum of the positions of the erroneous parity bits identifies the erroneous bit.

e.g. if P1 e P4 are wrong => the error is in bit 1+4 (D2)

- Because of the strong radiation exposure all the digital circuits must be Single Event Upset protected
- Both in the pixel cell and in the end of column, all the registers, state machines and counters are Hamming encoded (single error correction and double error detection, every clock cycle)
- The end of column FIFOs (where the rate is two orders of magnitude smaller than in the center of the chip) the data correction is applied only at the output of the buffer (not every clock cycle)
- SEU probability in those FIFOs is 6 10^{-10}
- Number of extra bits with Hamming codes is lower than using triple redundancy

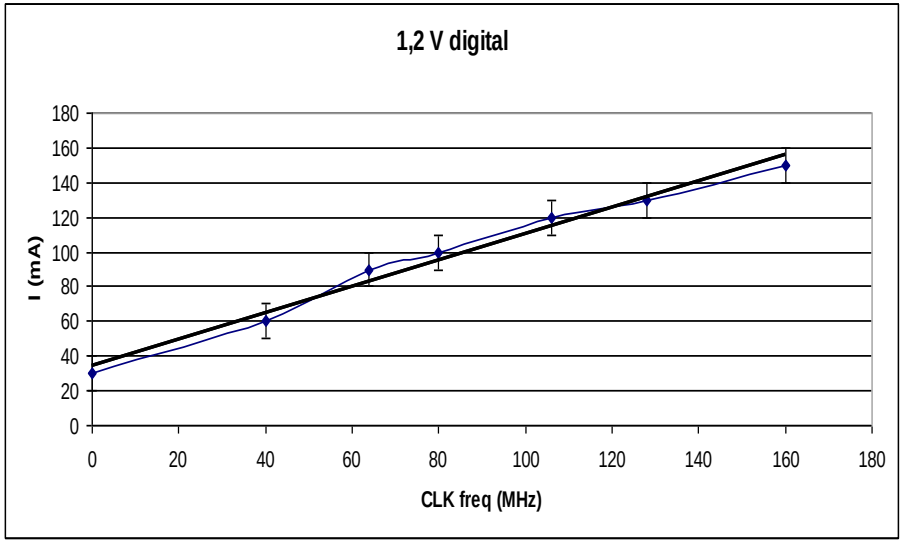
Test setup

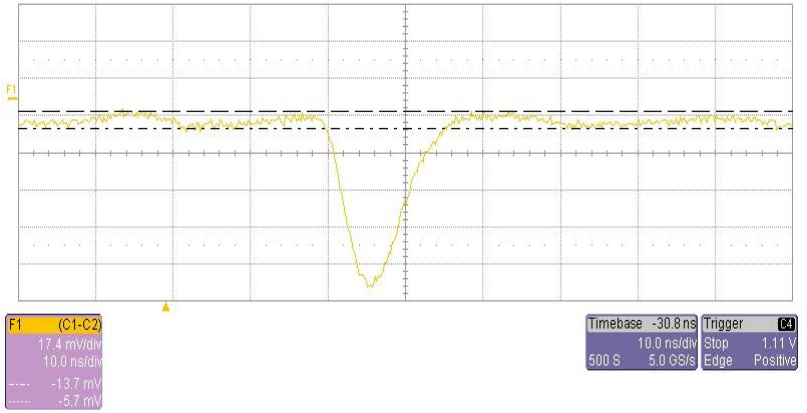




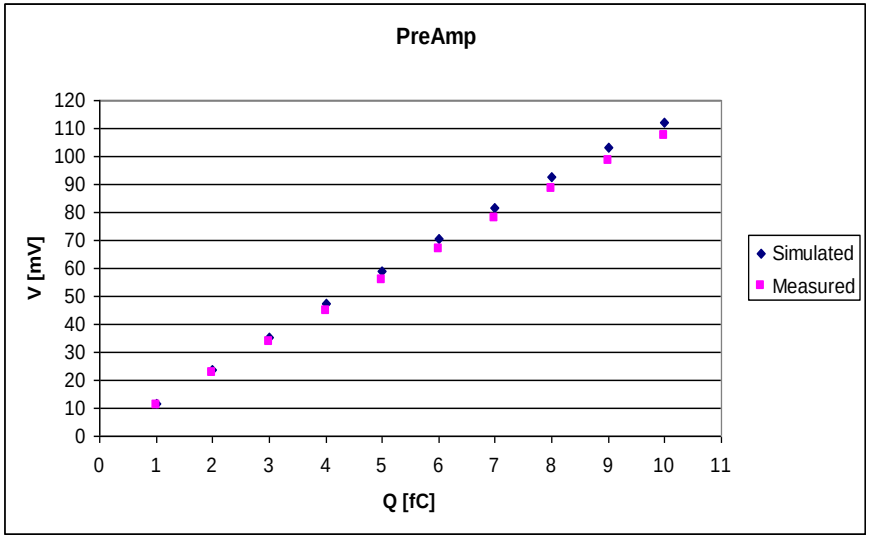
- Chip wire bonded on the sensor card
- Measurements performed by LSA and pattern generator (by the use of the adapter card) or by a FPGA development kit (Altera Stratix III)
- All instruments controlled through a LabView system

Power consumption / Preamp. out

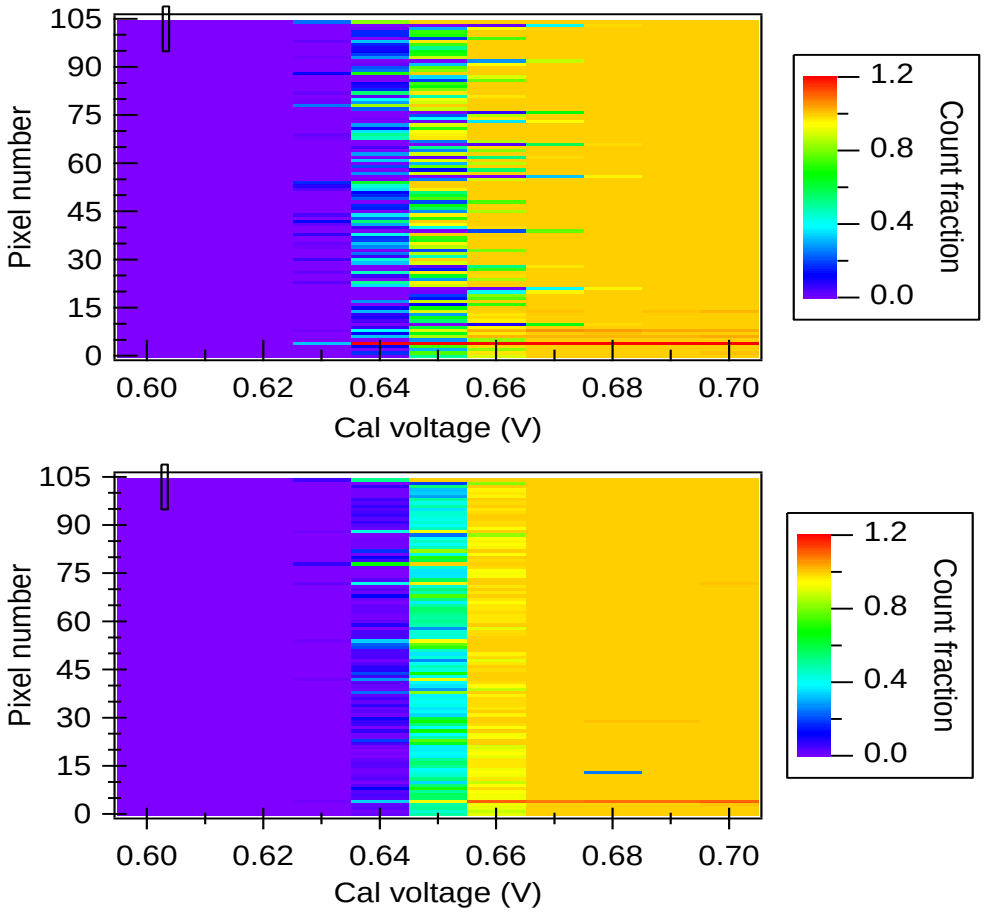


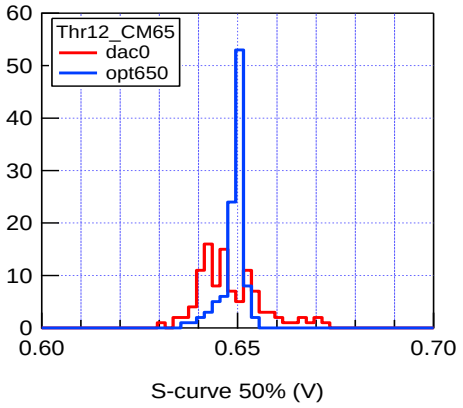


1.2V digital	150 mA
1.2V digital (test pixels)	30 mA
1.2V analogue	80 mA
2.5 V LVDS pads	60 mA



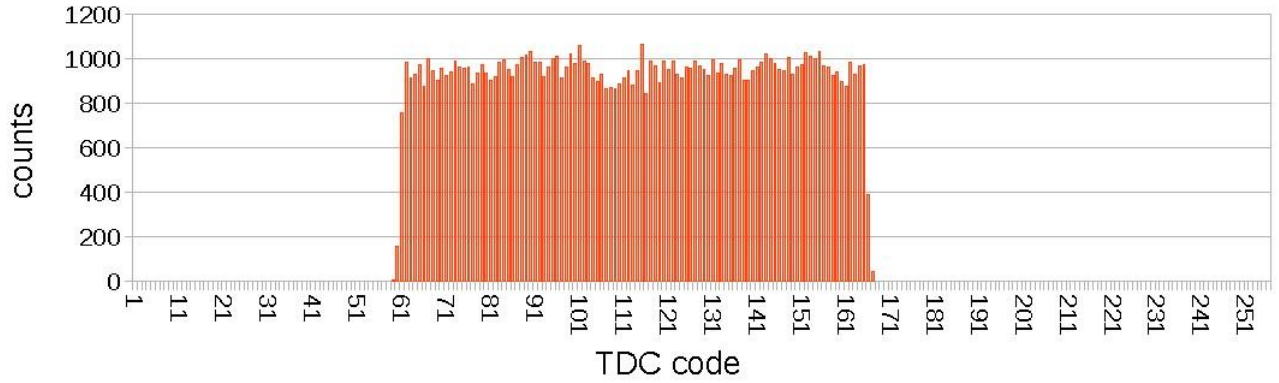
Efficiency

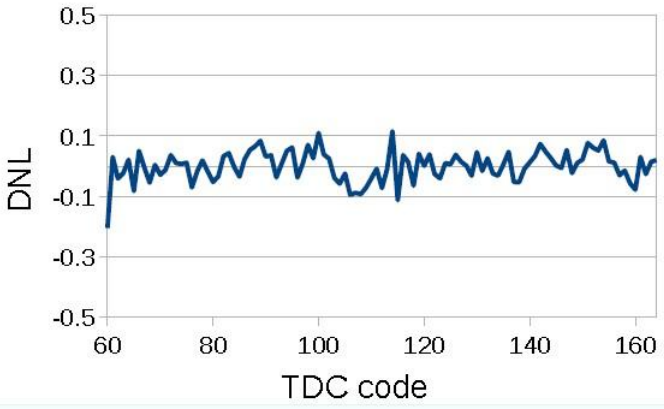


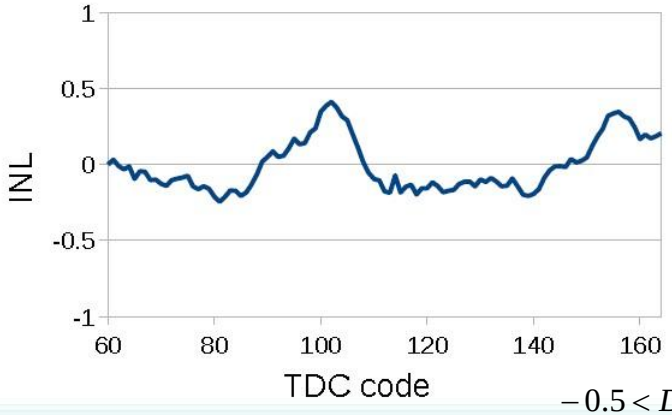


Input charge scan before and after local DAC tuning (1 fC ~ 45 mV)

TDC linearity





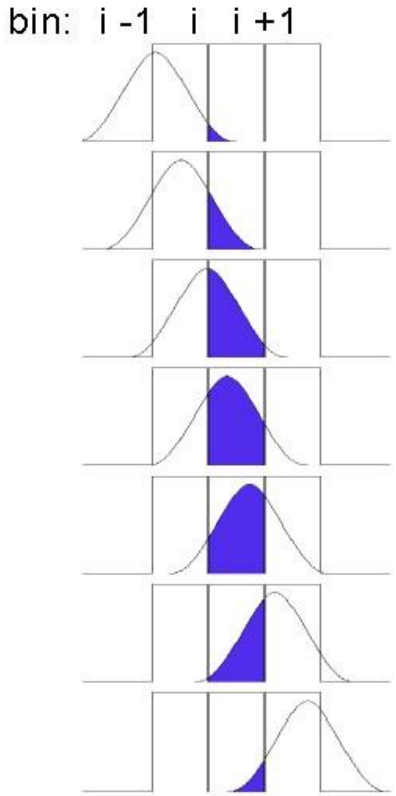


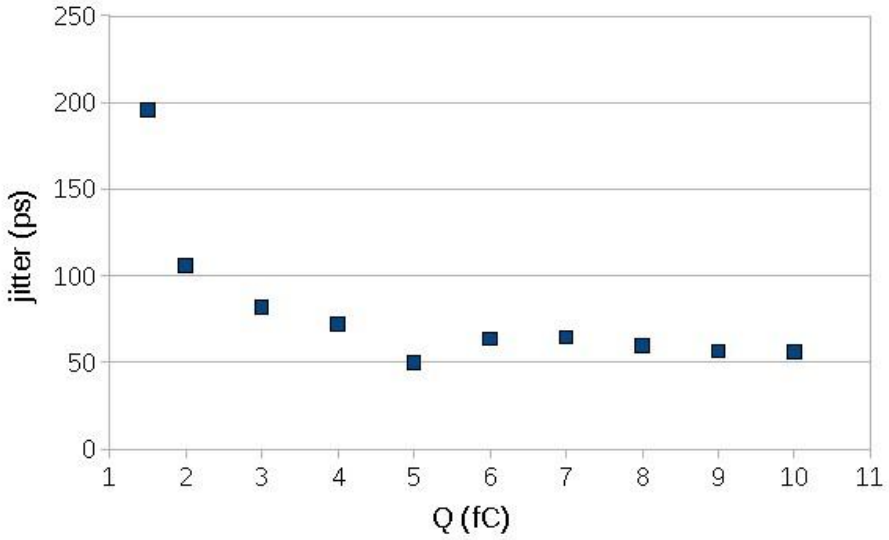
$$-0.5 < DNL(i) = \frac{N_{EXP}(i) - N_{th}(i)}{N_{th}(i)} < 0.5$$

10^5 random test pulses to the 7-bit TDC: $N_{th}=10^5/2^7$

$$-1 < INL(i) = \sum_{i=0}^{k} DNL(i) < 1$$

Jitter measurement





- Measurement of the CFD output time for a test pulse at a fixed phase with respect to the clock
- Pulse phase stepped in 20 psec through the clock period
- Jitter: RMS value of the obtained time distribution

Conclusions

- Efficiency within specification
- TDC preliminary results are in specs (|DNL(i)|<0.3 |INL(i)|<0.8)
- Some errors have been found and understood:
  - One undersized driver in the EOC logic requires to work at 1.5V and at lower frequency (~120 MHz)
  - Due to a wrong internal connection, the CFD performance can be fully characterized only in the test cell, while in the matrix it has to be used as a fast, leading edge discriminator. The CFD performance (measured in the test cell) are fully adequate for the application
- Other problems are being investigated:
  - A non negligible substrate noise has been observed, which gives a baseline modulation equivalent to 0.5 fC peak-to-peak
  - The problem is under investigation, but the end-of-column buffers that deliver the counter signal to the pixels are suspected to be the major contributor
- A beam test is in preparation for the end of September