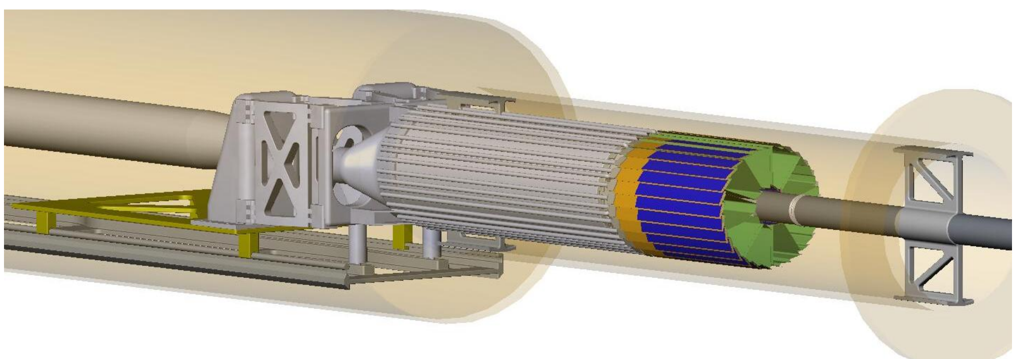
STAR Pixel Detector

A MAPS based vertex detector for STAR

with status of development and prototyping



LBNL
Leo Greiner, Eric Anderssen, Howard Matis, Thorsten Stezelberger, Joe Silber, Xiangming Sun, Michal Szelezniak, Chinh Vu, Howard Wieman

UTA
Jo Schambach

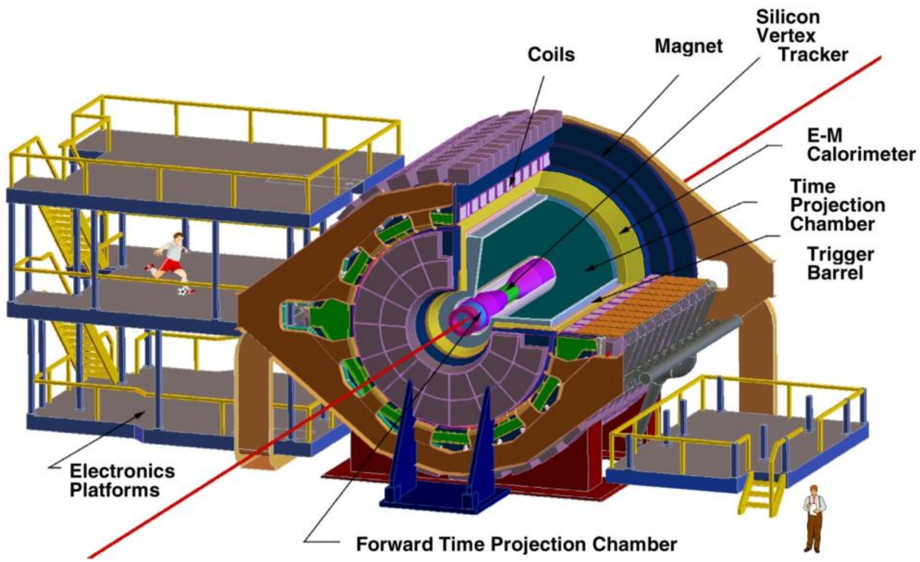
IPHC Strasburg
Marc Winter CMOS group

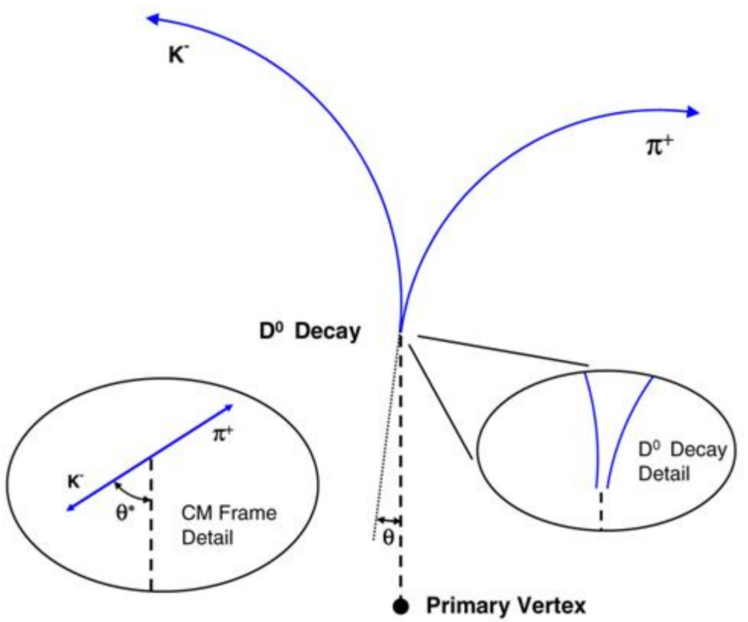
Talk Outline

The primarily focus of this talk is technical.

- STAR Upgrades at RHIC.
- Pixel detector requirements and design.
- Detector characteristics.
- Detector Development and Prototyping.
- Summary and plans.

Vertex Detector Motivation



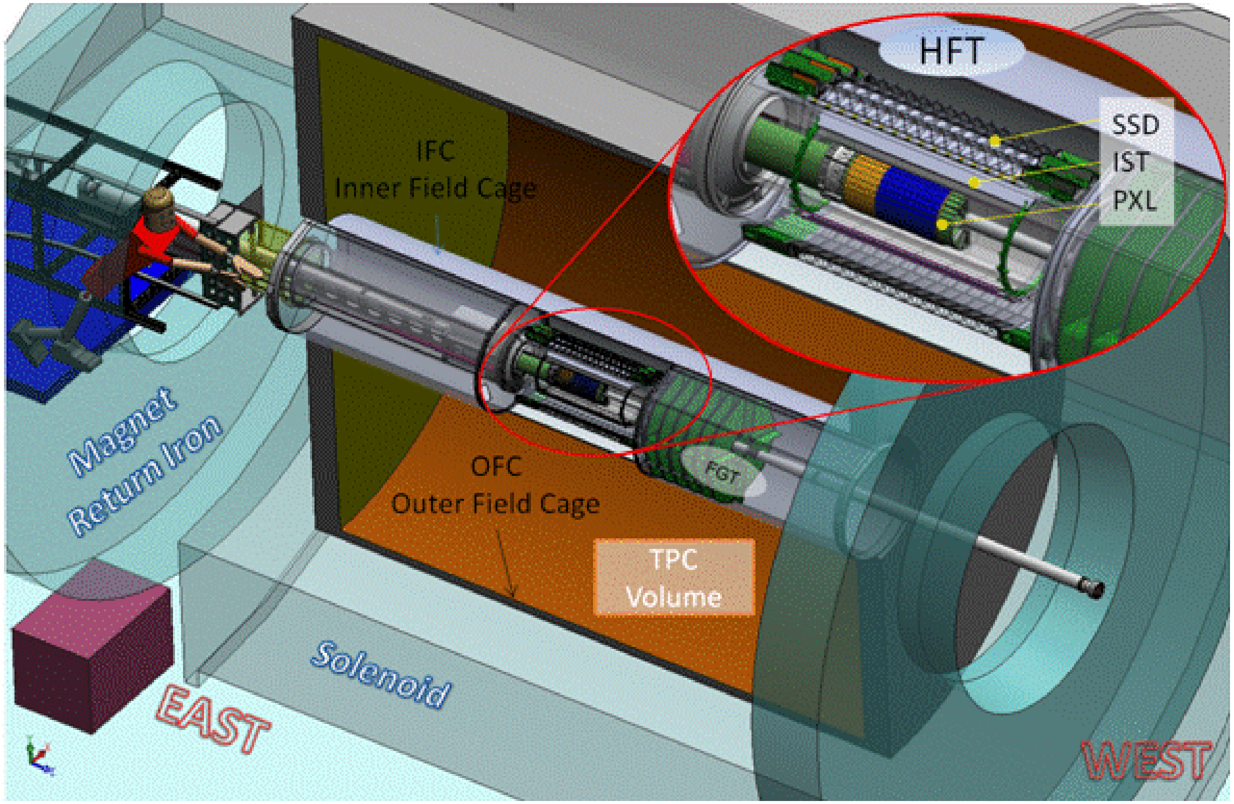


Direct Topological reconstruction of Charm

Detect charm decays with small $c\tau$, including $D^0 \rightarrow K\,\pi$

Method: Resolve displaced vertices (100-150 microns)

Inner Detector Upgrades



TPC – Time Projection Chamber
(main detector in STAR)

HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
  - r = 22 cm
- IST – Inner Silicon Tracker
  - r = 14 cm
- PXL – Pixel Detector
  - r = 2.5, 8 cm

We track inward from the TPC with graded resolution:

Detector Requirements and Characteristics

Requirements

- -1 ≤ Eta ≤ 1, full Phi coverage (TPC coverage)
- ≤ 30 μm DCA pointing resolution required for 750 MeV/c pion
  - Two or more layers with a separation of > 5 cm.
  - Pixel size of ≤ 30 μm
  - Radiation length as low as possible but should be ≤ 0.5% / layer (including support structure). The goal is 0.37% / layer
- ~200-300 hits / sensor (inner layer, 4 cm^2) in the integration time window (at operating point chosen).
- Survive radiation environment at the level (projected) of 20 to 90 k Rad /year and 2 x 10^{11} - $10^{12}/cm^2$ N_{eq} /year.

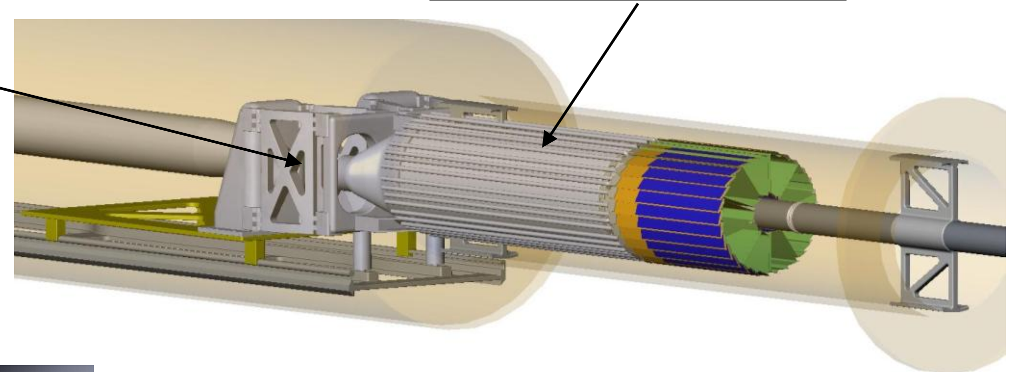
Design Choices

- MAPS Pixel technology
  - Sensor power dissipation ~170 mW/cm^2
  - Sensor integration time <200 μs ($L=8\times10^{27}$)
- Thinned silicon sensors (50 μm thickness)
- Air cooling
- Quick extraction and detector replacement

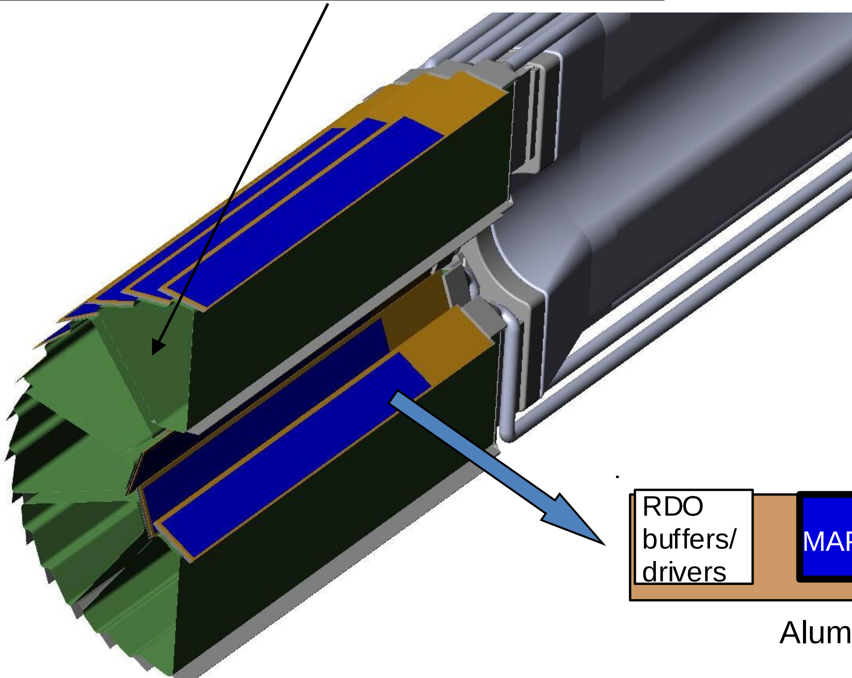
PXL Detector Mechanical Design

Cabling and cooling infrastructure

Mechanical support with kinematic mounts (insertion side)

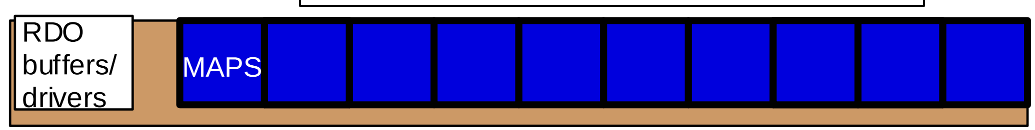


carbon fiber sector tubes (~ 200um thick)



Insertion from one side
2 layers
5 sectors / half (10 sectors total)
4 ladders/sector

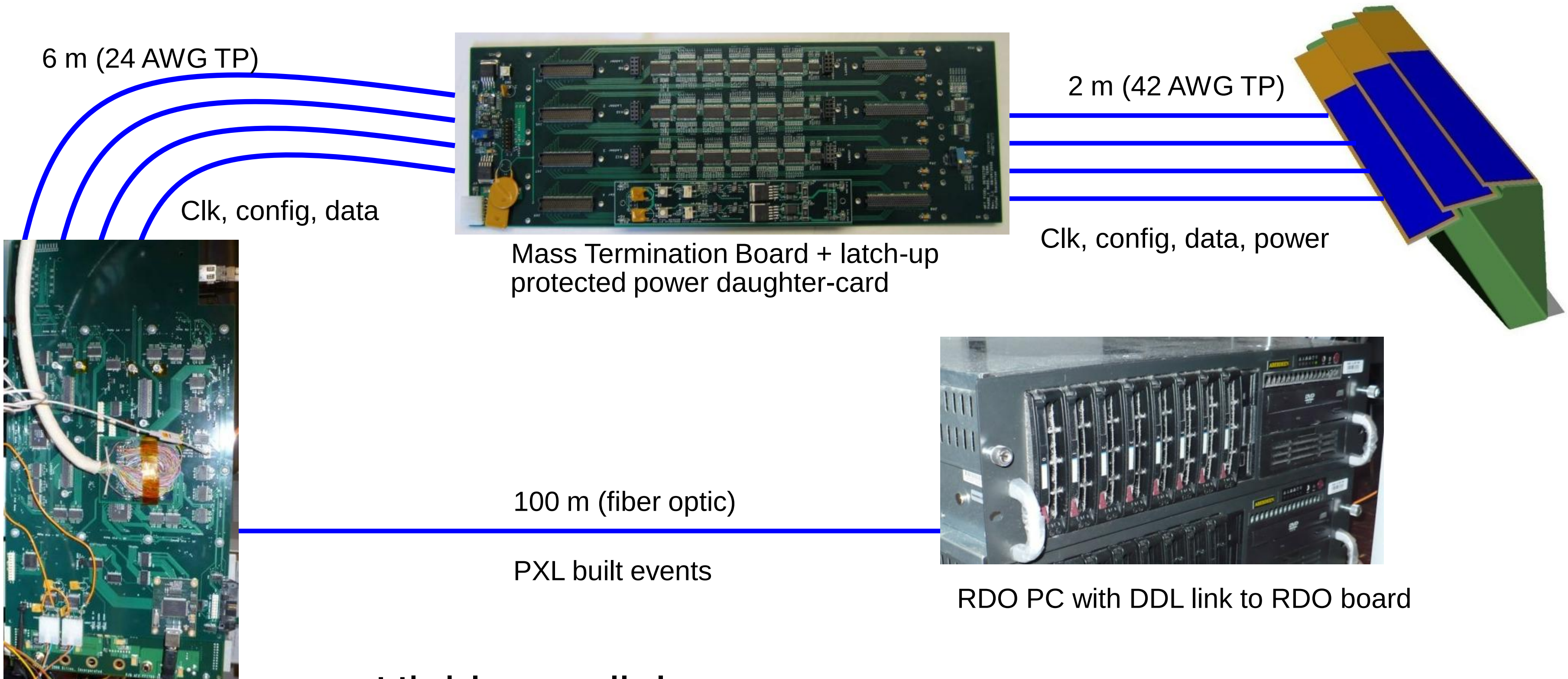
Ladder with 10 MAPS sensors (~ 2×2 cm each)



Aluminum conductor Ladder Flex Cable

← 20 cm →

PXL Detector Basic Unit (RDO)



RDO motherboard
w/ Xilinx Virtex-5 FPGA

<u>Highly parallel system</u>

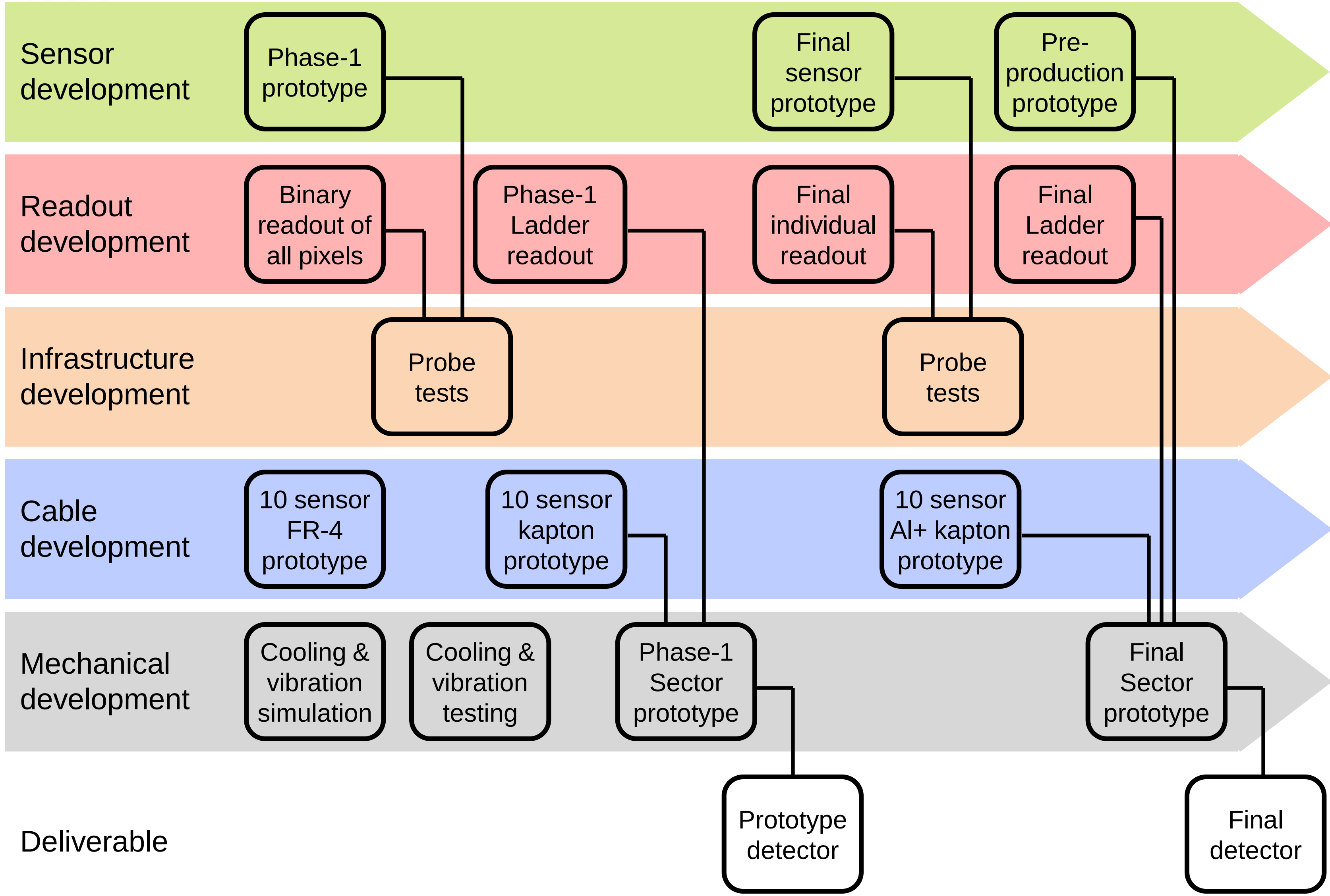
- 4 ladders per sector
- 1 Mass Termination Board (MTB) per sector
- 1 sector per RDO board
- 10 RDO boards in the PXL system

Detector Characteristics

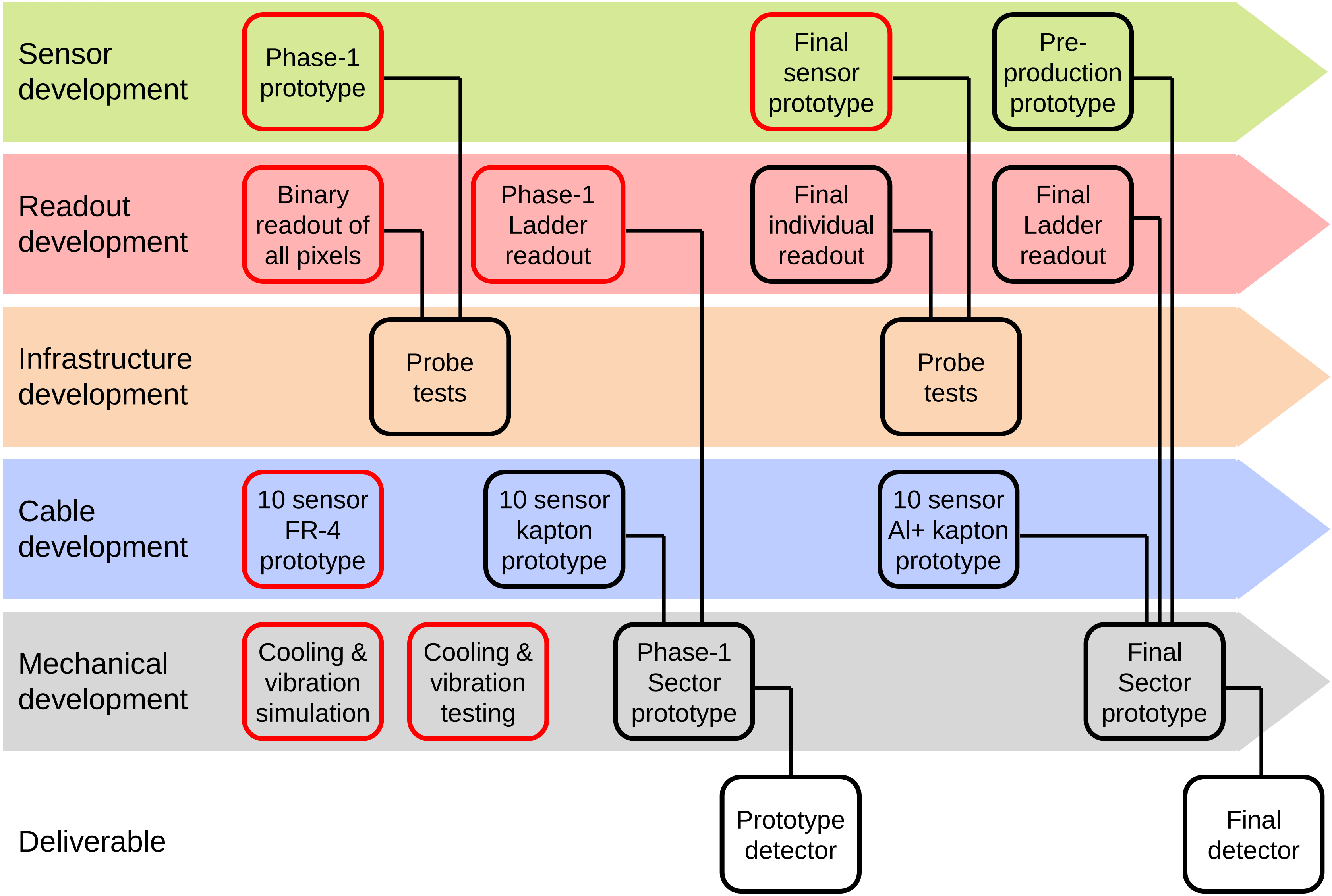
Pointing resolution	(12 $\oplus$ 19GeV/p·c) μm
Layers	Layer 1 at 2.5 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	6 μm
Position stability	6 μm rms (20 μm envelope)
Radiation length per layer	X/X_0 = 0.37%
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation requirement	20 to 90 kRad $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	< 8 Hours

356 M pixels on ~0.16 m^2 of Silicon

Detector Development Path

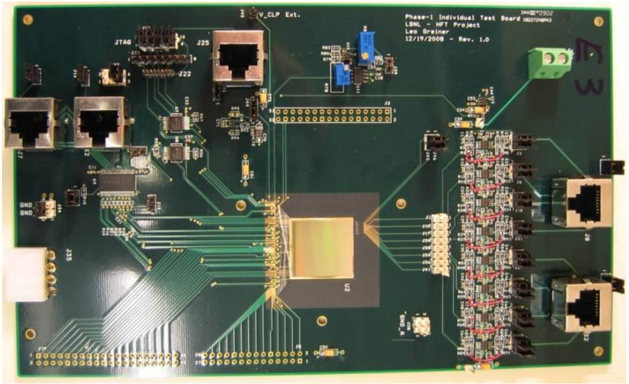


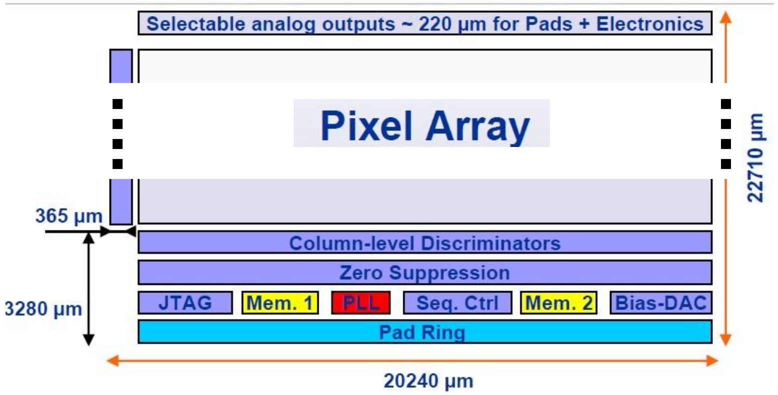
Detector Development Path



Sensor Development with IPHC

The following descriptions are terse.
Please see A. Dorokhov talk on Thursday





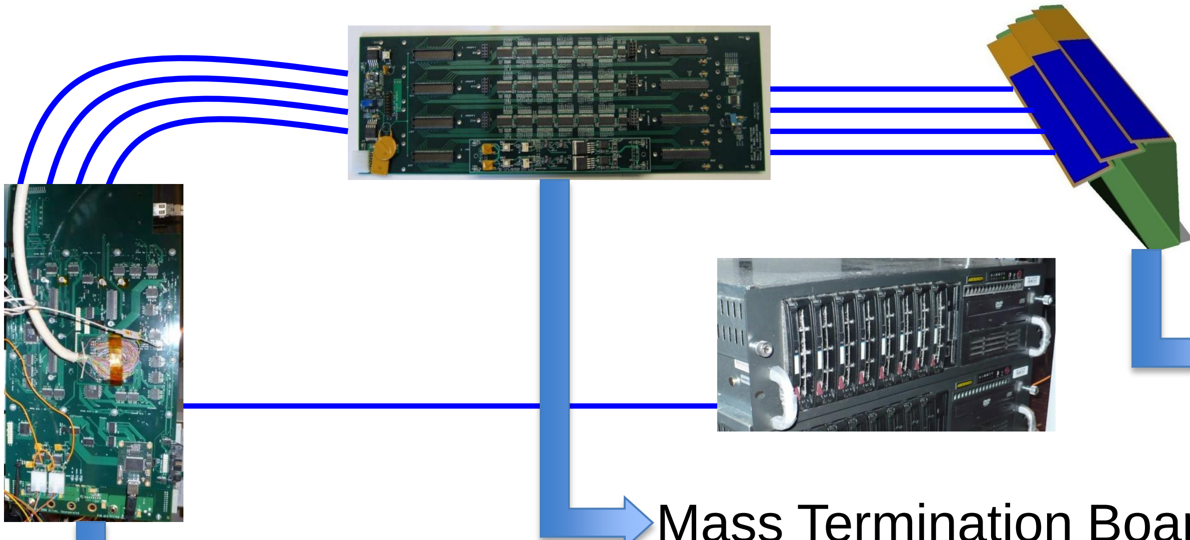
Phase-1 prototype

- Reticle size (~ 4 cm²)
  - Pixel pitch 30 µm
  - 640 x 640 array ~ 410 k pixels
- Column parallel readout
- Column discriminators
- Binary readout of all pixels
- Data multiplexed onto **4 LVDS outputs @ 160 MHz**
- **Integration time 640 µs**
- Functionality tests and yield look very good.
- Measured ENC is 15 e-.

Final Sensor

- Reticle size (~ 4 cm²)
  - Pixel pitch 20.7 µm
  - 928 x 960 array ~890 k pixels
- Reduced power dissipation
  - **Vdd: 3.0 V**
  - Estimated power consumption ~134 mW/cm²
- **Short integration time 185.6 µs**
- Optimized discriminator timing
  - Improved threshold uniformity
- **on-chip zero suppression**
- **2 LVDS data outputs @ 160 MHz**
- **High Res Si option – significantly increases S/N and radiation tolerance.**

Readout Development



Ladder- ITB Prototyped

Mass Termination Board – Prototyped and in use

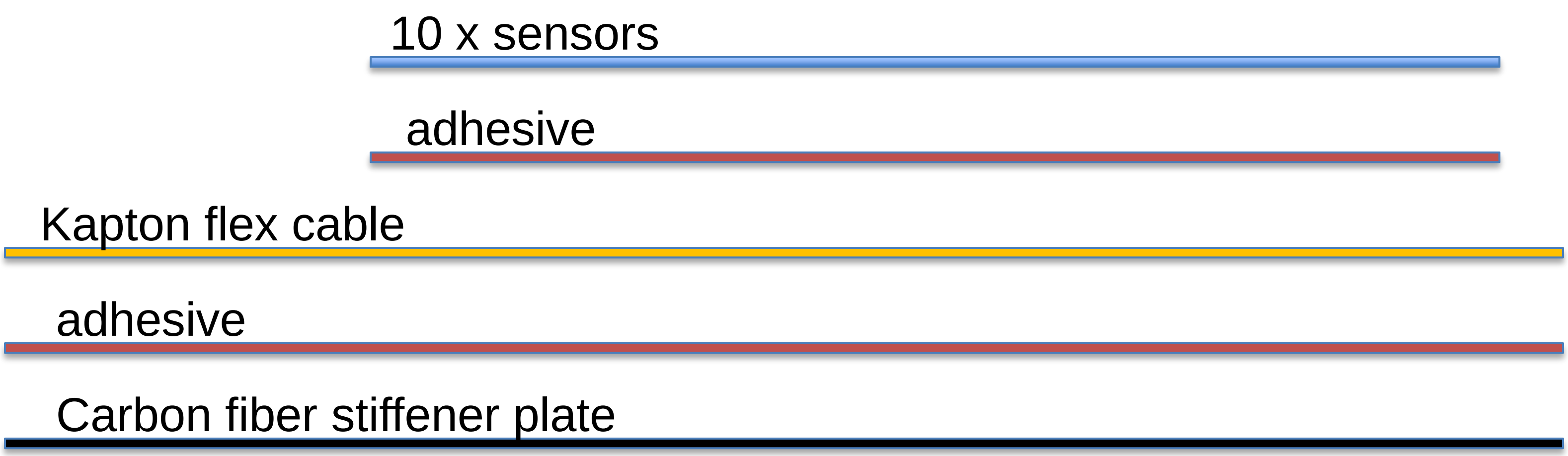
Readout Board – Prototyped and in use

System firmware and software – Prototyped and in use

- System architecture validated with 160 MHz data path testing. (BER < 10^{-14})
- Prototype RDO system (hardware, firmware and software) is in use for sensor characterization, probe testing and ladder prototype testing.
- RDO hardware is the same for both sensor generations, only the firmware changes.

PXL Ladder Structure

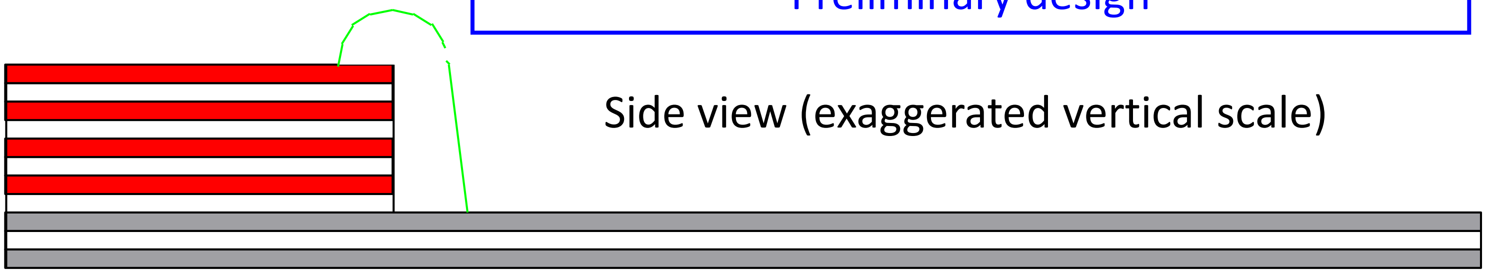
Each PXL ladder consists of three main elements



- Thinning sensors to 50 µm is a standard commercial process.
- The adhesive is a 50 µm acrylic film adhesive.
- The carbon fiber stiffener plate is a basket weave 90º prepreg.
- The flex cable is the component that requires a significant development effort.

Flex Cable Development

Hybrid Copper / Aluminum conductor flex cable
Preliminary design



Side view (exaggerated vertical scale)

Top View

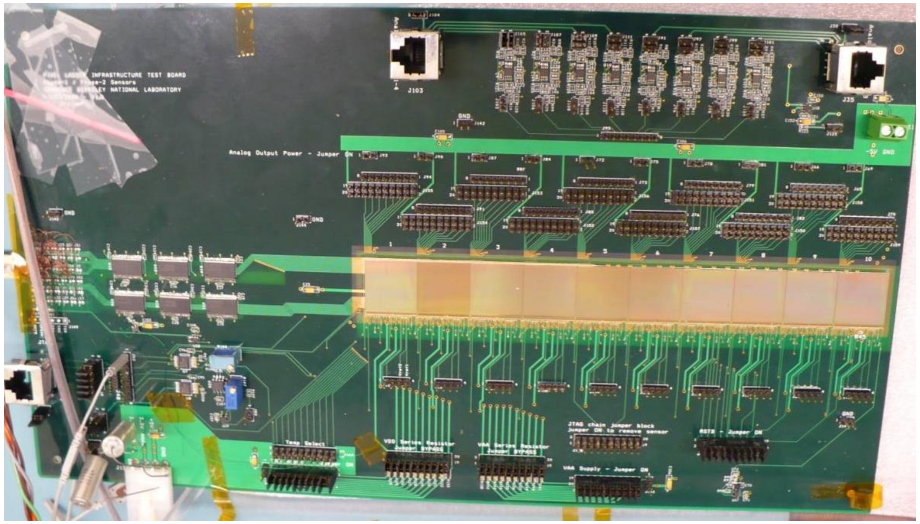
Low mass region calculated X/X_0 for Al conductor = 0.073 %
Low mass region calculated X/X_0 for Cu conductor = 0.232 %

<u>PXL Cable development is planned as a 4 stage process:</u>

1. Infrastructure testing board (large and configurable FR-4 ladder prototype).
   - Validate design concepts and determine envelope of sensor operation.
2. Prototype detector cable FR-4 with Cu traces.
3. Prototype detector cable Kapton with Cu traces.
4. Prototype detector cable Kapton with Al traces.

Infrastructure test board

- The ITB testing is effectively a ladder level system test with full thickness sensors.
  - complete chain of RDO system (MTB, RDO, long cables) at full system speed of 160 MHz.
- Multi-drop clock working.
- JTAG daisy chain working.
- 10 sensor synchronization working.
- Fully automated testing with working RDO.



	Noise
Individual sensor	100 %
All sensors on (high discriminator threshold → low switching/output activity) – expected running configuration	Up to 125 % (122 % on average)
All sensors on (low discriminator threshold → high switching/output activity)	Up to 145 % (138 % on average)

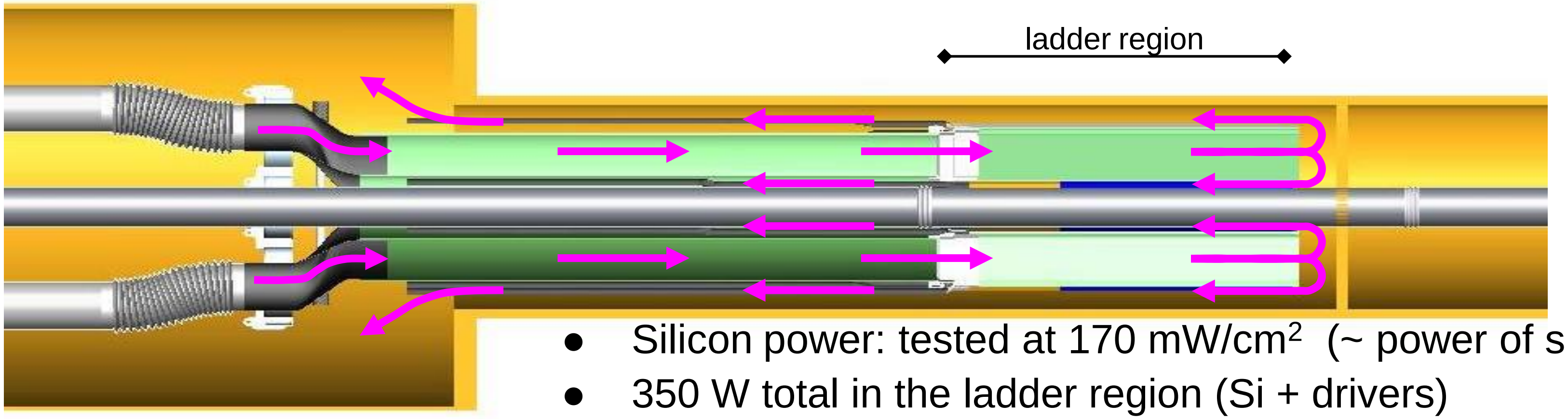
preliminary

- The noise coupling mechanism is under investigation.
- An ITB with thinned 50 μm sensors is ready for testing.
- Design of the next stage (FR-4 form factor size) will begin soon.

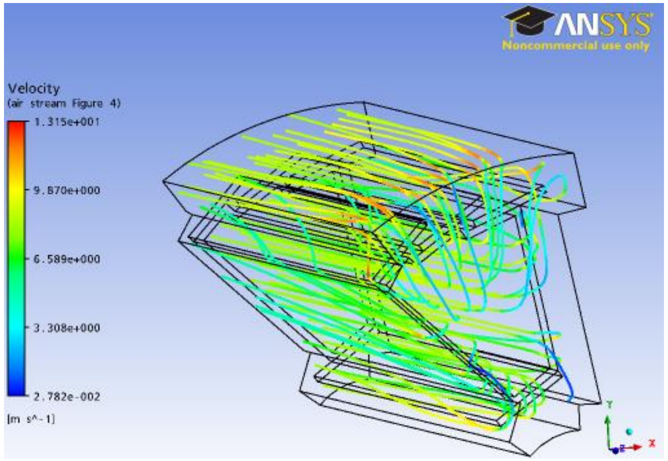
Mechanical Development

The CTE difference between silicon, carbon and the kapton ladder cable is a potential source of thermally induced deformation. FEA simulations give a maximum ΔT of 20° C

Air-flow based cooling system for PXL to minimize material budget.

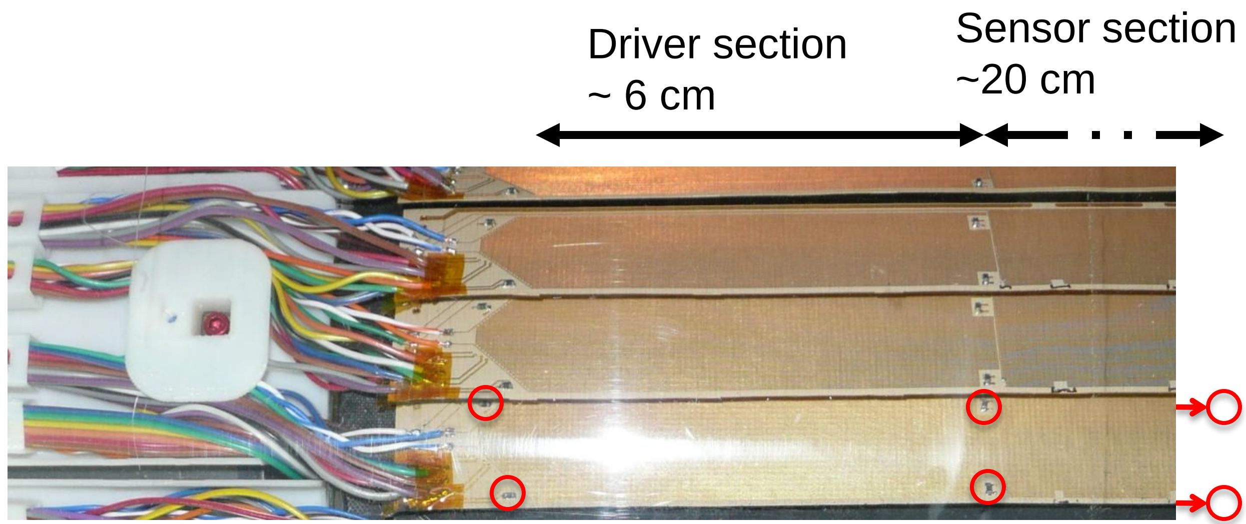


- Silicon power: tested at 170 mW/cm^2 (~ power of sunlight)
- 350 W total in the ladder region (Si + drivers)



computational fluid dynamics

Mechanical Development

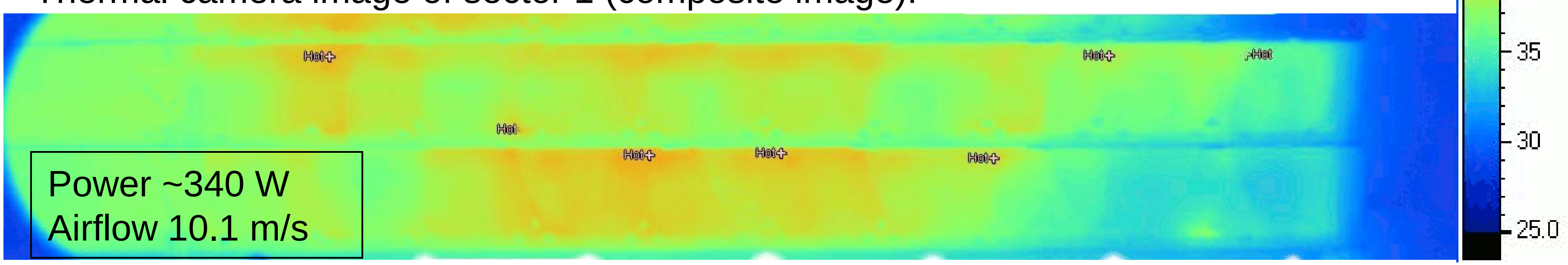


- Kapton cables with copper traces forming heaters allow us to dissipate the expected amount of power in the detector

- 6 NTC thermistors on each ladder

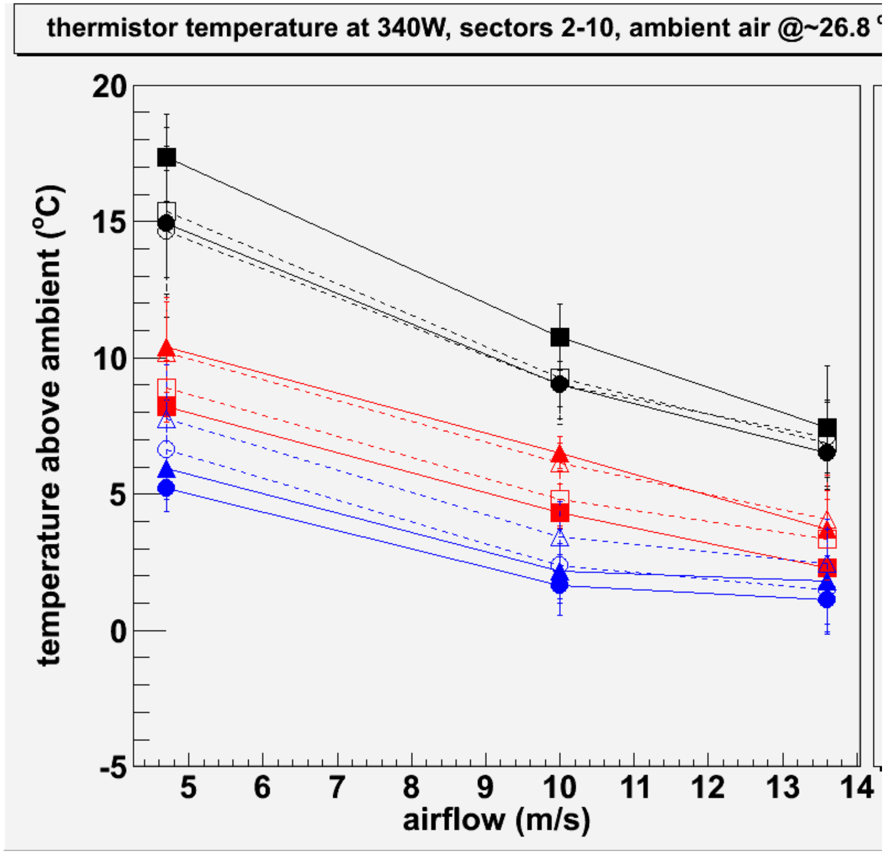
- Sector 1 was equipped with 10 thinned dummy silicon chips per ladder with Pt heaters vapor deposited on top of the silicon and wire bonded to heater power.

Thermal camera image of sector 1 (composite image):



Mechanical Development

unsuported end
mid-section
fixed end
Solid – inner layer
Open – outer layer



- Measurement results agree with simulations and meets calculated stability envelope tolerance.
- Air flow-induced vibrations (< 10 m/s) are within required stability window.

Summary and future plans

- We have a well advanced mechanical design that is in the process of being verified by simulation and prototyping.
- The prototype RDO system is performing well.
- Sensor development with IPHC is on schedule and we expect the first prototype final sensor delivery in Q1 2011.
- The ladder cable development is on schedule and we are evaluating the ITB performance with the full compliment of 10 working sensors.

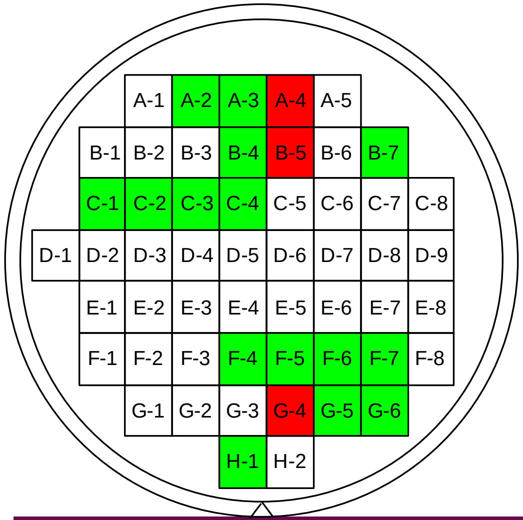
- We expect to have our DOE CD-2/3 review in January of 2011 (release of funding for full detector construction).
- Detector installation is scheduled for 2013.

backup

Probe testing thinned sensors

Probe testing on diced and thinned (50 μm) sensors – to meet yield requirements

- Dedicated probe pads in the sensor pad ring.
- Up to 3 probe tests on a sensor.
- Automated test system based on the prototype RDO system gives a qualitative analysis of probed sensors including identification of dead/stuck pixels/columns.
- 1st wafer of thinned sensors under test.



Vacuum chuck for probe testing 20 (50 μm thick) MAPS sensors per testing session.

Sensor Yield >90%
Thinning (individual method) yield => >90%
Thinning (pre-scribe method) initial yield => ~70%*

* Expected yield is >90%

Simple Data Rate

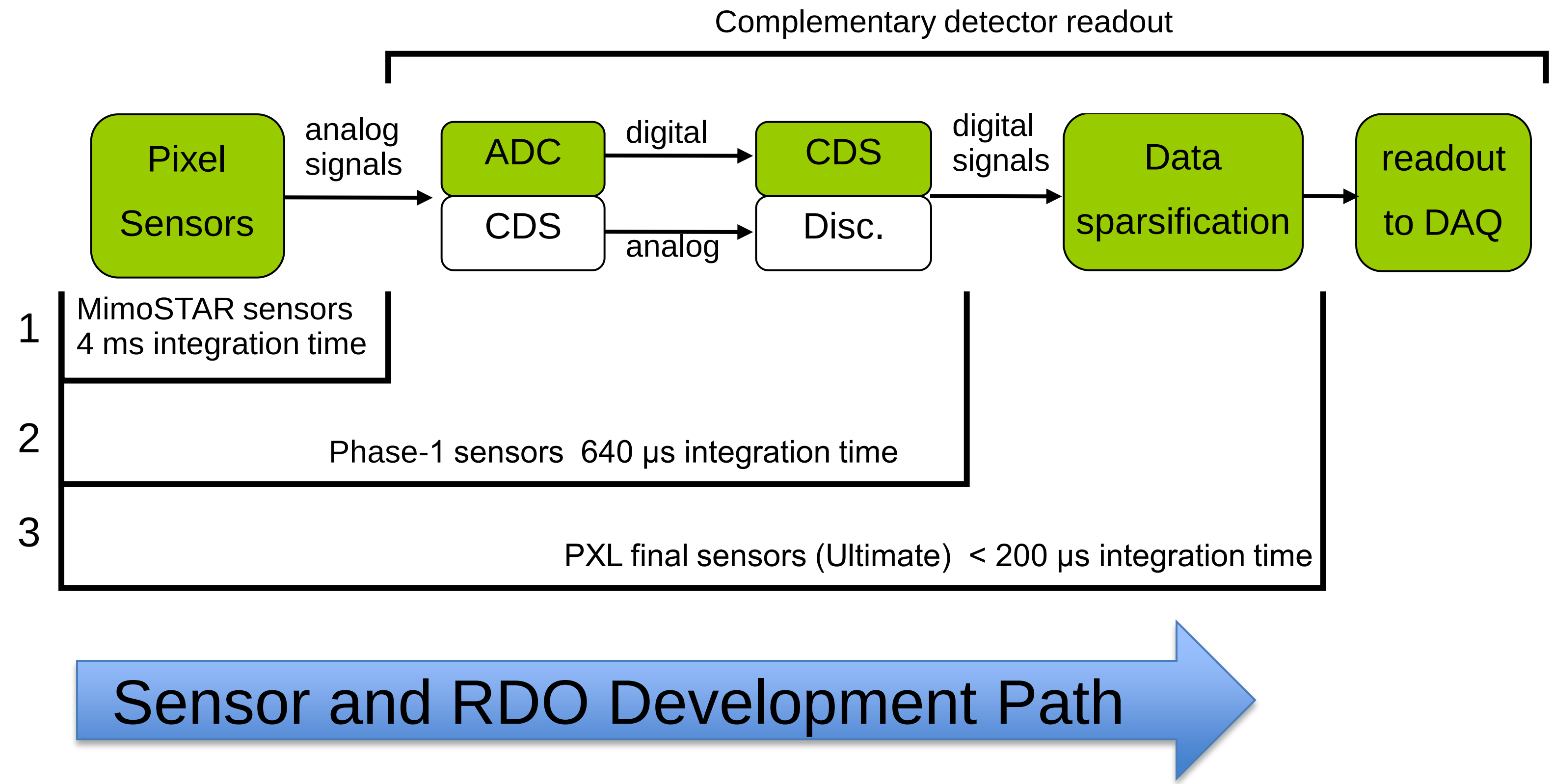
PXL System

Item	Number
Bits/address	20
Integration time (μs)	200
Luminosity ($cm^{-2}s^{-1}$)	8×10^{27}
Hits / frame on Inner sensors (r=2.5 cm)	246
Hits / frame on Outer sensors (r=8.0 cm)	24
Final sensors (Inner ladders)	100
Final sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

- Data rate to storage = 199 MB/sec (1kHz trigger)
- 199 kB / event

Sensor generation and RDO attributes

The sensor and readout development are strongly coupled



RDO System Design – Physical Layout