Development of n-in-p Silicon Planar Pixel Sensors and flip-chip modules for very high radiation environment

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For
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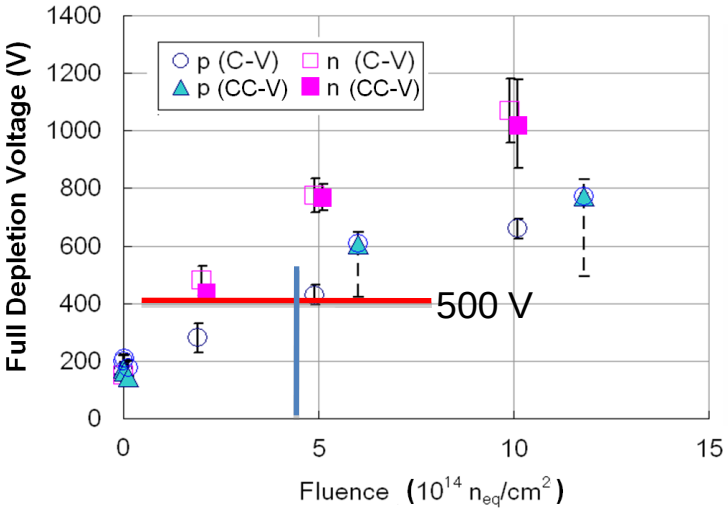
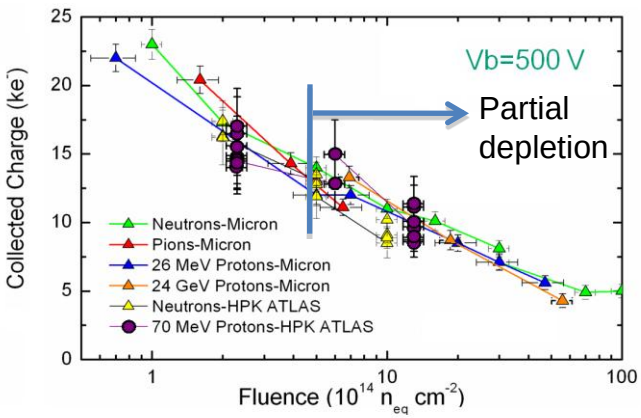
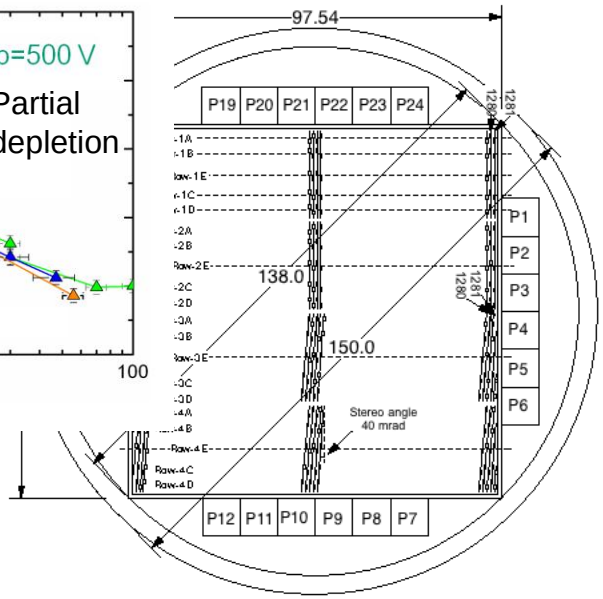
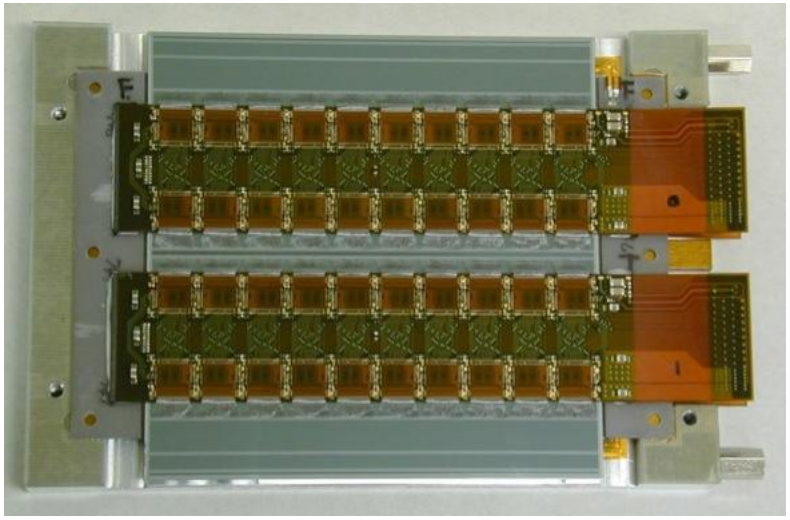
R&D of P-type Silicon Sensors







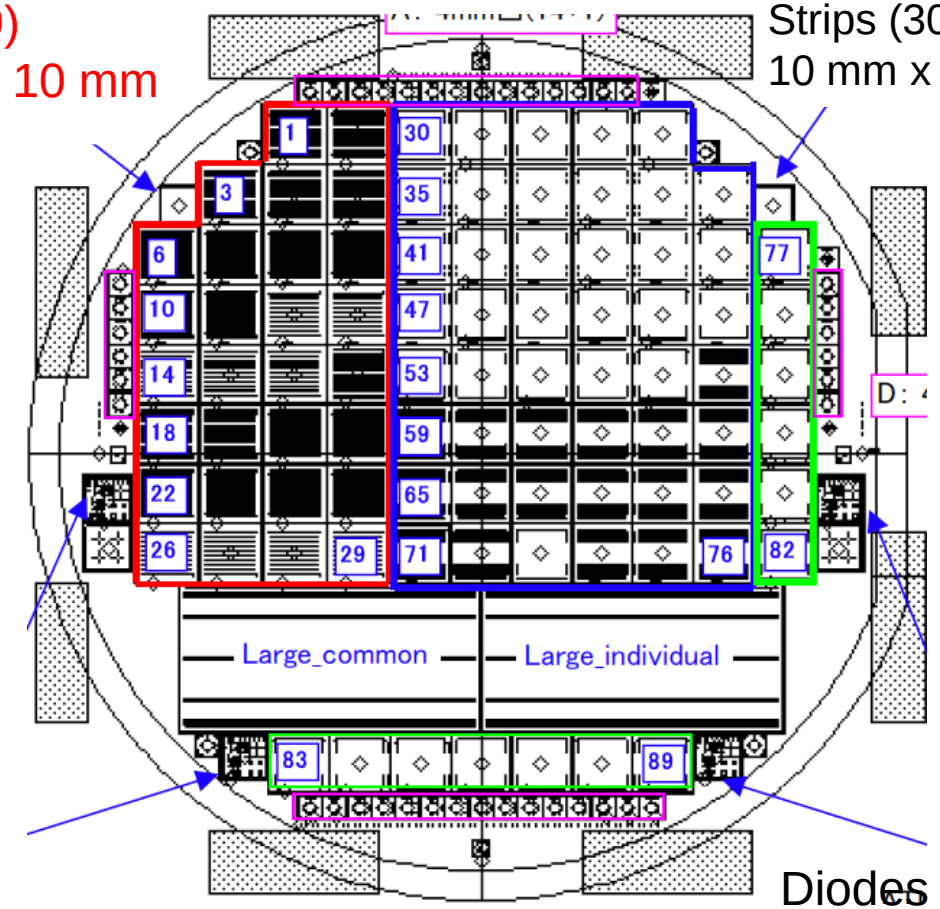
- R&D of N-in-P Strip sensor
  - 6-inch (150 mm dia.) P-type FZ wafer, 320 µm thickness
  - 1 cm x 1 cm (miniature) , 9.75 cm x 9.75 cm (main)
  - fabricated by Hamamatsu Photonics K.K. (HPK)
- Reported in the 7th International "Hiroshima" Symposium…, Hiroshima, 28 Aug. – 1 Sep. 2009. Achievements, e.g.
  - N-side isolation
  - No breakdown (onset of microdischarge) up to 1 kV
  - Radiation damage tested by protons and neutrons up to ~ 10^15 1-MeV-neutron equivalent(neq)/cm^2
  - Single- and Double-sided strip prototype modules
- A goal of the R&D of Pixel sensor is
  - To work ≥10^16 neq/cm^2
  - Operable up to 1000 V
    - To collect more charges than 500 V
    - "Charge multiplication(?)" towards 1000 V

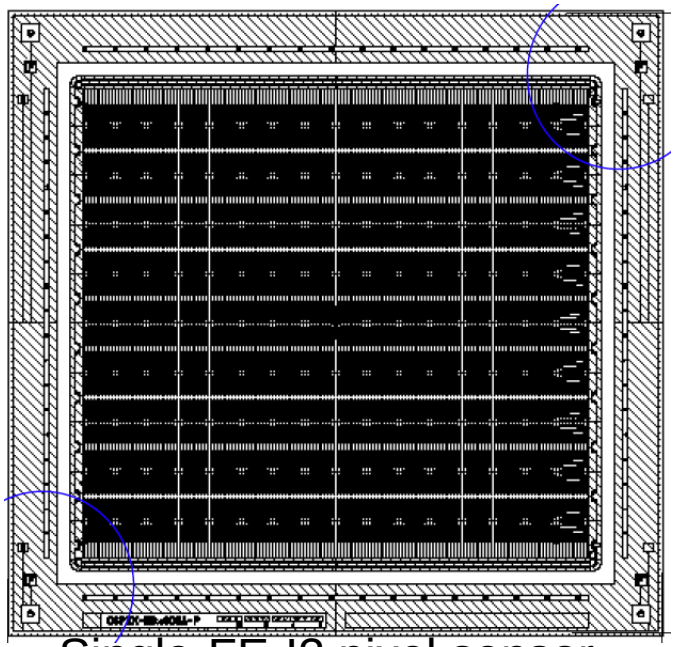


R&D of Pixel Sensors Wafer #1

- Single-FE-I3 pixels
- Slim-edge study
  - Diodes: 1-20
- Guard-ring study
  - Diodes: 21-32
- 6in P-sub (~4 kΩcm) and N-sub (~4kΩcm) wafers
- Nominal 320 µm and thinned 200 µm

Pixel (1-29)
10.5 mm x 10 mm



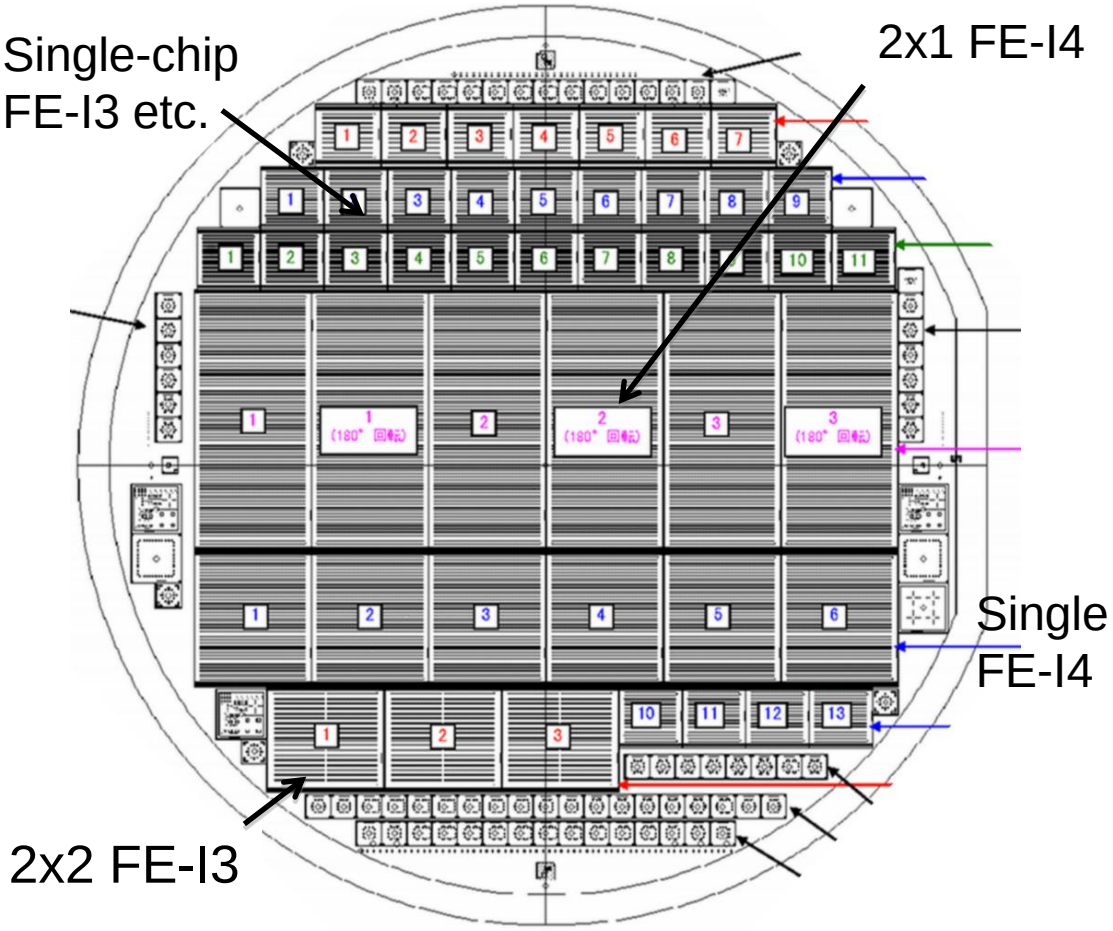


Single-FE-I3 pixel sensor

- HPK 6 in. (150 mm) wafers, p-type and n-type

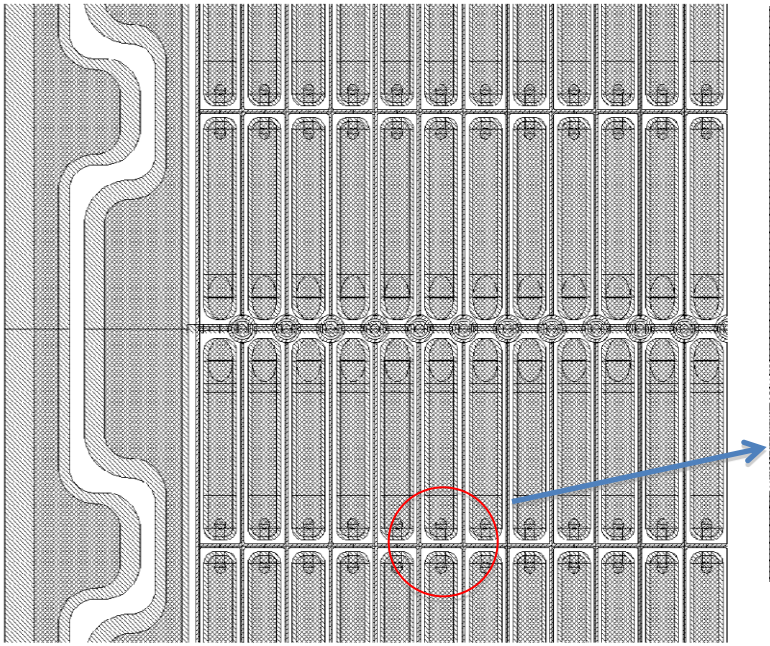
R&D of Pixel Sensors Wafer #2

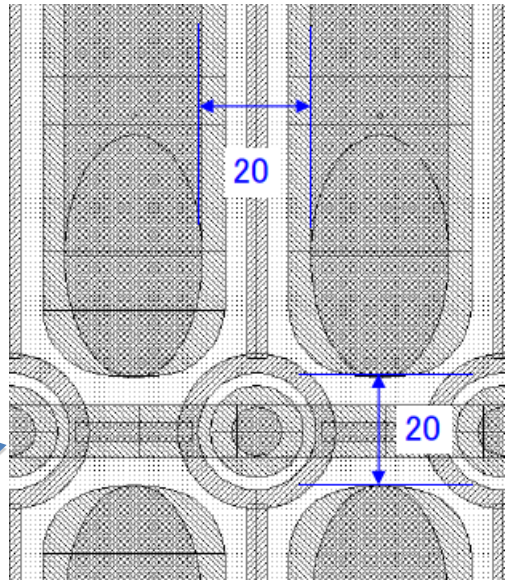
- Mainly FE-I4 pixel sensors
  - 2x1 FE-I4 sensor
  - ATLAS IBL design, 18.8 mm x 41.3 mm, with the edge space of 0.450 mm
- N-side isolation x bias method
  - p-stop (common, individual), p-spray)
  - 1 type of bias (PT)
- Thickness
  - 320 um and Thinned 150 um
- Others
  - single-chip FE-I4,
  - single-chip FE-I3 (3 types of isolation x 2 types of bias (PT, PolySi)),
  - 2x2 FE-I3 sensors (3 types of isolation x PT), etc.



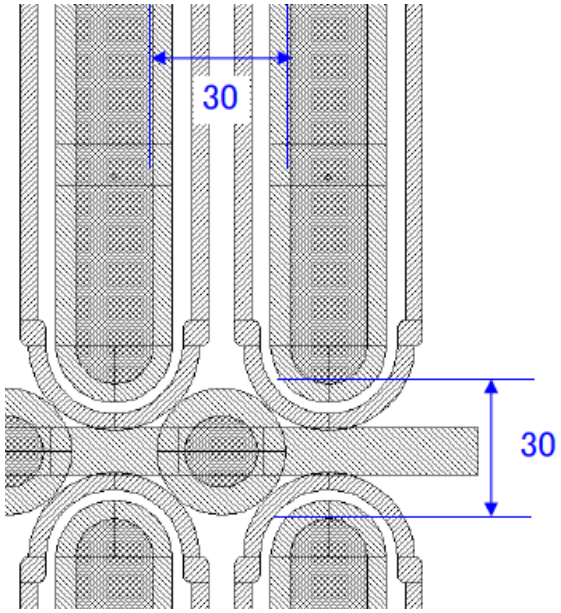
- Out of fabrication expected
  - Normal thickness (320 µm): End Aug. 2010
  - Thinned (150 µm): End Sep. 2010

New Punch-Thru (PT) Bias layouts





Common p-stop

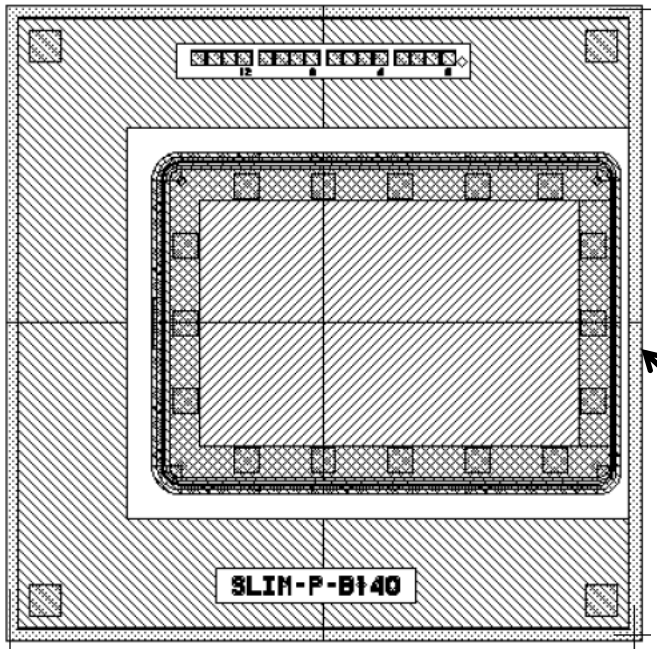


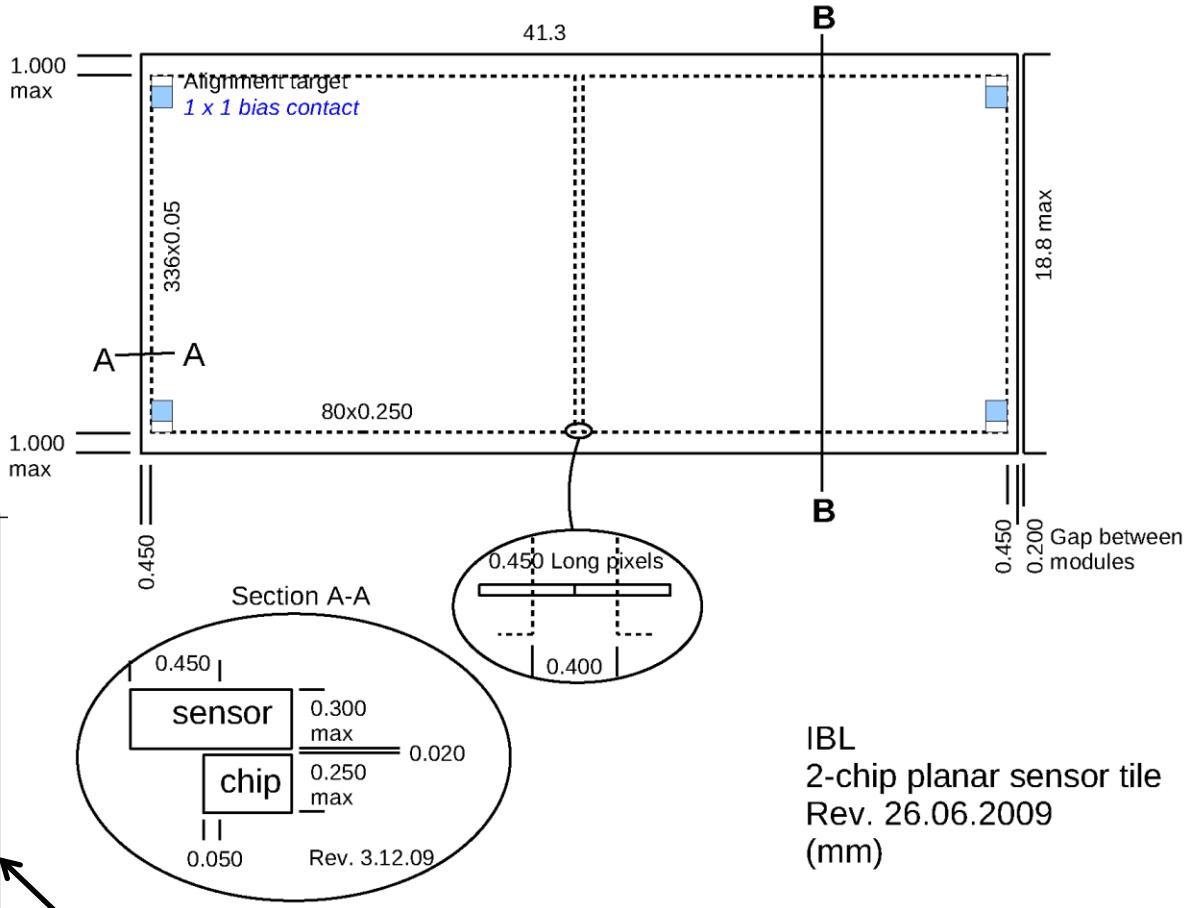
Individual p-stop

- FE-I4 pixel: 50 µm x 250 µm pitch
- A bias dot for 4 pixels
  - To minimize insenstive area
  - We might loose a bit more charge at the 4-corner
    - An usual option is to bias the dot towards the backplane bias to enhance the field
- The gap between the pixel implants
  - 20 µm in common p-stop, same as in the p-spray design
  - 30 µm in individual p-stop

Slim-Edge Study

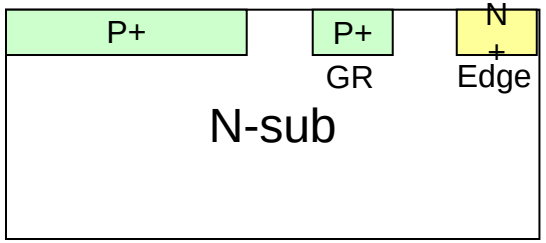
- A goal
  - ATLAS Insertable B-Layer (IBL) 2x1 Planar Pixel Sensor Envelope
  - Distance from active pixel edge to dicing edge: 0.45 µm

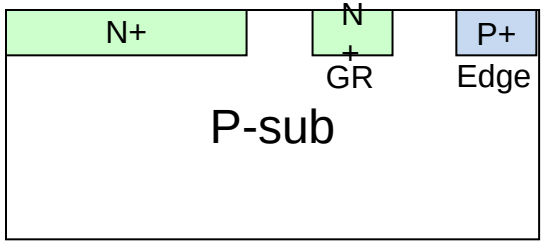


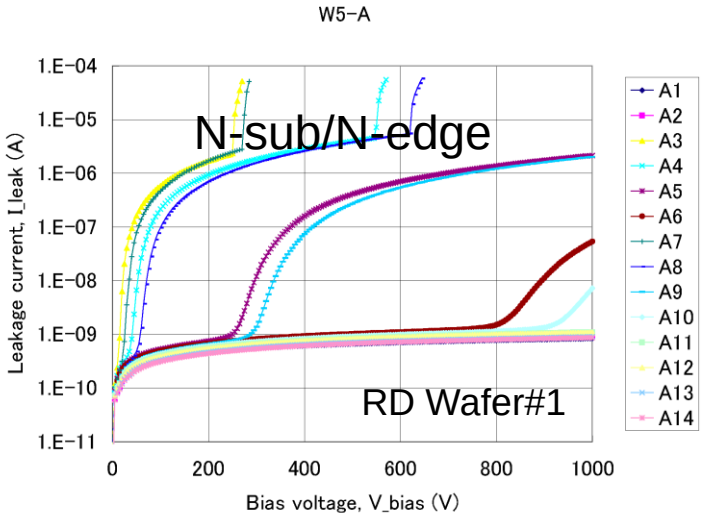


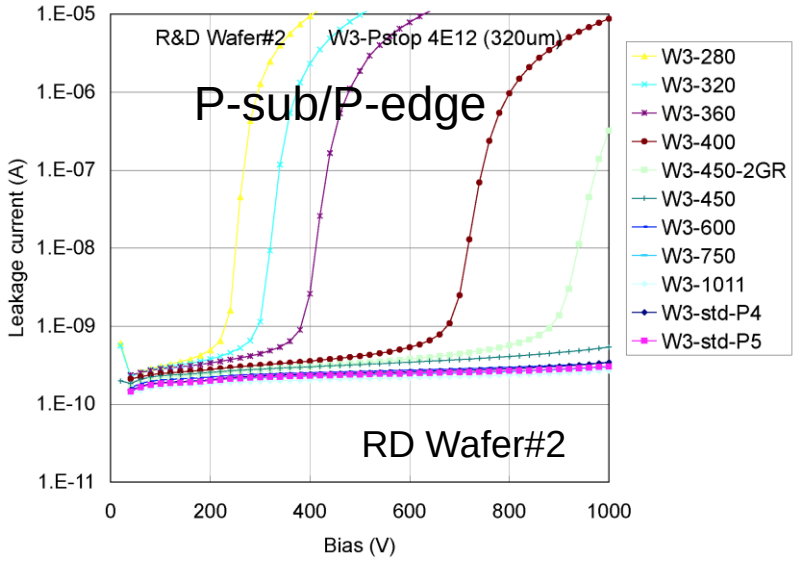
Only in one side, the distance-to-edge is varied from 80 to 1000 µm

Slim-Edge - Measurements





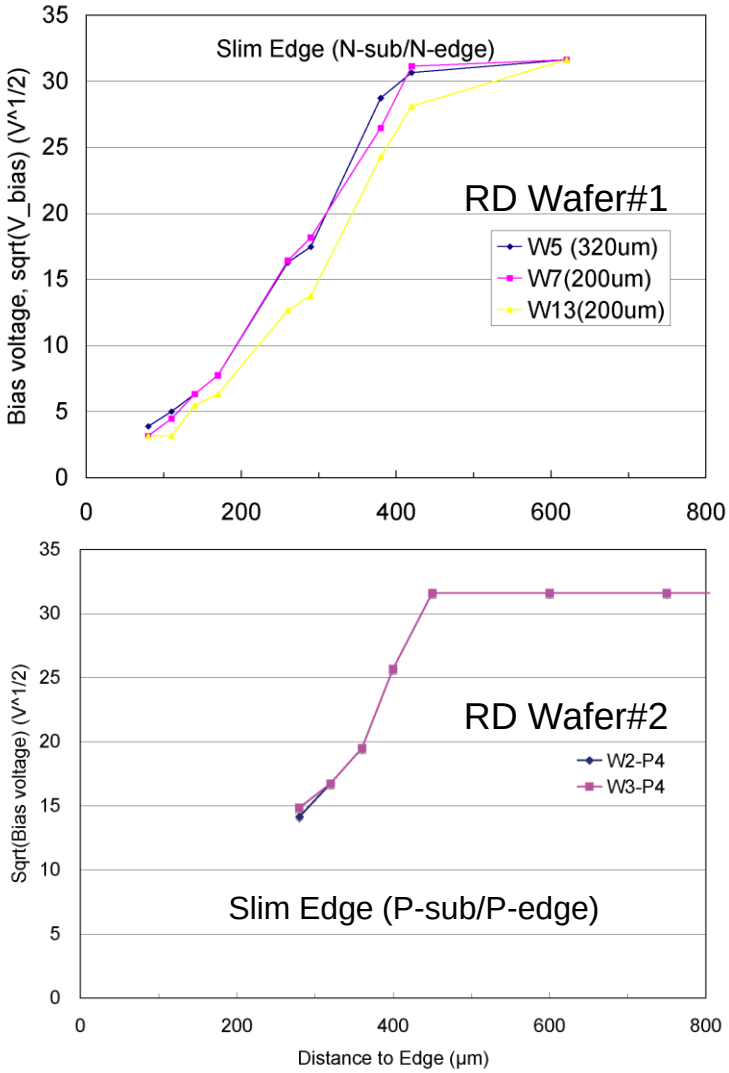




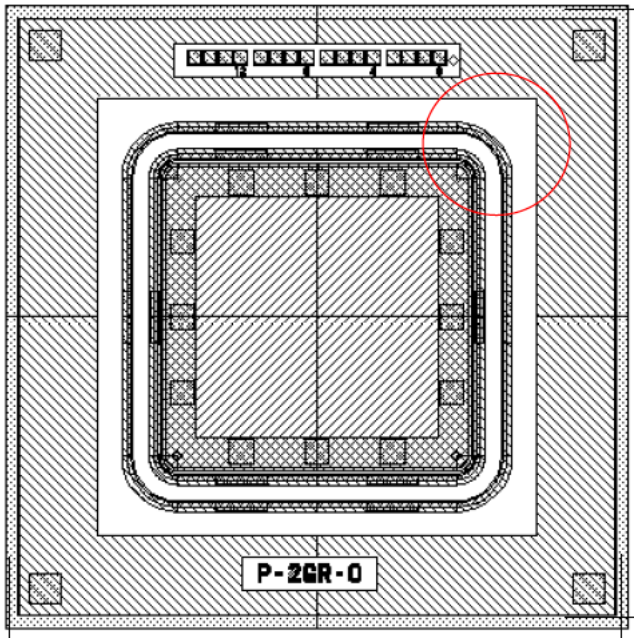
- N-sub wafer
  - Thickness: 320 µm (W5), 200 (W7,13) µm
  - Distance-to-edge: 80 – 640 µm
- P-sub wafer
  - Thickness: 320 µm
    - 150 µm to come
  - Distance-to-edge: 280-1011 µm
  - Leakage current ~7 nA/cm^2

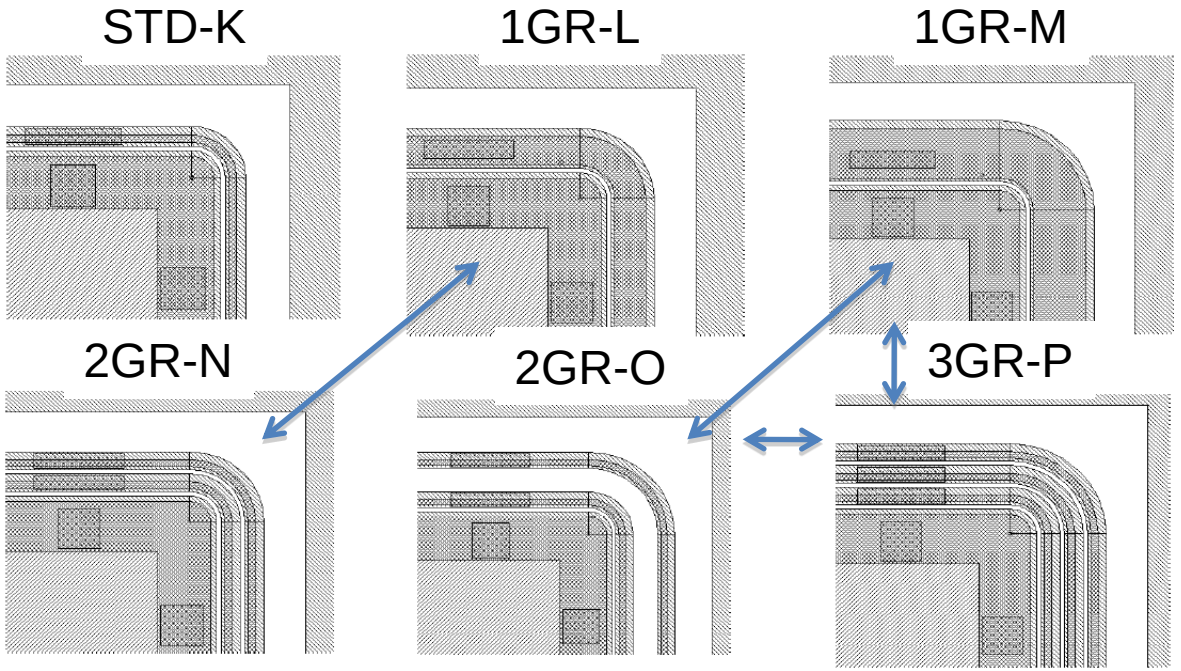
Slim-Edge – Distance vs Onset voltage

- Wafer thickness: 320 µm
  - Both N- and P-sub wafers
- Linear dependence of square root(V_bias) on the distance to edge
  - Reflecting the depletion along the surface
- Distance-to-edge
  - ~450 µm is expected to hold 1000 V



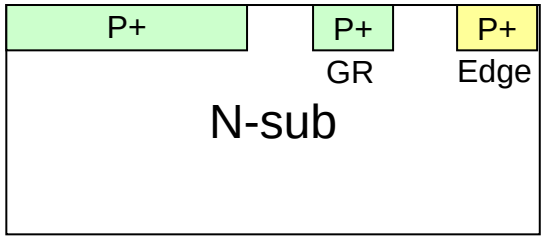
Guard Ring Study

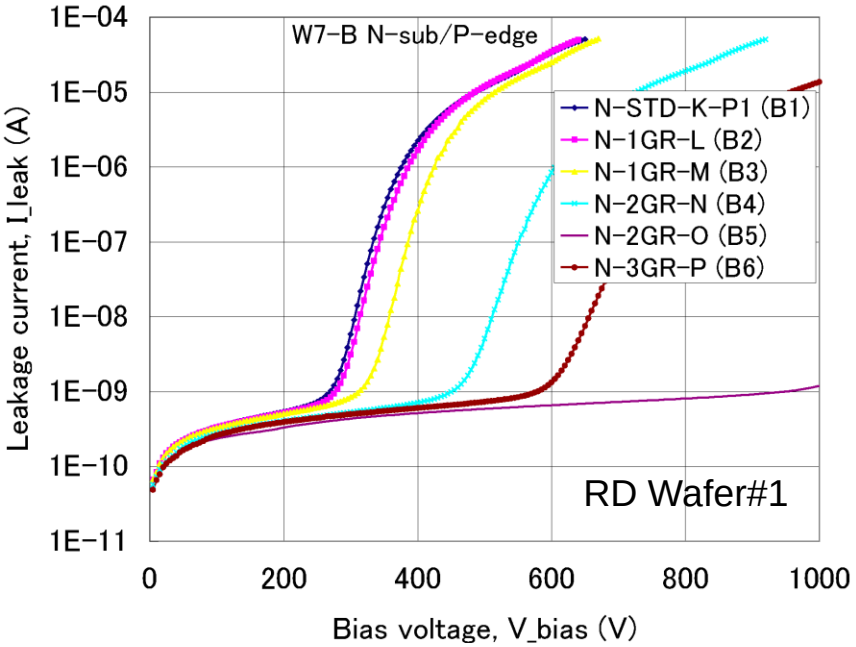




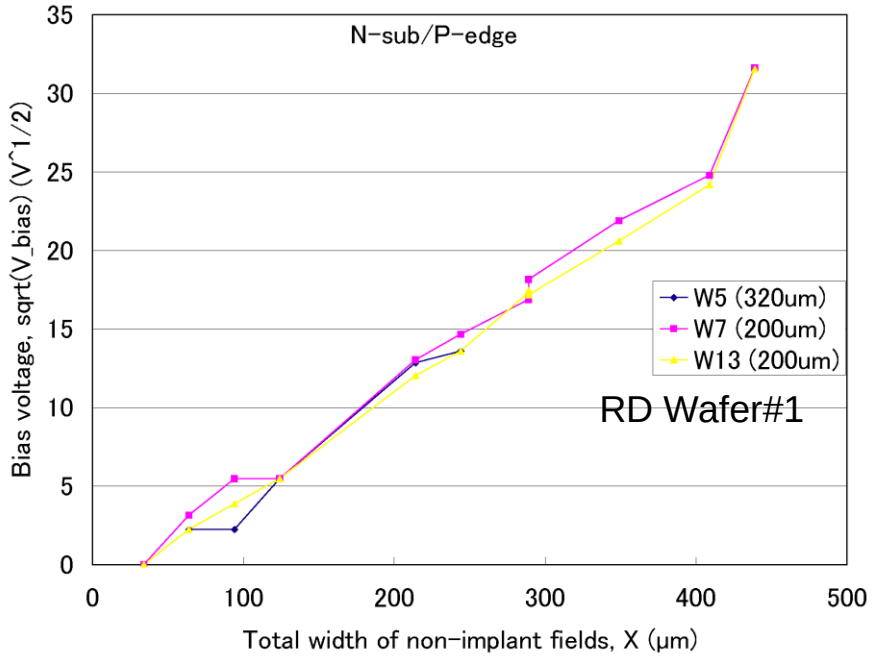
- Investigation whether the number of guard rings will help to reduce the distance to edge
  - Variation up to 3 guard rings
- Systematics for the width of guard rings
  - Edge-to-Edge of guard rings are
    - 1GR-L = 2GR-N
    - 1GR-M = 2GR-O = 3GR-P

Guard Ring Study



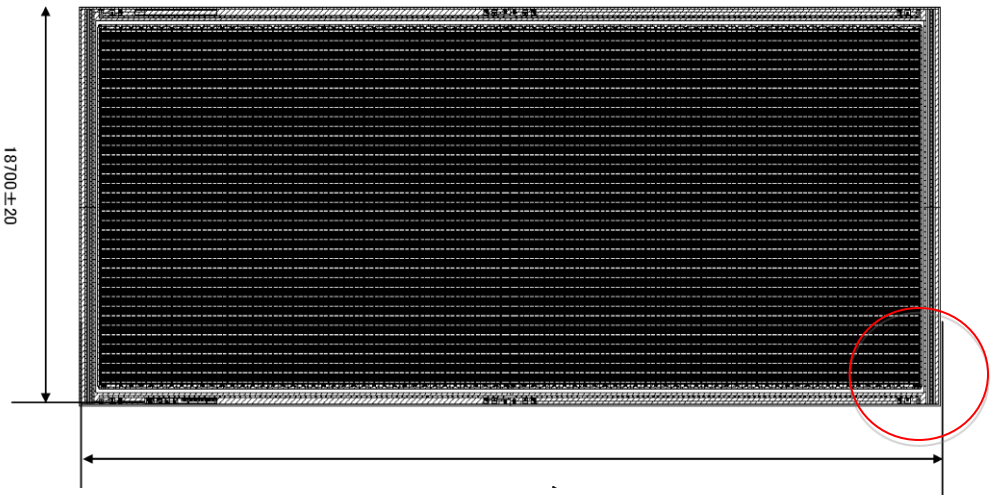


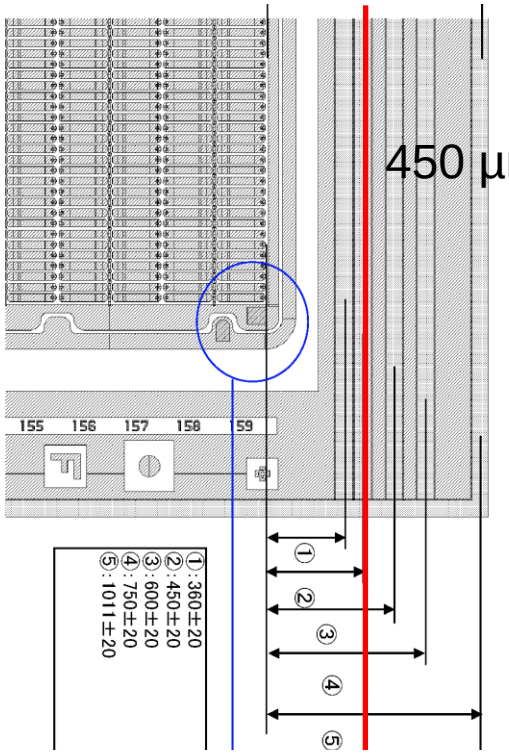
- I-V measurements
  - N-sub/N+ edge holds 1 kV
  - N-sub/P+ edge for investigation
    - Breakdown when depletion reaches P+ edge



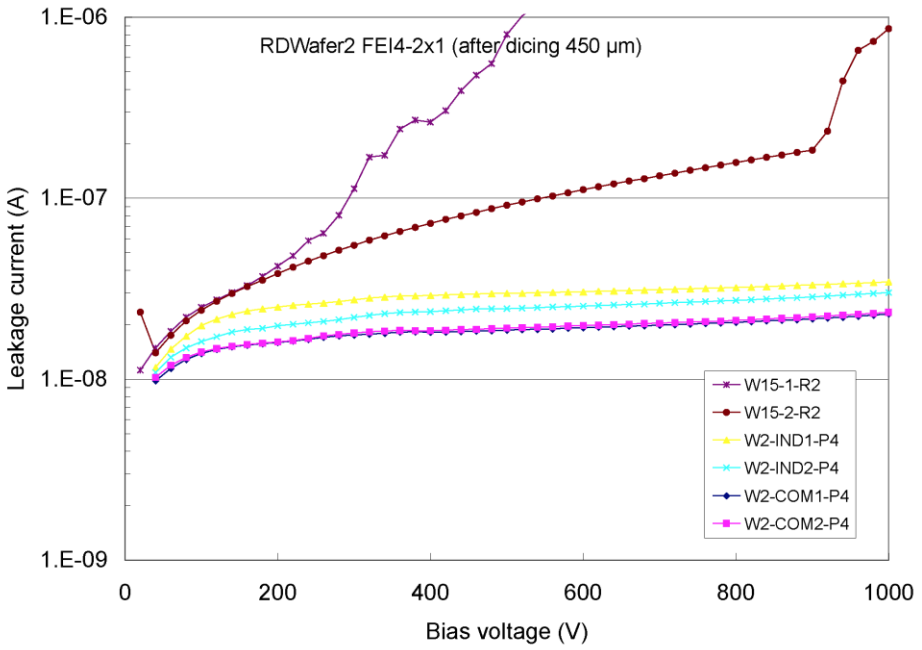
- Systematic onset as a function of gap
  - Axes:
    - Horizontal: total width of fields without implantation
    - Vertical: square root of bias voltage
  - Linear increase == depletion along surface
- Number of guard rings
  - irrelevant to reduce the distance to edge
  - May help to reduce some electric field at the edge of the bias ring

2x1 FE-I4 Pixel Sensor





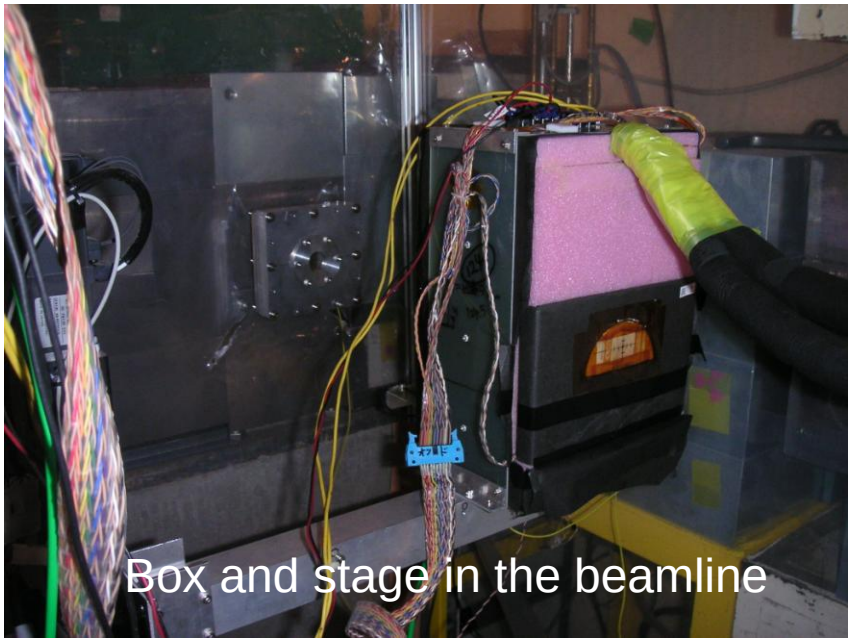
450 µm dicing

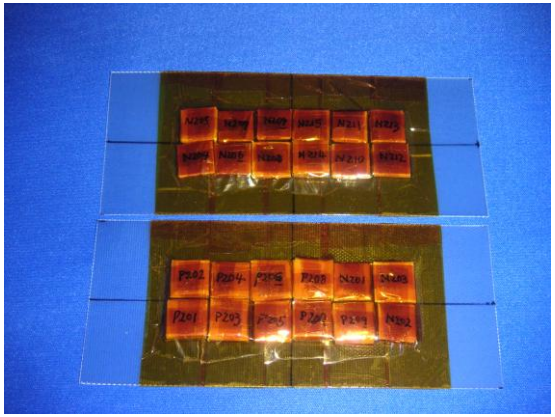


- FE-I4 2x1 sensor: 18.7 mm x 41.5 mm x 320 µm
  - Distance-to-Edge: 450 µm
  - P-stop 4x10^12 or P-spray 2x10^12 cm^-2
- I-V measurement after dicing
  - Excellent I-V performance
  - No onset of MD up to 1000 V (p-stop)
  - ~4 nA/cm^2
- (FE-I3 thinned (200 µm, N-sub) holds 1000 V.)

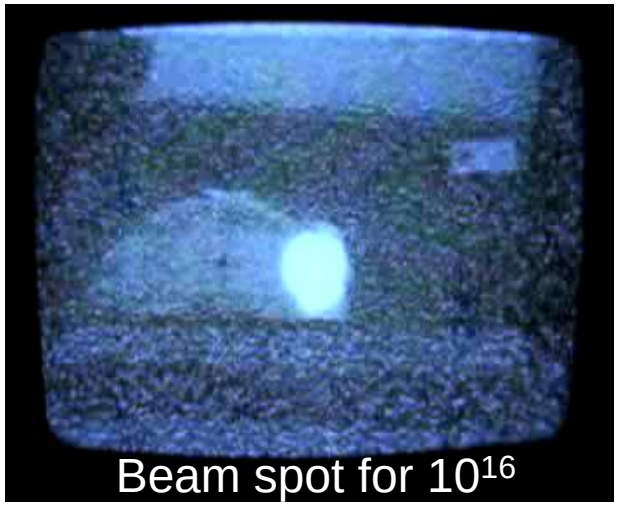
Irradiation

- CYRIC cyclotron in Japan
  - 70 MeV protons, a few-800 nA
- Latest irradiation
  - 21-22 July 2010
  - $5x10^{12}$, 10^{13}, 10^{14}, 10^{15}, and 10^{16}
- Samples
  - From RD Wafer#1 (and a diamond)
  - Results to be presented in a next conference

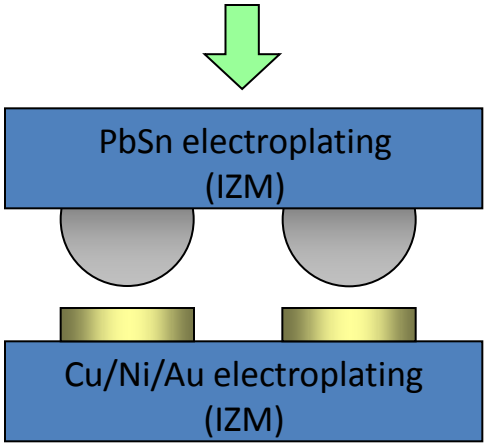

Box and stage in the beamline


Typical packaging

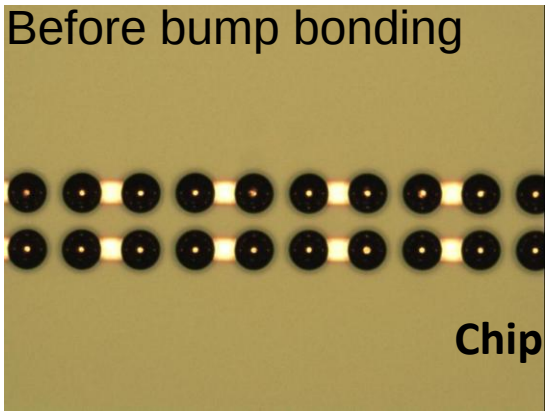

Irradiation box

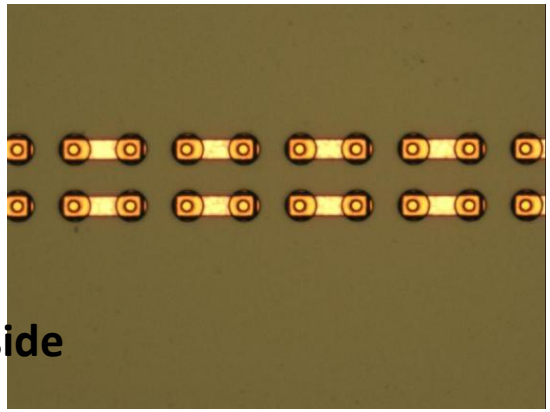

Beam spot for 10^{16}

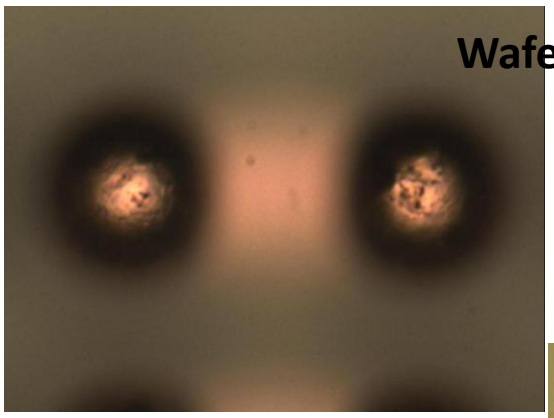
PbSn Solder Bump-bonding at HPK

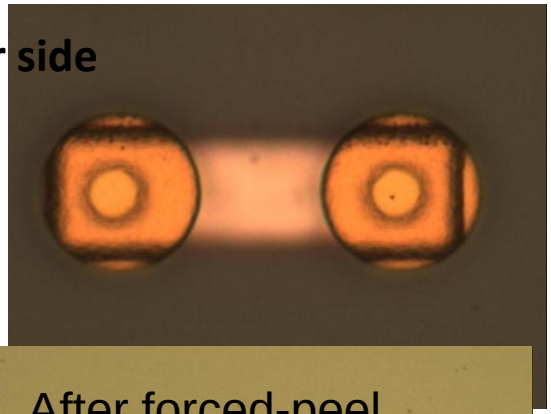


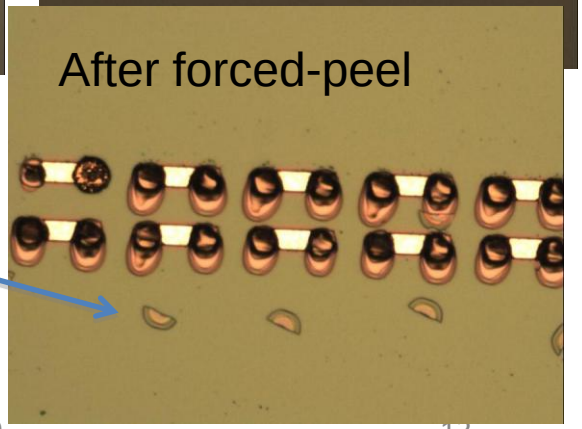
- With Al-pattern dummy chips
- PbSn solder bumps
  - Pb-solder bump by IZM (as FE-I3)
- Bump side: Height 28.8 µm
- UBM side: Height 6.3 µm
- Parameter optimization for
  - Small bump deformation
  - Most of the peel from substrate
  - Fractures in the solder
  - Good melt of solder and UBM
  - Without open or short







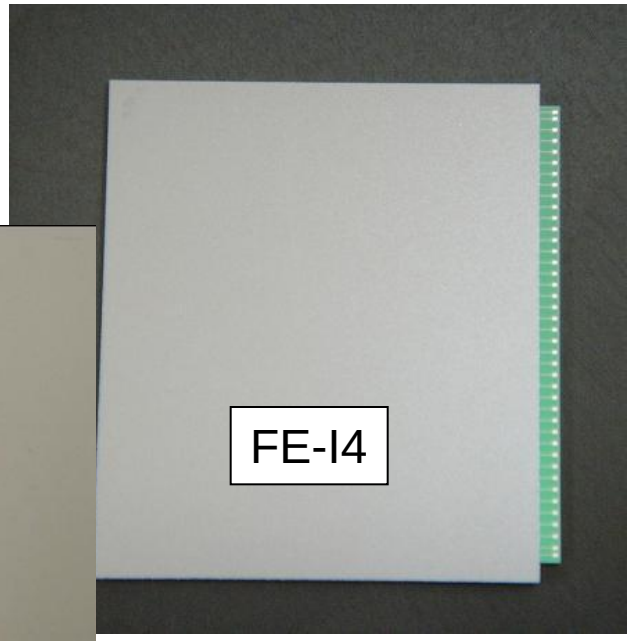


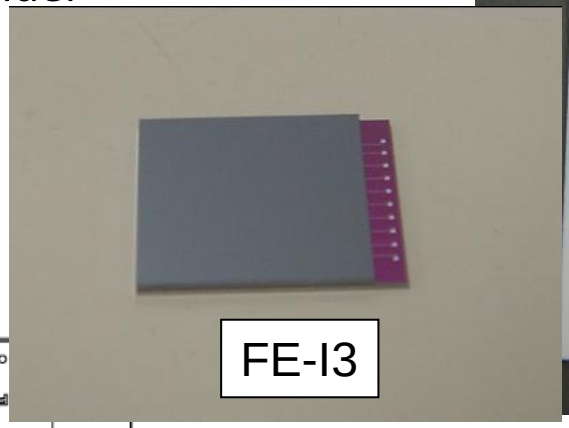


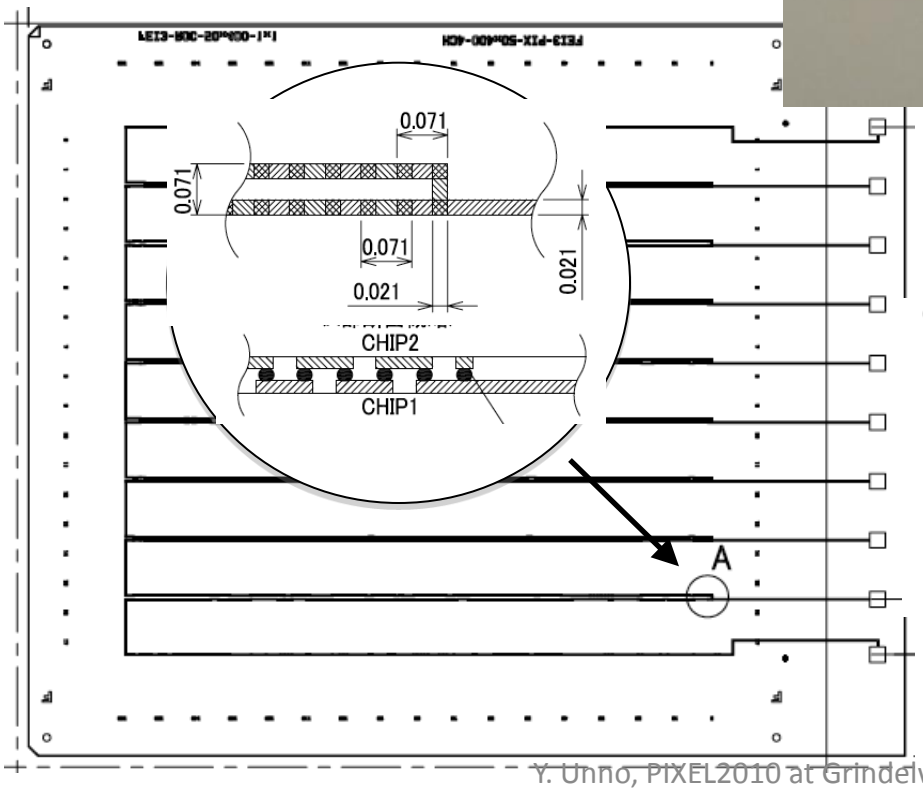
"half moon" residues are peels from substrate

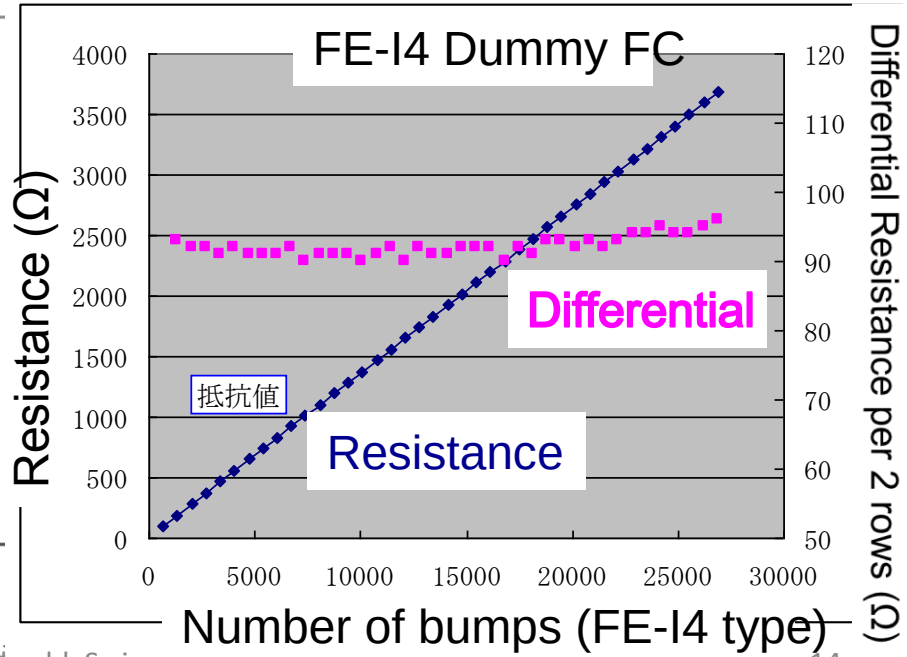
Bump yield tests

- Al-pattern with bumps
  - Pb (PbSn) and Pb-free (SnAg) solder
  - FE-I3 and FE-I4 pattern
  - Single chips
    - Multi-chips next
- Results
  - Good peel strength
  - Good yield of bump connection

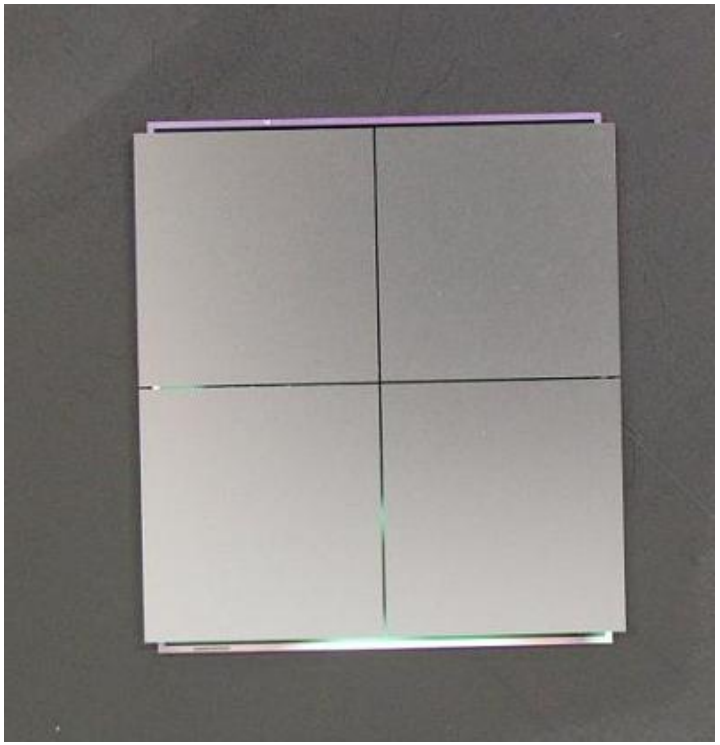






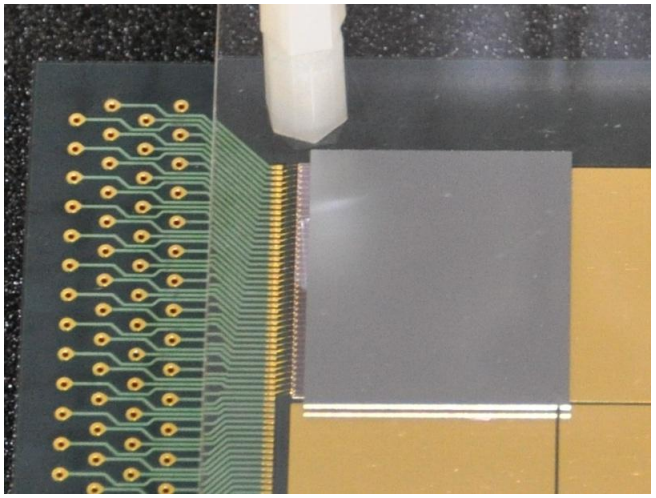


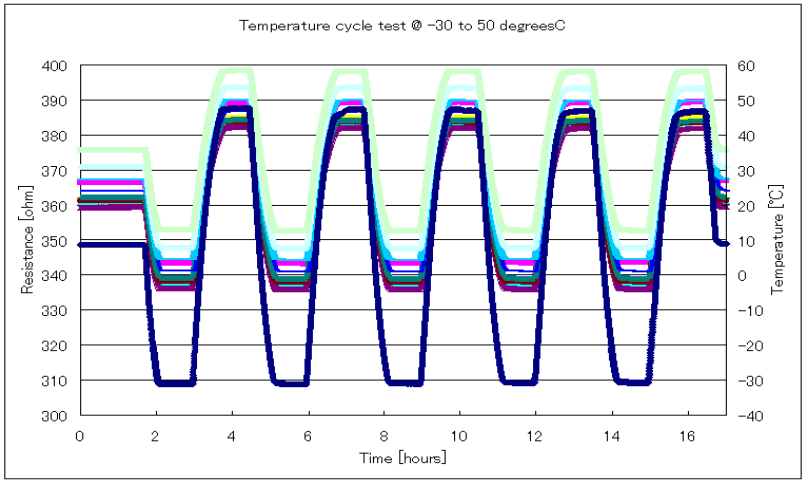
2x2 Multi-chip Stack

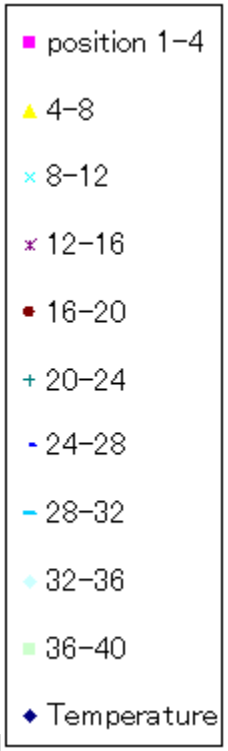


- Samples - 2 stacks each
  - Two 2x2FE-I3
  - Two 2x2FE-I4
- Daisy chain resistance
  - Very little open
  - Some shorts

Thermal Cycling

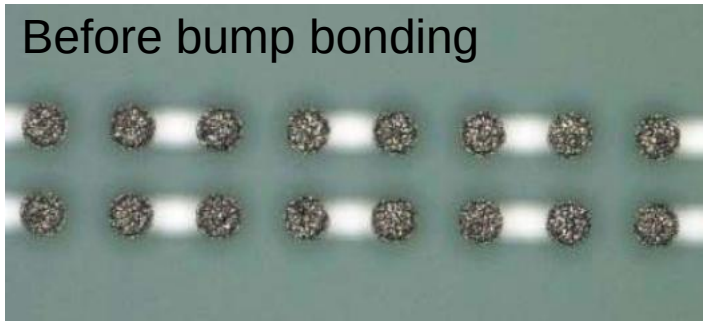


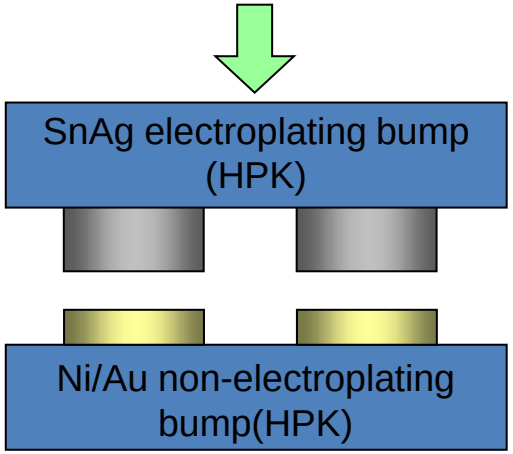


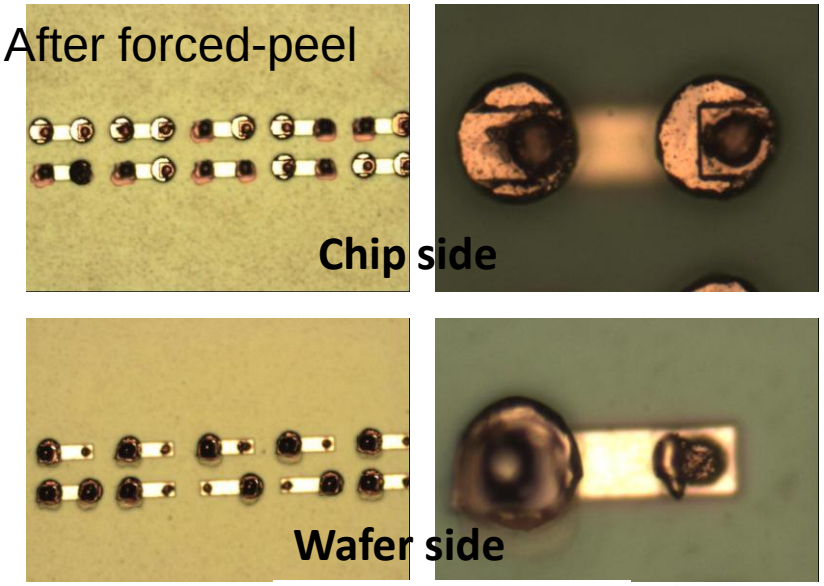


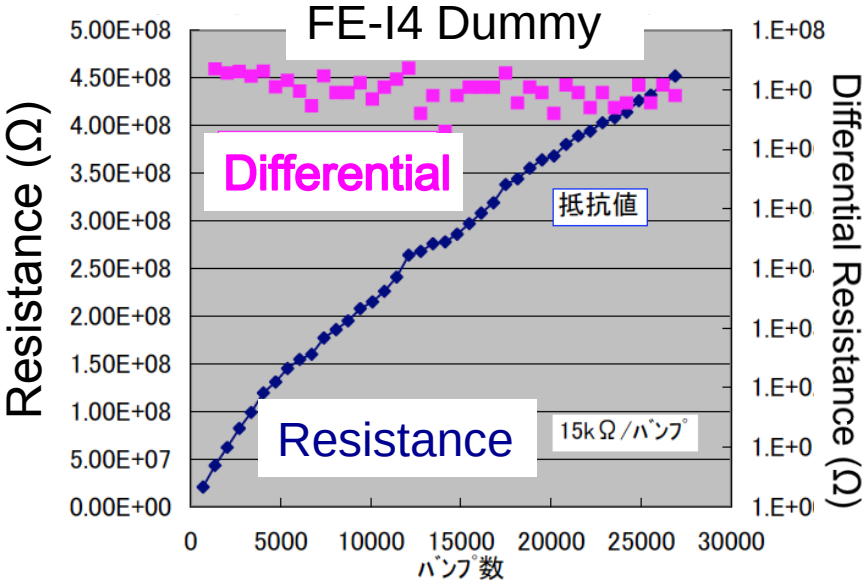
- Two FE-I4 dummies were tested
  - -30 °C - +50 °C, 10 cycles
- No bump failure was observed

Pb-free (SnAg) Bump-bonding



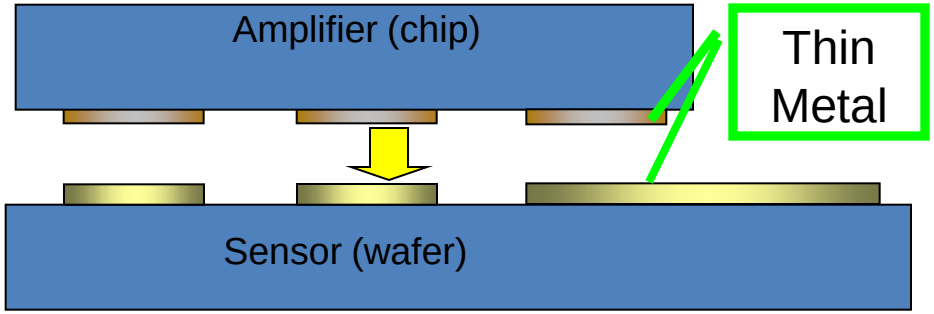


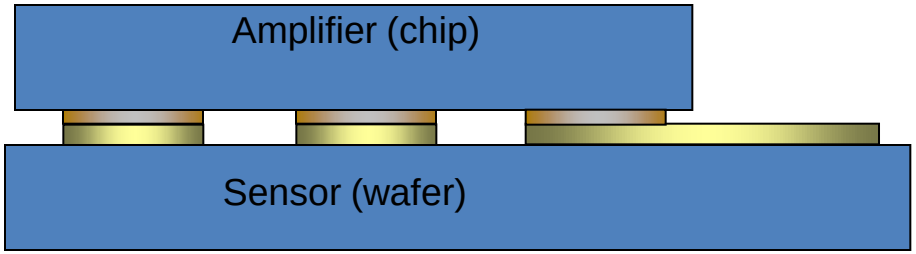




- Results
  - Strong peel-strength
    - Chip cracks when peeled off
  - Peel from substrate/Solder fracture 50/50
  - No open/sort
- Need further optimization
  - Large contact resistance (~1kΩ/bump)

Bumpless Bonding at HPK



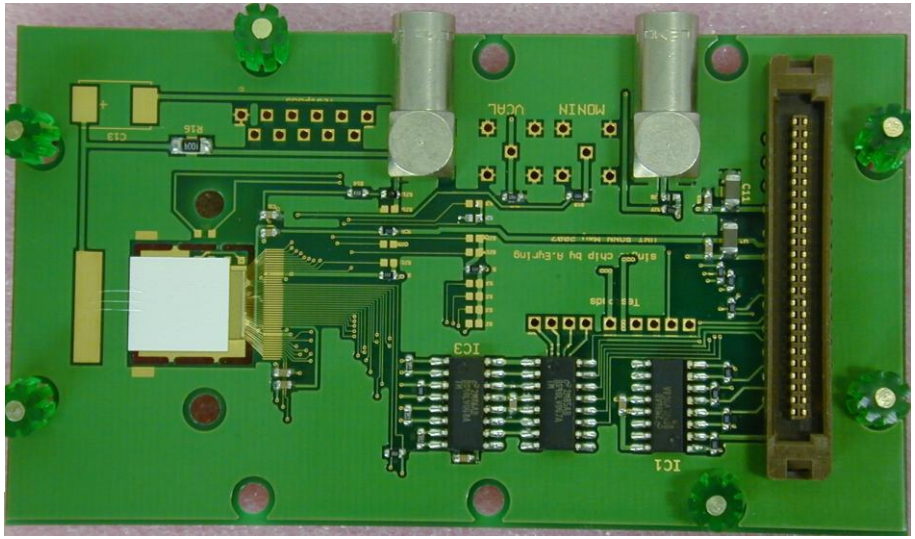


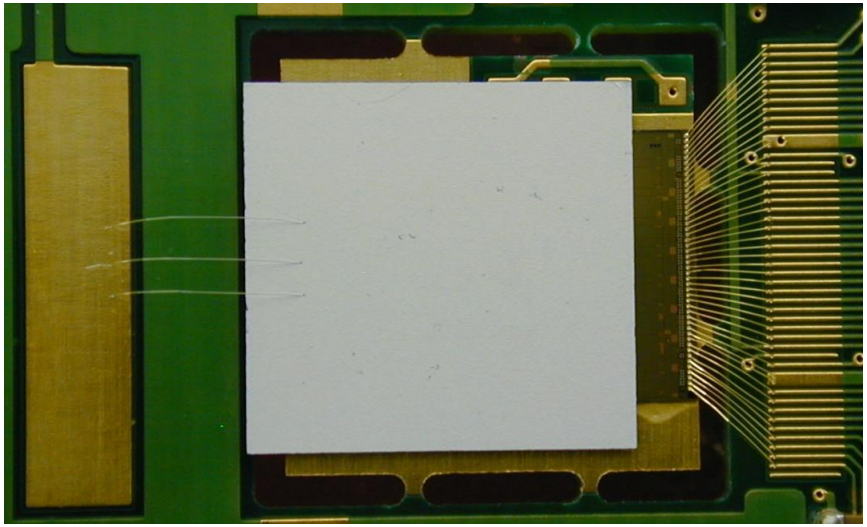
- We are looking forward to the “bumpless” bonding at HPK for future.
- Bumpless bonding contributes to low-cost and small volume of metal because of thin metal electrodes
- Chip-to-Wafer bonding is more relevant than wafer-to-wafer because of the difference of the chip/wafer size and yield of the IC and the sensor.

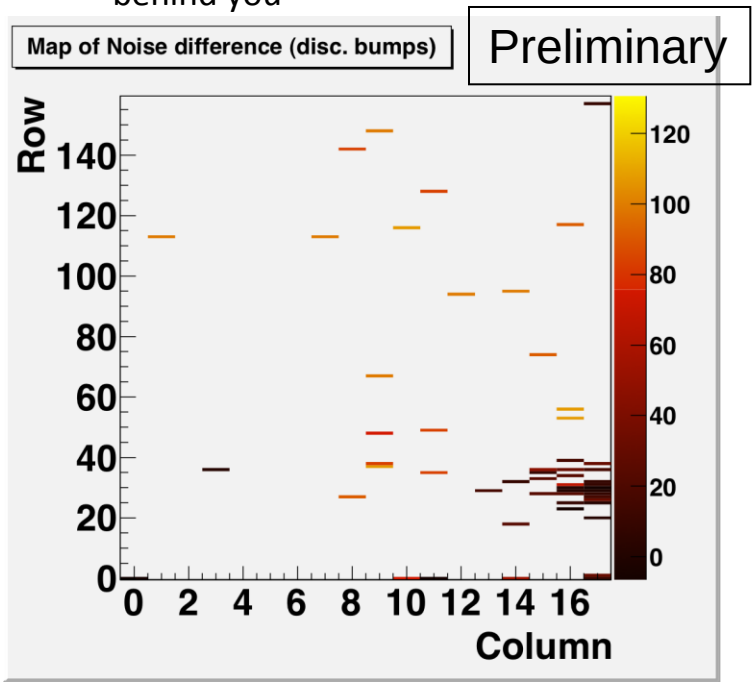
Method	Thermal Compression	Plasma Activation (PAB)	Surface Activation (SAB)
Activation	Ar plasma	Sequential	Ion beam
Bonding	Thermal compression	ON radical	Bond arm+Metal
Bond medium	Au-Au	Si/SiO2-Si/SiO2	Si/SiO2-Si/SiO2 Au-Au
Temperature	100-200˚C	<100˚C <200˚C	Room T.
Electrode	Au, Cu	Au, Cu	Au, Cu, Al
Availability	Planned	Planned	Soon

HPK n-in-p Pixel Sensor/FE-I3 Module

- PbSn solder bump bonding by HPK
  - With IZM PbSn solders on FE-I3
  - With HPK non-electroplating UBM on pixel sensors
  - Bump yield ~98%
    - Non-electroplating - an issue
- 1st pixel sensor and bump-bonded module made by HPK for us (for HEP community)
  - Although not a perfect and ~10 yrs(?) behind you







Summary

- We have fabricated
  - N-in-P Pixel sensors in two R&D wafers, #1 with FE-I3 and #2 with FE-I4 designs
  - The study on the distance-to-edge has shown
    - ~450 µm distance is expected to hold 1000 V bias voltage, both in the N-sub and P-sub wafers
  - The study on the number of guard ring has shown
    - Irrelevant to reduce the distance to edge
  - Thinned sensors, 200 µm thick, hold 1,000 V
- Bump-bonding development is on-going
  - PbSn solder bumping has been successful
  - SnAg (Pb-free) solder bumping has been started
  - 1st Real (pixel sensor+Pixel ASIC (FE-I3)) has been made for us (HEP community) by HPK
- Looking forward to the performance after irradiation

PIXEL2010 at Grindelwald

Thank you for excellent organization