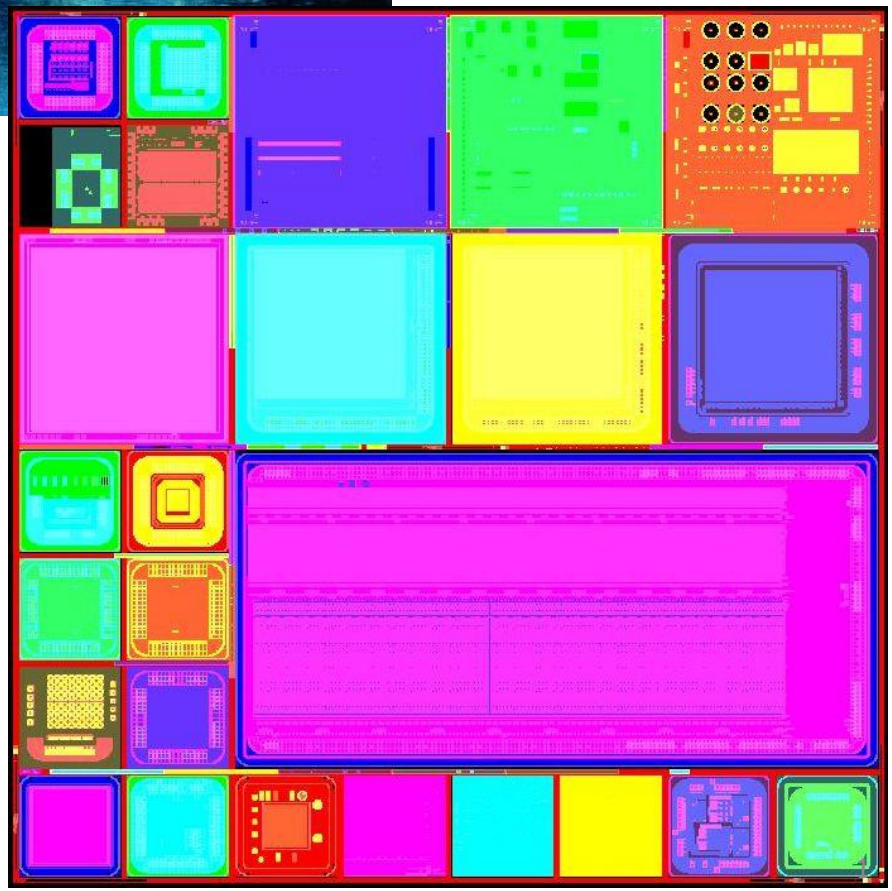


Progress of SOI Pixel Detectors

Sep. 9, 2010 @PIXEL2010
Yasuo Arai, KEK
yasuo.arai@kek.jp
http://rd.kek.jp/project/soi/

OUTLINE

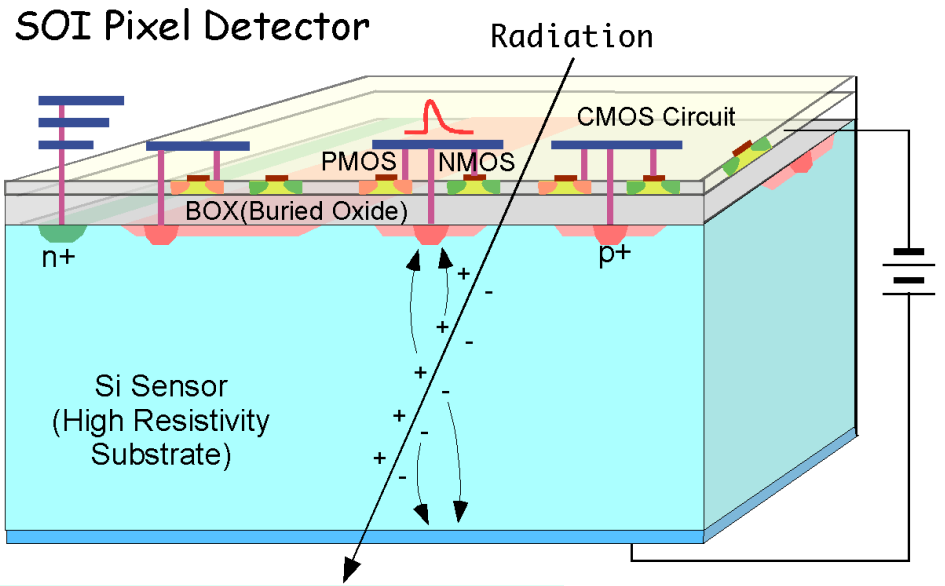
1. Overview of SOIPIX activities
2. On-Going R&Ds
   Buried P-Well
   Wafer Thinning
   FZ-SOI Wafer
   Nested BNW/BPW Structure
   Double SOI Wafer
3. Summary

Other SOI related talks

- XFEL – MVIA → T. Hatusi
- ILC Pair Monitor → Y. Sato
- LBNL/Padva → P. Giubilato
- Vertical Integration → M. Motoyoshi
  R. Yarema

SOI Pixel Detector

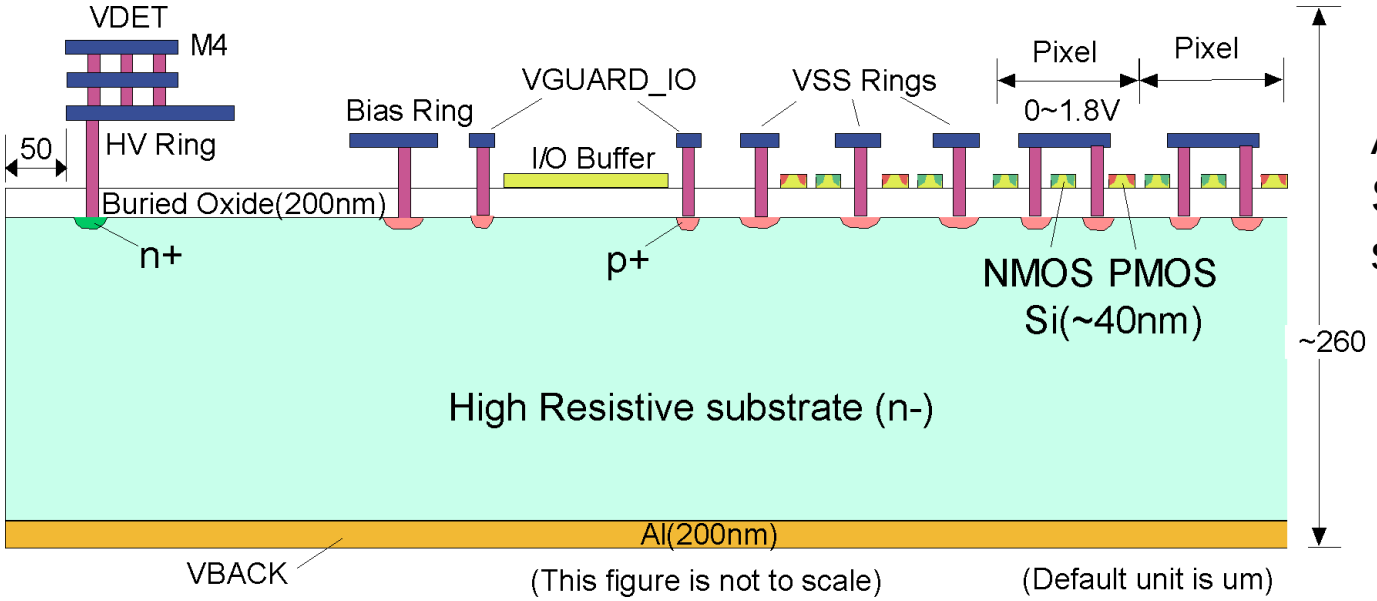
Monolithic detector using Bonded wafer (SOI : Silicon-on-Insulator) of Hi-R and Low-R Si layers.



- No mechanical bump bondings
  - -> High Density, Low material budget
  - -> Low parasitic Capacitance, High Sensitivity
- Standard CMOS circuits can be built
- Thin active Si layer (~40 nm)
  - -> No Latch Up, Small SEE Cross section.
- Based on Industrial standard technology
- Seamless connection to Vertical Integration

OKI 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI) 1 Poly, 4 (5) Metal layers, MIM Capacitor, DMOS option Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、~700 Ω-cm (*n-type)*, 650 μm thick
Backside	Thinned to 260 μm and sputtered with Al (200 nm).



An example of a SOI Pixel cross section

MPW (Multi Project Wafer) run

~Twice per Year

SOI MPW run Users

KEK, Tsukuba Univ., Tohoku Univ., Kyoto Univ.,
Kyoto U. of Education, Osaka Univ., JAXA/ISAS,
RIKEN, AIST

LBNL, FNAL, Univ. of Hawaii

INP Krakow, INFN Padova, Louvain-la-Neuve Univ.,
Universität Heidelberg

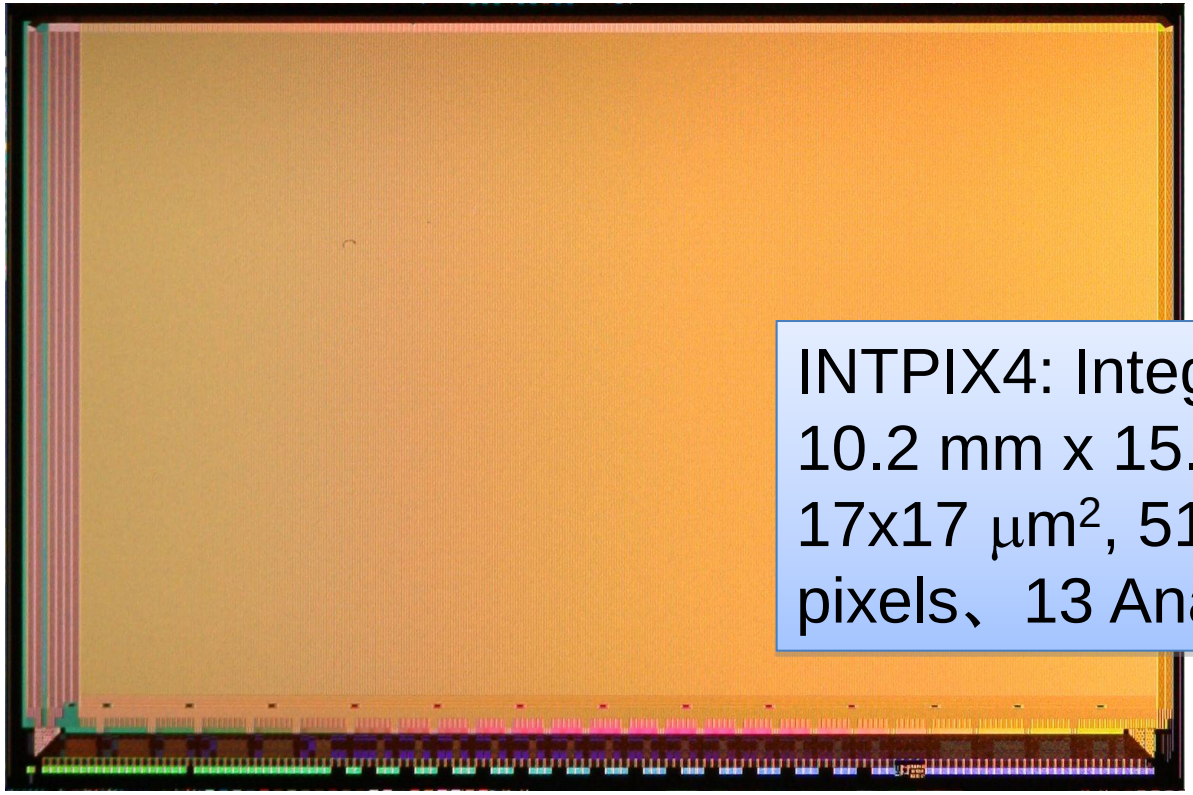
IHEP China
Budker Institute of Nucl. Phys.

Open to anybody!

Supporting Companies

OKI Semiconductor Co. Ltd. ,
OKI Semiconductor Miyagi Co. Ltd. ,
T-Micro Co. Ltd., Rigaku Co. Ltd.

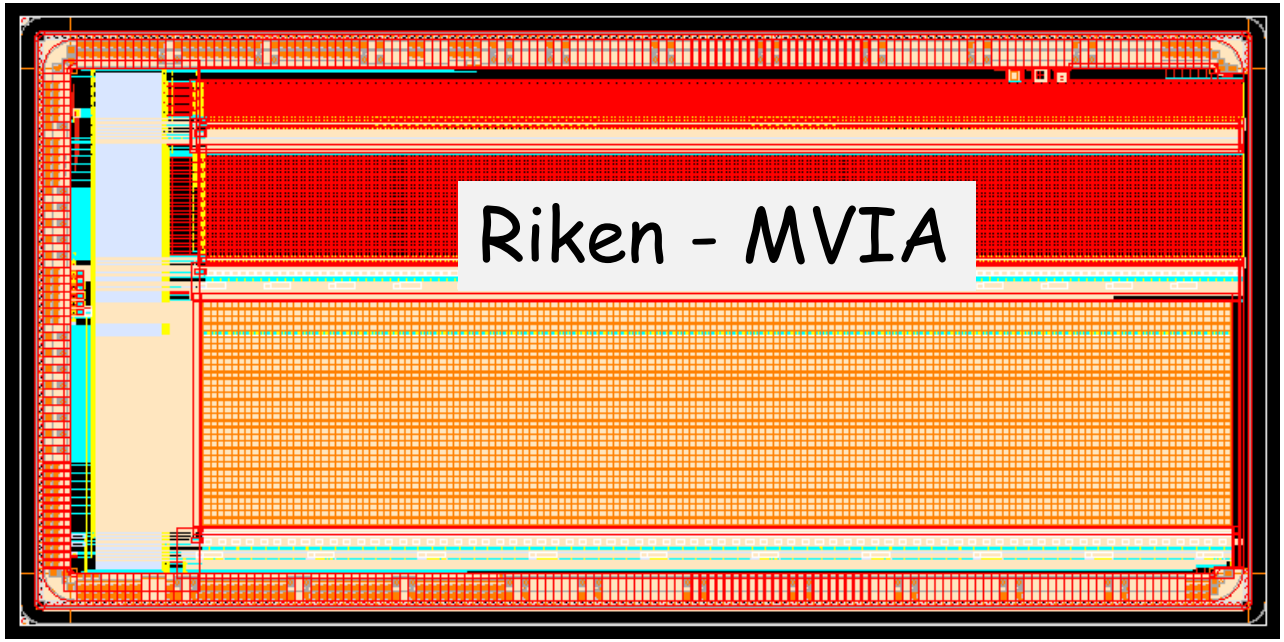
KEK SOI Pixels

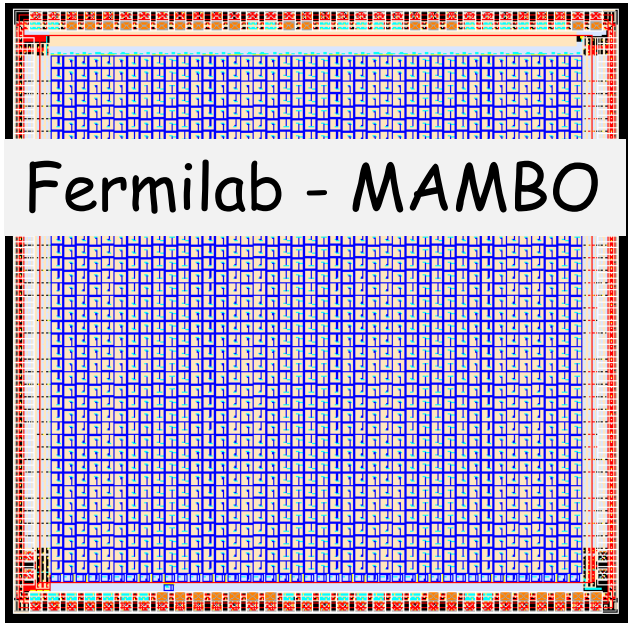


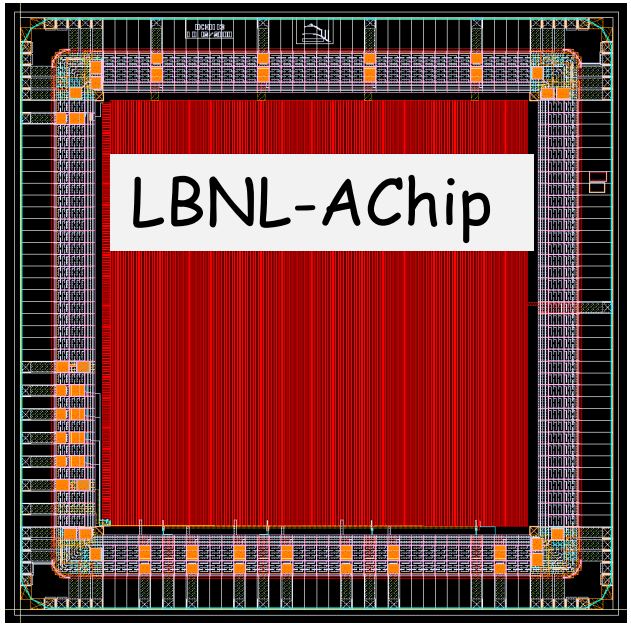
INTPIX4: Integration Type
10.2 mm x 15.4 mm
17x17 μm^2, 512x832 (~430k) pixels、13 Analog Out、CDS.

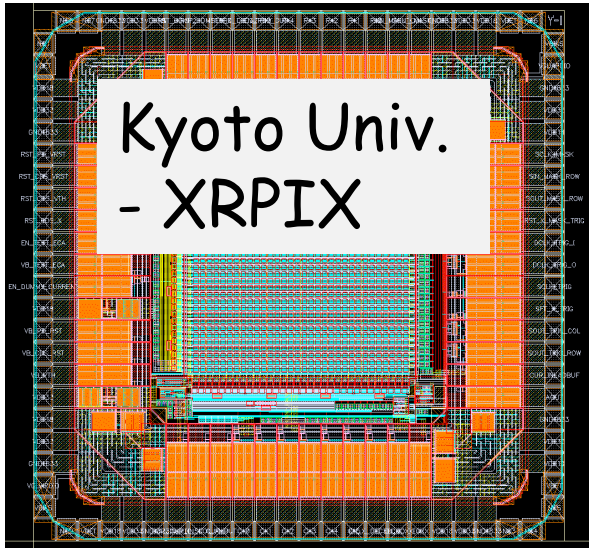
CNTPIX5: Counting Type
5 mm x 15.4 mm
64 x 64 μm^2, 72 x 272 pixels
Amp+Shaper+2xDiscri+2x9b Counter

Other SOI Pixels



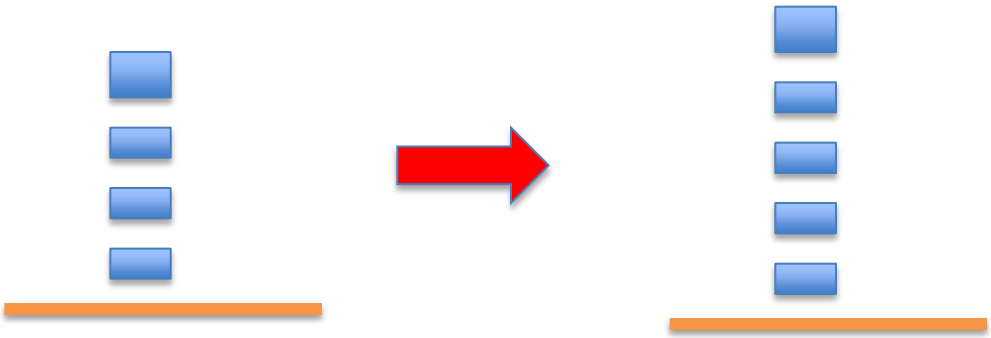




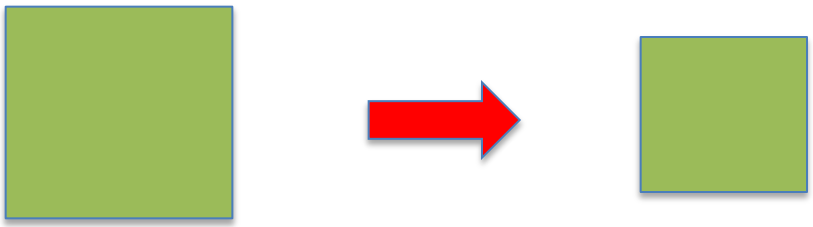


Recent Process Improvements

- Increase No. of Metal Layer : 4 -> 5 layers
  --> Better Power Grid and Higher Integration

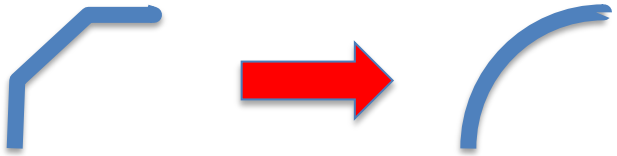


- Shrink MIM capacitor size : 1 -> 1.5 fF/um^2
  --> Smaller Pixel size become possible

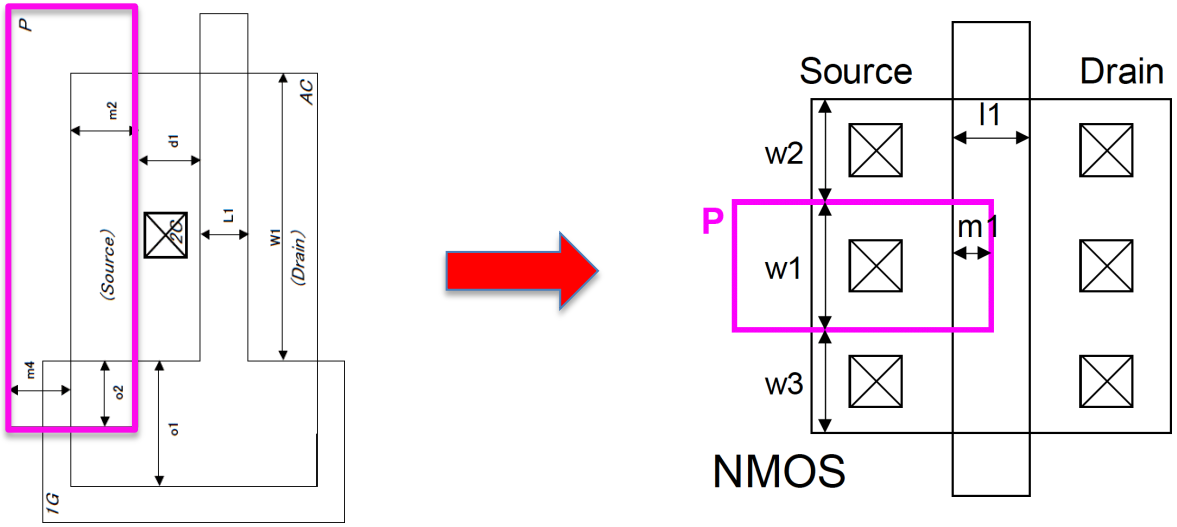


Recent Process Improvements

- Relax drawing rule : 30º, 45º -> Circle
  --> Smooth field and Higher Break Down Voltage



- Introduction of source-inserted body contacts
  --> Better body contacts (Less kink and history effects, Lower noise).



On-Going R&Ds

a. Back Gate Effect : Sensor voltage affect Transistor characteristics
   → Buried P-Well (BPW) layer

b. Wafer Thinning : Thin Sensor
   → TAICO process

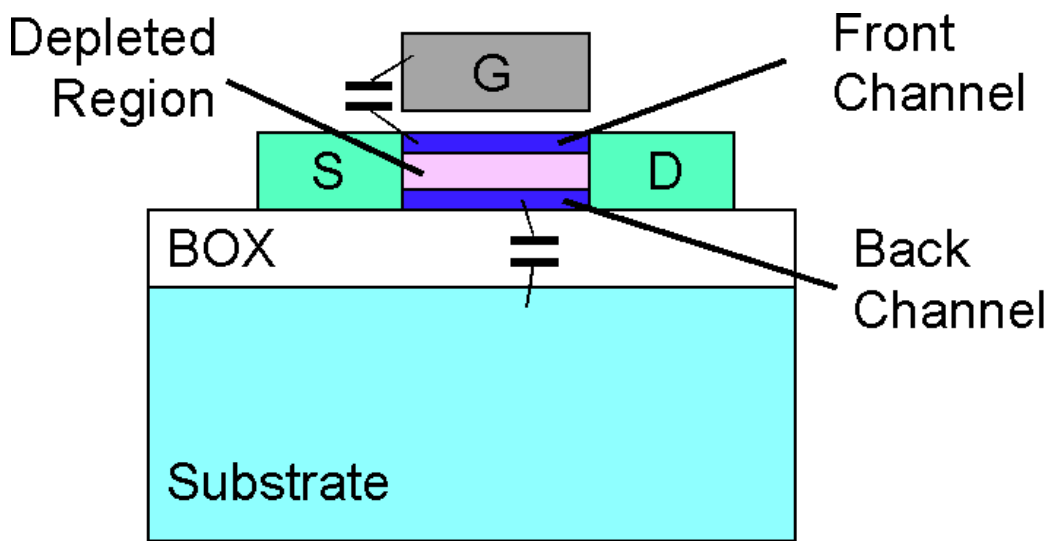
c. Wafer Resistivity : Lower depletion voltage
   → FZ SOI wafer

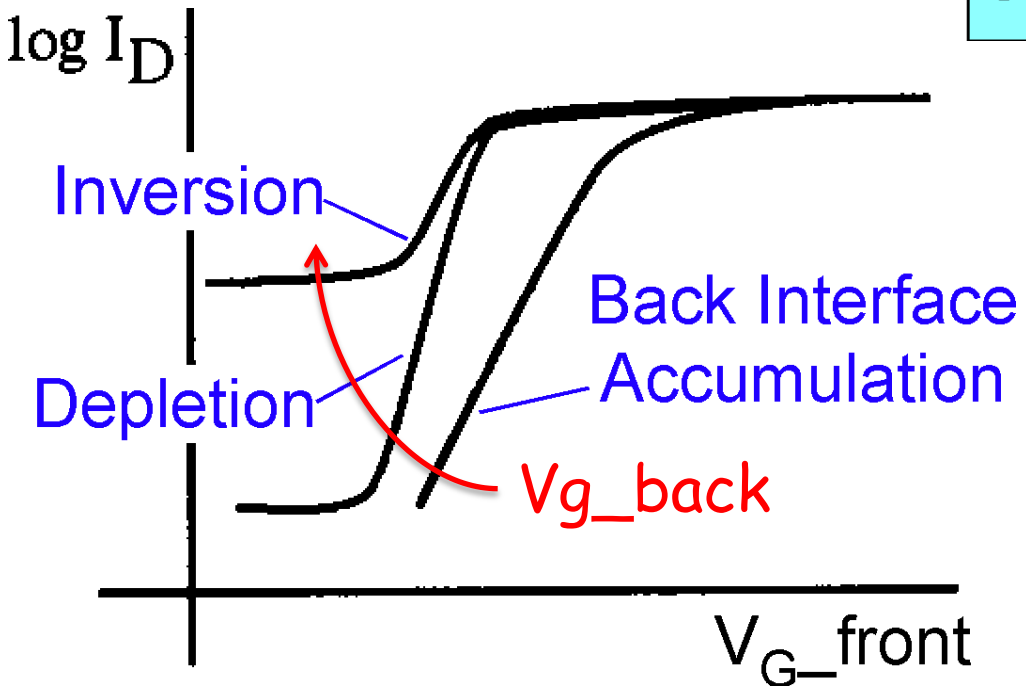
d. Cross Talk : Reduce coupling between Sensor and Circuit
   → Nested BNW/BPW Structure

e. Radiation Hardness : Compensate traped charge
   → Double SOI Wafer

a. Back Gate Effect

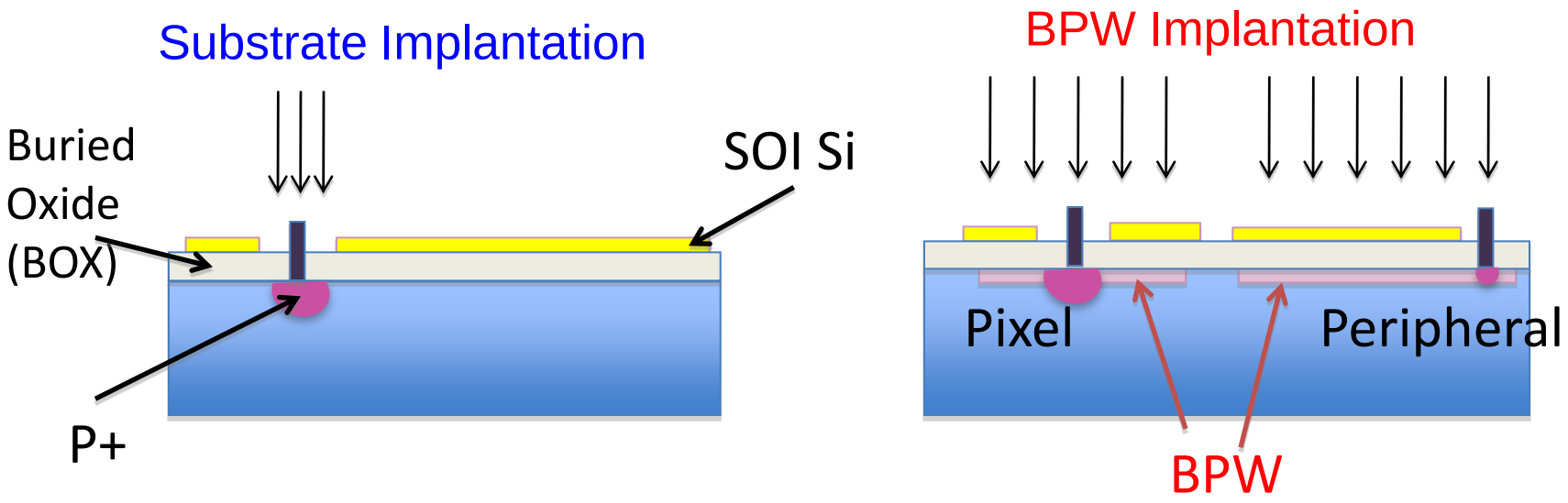
Front Gate and Back Gate are coupled. (Back Gate Effect)





$$\Delta V_{TH\_front} \approx \frac{C_{gate\_oxide}}{C_{BOX}} \Delta V_{G\_back}$$

Buried p-Well (BPW)



- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

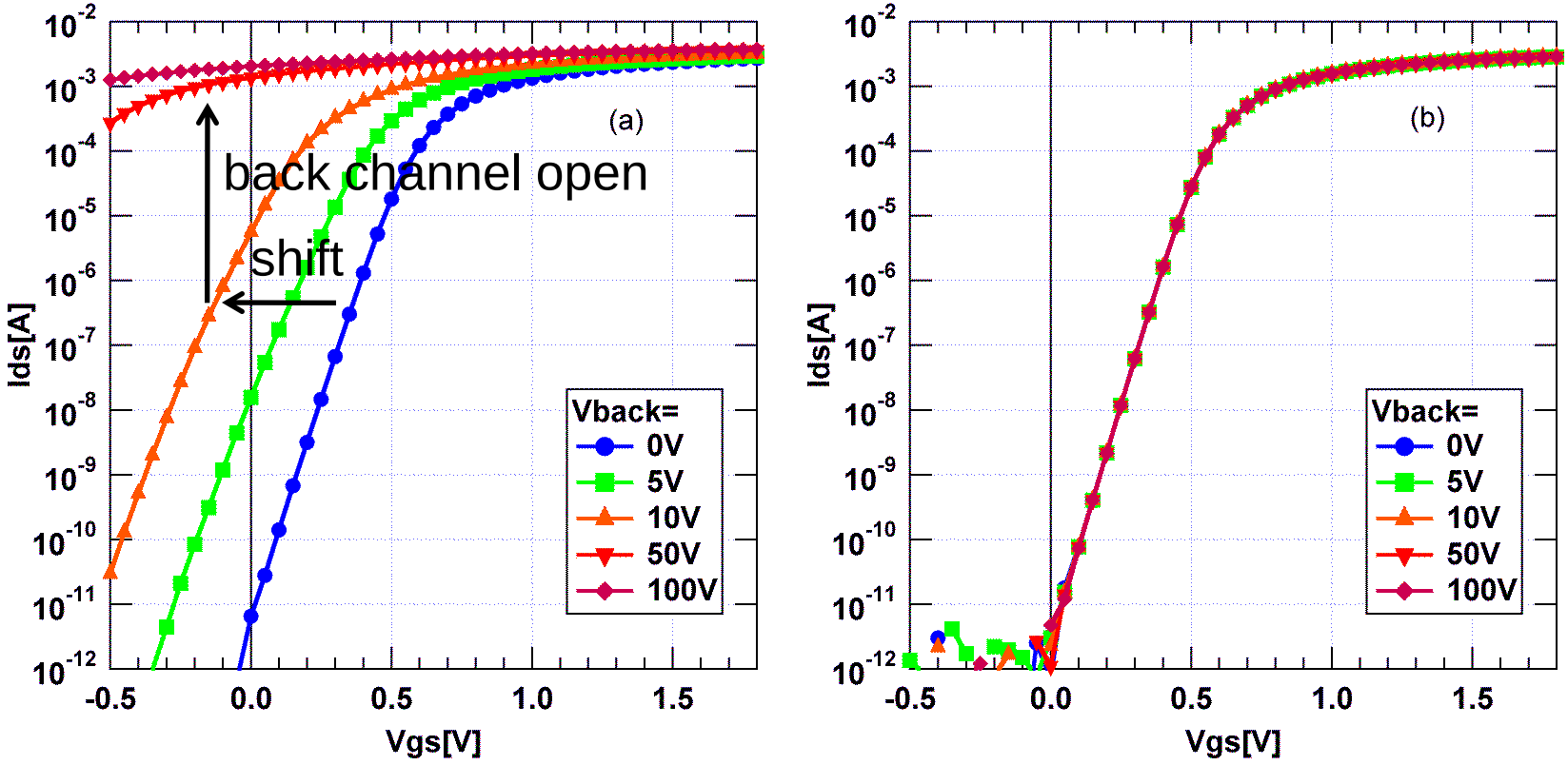
- Suppress the back gate effect.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which may improve radiation hardness.

I_d-V_g and BPW

w/o BPW

with BPW=0V

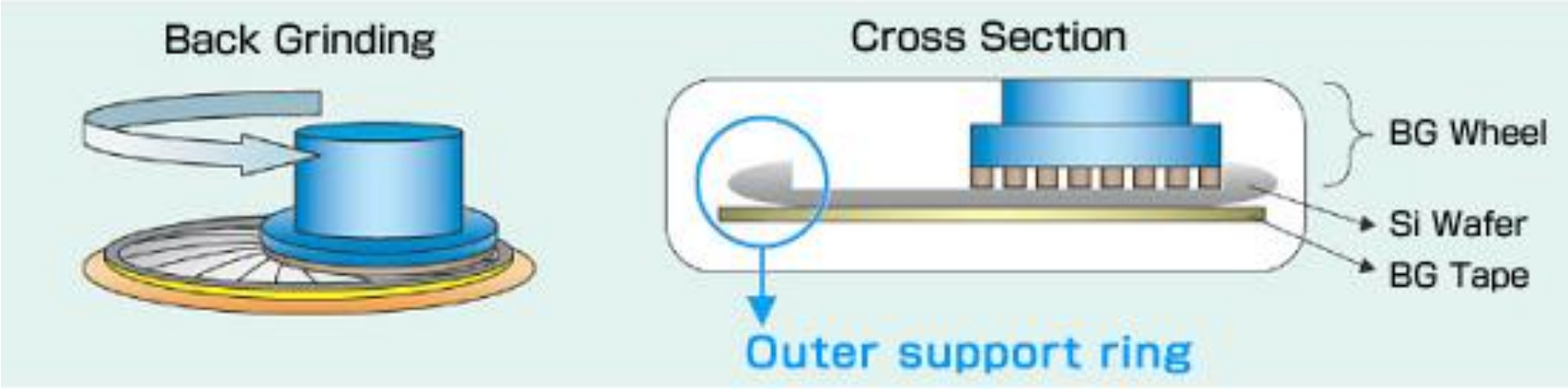
NMOS



Back gate effect is suppressed by the BPW.

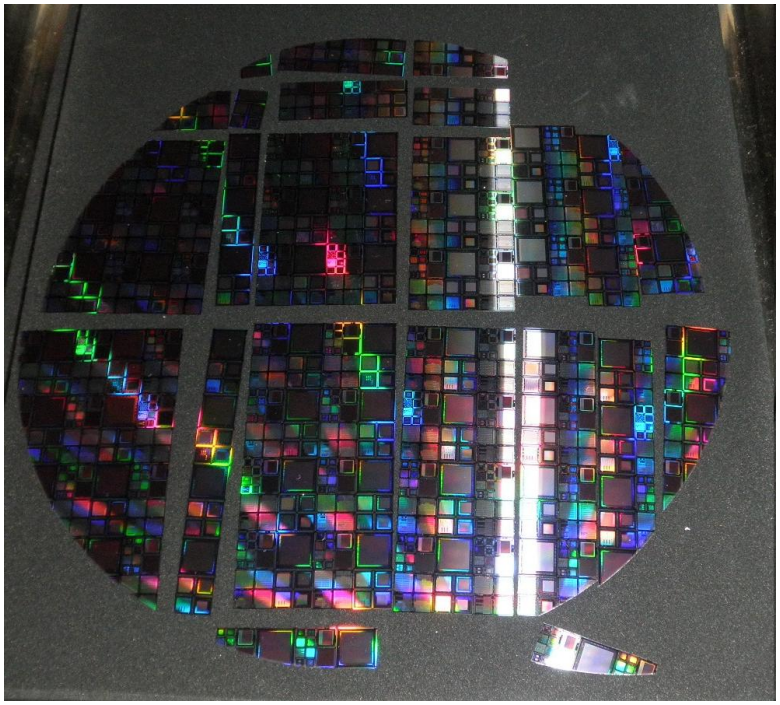
b. Wafer Thinning :TAIKO process

DISCO
Kiru·Kezuru·Migaku Technologies

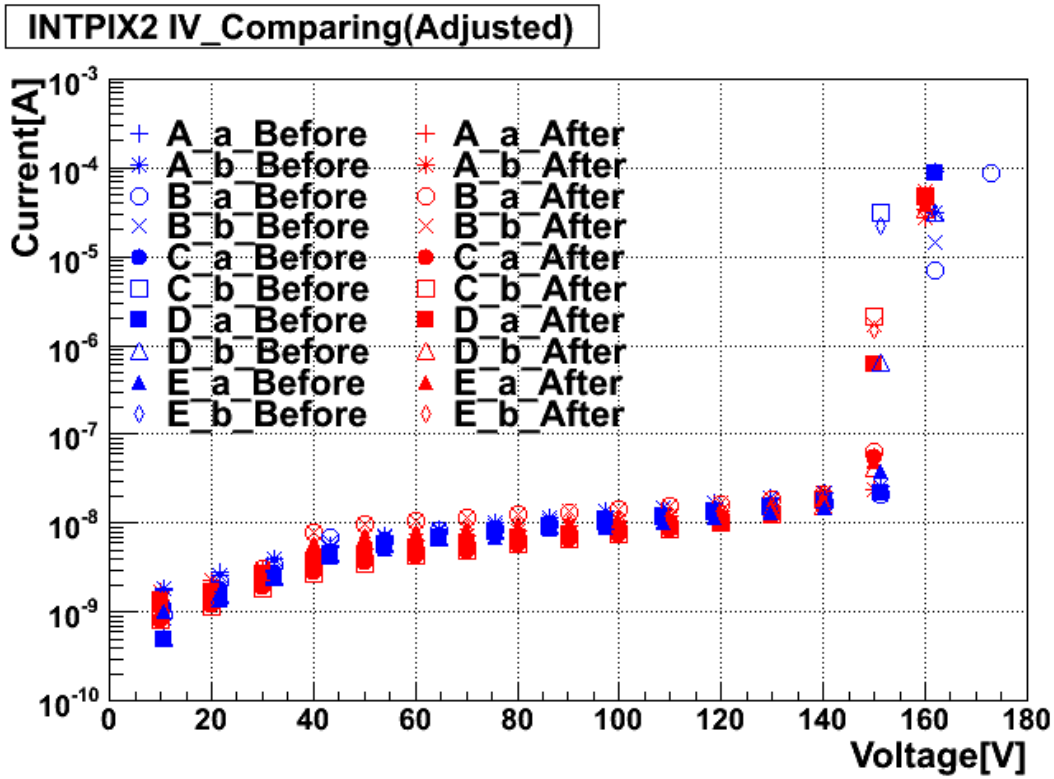


Back side process still can be done after thinning.

Thinned to 110 um and diced

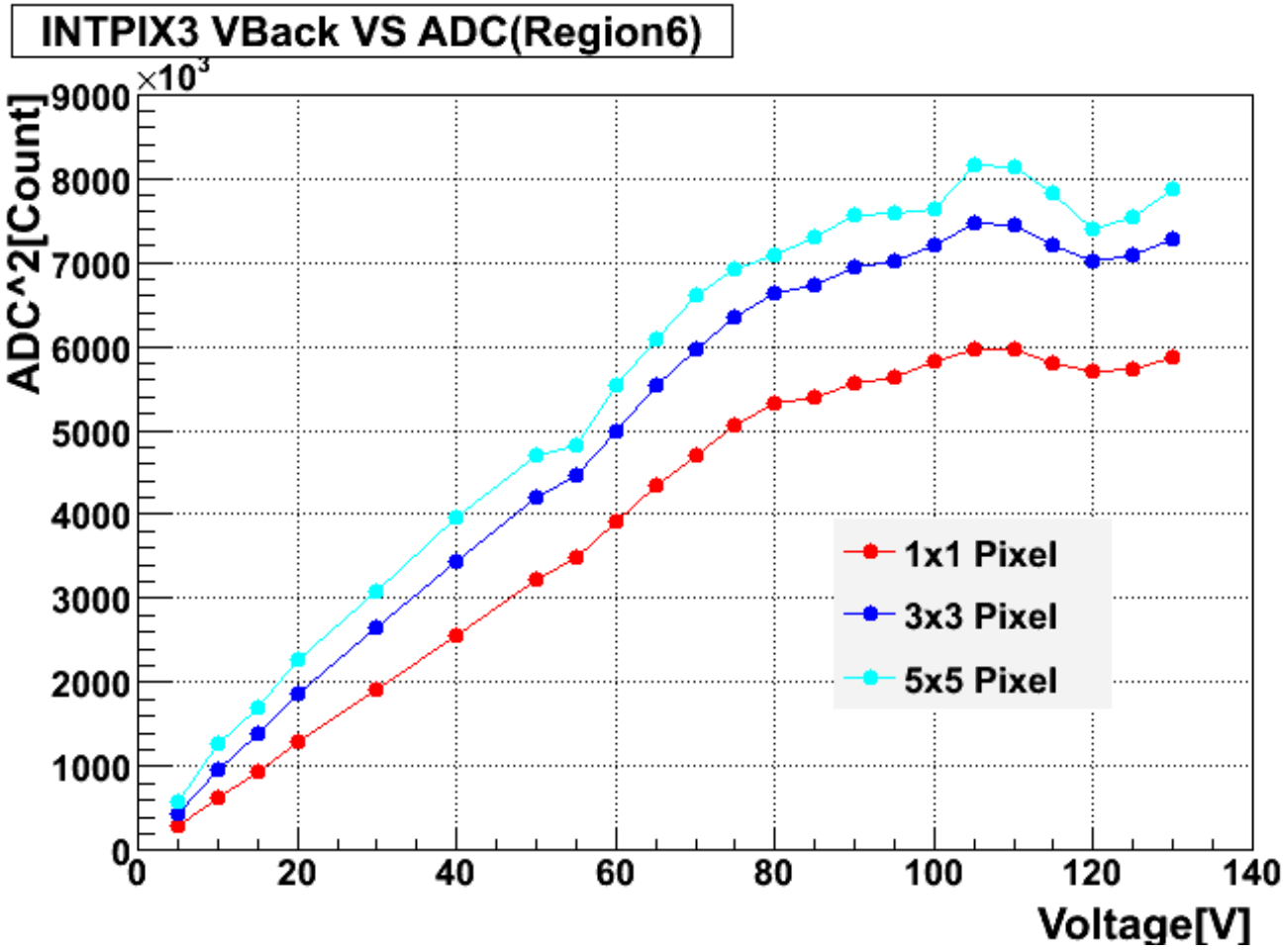


I-V Characteristic
Before & After Thinning



No difference seen after thinning

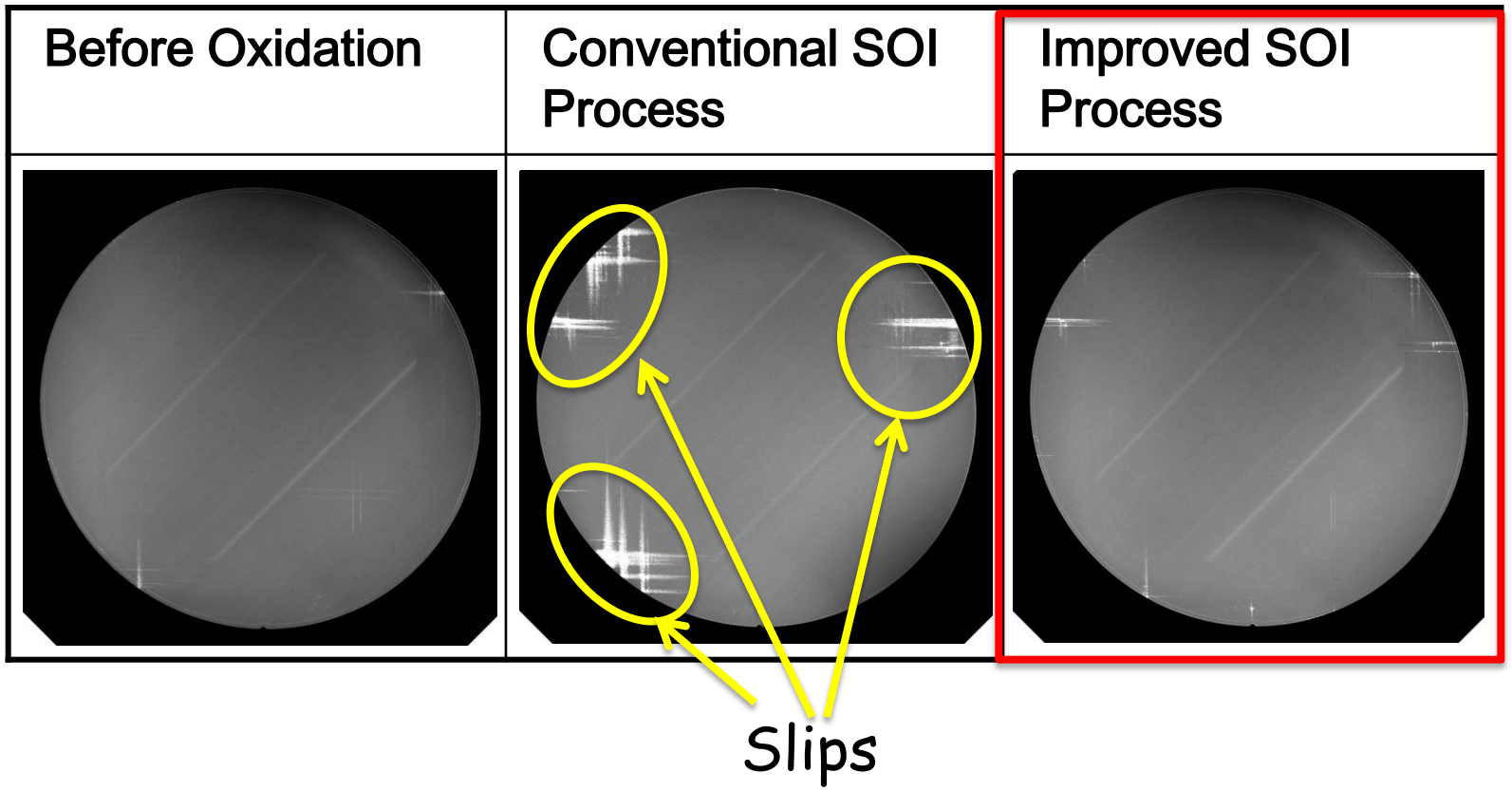
Infrared Laser (1064 nm) Response of Thinned Chip



Full Depleted around 100V

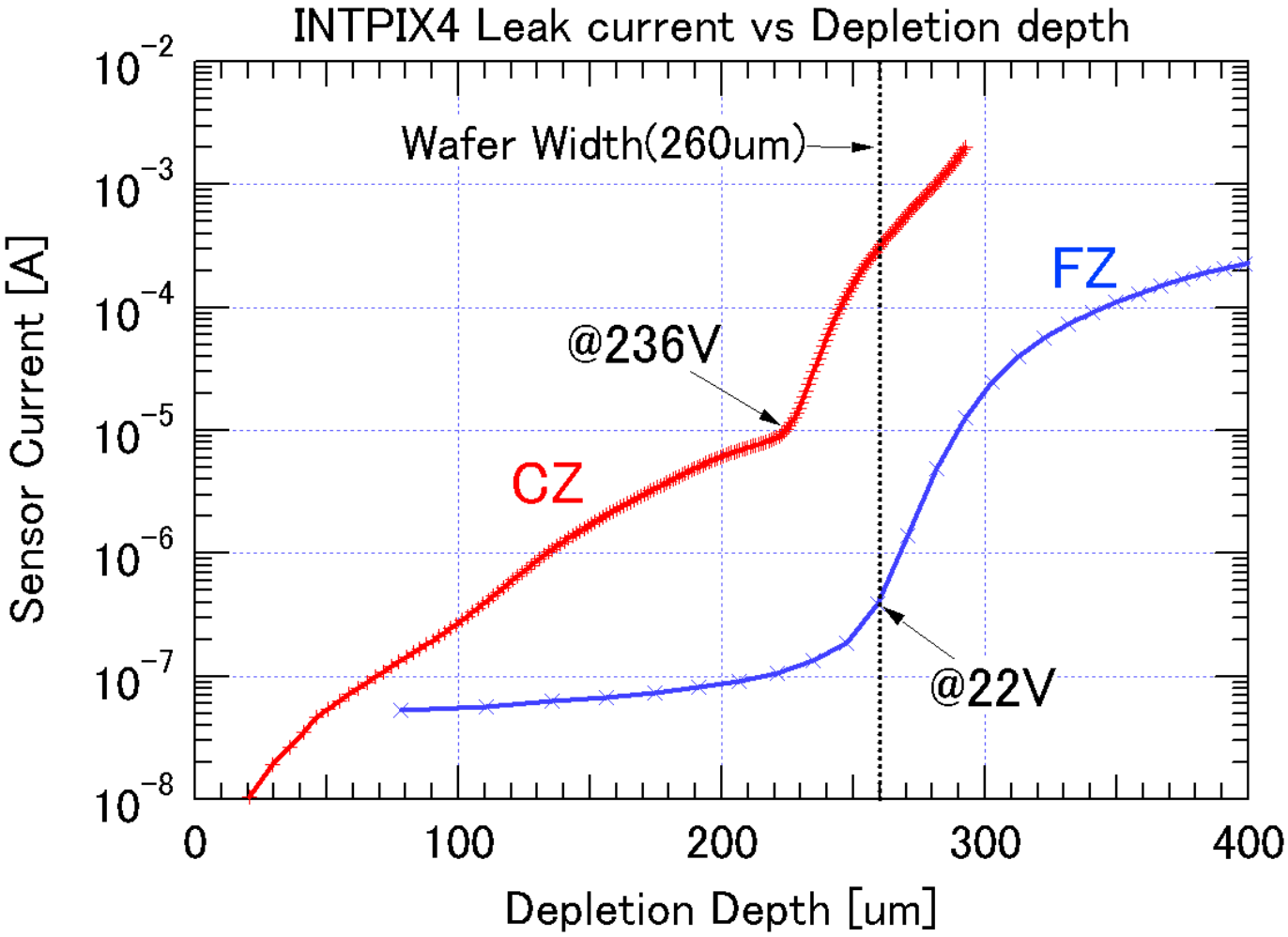
c. Wafer Resistivity : FZ SOI Wafer

During the conventional SOI process, many slips were generated in the 8” FZ-SOI wafer.



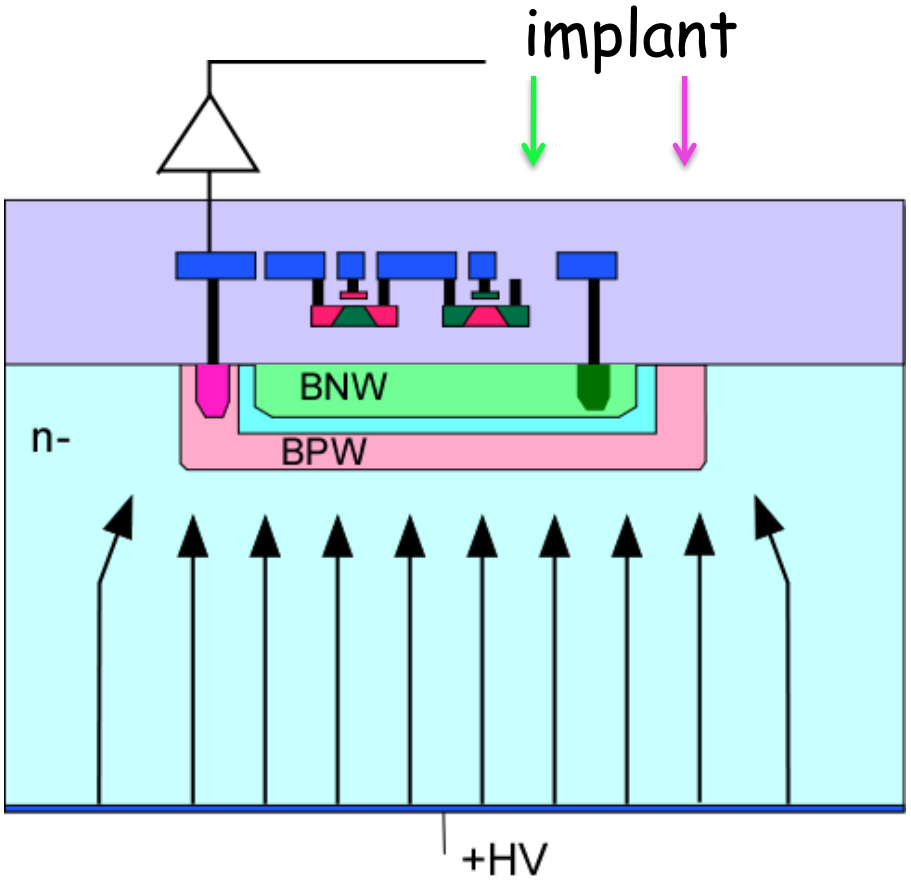
We optimized the process parameters, and succeeded to perform the process without creating many slips.

FZ-SOI Wafer Depletion



Full Depleted @22V

d. Nested BNW/BPW Structure

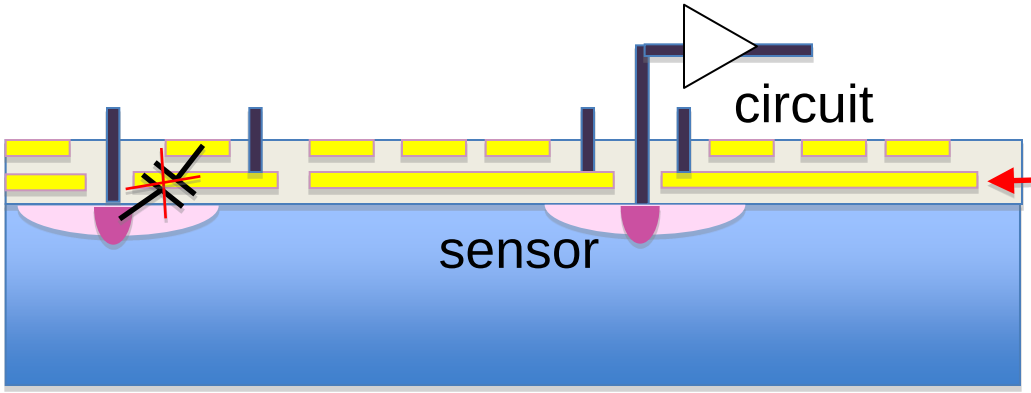


- Signal is collected with the deep Buried P-well.
- Back gate and Cross Talk are shielded with the Buried N-well.
- Test chip is under process.

Structure developed in cooperation between
G. Deptuch (Fermilab) and I. Kurachi (OKI Semi)

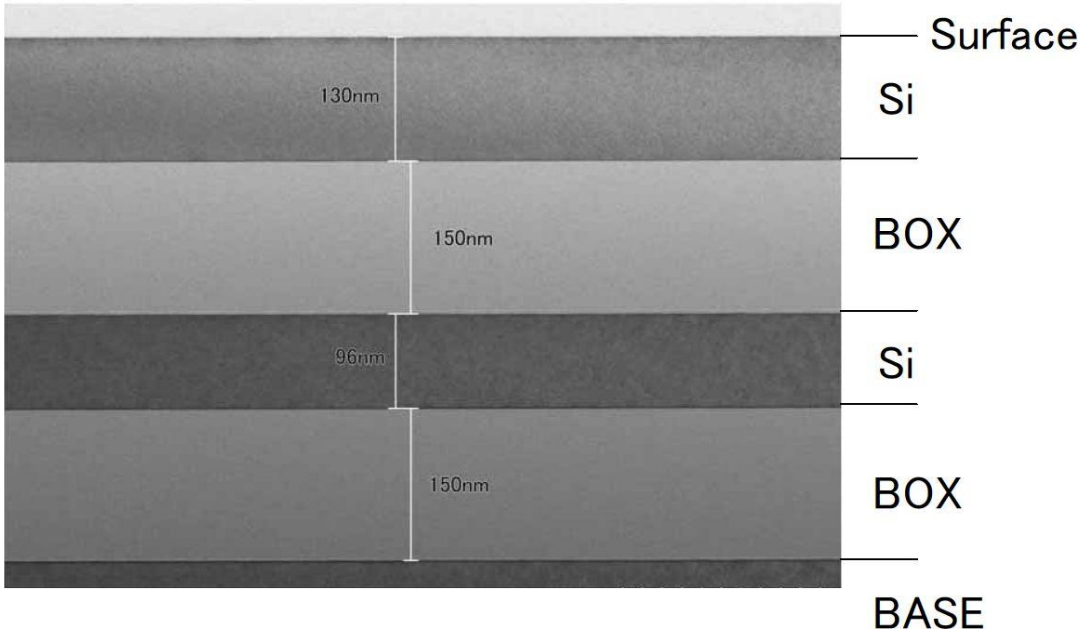
e. Double SOI Layer wafer

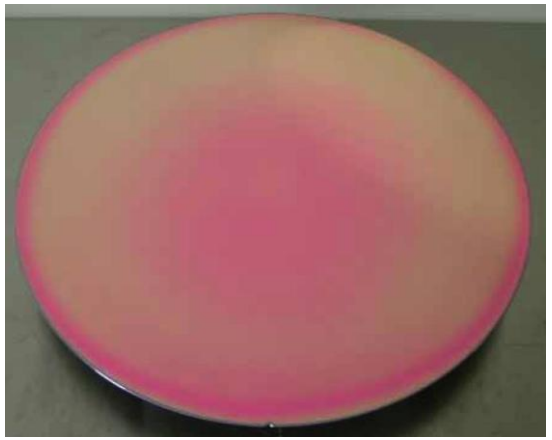
Increase radiation hardness by compensating Oxide/Interface Trap charge with middle layer bias.



additional conduction layer

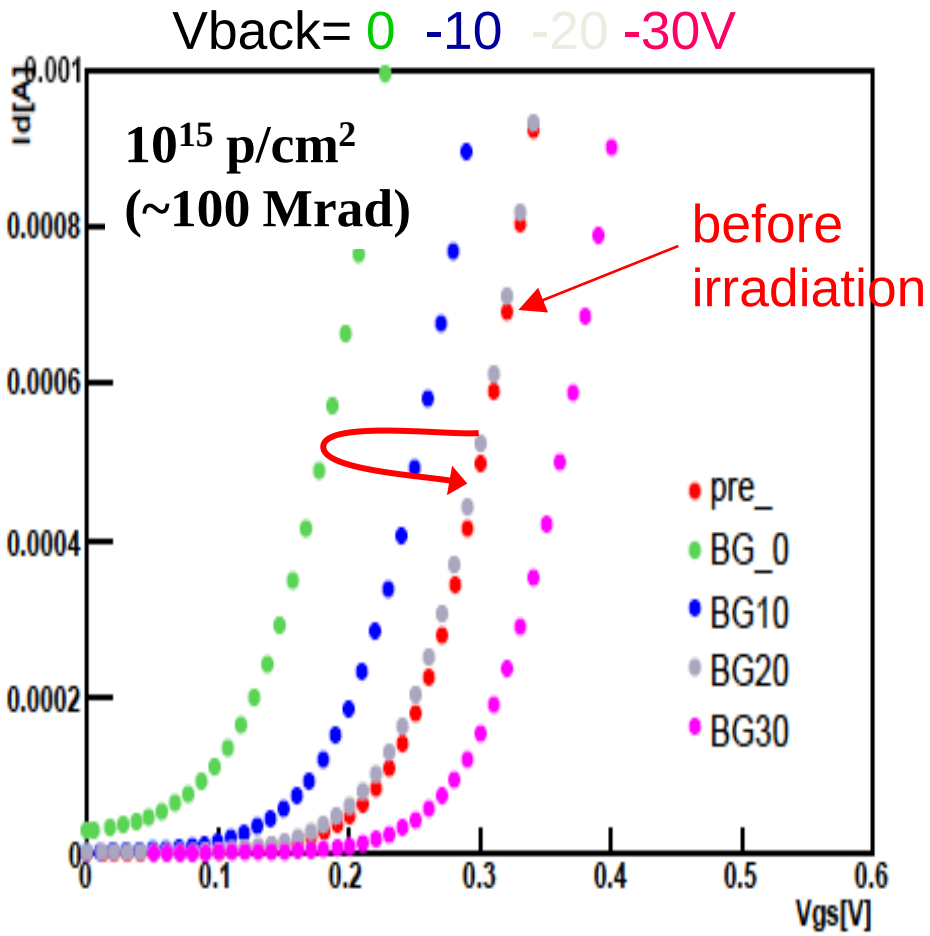
Shield sensors from circuit

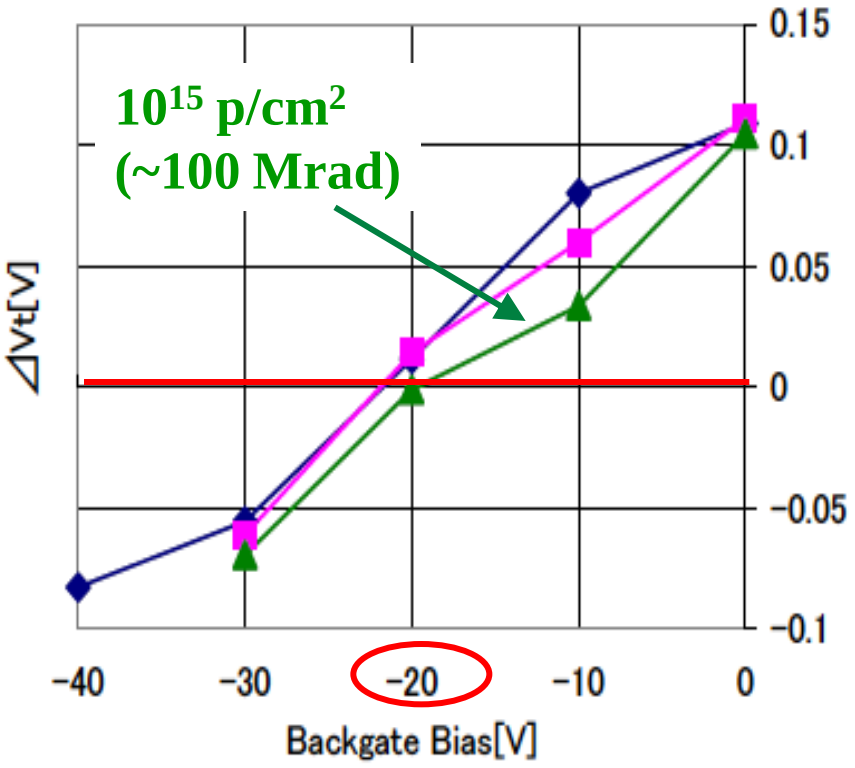




Total Ionization Dose effect can be compensated by back bias

Leak Current and V_{Th} resumes to nearly original value by biasing back side even after 100Mrad.





Summary

- Our SOI MPW run is operated regularly twice per year.
- In addition to many chip designs, a lot of activities are going.

a. Buried P-Well technology is very successful to suppress the Back Gate problem.

b. Thinning to 110um by TAICO process works very well.

c. Wafer resistivity is greatly increased by using FZ-SOI wafer.

d. Nested BNW/BPW structure may resolve cross talk problem and opened possibility of new sensor structure.

e. Manufacturing of Double SOI wafer is being discussed with supply and processing companies.

- Vertical integration → Motoyoshi san's Talk

Supplement

KEK-OKI semi SOI Brief History

'05. 7: Start Collaboration with OKI Semiconductor.

'05.10: First Submission in VDEC 0.15 um MPW.

'06.12: 1st (and last) 0.15 um KEK MPW run.

'07.3: 0.15 um lab. process line was closed.

--> move to 0.2 um mass production line.

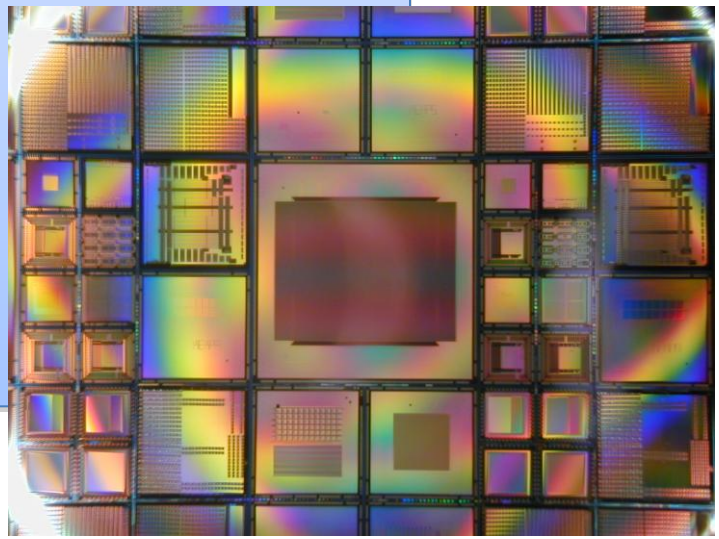
'08.1: 1st KEK SOI-MPW run.

'09.2: 2nd KEK SOI-MPW run.

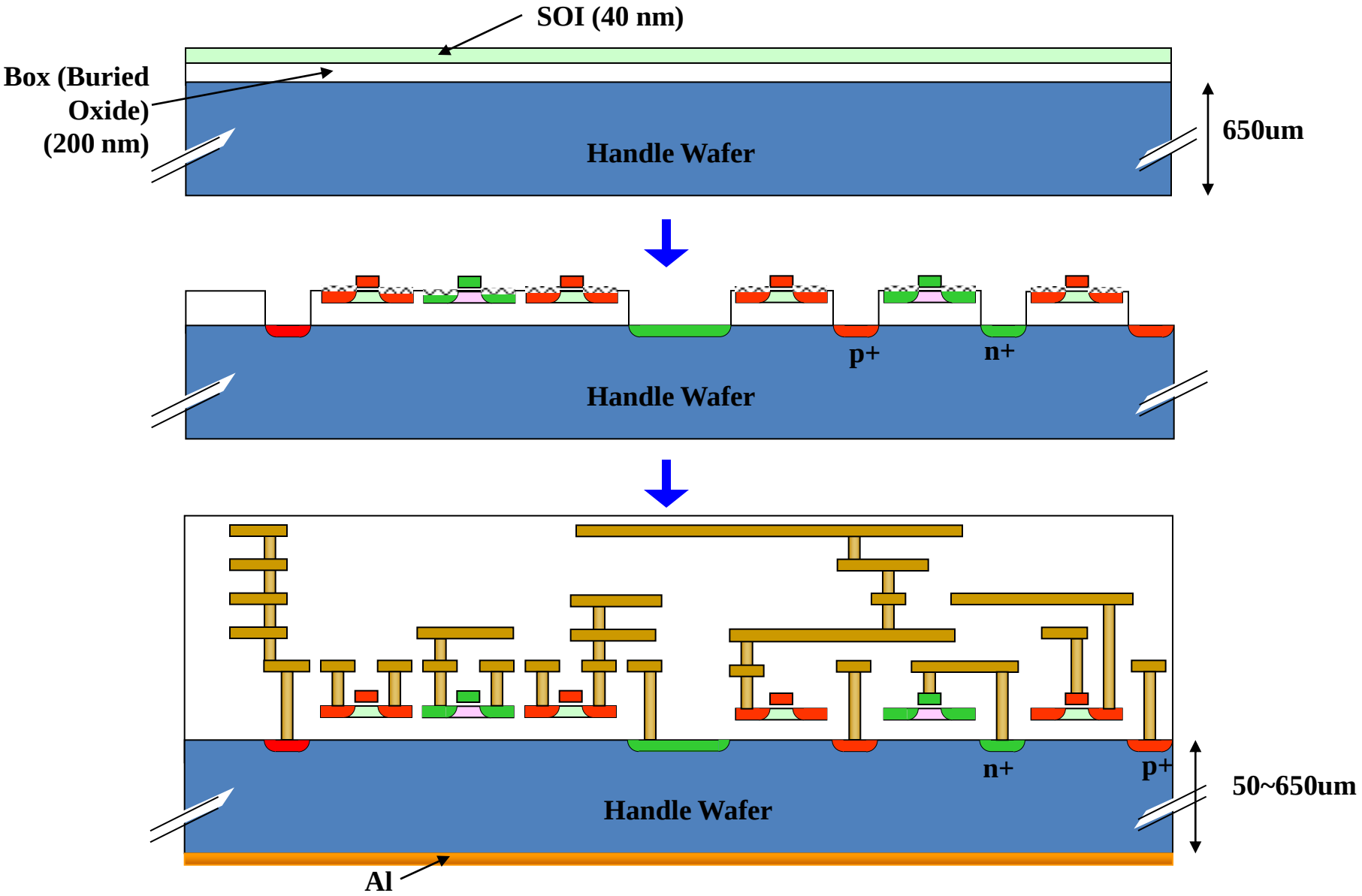
'09.8: 3rd KEK SOI-MPW run.

'10.1: 4th KEK SOI-MPW run.

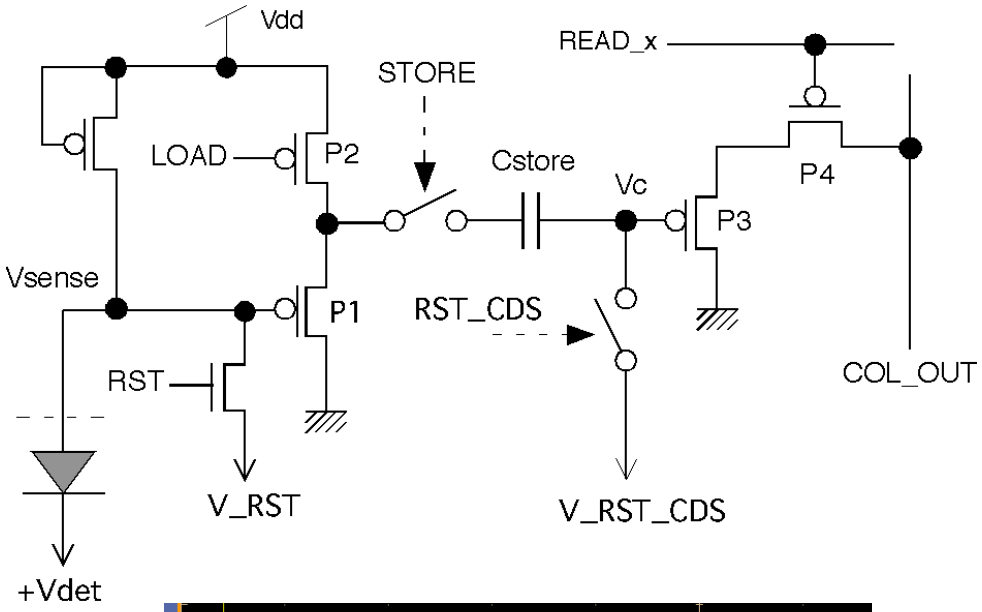
'10.8: 5th KEK SOI-MPW run.

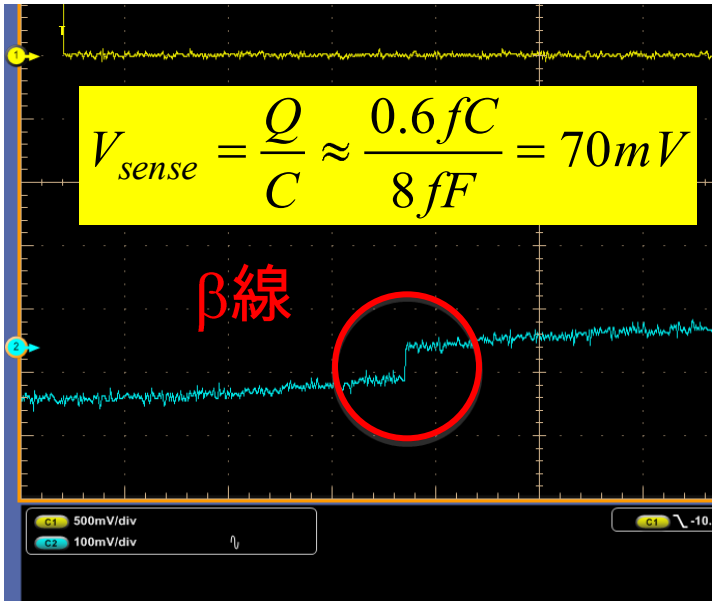


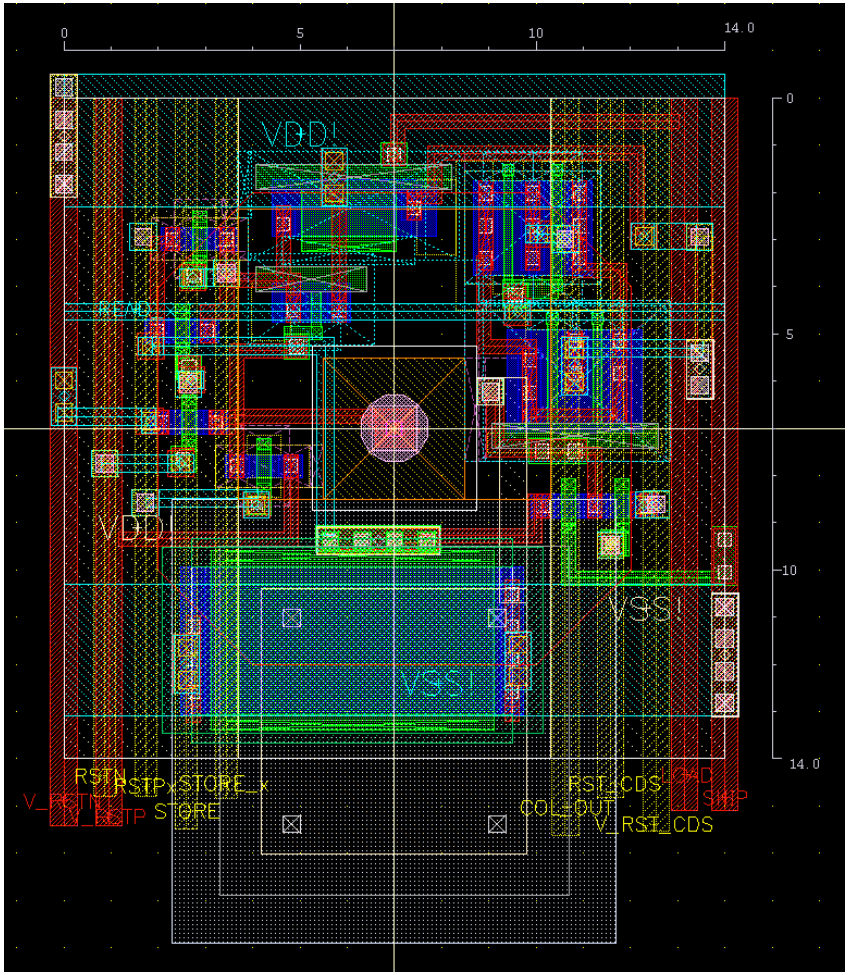
SOI Pixel Process Flow



Integration Type Pixel (INTPIX)

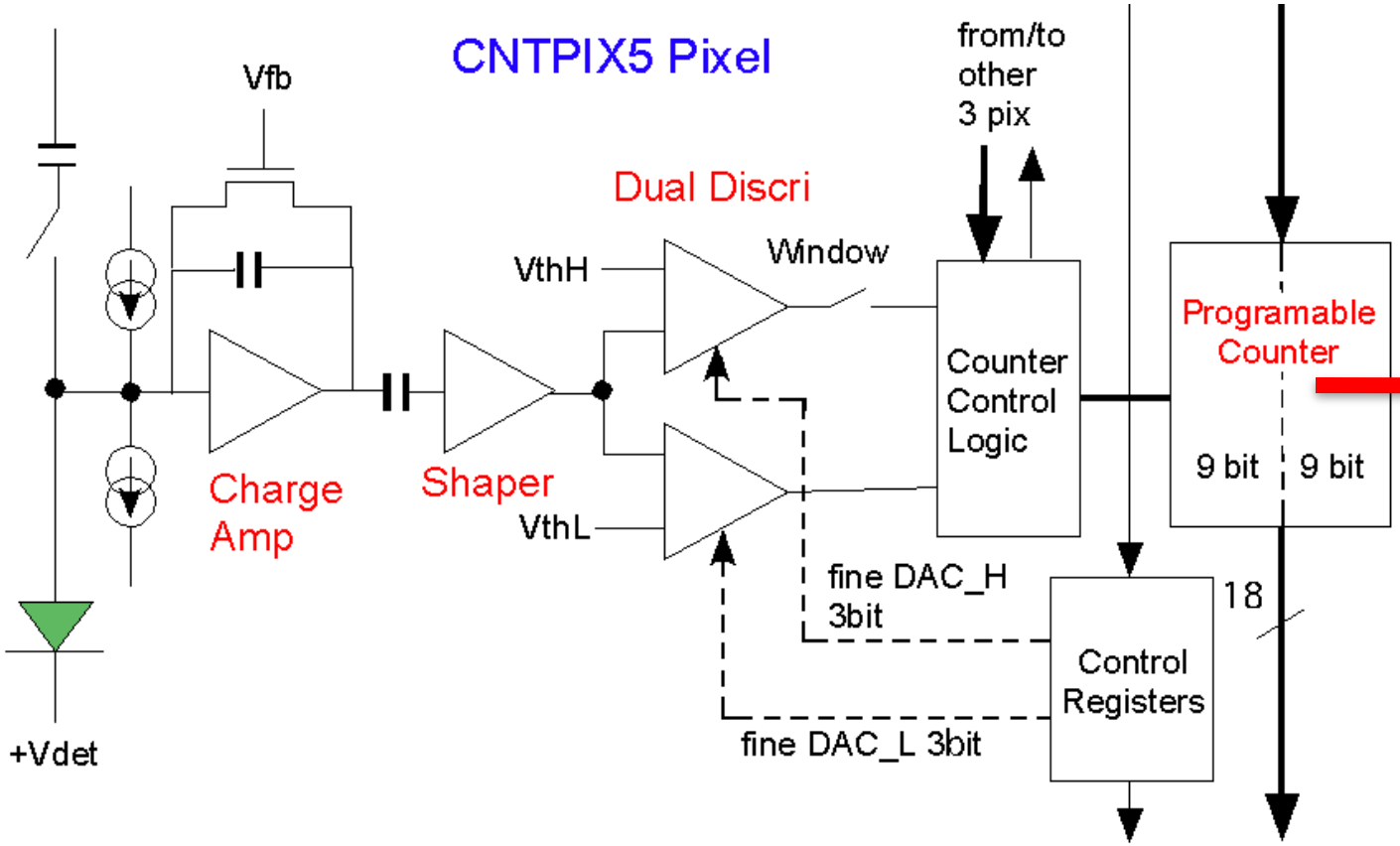


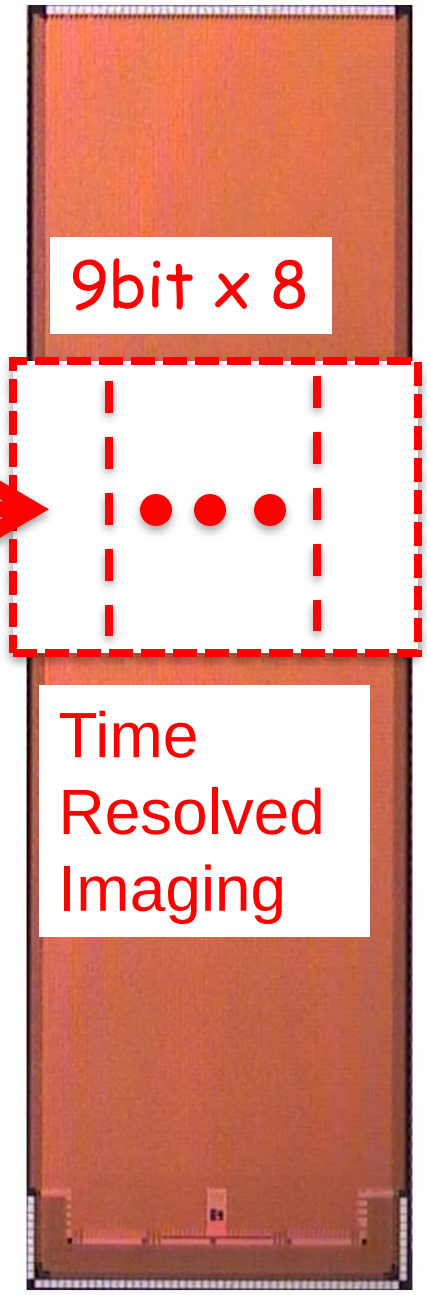




Size : 14 μm x 14 μm
with CDS circuit

Counting Type Pixel (CNTPIX5)



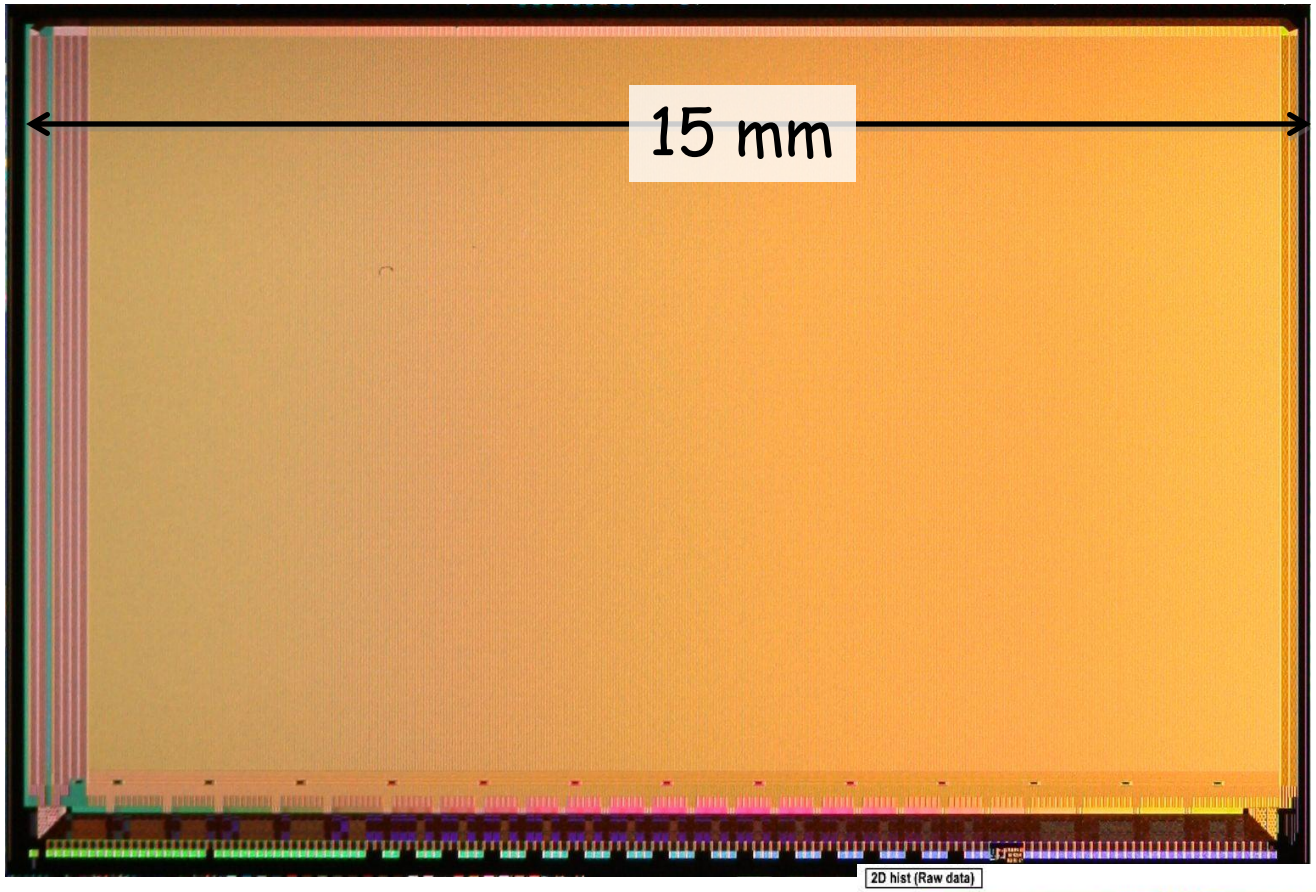


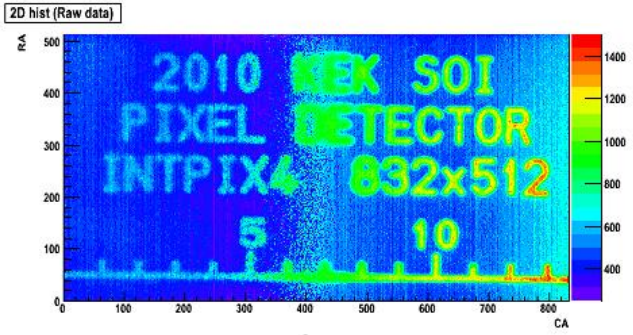
Energy selection and
Counting in each pixel

5 x15.4 mm^2
72 x 272 pixels
64um x 64 um pixel

Integration Type Pixel (INTPIX4)

Largest Chip so far.





17x17 μm, 512x832 (~430k) pixels、13 Analog Out、CDS circuit in each pixel.