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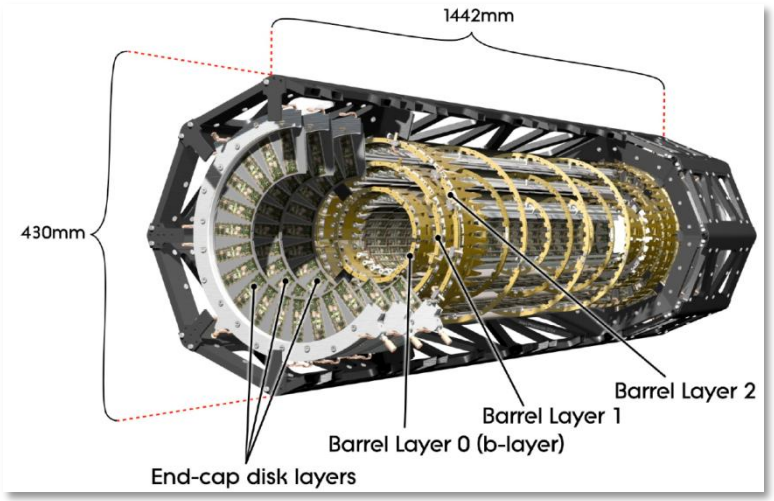
The ATLAS Insertable B-Layer Detector (IBL)

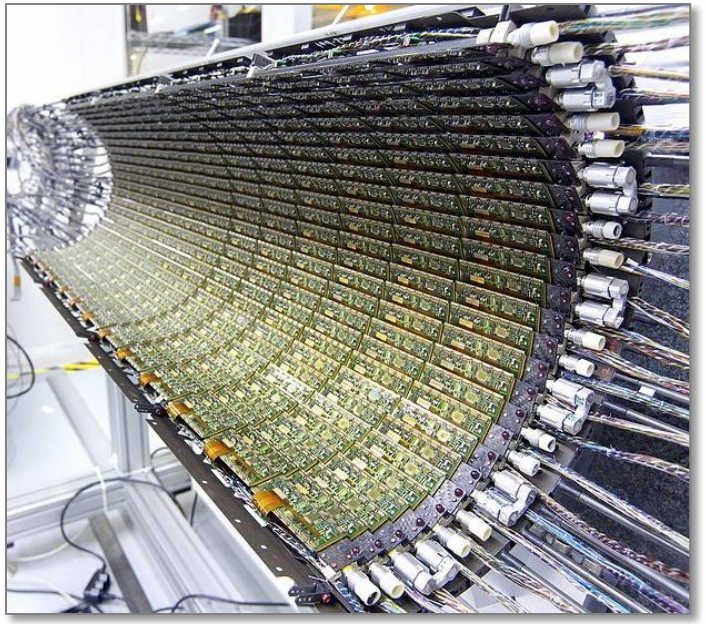
F. Hügging on behalf of the ATLAS IBL collaboration

Pixel 2010
5th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging, Sept. 6 – 10, 2010
Grindelwald, Switzerland

The ATLAS Pixel Detector

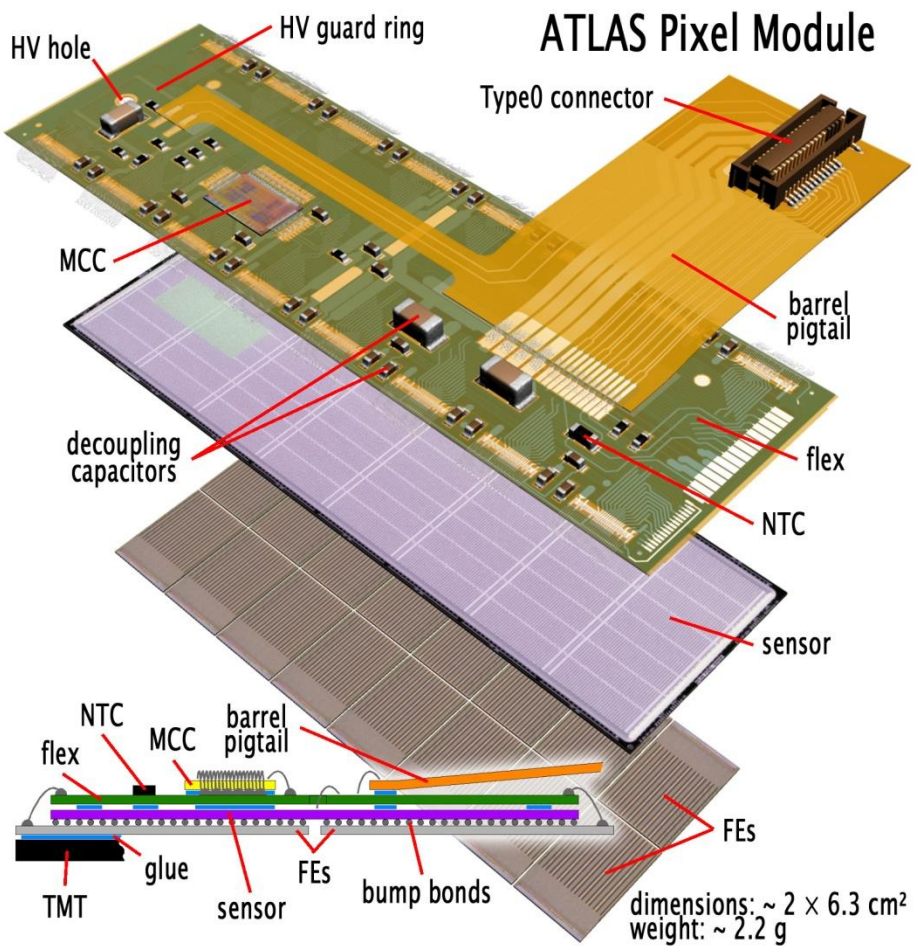
- 3 Barrel + 6 Forward/Backward disks
- 112 staves and 48 sectors
- 1744 modules
- 80 million channels



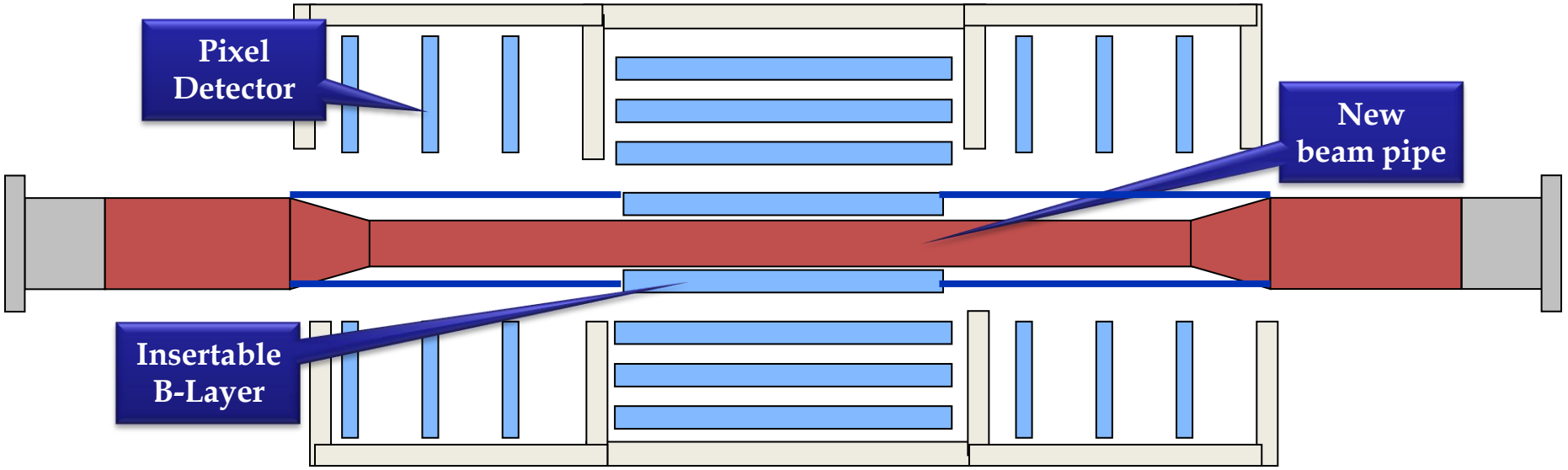


The ATLAS Pixel module

- 16-frontend chips (FE-I3) modules with a module controller chip (MCC)
- 47232 pixels (46080 R/O channels), 50 x 400 μm^2 (50 x 600 μm^2 for edge pixel columns between neighbour FE-I3 chips)
- Planar n-on-n DOFZ silicon sensors, 250 µm thick
- Designed for 1 x 10^{15} 1MeV n_{eq} fluence and 500kGy (50 MRad)
- Opto link R/O: 40÷80 Mb/link



Phase 1 Upgrade: IBL



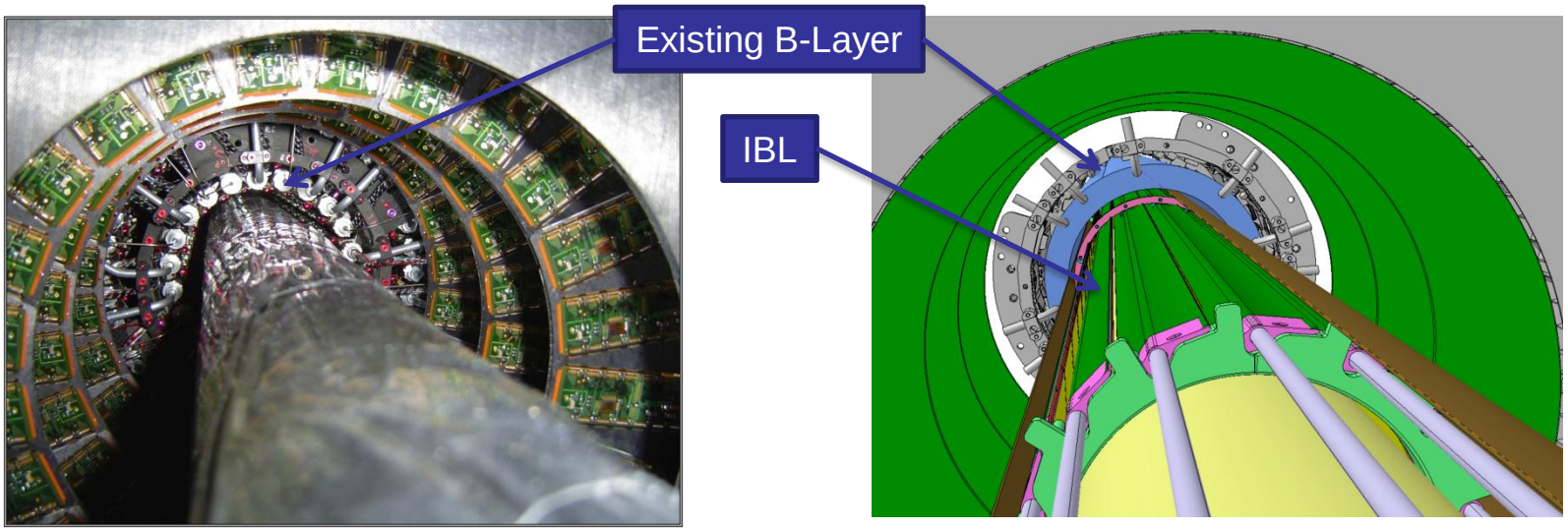
- Insertable B-layer in 2016:
  - Fourth pixel layer at r = 3.2 cm in addition to existing detector.
  - Insertion together will a new beam-pipe.
  - Peak luminosity 2-3x10^{34} cm^{-2} s^{-1}, 75 pile-up events and 3x$10^{15}$$n_{eq}$ /cm^2
- this constraints the design of the IBL:
  - Mechanical layout is challenging, service routing is complex.
  - Electronics/readout has to fit to current pixel detector (ROD, BOC etc.)

The 4th Pixel layer: Insertable B-Layer

- Add a 4th low-mass pixel layer inside the present B-Layer: The Insertable B-Layer:
  - Improve performance of existing system.
  - Maintain performance when present B-Layer degrades.
  - Existing Pixel Detector stays installed and a 4th is inserted inside the existing pixel system together with new beam pipe → requires new, smaller radius beam pipe to make space.
  - It needs to be inserted in a long shutdown (at least 9 months required). Build detector ready for installation in 2016.
- It serves also as technology step from now to sLHC:
  - IBL project will be first to use of new technologies currently under development for sLHC.
  - Radiation hardness 5×10^{15} n_{eq}/cm^2 or 250 MRad (2.5 MGy).
  - Front-end (FE-I4): go to IBM 130nm process and improve readout architecture.
  - Sensors: investigate new planar Si sensors, 3D-Si sensors and CVD diamond sensors.
  - Readout system & optolink: 160MB/s for data transmission.
  - CO_2 cooling system & mechanics: develop light-weight support.

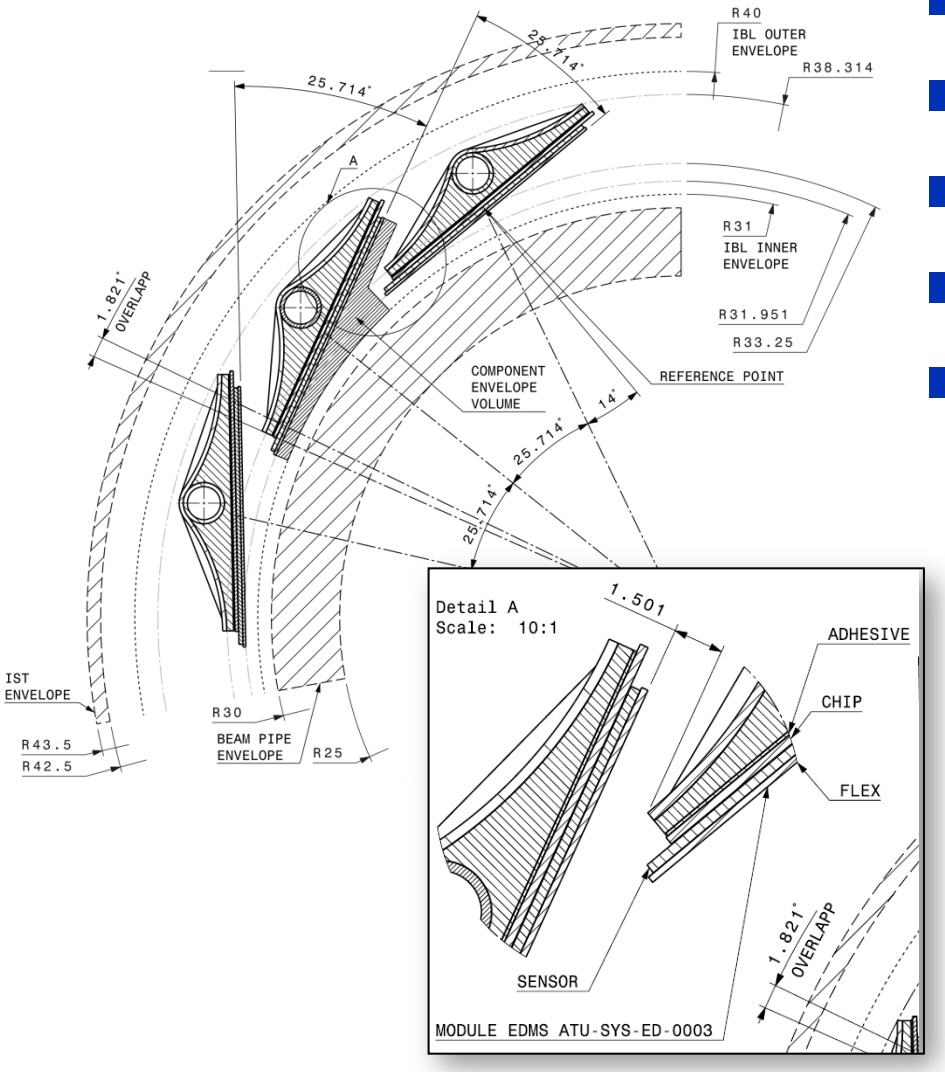
IBL Layout (1)

- The envelopes of the existing Pixel Detector and of the beam pipe leave today a radial free space of 8.5mm.
- The reduction of 4mm in the beam pipe radius brings it to 12.5mm.
- Entire IBL has to fit in this space!



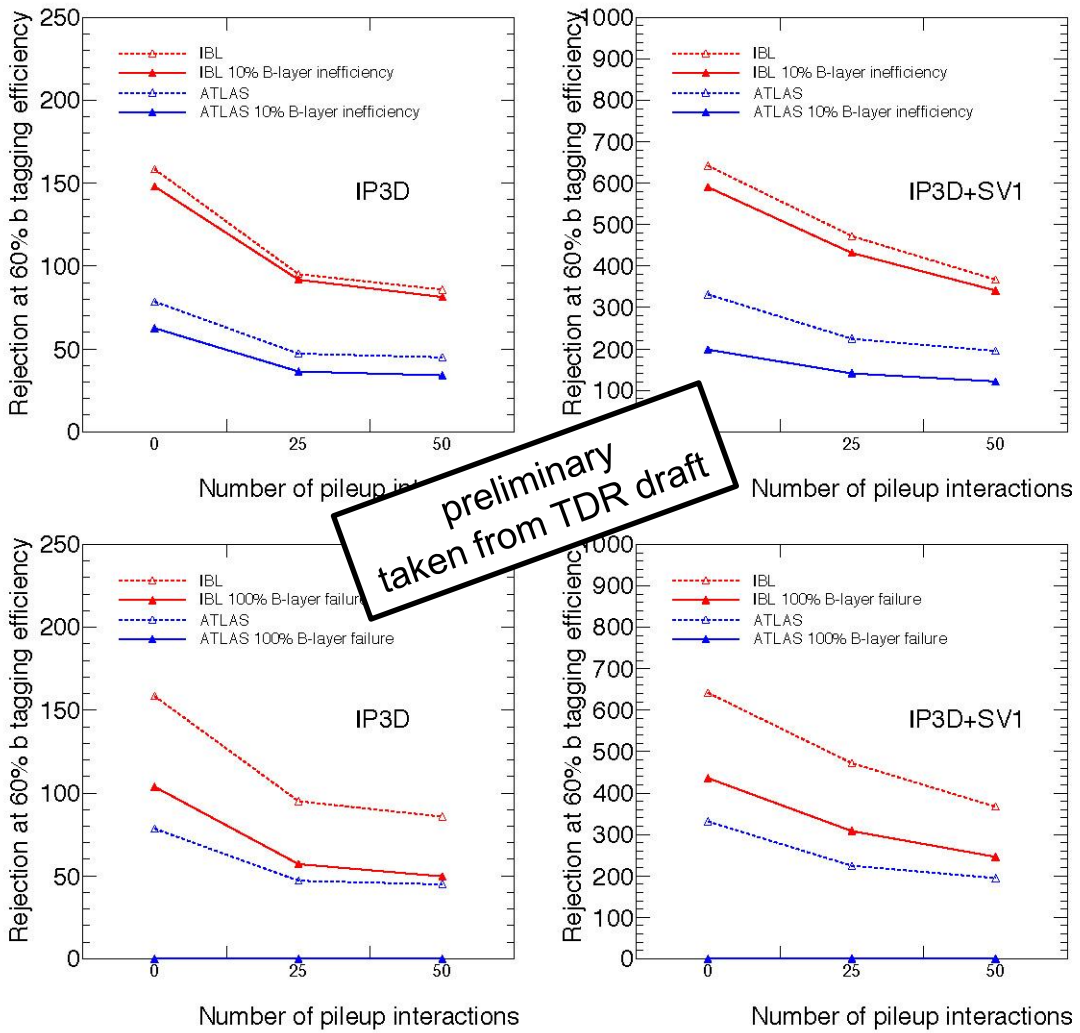
IBL Layout (2)

- Baseline geometry defined:
- 14 staves
  - R_{in} = 31mm
  - R_{out} = 34mm
  - $<R_{sens}>$ = 33mm
  - Z = 664mm
- 32 FE-I4‘s per stave with sensors facing the IP.
- Stave tilt angle in Φ = 14
- No module overlap in z-direction.
- Total sensor surface only ~0.2m^2.



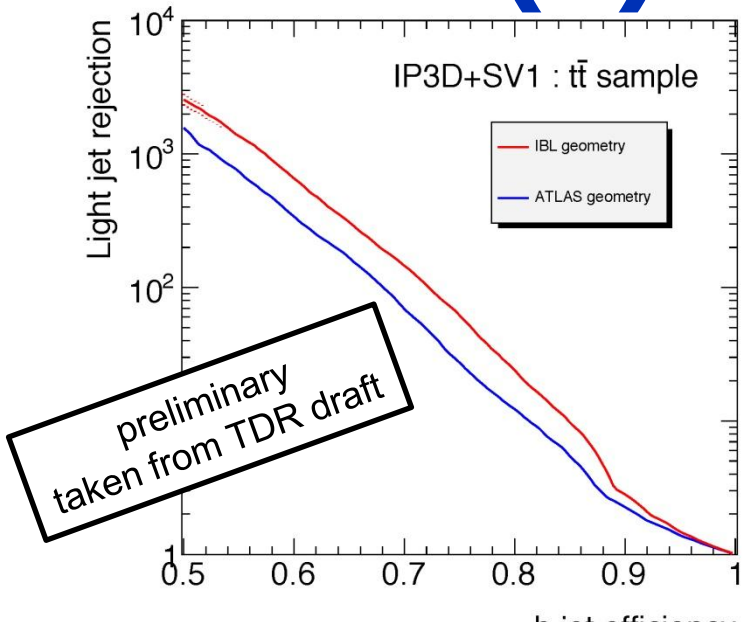
IBL Performance (1)

- Main target is to keep performance of the pixel system:
  - for more pile up events at higher luminosities.
  - for failures of modules esp. in the ‘old’ b-layer.
  - b-tagging efficiency without ‘old’ b-layer.
- Older studies (ATLSIM/GEANT3) suggest improved performance with the addition of IBL.
- IBL physics and performance taskforce installed to investigate the physics performance of IBL further:
  → see results on light jet rejection at 60% b jet efficiency on the right for two simulated failure scenarios.

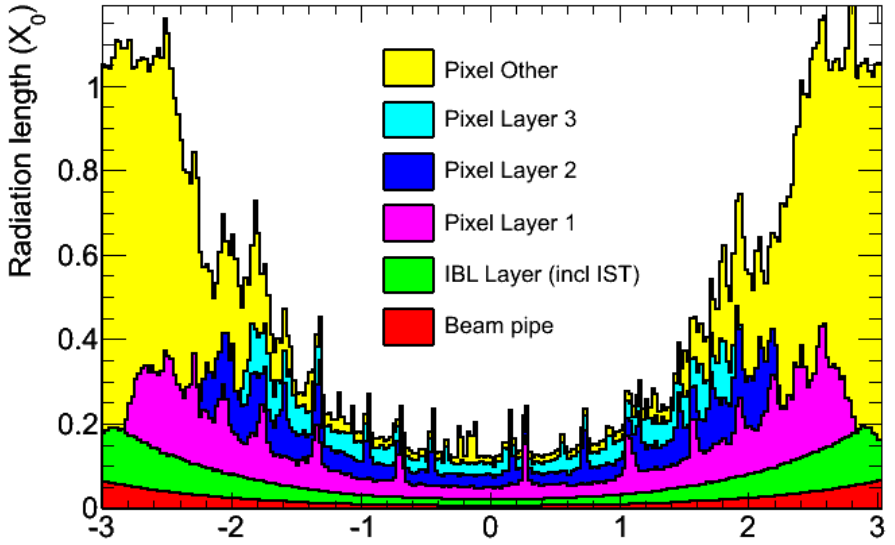


IBL Performance (2)

- Physics performance studies are ongoing for the IBL TDR using ATHENA/GEANT4.
- Performance improvement due to low mass and smaller radius of IBL:

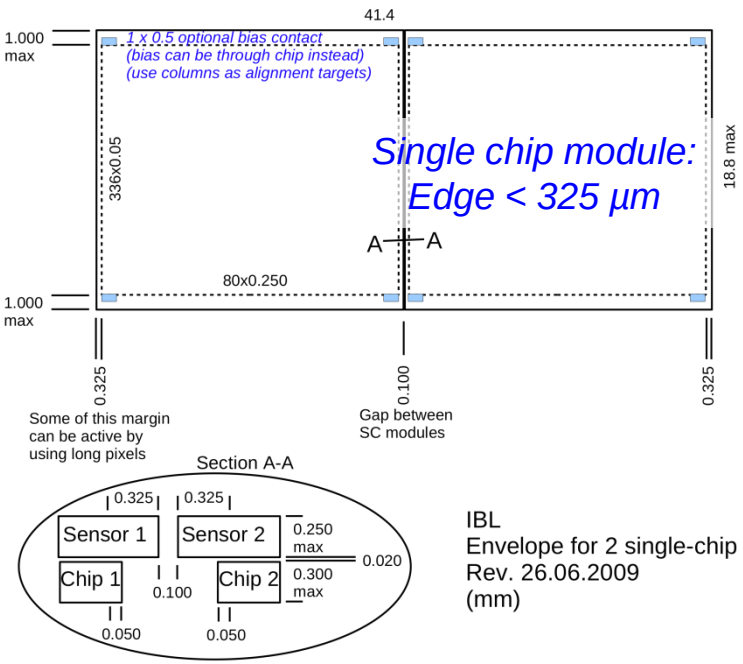


Component	% X_0
beam-pipe	0.6
New BL @ R=3.2 cm	1.5
Old BL @ R=5 cm	2.7
L1 @ R=8 cm	2.7
L2 + Serv. @ R=12 cm	3.5
Total	11.0

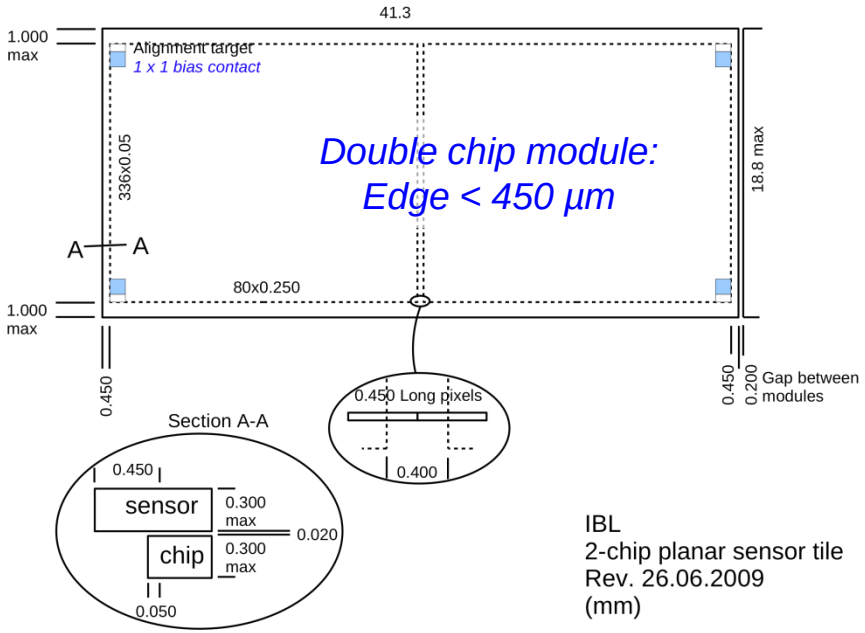


IBL Module Design

- Module design decoupled from sensor technology → only a few technology dependencies.
- Each FE chip has 336x80 pixel of 50x250µm^2.
- Decision on sensors after prototyping with FE-I4.
  - Need module prototypes with FE-I4 (2010/2011)
- Common sensor baseline for engineering and system purposes.
  - 3D sensors → single chip modules
  - Planar and Diamond sensors → 2 chip modules
- Sensor/module prototypes for ~10% of the detector in 2010/2011
  - Stave prototype tested with modules and cooling



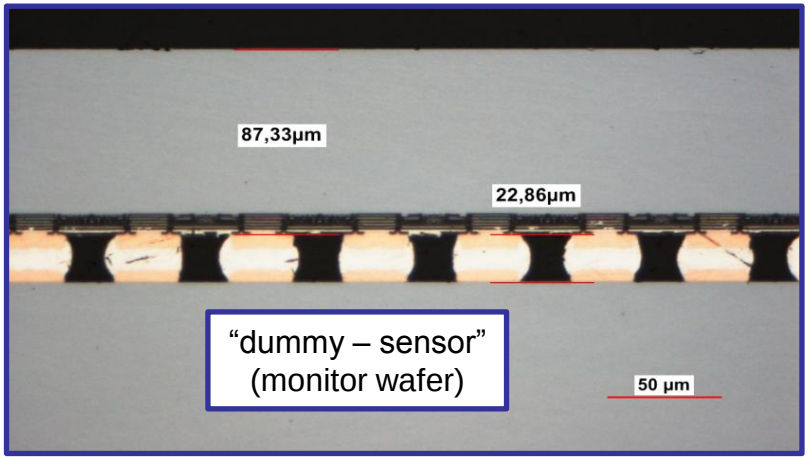
IBL
Envelope for 2 single-chip 3-D modules
Rev. 26.06.2009
(mm)



IBL
2-chip planar sensor tile
Rev. 26.06.2009
(mm)

Bump Bonding

- Requirements for bump bonding of IBL modules are:
  - a fine bump pitch of 50µm
  - a high bump density of 80 bumps per mm^2 (26,880 bumps per IC)
  - high yield with defect rate < 10^{-4}.
  - IC thickness below 200µm to save material.
- Large volume bump bonding experience from ATLAS Pixel Detector.
- Program to qualify for FE-I4 and different sensor technologies.
  - Goal is go below 200µm chip thickness: target is 90µm.
  - Crucial point is the behavior of the thinned IC during the high temperature reflow process.
  - See L. Gonella's and T. Fritzsch talks on Thursday for more details.



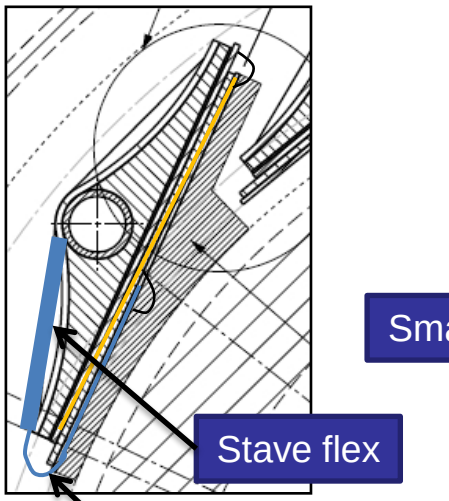
Prototype test of advanced AgSn bumping with 90µm FE-I4 size dummies.

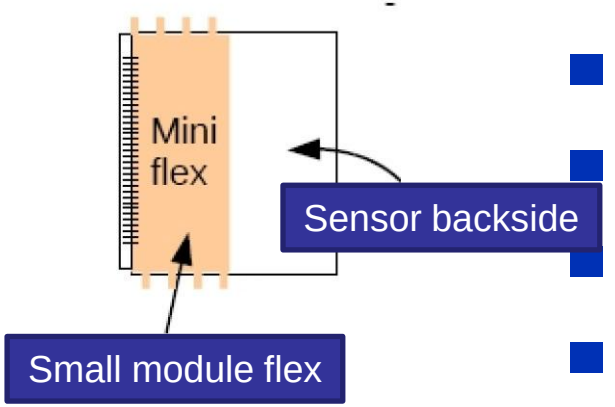
JINST 3 P0707 (2008)

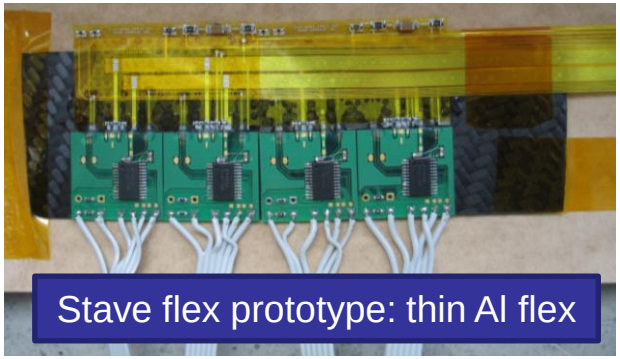
	Indium		PbSn		Total	
	Modules	Fraction	Modules	Fraction	Modules	Fraction
Assembled	1468		1157		2625	
Rejected	172	11.7%	35	3.0%	207	7.9%
Accepted (total)	1296	88.3%	1122	97.0%	2418	92.1%
Accepted as delivered	1101	75.0%	1035	89.5%	2136	81.4%
Accepted after reworking	195	13.3%	87	7.5%	282	10.7%

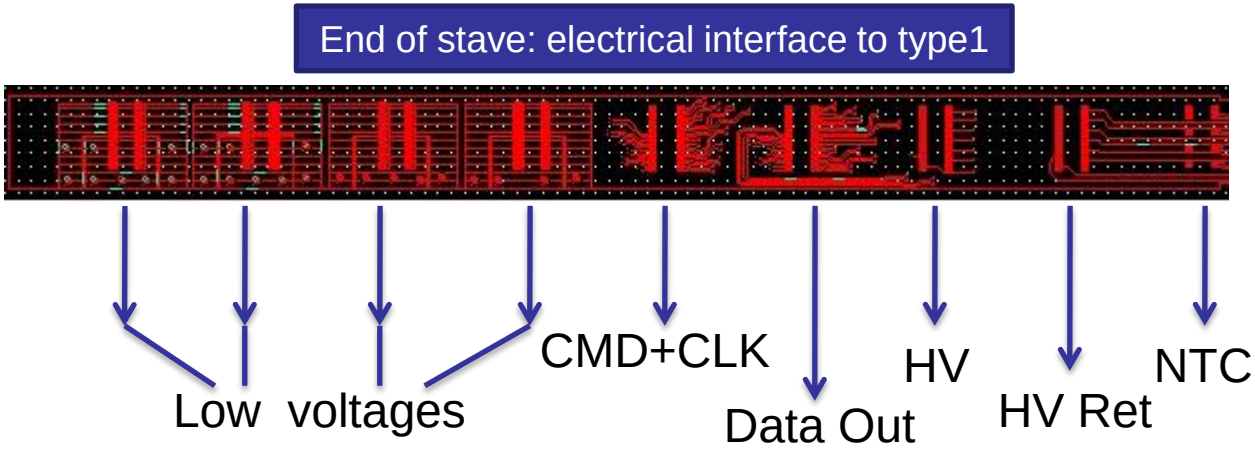
Module design: Electrical interface

- Basic idea: flex cable glued to stave backside carries all signal and voltage traces for a half stave, i.e. 8 2-chip modules.
- Connection to module via a wing which is bent to stave front side for each module.
- Wire bond connects to module onto a small module flex.
- At the end of stave all signals and voltages connects to type1 cables via low mass connectors
- 2 prototypes are under development for the stave cables:
  - Multilayer flex solution
  - thin single sided Al-flexes



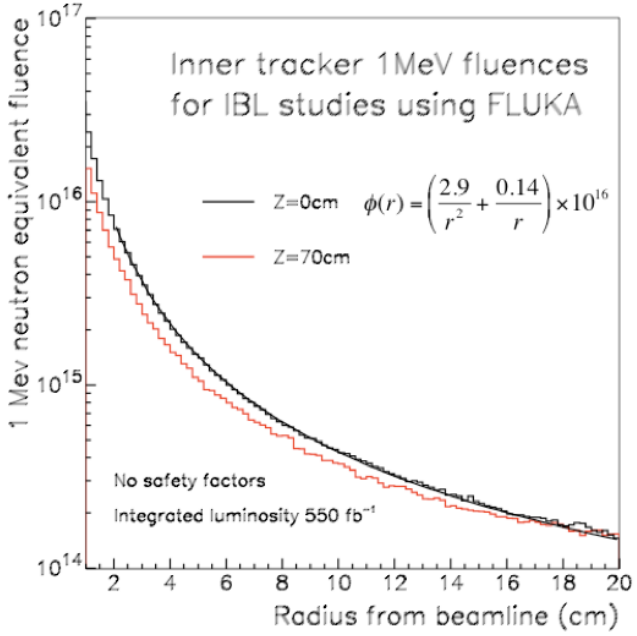


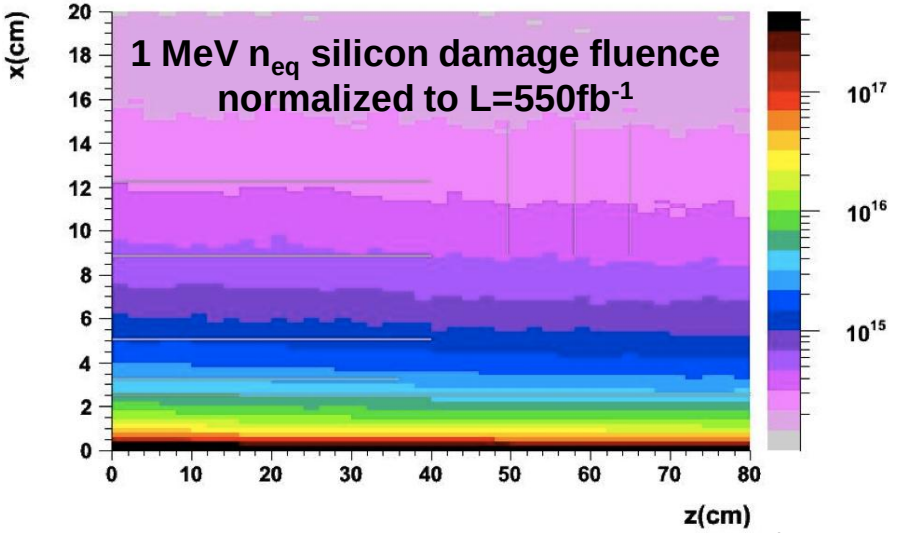

Stave flex prototype: thin Al flex



Sensors for IBL (1)

- Requirements for IBL sensors:
  - Integrated luminosity seen by IBL is 550fb^{-1} → survive until sLHC phase 2
  - NIEL dose: 3.3x10^{15} + „safety factor“ = 5x10^{15} n_{eq}/cm^2.
  - Ionizing dose = 2.5MGy (250MRad)
  - Low dead area in Z: slim or active edge
  - Max. Sensor power density < 200mW/cm^2 normalized to -15°C sensor temperature
  - Max. Bias voltage (system issue) = 1000V



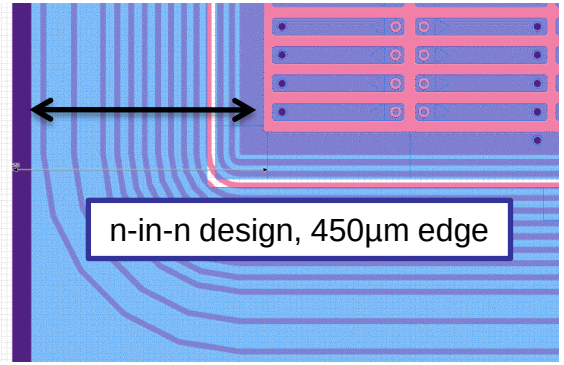


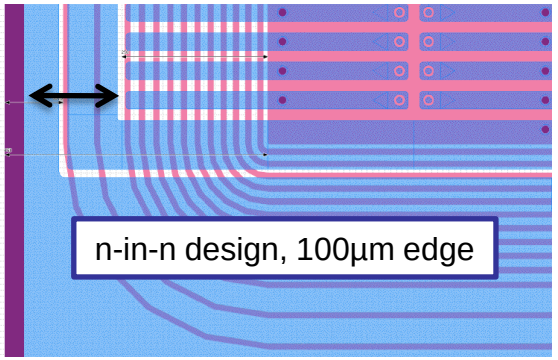
- Fit made for 2 < r < 20cm for L = 550fb^{-1}.
- For IBL @ 3.2cm: Φ = 3.3x10^{15}n_{eq}/cm^2 (1.6MGy)

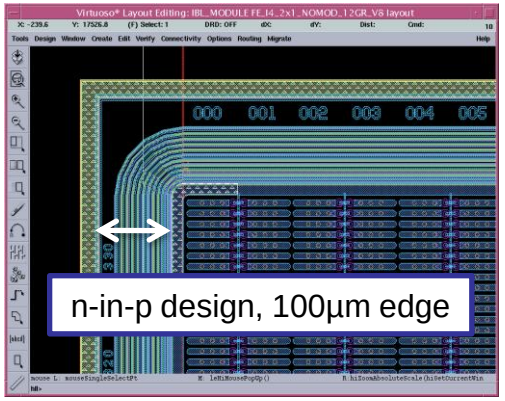
Sensors for IBL (2)

- 3 sensor concepts are beeing considered for IBL:
  - Planar n-in-n silicon sensors:
    - Similiar design as for ATLAS Pixel.
    - Radiation tolerance proven to several $10^{15} n_{eq}/cm^2$.
    - Main focus in development of slim edges.
  - Planar n-in-p silicon sensors, thinned to 150µm:
    - Utilize the advantages of thinned sensors at a given maximum bias voltage
    - Standard 450µm wide inactive edge
    - Special passivation layer (BCB) needed for HV operation

→ More details given on Wednesday morning by D. Münstermann, A. Macchiolo and Y. Unno.

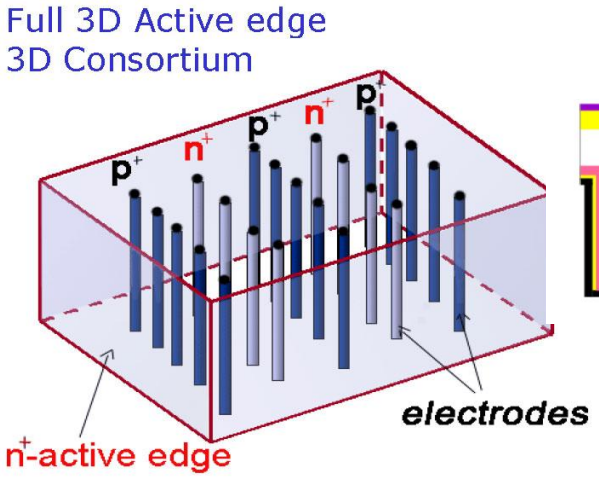


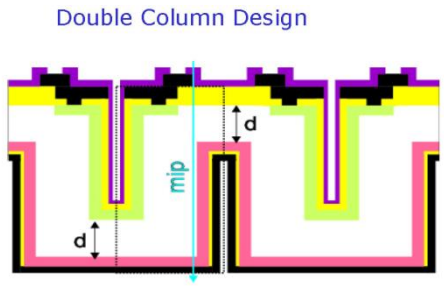




Sensors for IBL (3)

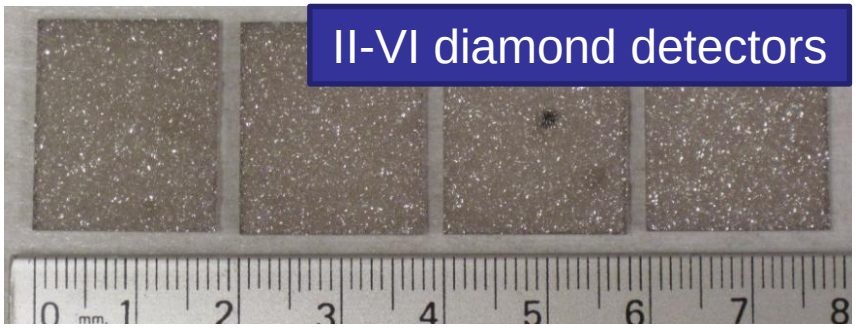
- 3D silicon n-in-p sensors:
  - Radiation tolerance is achieved by short charge collection distances decoupled from sensor thickness (230µm).
  - 2 design option with different edge sizes:
    - Full 3D active edge design → 50µm edge.
    - Double column design → 200µm slim edge
  - More details given on Wednesday by A. Micelli.
- Diamond pixel sensors:
  - Sufficient radiation tolerant for IBL fluences and very low leakage current (less cooling).
  - Slim edges possible.
  - 2 manufacturer (DDL, II-VI) with acceptable performance (CCD > 230µm) under investigation.
  - Full processing (pixel metallization and UBM) are industrialized at IZM, Berlin.





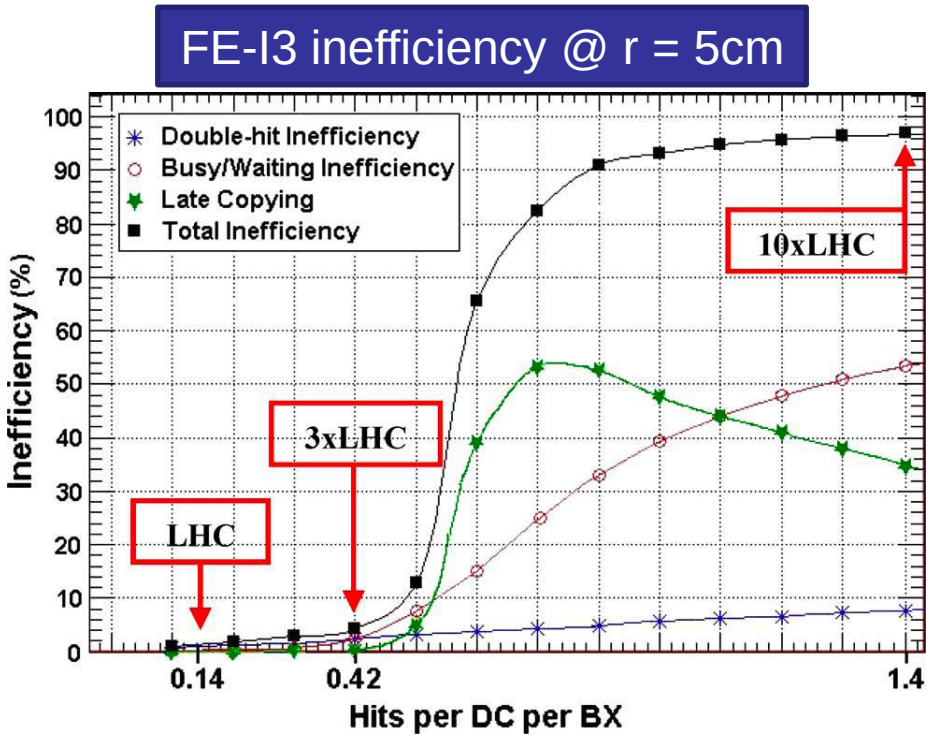
DDL diamond detectors

II-VI diamond detectors



IBL FE-electronics

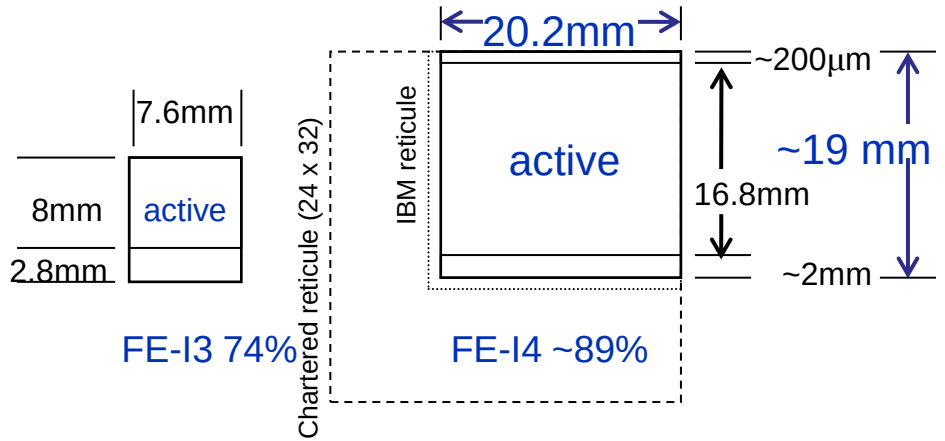
- Reason for new FE chip:
  - Increased radiation tolerance required: 2.5MGy
    - → Go to smaller feature size technology 130nm and utilize its improved radiation hardness.
  - New architecture to reduce inefficiences at higher luminosities.
    - → Local storage of hit in pixel matrix until trigger arrives.
    - → Higher output bandwidth.
  - Improve cost effectiveness:
    - → Larger chip improves the ratio between active area and periphery and is advantageous for bump bonding while the yield can still be high.



FE-I3 → FE-I4

- The first version of full FE-I4 chip has been submitted in July 2010 and is expected back on 14th of Sept.
  - Biggest chip in HEP to date (70 millions transistors, 6 Cu and 2 Al routing layers)
  - Lower power: don‘t move hits around unless triggered
  - No need for extra module control chip: significant digital logic block on array periphery.
- FE-I4 collaboration:
  - Bonn: D. Arutinov, M. Barbero, T. Hemperek, A. Kruth, M. Karagounis.
  - CPPM: D. Fougeron, M. Menouni.
  - Genova: R. Beccherle, G. Darbo.
  - LBNL: S. Dube, D. Elledge, M. Garcia-Sciveres, D. Gnani, A. Mekkaoui.
  - Nikhef: V. Gromov, R. Kluit, J.D. Schipper.
- More details on FE-I4 on Tuesday by M. Barbero‘s talk „*FE-I4 Chip Development for Upgraded ATLAS Pixel Detector at LHC”*.

	FE-I3	FE-I4
Pixel size [µm²]	50x400	50x250
Pixel array	18x160	80x336
Chip size [mm²]	7.6x10.8	20.2x19.0
Active fraction	74%	89%
Analog current [µA/pix]	26	10
Digital current [µA/pix]	17	10
Analog Voltage [V]	1.6	1.4
Digital Voltage [V]	2.0	1.2
Pseudo-LVDS out [Mb/s]	40	160



IBL cooling

Thermal runaway happens in sensors if not adequately cooled:

→ Leakage current shows exponential behavior.

Stave thermal figure of merit ($\Gamma = [\Delta T \cdot cm^2/W]$) main parameter for thermal performance.

Power design requirements for IBL:

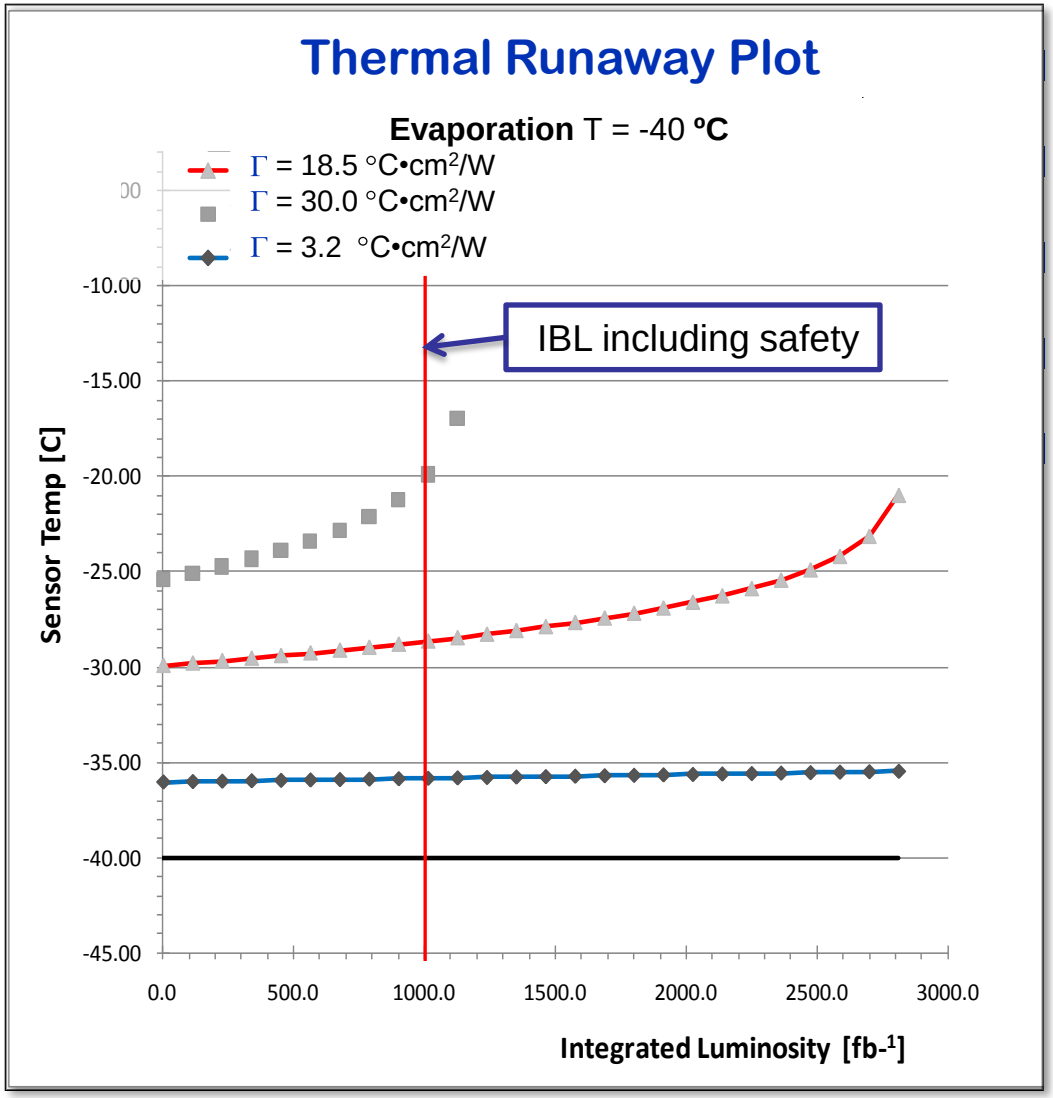
- Sensor Power: 200 mW/cm^2 @ -15 °C
- FE power: 400 mW/cm^2

Stave prototype qualification program:

- Titanium / carbon fiber pipes (D = 2÷3 mm)
- Cooling CO_2 and C_3F_8
- Carbon foam density: 0.25÷0.5 g/cm^3

Radiation length: 0.36÷0.66 %X/X_0

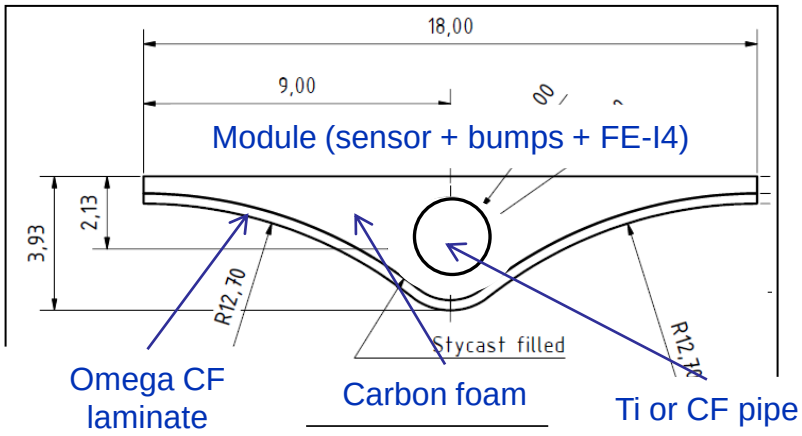
- Pipe + stave structure + coolant



IBL stave structure

Stave structure made of carbon foam + cooling pipe:

- The stiffness is provided by a carbon fiber laminate:
- Carbon foam diffuses the heat from the module to the cooling pipe



Additional technical requirements:

- Max pressure of cooling pipe: 100 bar.
- Develop pipe joints and fittings.
- Gravitational / thermal deformation < 150 µm.
- Isolation of the carbon foam from sensor high voltage.
- Mock-up for thermal measurements.

STAVE TYPE	Omega Thickness [µm]	Foam Density [g/cm³]	Pipe Material	Pipe Diameters [mm]	Radiation Length X/X_0 [%]		Thermal Figure of Merit Γ [°C.cm²/W]	Thermal Def. [µm]
					Bare Stave	Full Stave Assembly		
Ti pipe Stave	300	0.25	Ti grade II	ID=2 OD=2.2	0.57	1.166	11	41
CF Pipe Stave	150	0.25	CF	ID=2.4 OD=3	0.36	0.956	25	50

Conclusions

- IBL is the upgrade for the ATLAS Pixel Detector in LHC phase 1 upgrade:
  - A 4th layer will be inserted into the Pixel system.
  - IBL will improve physics performance of ATLAS and it is a “safety insurance” for present B-Layer.
  - TDR and MoU in progress – project cost evaluated.
- IBL is a challenging project:
  - Tight envelopes, material budget reduction, radiation dose and R/O bandwidth requirements.
  - New technologies are in advanced prototype phase:
    - Sensors, FE-I4, light supports, cooling, etc.
  - Can be beneficial for sLHC tracker upgrades.

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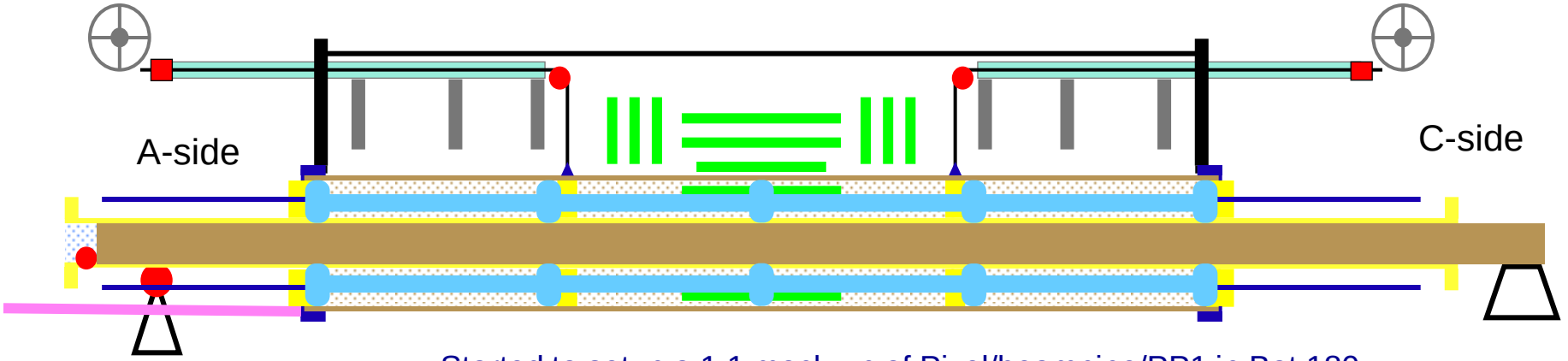
Backup

Installation scenario

- Two global support / installation scenarios: IBL support tube (1) / no tube (2):
  - An IBL support tube would have advantage on stiffness and simplicity/safety for IBL installation, but drawback are envelope needs (~1÷1.5 mm) and increase of radiation length
- Procedure studied on mock-up at bld.180 - procedure (1) animation:
  - The beam pipe flange on A-side is to close to the B-layer envelope - Need to be cut on the aluminum section
  - A structural pipe is inserted inside the Beam Pipe and supported at both sides.
  - The support collar at PP0 A-side is disassembled and extracted with wires at PP1.
  - Beam pipe is extracted from the C-side and it pulls the wire at PP1
  - New cable supports are inserted inside PST at PP0.
  - A support carbon tube is pushed inside the PST along the structural pipe.



Started to setup a 1:1 mock-up of Pixel/beampipe/PP1 in Bat 180