14.4. Readout systems for innovative calorimeters

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WP 14.4

February 13, 2020

- **Milestone 58: Definition of optical and electrical coupling of readout, interface functionality and DIF design**
- **Deliverable 14.5: Common running of calorimeter prototypes**
- **Deliverable 14.6: Adaptation of readout system for operation in compact LC detectors**

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DESY

Deliverable 14.6: Adaptation of readout system for operation in compact LC detectors

Connected to Milestone 58

SiECAL: new development of full system

- talk by Jihane Maalmi

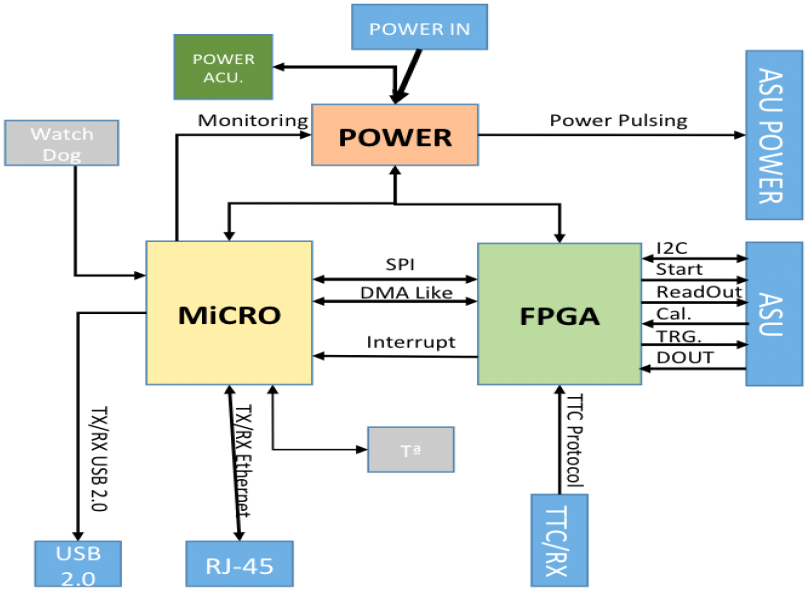
AHCAL: full system

- Current generation of interfaces designed to fulfill specs
- System produced and used in testbeam

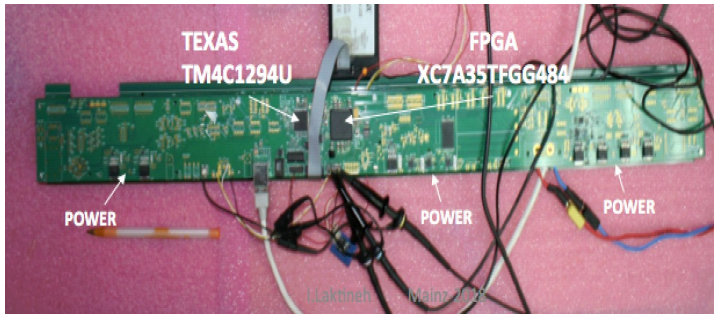
SDHCAL:

- new version to operate a whole detector plane with 1 DIF only developed by CIEMAT

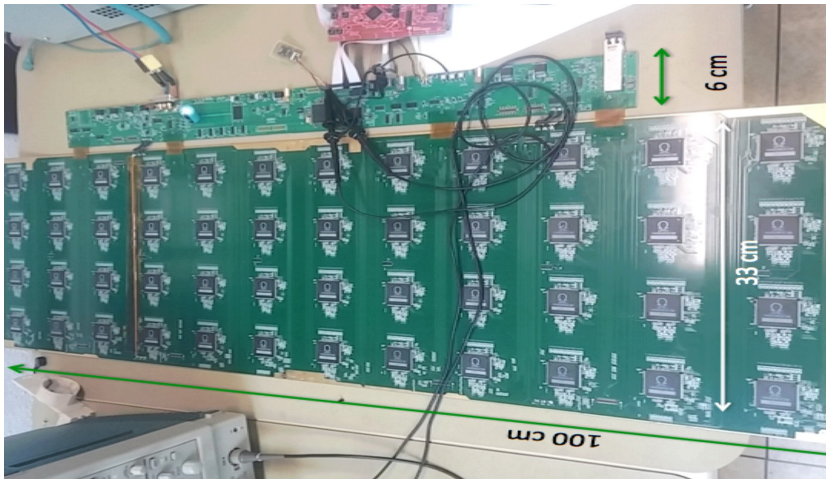
DIF sends DAQ commands (config, clock, trigger) to front-end and transfer their signal data to DAQ. It controls also the ASIC power pulsing



Only **one DIF per plane** (instead of **three**)
DIF handle up to **432 HR3 chips** (vs **48 HR2** in previous DIF)
HR3 **slow control** through **I2C bus (12 IC2 buses).**
Keeps also **2 of the old slow control buses as backup & redundancy**.
Data transmission to/from DAQ by **Ethernet**
Clock and synchronization by **TTC** (already used in LHC)
93W Peak power supply with super-capacitors
(vs **8.6 W** in previous DIF)
Spare I/O connectors to the FPGA (i.e. for GBT links)
Upgrade **USB 1.1** to **USB 2.0**



The firmware is being developed. DIF to be tested with large ASU equipped with HR3.



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Deliverable 14.5: Common running of calorimeter prototypes

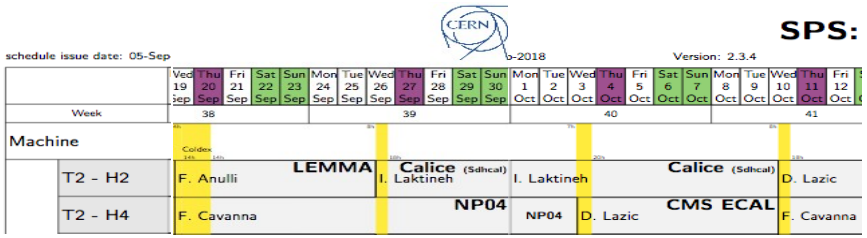
Deliverable: Data acquisition system to allow for a common data taking of different highly granular calorimeter prototypes in beam tests at CERN and DESY. These tests should provide data files containing events synchronised between the subsystems.

Continued developments:

- **in September 2018: CALICE SiECAL + SDHCAL testbeam at CERN SPS**
- **in October 2018: CMS HGCAL + CALICE AHCAL testbeam at CERN SPS**
- **in March 2019: CALICE AHCAL + Beam instrumentation**
- **in May 2019: CALICE AHCAL + Beam instrumentation**
- **in August 2019: CALICE AHCAL + Beam instrumentation**
- **in March+November 2020: CALICE SiECAL + AHCAL at DESY**

Combined CALICE SiECAL+SDHCAL testbeam 2018

2 weeks on H2 beam line at CERN SPS 25/09–10/10/2018

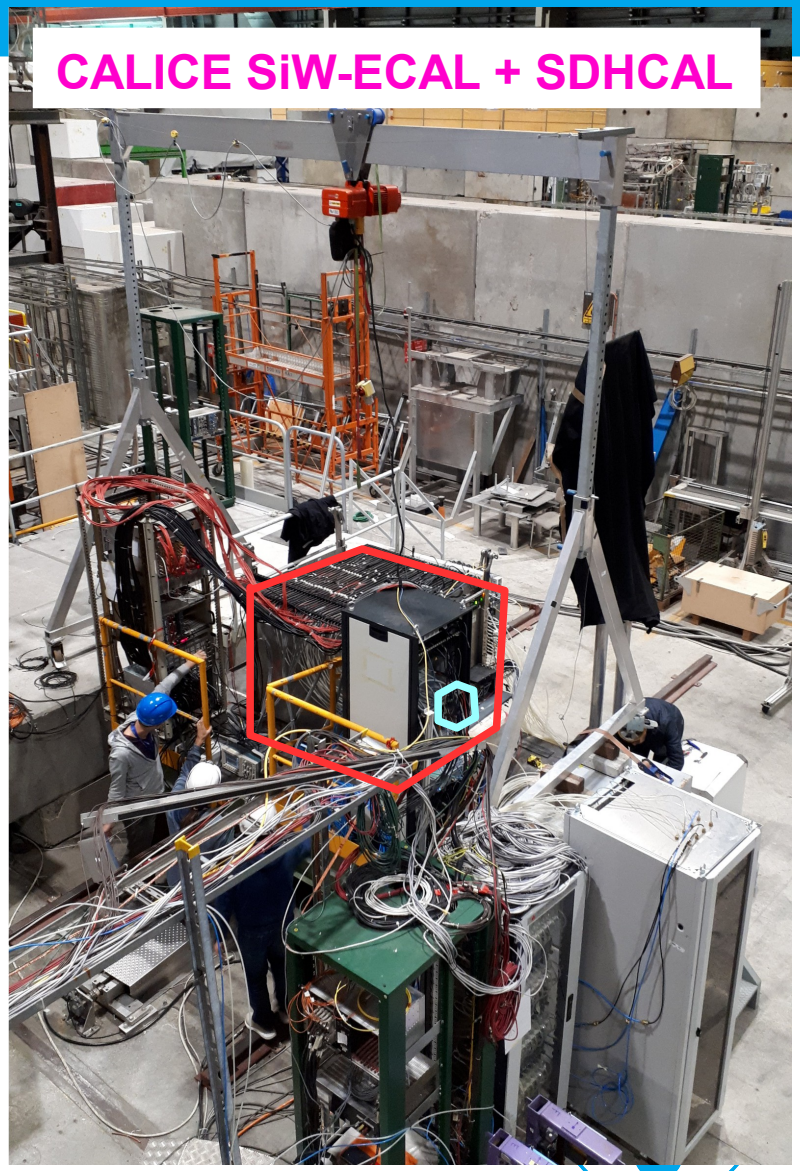


37 layers of SDHCAL RPC, 5MHz clock

10 layer of SiW-ECAL: 2.5 MHz and 5 MHz, FEV12 and FEV13.

Required some work on DAQ:

- HW and SW synchronisation
  - Solution of CERN-2016 + 40 MHz clock on both
  - first combined test since 2016



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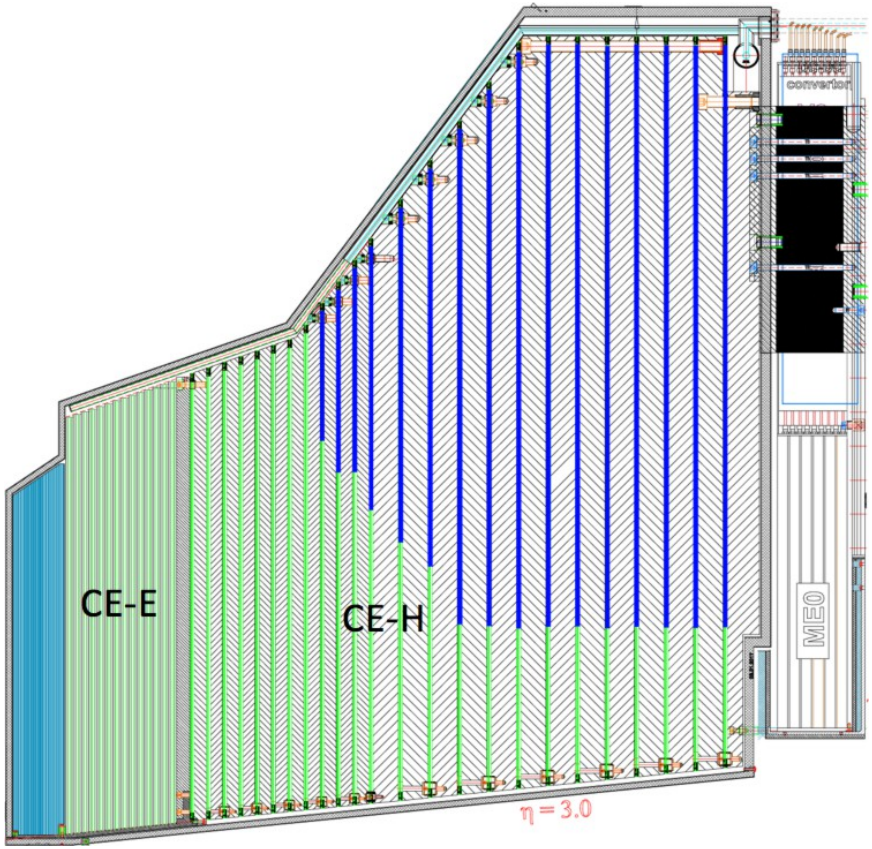
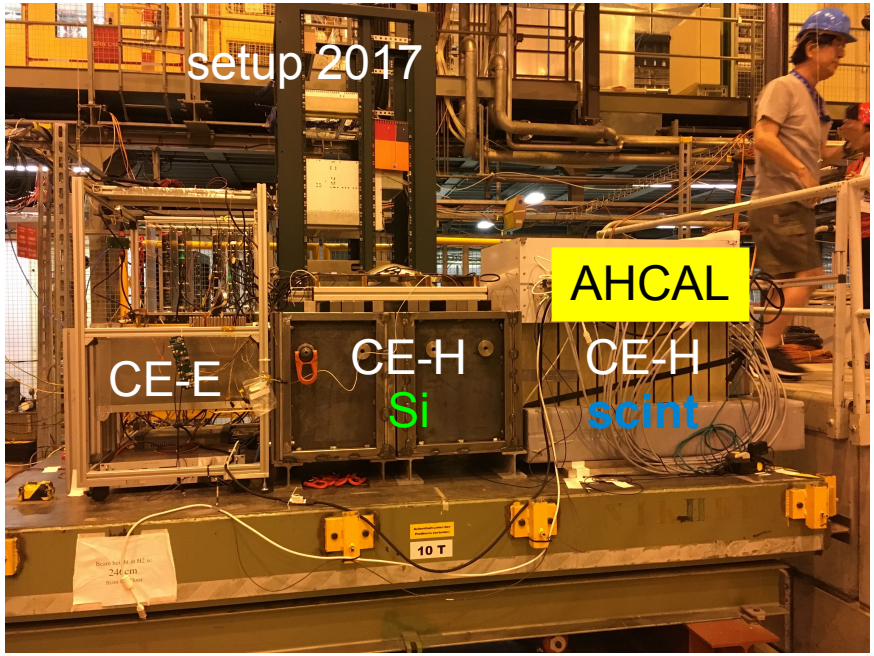
CMS HGCAL + CALICE AHCAL testbeam

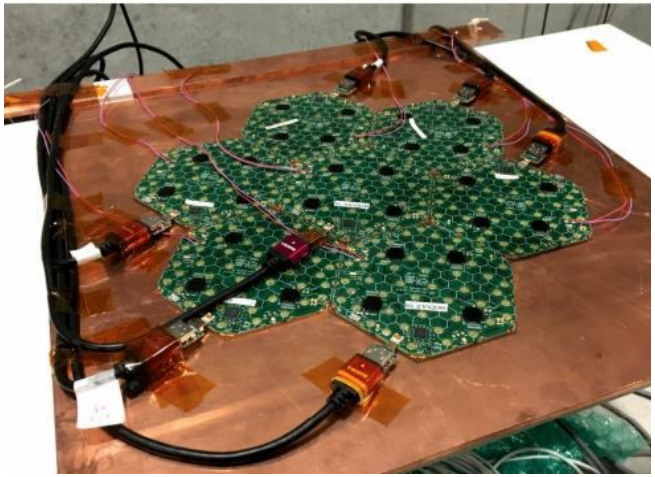


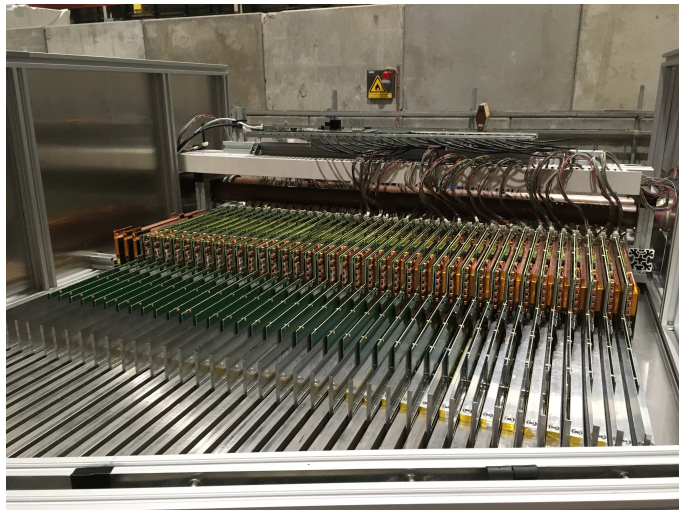


Electromagnetic calorimeter (**CE-E**): **Si**, Cu & CuW & Pb absorbers, 28 layers, 25 X_0 & ~1.3λ
Hadronic calorimeter (**CE-H**): **Si** & **scintillator**, steel absorbers, 24 layers, ~8.5λ

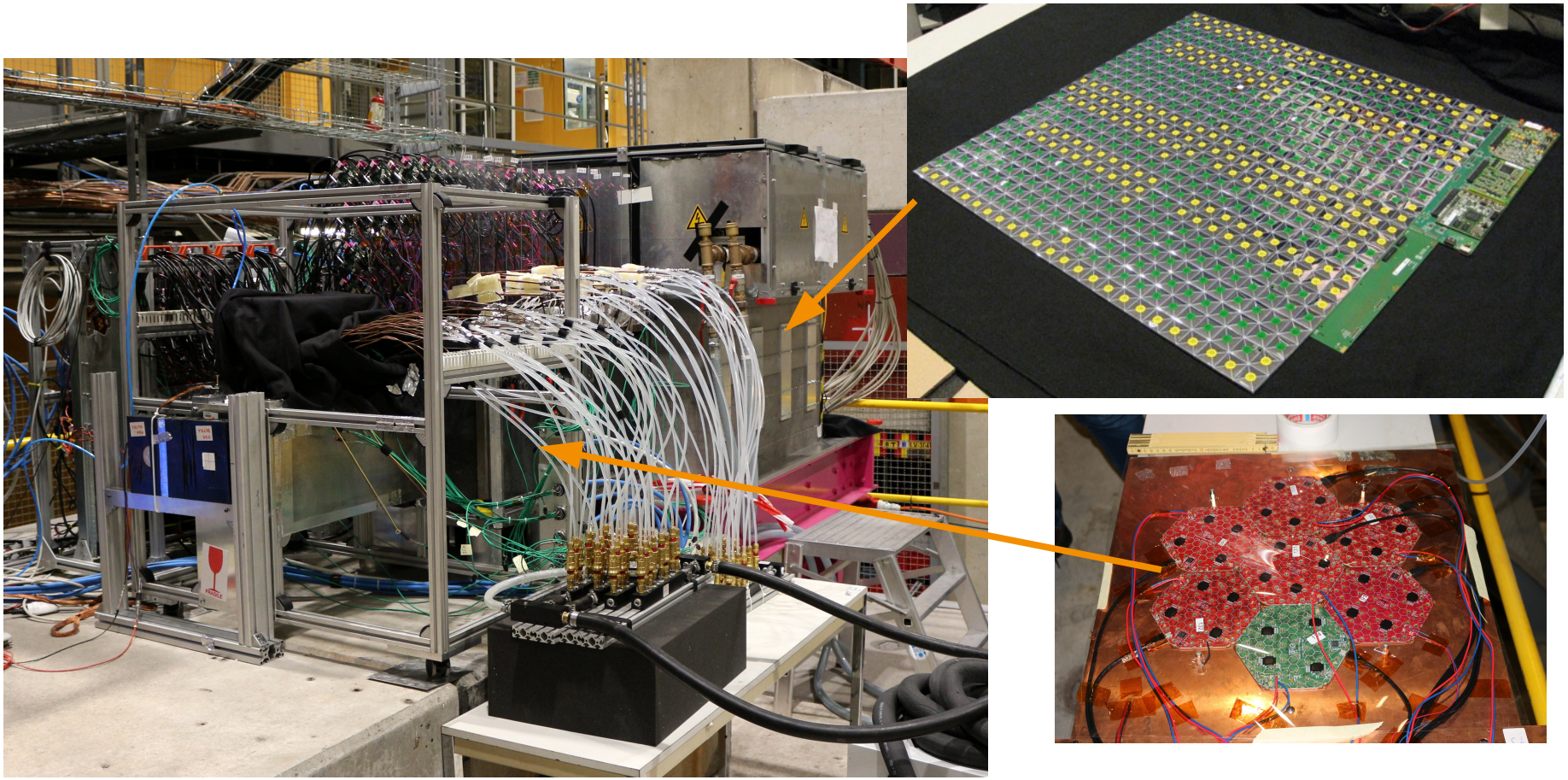
CMS HGCAL + AHCAL testbeam at SPS in October 2018

- beamtime 10 – 24 October 2018 in H2 at SPS
- main goal: energy scan with pions (maybe last chance for combined setup)
- HGCAL hardware: 94 HGCAL hexaboards
  - fully equipped CE-E (28 layers, 1 board per layer)
  - nearly fully equipped CE-H (12 layers, 9 layers with 7 boards and 3 layers with 1 board)
  - CE-E was in testbeam in June 2018, detector much better understood now (noise problem solved)
- AHCAL hardware: new large prototype
  - 39 layers of 2*2 HBUs
  - **in total ~22'000 channels**
- **combined DAQ based on EUDAQ2**





HGCAL + AHCAL setup in 2018



- 28 layers HGCAL EE (silicon/lead), 12 layers HGCAL FH (silicon/steel), 39 layers AHCAL (scintillator/steel)

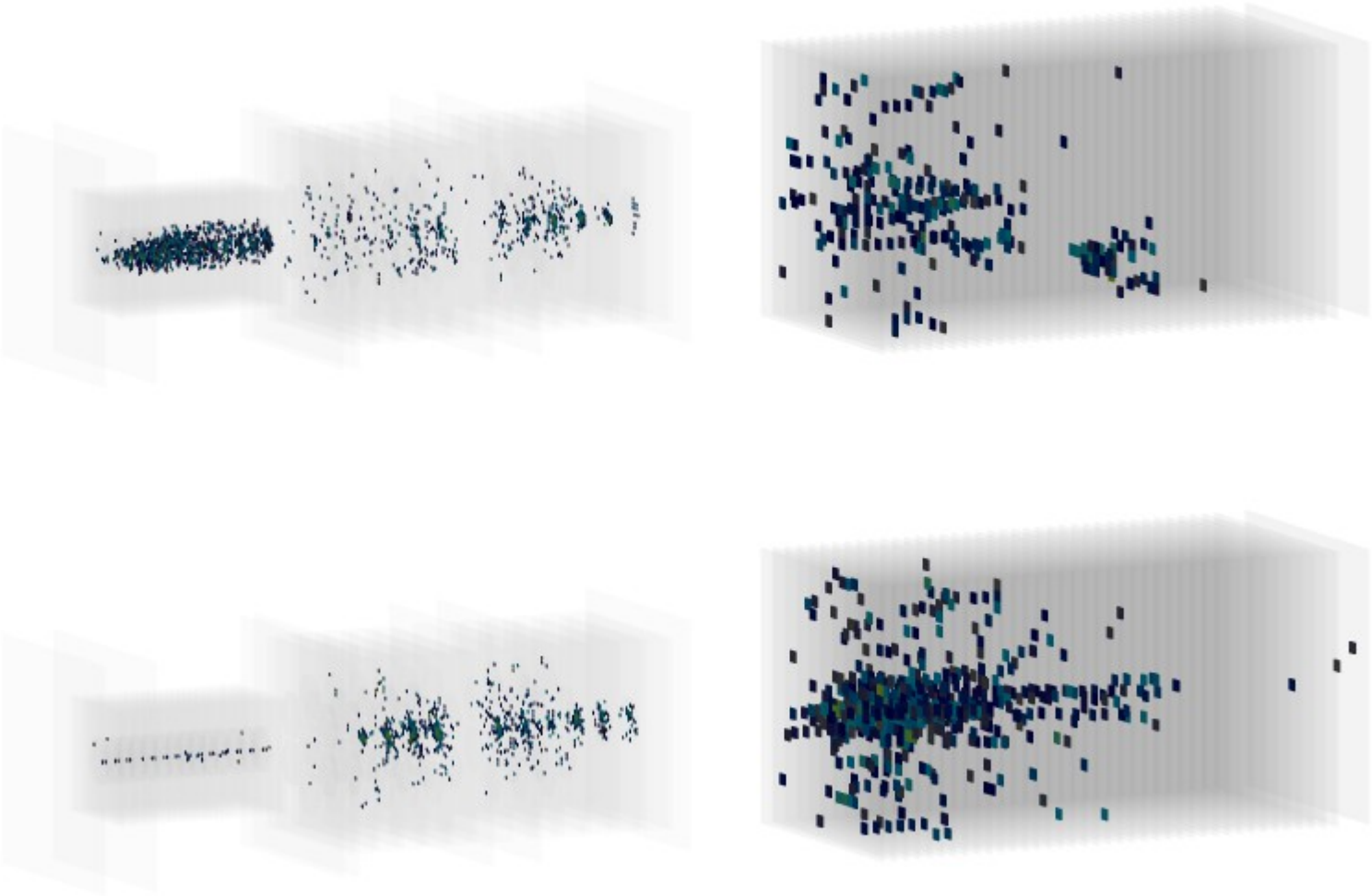
AHCAL + HGCAL combined DAQ

- Setup
  - HGCAL SYNC board as master (no TLU)
  - HGCAL prototype: externally triggered (beam scintillators)
  - large AHCAL prototype: self-triggered, power pulsing
  - Delay Wire Chambers
  - Cherenkov detector

- synchronization of the two detectors
  - common 40 MHz clock for HGCAL and AHCAL, DWC clock independent
  - moved from EUDAQ1 to EUDAQ2 -> adapted producers

Event displays: 300 GeV hadron showers

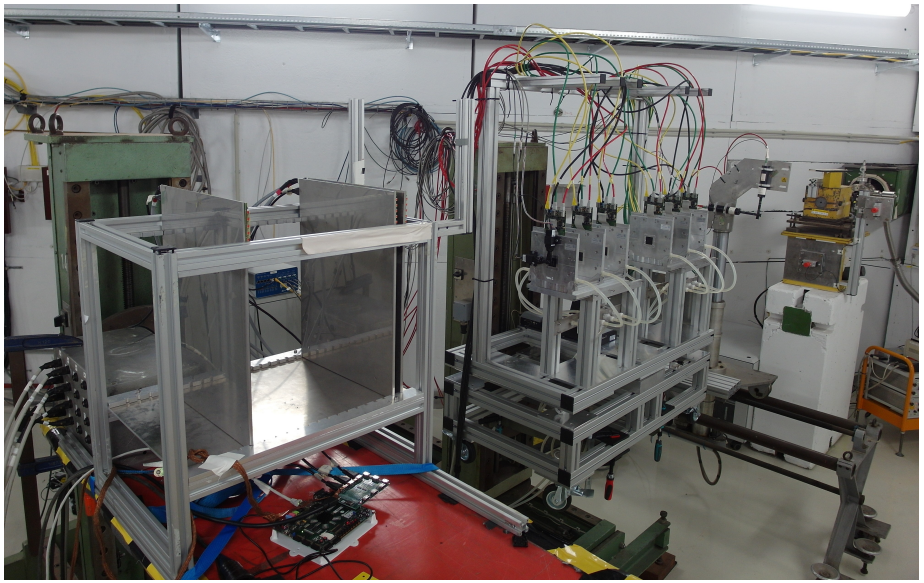
Synchronization works!



from A. Steen

AHCAL testbeams at DESY in March and May 2019

- beamtimes 18-24 March and 13-19 May 2019 in TB24 at DESY
- main goal: test HBU with Megatiles (Mainz)
  - Light Yield
  - MIP uniformity within a tile
  - optical cross talk to neighbouring tiles
  - ➔ telescope for precise position measurement
- May setup: 3 single HBUs in total + beam telescope + BIF



AHCAL testbeams at DESY in TB24 5.-11. August 2019

Goals:

Characterise ILC mode: Fast timing TDC clock/ramp - 200 ns clock period

- Compare to „normal" test beam mode (4 µs clock period)

Measure/investigate gaps between tiles/slabs

Setup:

5 large AHCAL layers in airstack (each 2x2 HBUs) = 2880 channels

Telescope: 4 new ALPIDE sensor planes

- Pixel matrix of 512 x 1024 pixels
- Pitch of 26.88 µm × 29.24 µm ◊ active area of about 15 mm x 30 mm
- Much faster than previous generation of DESY pixel telescope

Measurements:

LED gain calibration runs

Centered runs with and w/o absorber and telescope

MIP scans over layer area with telescope

- Tracking done with EUTelescope
  - Uses ilcsoft/LCIO out-of-the-box compatibility
  - Generic enough to work with only four telescope detectors
  - Can either process data with CALICE software before or after
- Track extrapolation from telescope onto AHCAL prototype

Spatially resolved map of tracks with no detected hit on the first AHCAL layer ("*inefficiency map*")

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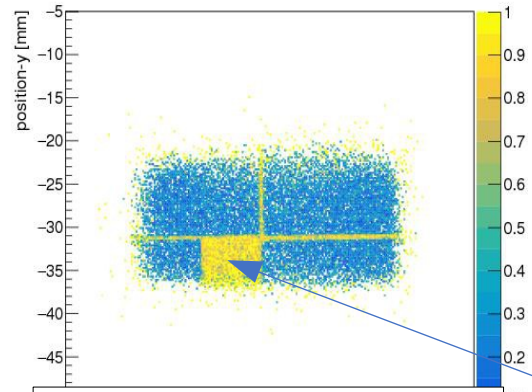
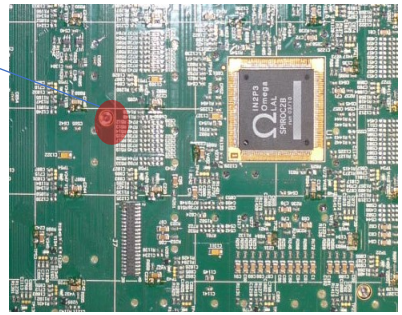
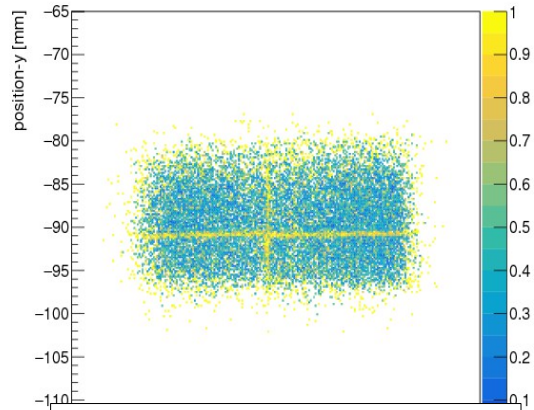


tiles with cut-outs for screws





tiles w/o cut-outs for screws

Summary

WP14.4 Summary:

- EUDAQ provides a great framework for integration of multiple detectors
- All milestones and deliverables fulfilled
- Further activities this year :)

Papers and Talks:

- “EUDAQ − A Data Acquisition Software Framework for Common Beam Telescopes” http://inspirehep.net/record/1756754?ln=en
- “EUDAQ2—A flexible data acquisition software framework for common test beams, http://inspirehep.net/record/1746258?ln=en
- R. Poeschl, CHEF
- A. Irles, IEEE