Summary of fast reaction PLC modules test

Beckhoff
EL1259-1001 full hardware implementation following CERN specifications simple logic diagram:

Internal execution timing:

The card is fully stand alone does not require CPU time to execute, registers are exchanged with the PLC CPU for information and reset.
The test bench is as follows:

Measurement results 2 cards in series jitter between 30..40 usec
Yellow DO out / green first EL card out / red second EL card out
V2.0 of the card with fine-tuning of the internal clocks:
B&R reaction module 8001 4DI 4DO

Test of a B&R PLC with reaction cards simple program read one DI write one DO
The 8001 card has a mini PLC task running on an FPGA that is loaded from the PLC main CPU and executed locally by enabling an RT task on the 8001 module. There is a specific library of functions to be use, this in parallel with a standard PLC code.

Test code:

![Diagram](image)

with RT clock 10us Read DI write DO simple code with 2 FB gives a delay of ~24us

![Graph](image)

with rt clock 1us Read DI write DO simple code with 2 FB gives a delay of ~7us
Full logic implemented

with rt clock 2us Read DI write DO simple code with 2 FB gives a delay of ~10us
Actual hardware interlocks

As comparison our present full hardware implementation with FPGA home mad modules, same logic as the Beckhoff test card same test set-up

Note:

The yellow signal (IN) is a pulse generator the output is loaded with R=300 and connected to +5Vdc so the green signal (OUT) is inverted

The delay is ~14us