# Tell40 architecture

- Requirements
- ATCA standard
- Proposed architecture
  - Readout
  - Supervision
  - Time distribution


Pierre-Yves Duval and Jean-Pierre Cachemiche
on behalf of the Marseille group

# Requirements

## Requirements drawn from previous discussions

- Because compression would be made in the FE electronics,
  ouput flow of a Tell40 board ≈ input data flow.

- GBT is built to transport data aquisition, slow control and time distribution on a single bidirectional channel.

  - **Slow Control**: having an output link for each data input link would increase the number of links.
    It looks better **to split data acquisition from slow control** and adjust the ratio between them.

  - **Time Distribution**: same remark concerning the number of links.
    A tight communication with the Tell40 is necessary to manage the destination addresses of the farms and to receive throttles.

- The complexity of TFC will require the **design of a specific board**.
  Can we merge Slow Control and Time Distribution on the same boards ?
  - This point has to be discussed.

## Implementation

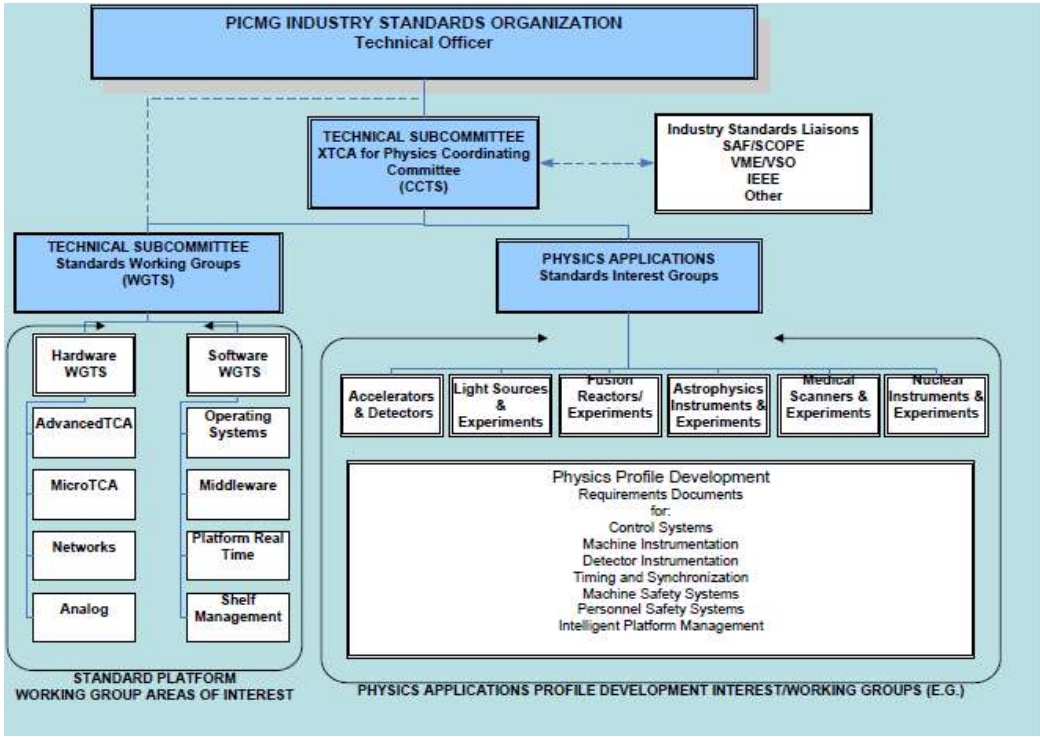
- From these requirements we propose a **flexible and scalable architecture, compliant to the ATCA standard**, that should adress the above requirements while remaining open to future evolutions.

# ATCA standard

## Considered as successor of VME

- VME was based on parallel busses
- ATCA based on serial busses

- Large support from external sources
  **Save development efforts**




## Increasing interest in Physics community

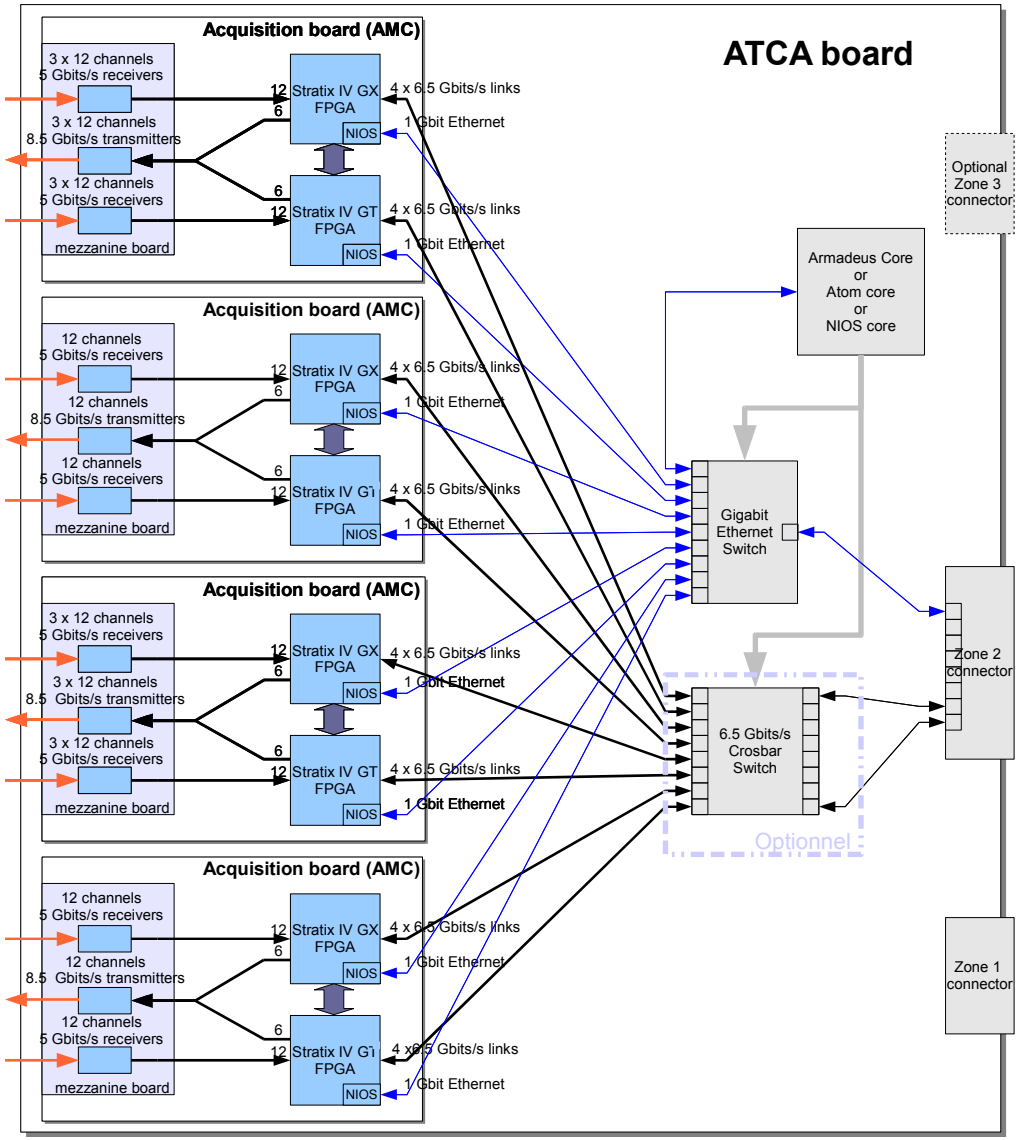
- New **xTCA for Physics Committee** created early 2009
  - WG1: Physics xTCA I/O, Timing and Synchronization
  - WG2: Physics xTCA Software architectures and protocols

- Many contributors in our community:
  DESY, SLAC, IHEP, FNAL, ANL, BNL, KEK, CERN, FZJ, IN2P3, IPFN, JET, …

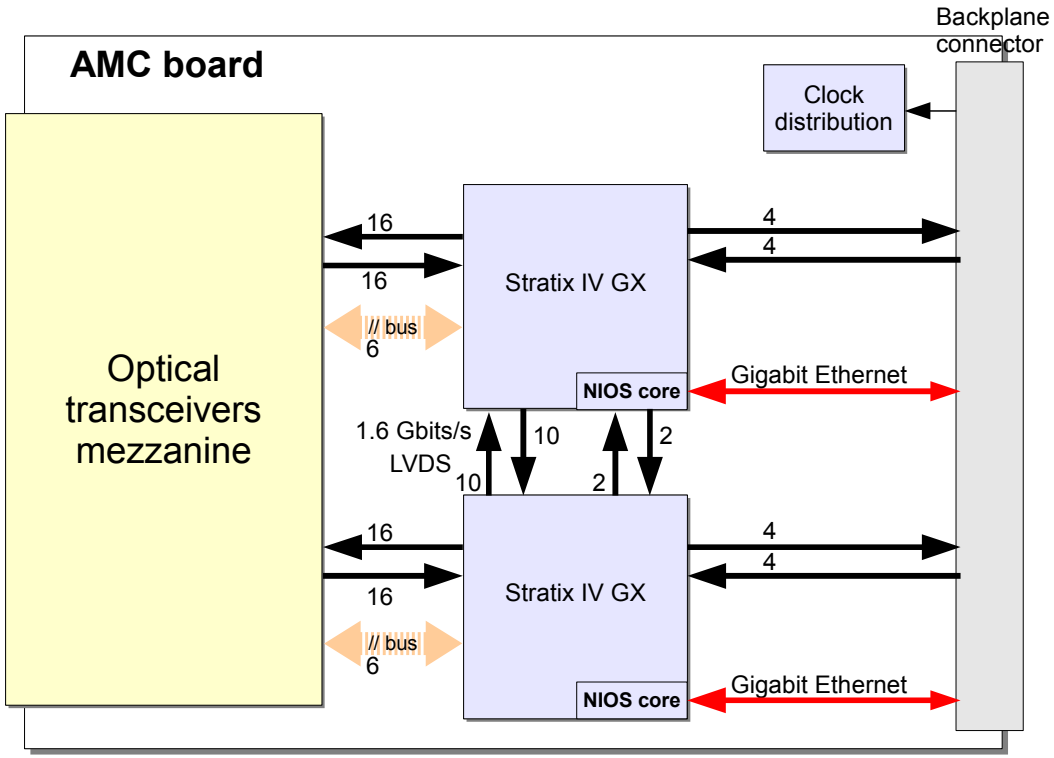
- Foreseen to be used on following projects:
  XFEL, ILC, ITER, JET, ATLAS Upgrade, FAIR, AGATA, …

# TELL40 board based on ATCA standard

- Main board is an **ATCA board** (8U x 288mm)
  Includes :
  - power management
  - clock distribution
  - slow control switch
  - optionally local supervision
  - optionnally communication between modules
- **4 AMC** modules with :
  - 2 Stratix IV GX each
  - 24 GBT input channels
  - 12 output channels to the farms
- We can rapidly achieve this
  from **existing developments**
  **+ COTS available in the industry**



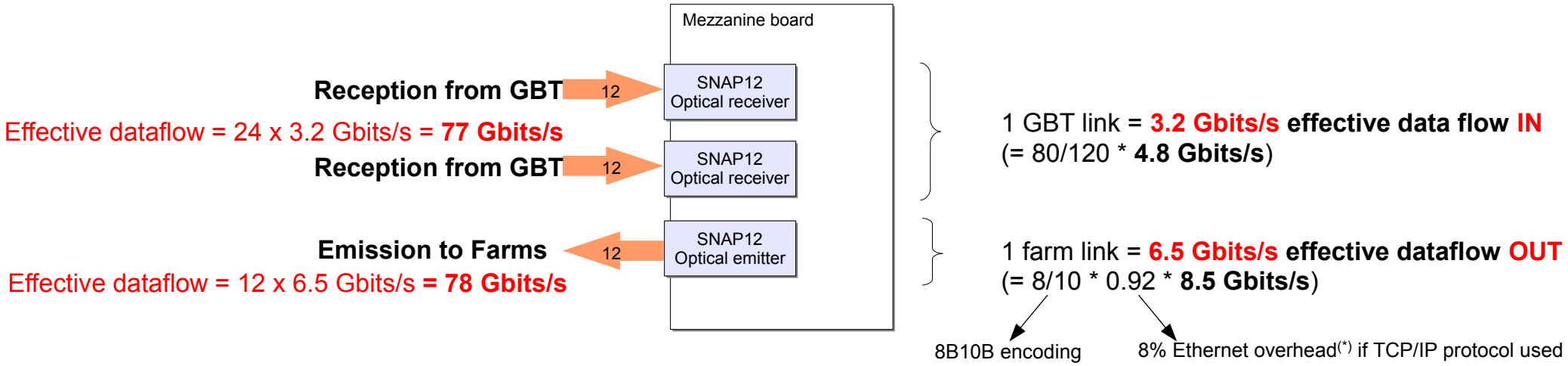
# Acquisition board (AMC)




- Concept of **« Optics transceiver on mezzanine »** allows many configurations
  Only limited by space available on the front plate (~ 3 SNAP12)

- **Prototype developped at CPPM has exactly the structure of such an acquisition board**

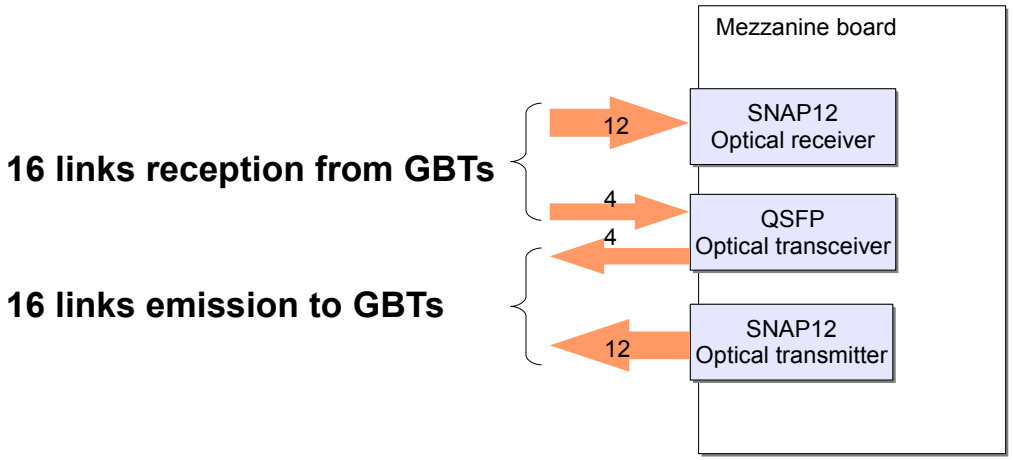
# Optical mezzanine
# Balanced I/O dataflow for processing




(*) source http://sd.wareonearth.com/~phil/net/overhead/

# Optical mezzanine
# Bidirectional I/O dataflow for slow control

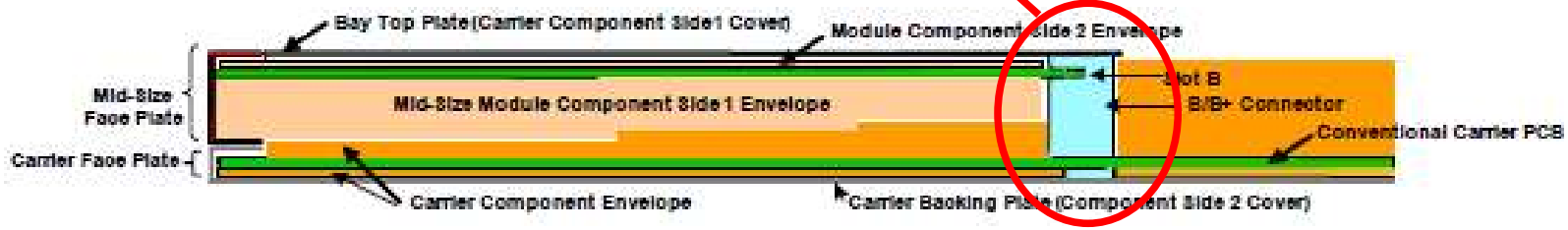
- No need to have downstream data flow on each read-out board
  - a single bidirectional link per front end board is sufficient
  - all slow control interfaces can be concentrated on few boards



# Connection on a main board

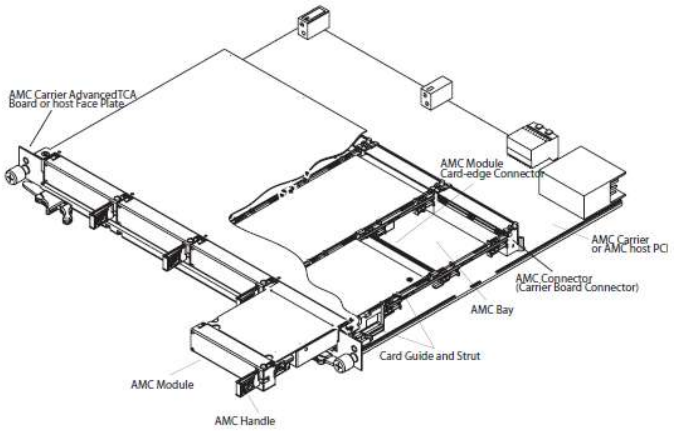
- Standard connectors exist in the ATCA standard
- Can transport high speed serial data links (10 Gb/s)

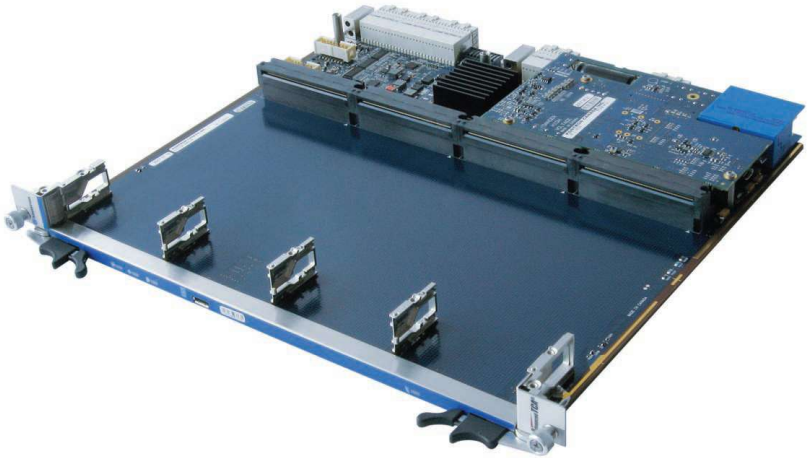
EPT AMC B+ connector



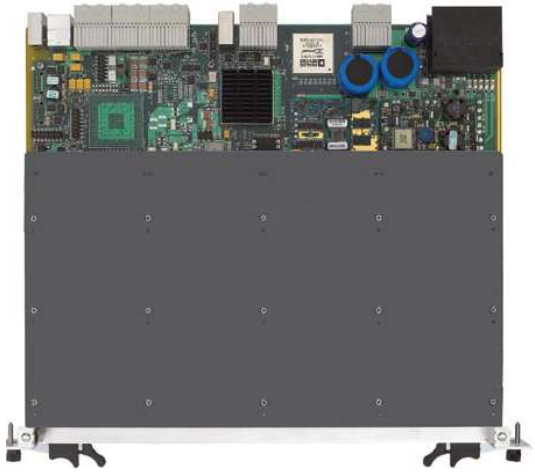
# Commercial carriers boards

- Can welcome up to 4 AMC mezzanines
- Comes with
  - Power management system,
  - Ethernet supervision system,
  - Embedded switch
  - Local processor running Linux



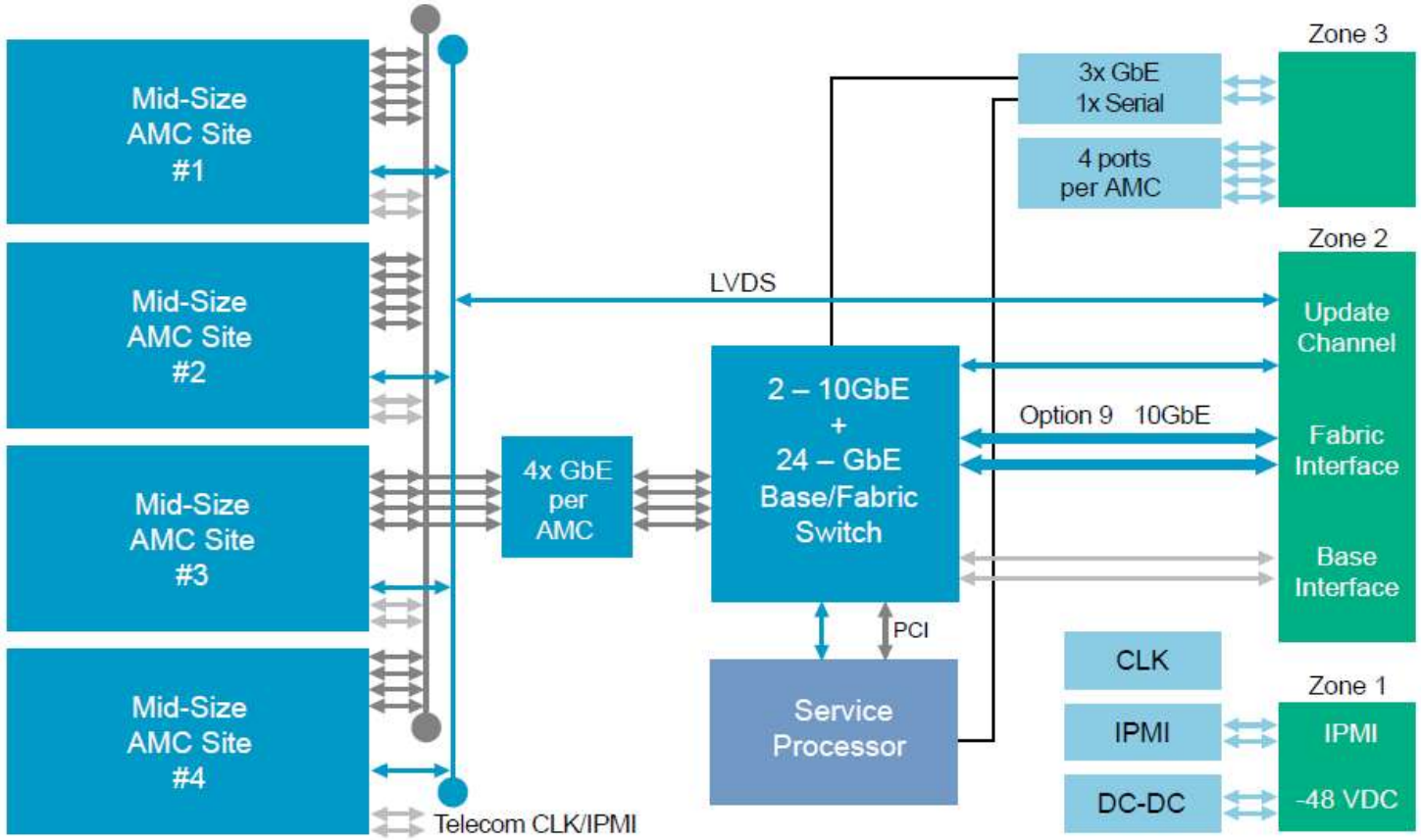



Kontron carrier



Emerson carrier

# ATCA carrier typical architecture




Emerson carrier architecture

Does not allow real time exchanges between AMC boards

# ATCA Commercial crates

## ATCA crate

- Can embed from 2 to 16 boards
- Includes power supply, cooling, etc ...
- Light versions exist
  - cheaper

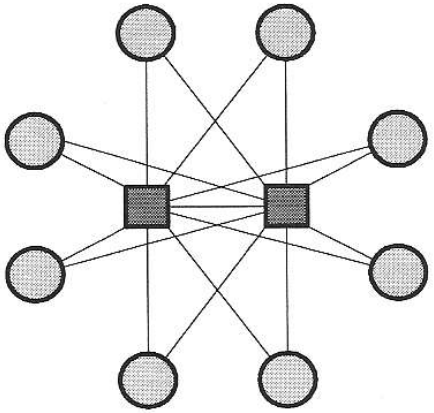

Emerson crate

Schroff crates

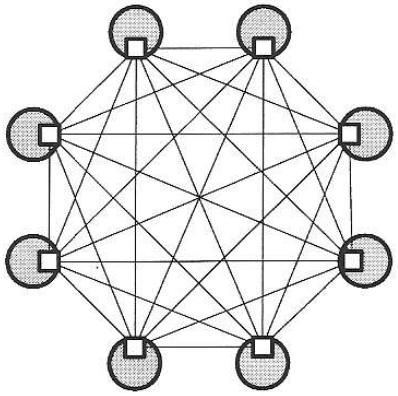
# Standard backplanes provided

**Features**

- Power distribution
- Geographical addressing
- Clock distribution
- **Standard serial interconnections between boards**
  - Several standard topologies
    - Star, dual star
    - Full mesh
  - Some dedicated to transport **control** (Ethernet for example)
  - Others dedicated to **data**
  - Communication protocol is free



Dual star topology



Full mesh topology

# Mockup read-out system

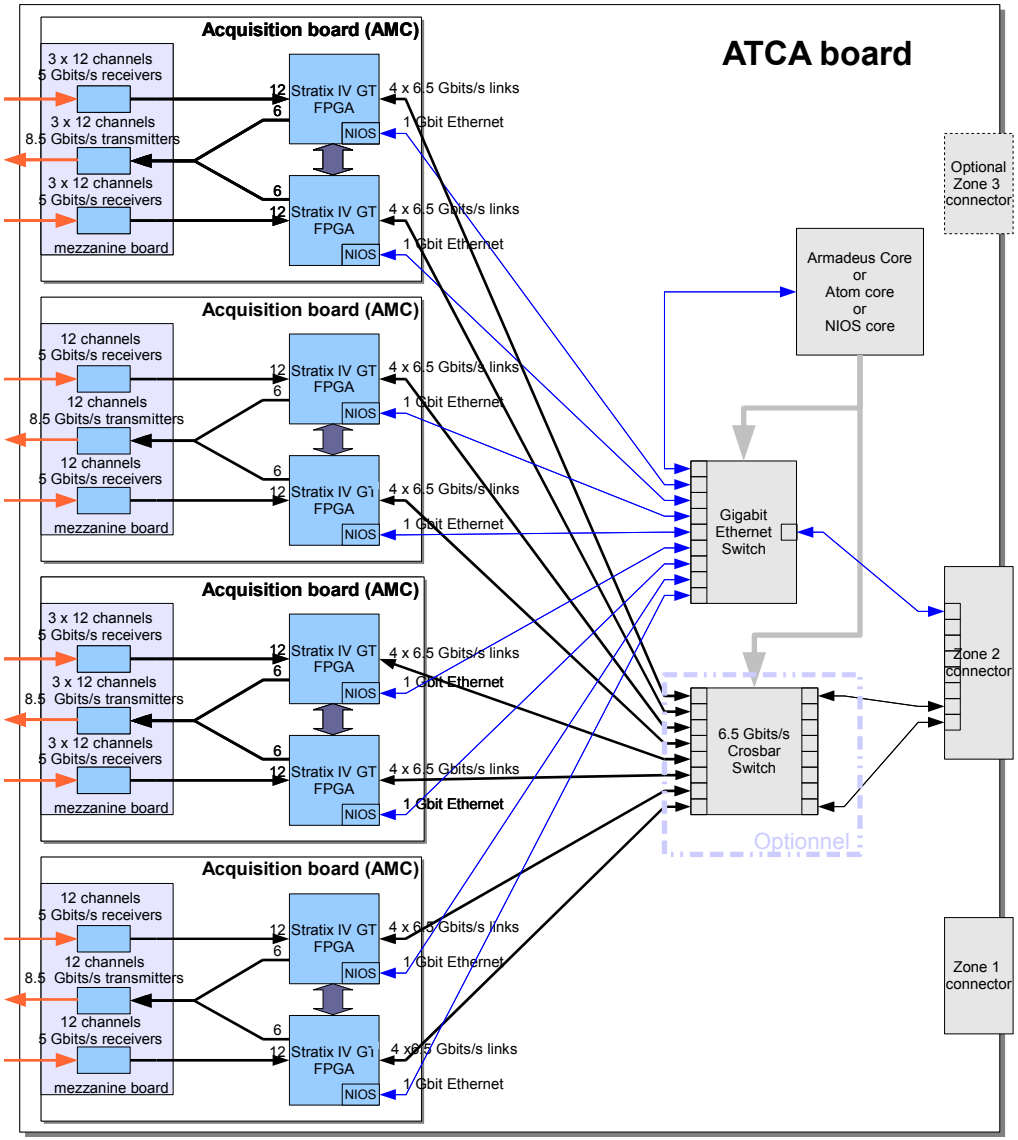
- With this approach and with minimum development efforts we are able to build a **minimum readout system very rapidly** mapped either on ATCA or µTCA
- It can be provided to groups to experiment and pilot their front-ends.
- Gives more time to design a specific ATCA board
  with functions not found in commercial boards if required.


Emerson low cost ATCA crate

Elma low cost µTCA crate

# Dimensionning of a TELL40 ATCA board

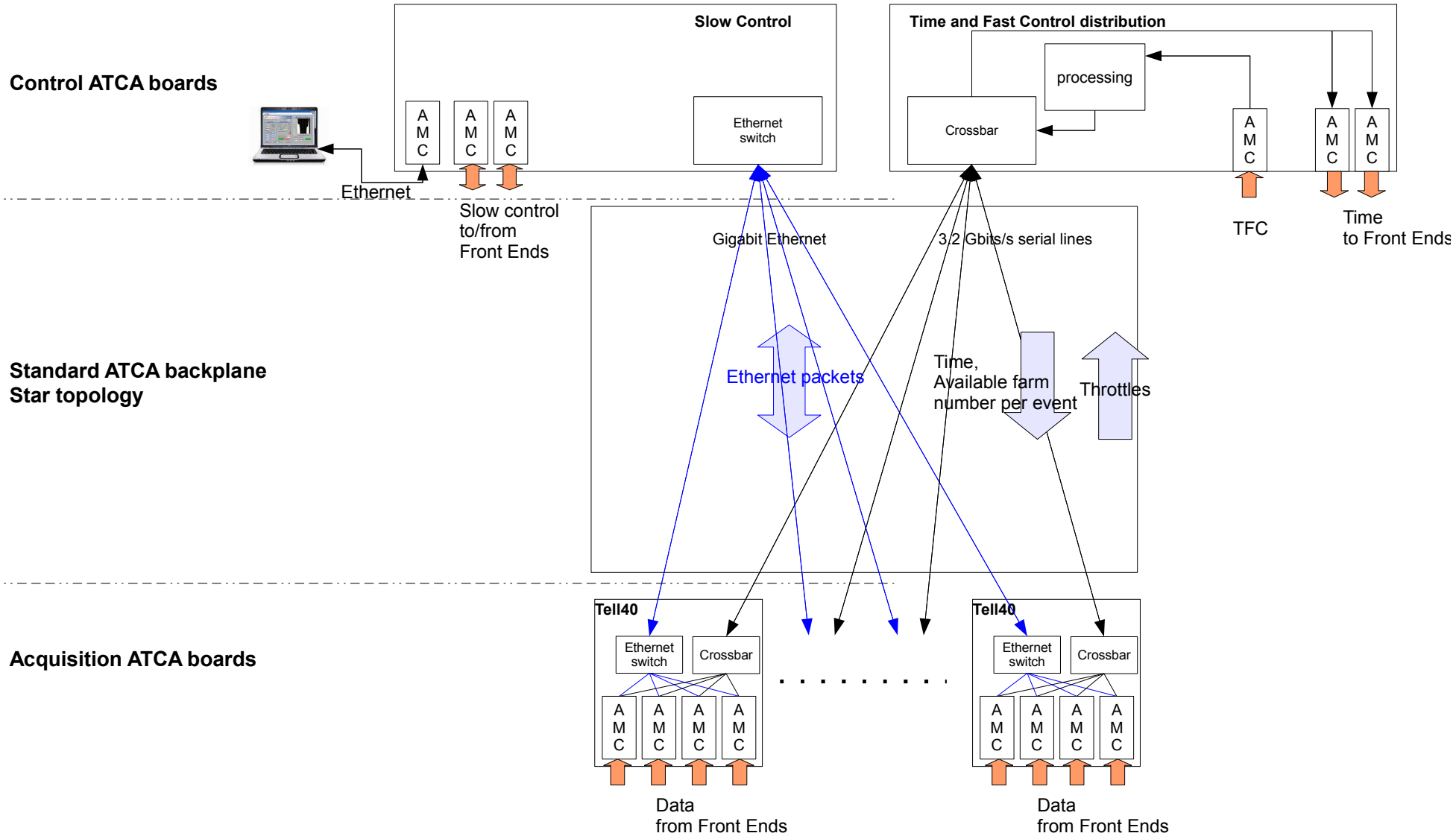
- Input : **96 links** at 4.8 Gbits/s per ATCA board
  - 460 Gbits/s raw
    or 307 Gbits/s effective
- Output : **48 links** at 8.5 Gbits/s
  - 408 Gbits/s
    or 312 Gbits/s effective
- If ZS: 9532 links required (estimation Ken)
  - **100 ATCA boards**
- **8 crates** for readout
- Around **25 kCHF / board**



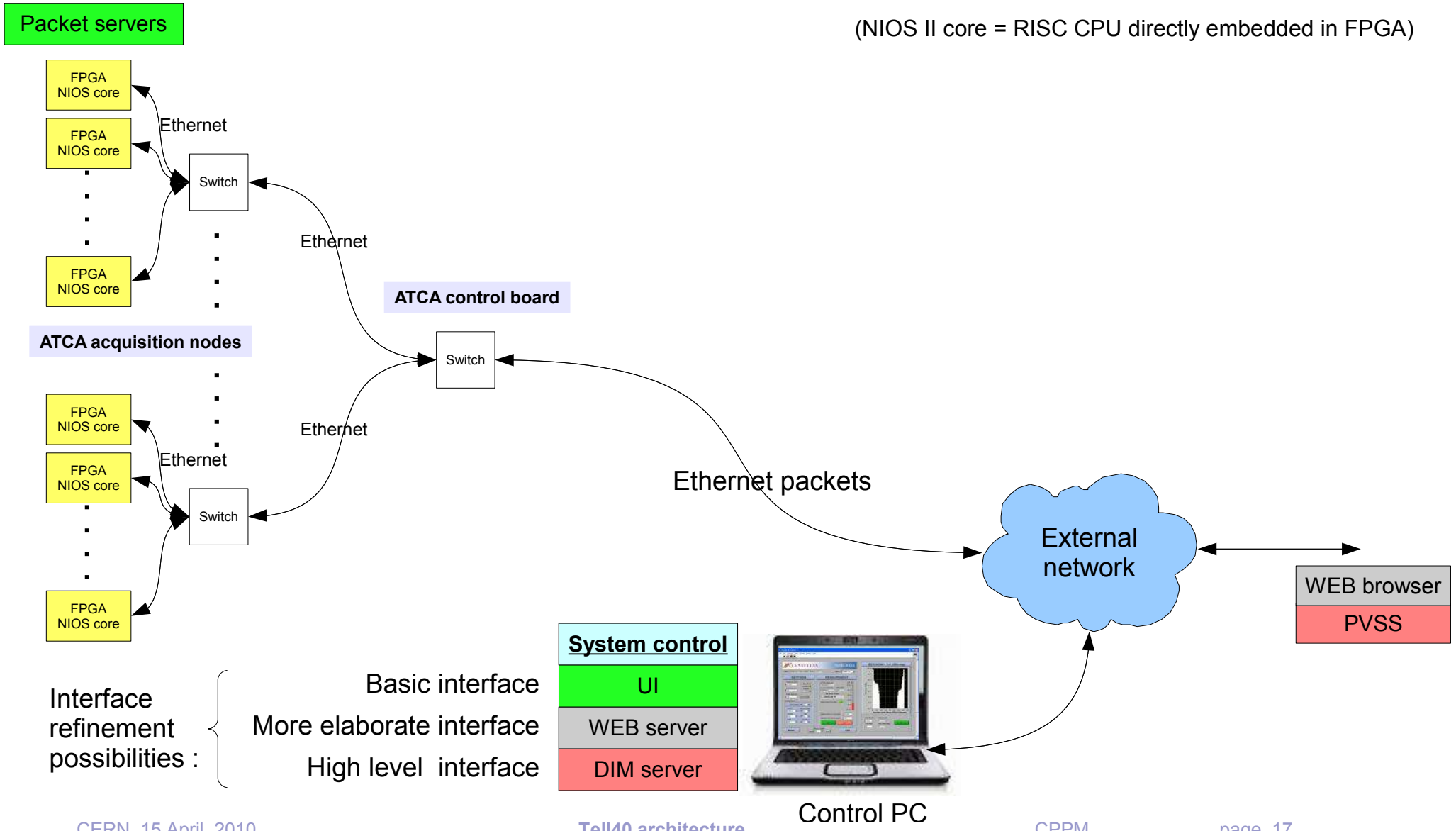
# TELL40 architecture

## System control

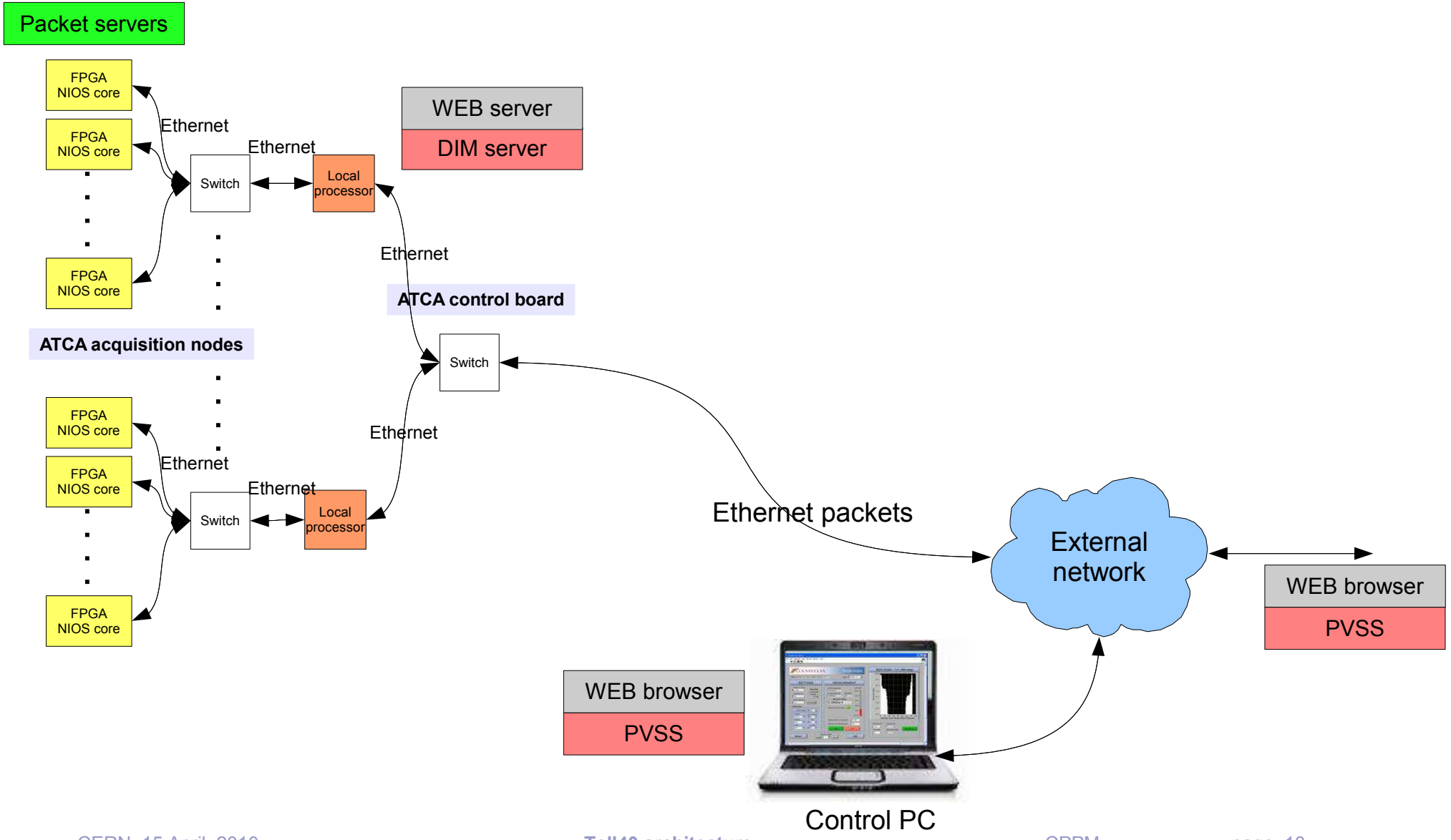
# System control



# Basic TCP/IP packet server running on NIOS II core



# Intermediate concentration with a local processor on each board



# Feasibility of a scalable supervision system relying on NIOS II cores

- A NIOS core with a triple speed Ethernet interface takes **only 4%** of the logic in a EP4SGX230
- Several sucessful trials made by Pierre-Yves Duval for validating the concept:
  - **Implementation of a basic server** running over a microC/OSII realtime kernel with Interniche TCP/IP stack from Micrium (fully supported by Altera)
    **1.25 ms on average per transaction** (individual write + readback) → allows 800 transactions per seconds with a simple NIOS core running at 50 MHz.
    Data transmission time negligible before the transaction time.
  - **Implementation of µCLinux + Dim server** (thanks to S. Bablok, people from LAL and Clara) : works fine.
    Requires external memory to the FPGA.
    No performance measurement yet but probably similar.
- Paves the way to a **low cost scalable slow control system**

# Conclusions and perspectives

## Tell40 can be designed using ATCA standard

- Its flexibility allows many configurations from simple system to complex one.
- Available commercial products + duplication of current AMC prototypes would allow to get a workable hardware platform very soon:
  - **Groups can experiment quickly** and pilot their FE electronics.
- Standard carriers can be used if no communication between FPGAs
  Otherwise an ATCA design will be required

## Supervision can rely on NIOS core embedded in FPGAs

- Measured performance sufficient for slow control
- No extra room taken on boards
- Cheap
- Scalable