LHCb Upgrade
Front End→Back End
Readout Architecture Proposal

- An Orchestra Director view -

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Aim and not aim of this presentation

- A somewhat different presentation approach than usually
  - Concentrate on outlining global concepts on few slides and words and not drown them in details – Top-down approach
    - Hold back description of implementation
    - Hold back on choice of technology
      - *Often detrimental to the constructive discussion of the true requirements*
- Why?
  - Because we are turning around in circles on trigger and readout strategy
  - Because I believe there are concepts which have to have common census on today
  - Start development against *common* specifications
  - Of course stay flexible allowing choices of new technologies but goes hand in hand with the requirement of versatility

The details of what we present here are available and in development:

- December 2008: http://indico.cern.ch/conferenceDisplay.py?confId=44442 (LHCbWeek)
- May 2009: http://lhcb-doc.web.cern.ch/lhcb-doc/presentations/conferencetalks/postscript/2009presentations/Alessio-IEEE-NPSS.ppt (RT2009)
- September 2009: http://cdsweb.cern.ch/record/1209646?ln=en (TWEPP09)
- September-December 2009: http://indico.cern.ch/conferenceDisplay.py?confId=65307 (Simulation framework)

Readout Slice - Global Concepts

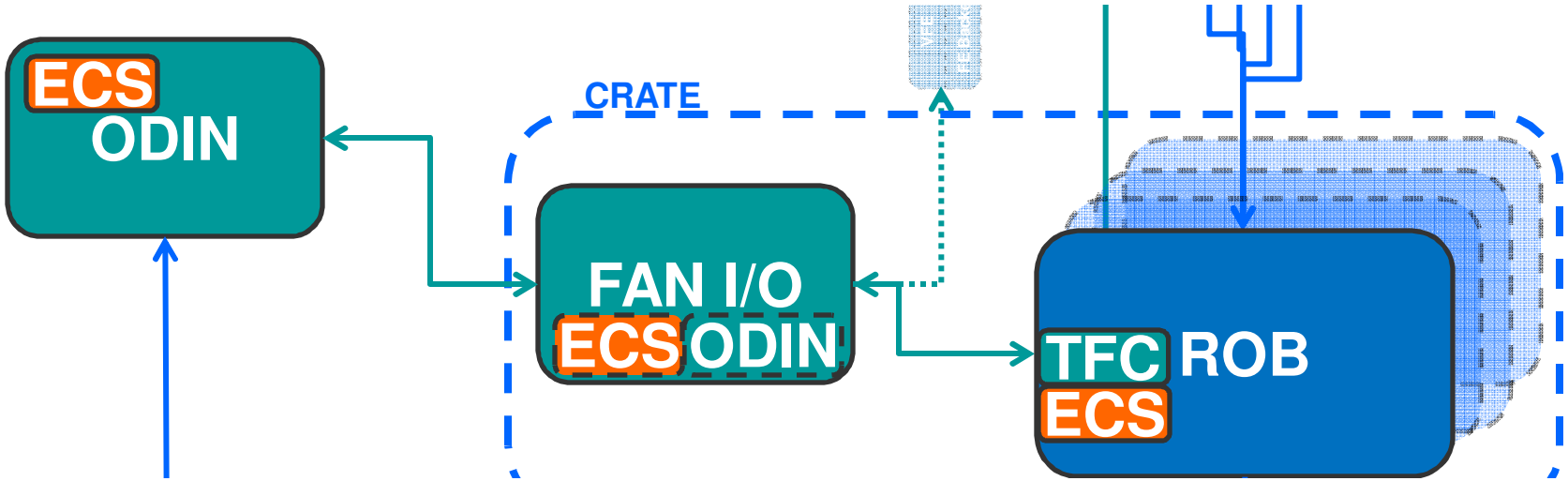
TFC plug'n'play firmware block – relay of TFC to FE and ECS to/from FE

ROB is ECS interface for FE – common approach allow making it available now

Distributed and hierarchical ECS

Nail this down, incorporate a trigger

- Procedure: Don't care what is "*in principle possible not to need it*", get a flexible and simple solution and integrate it



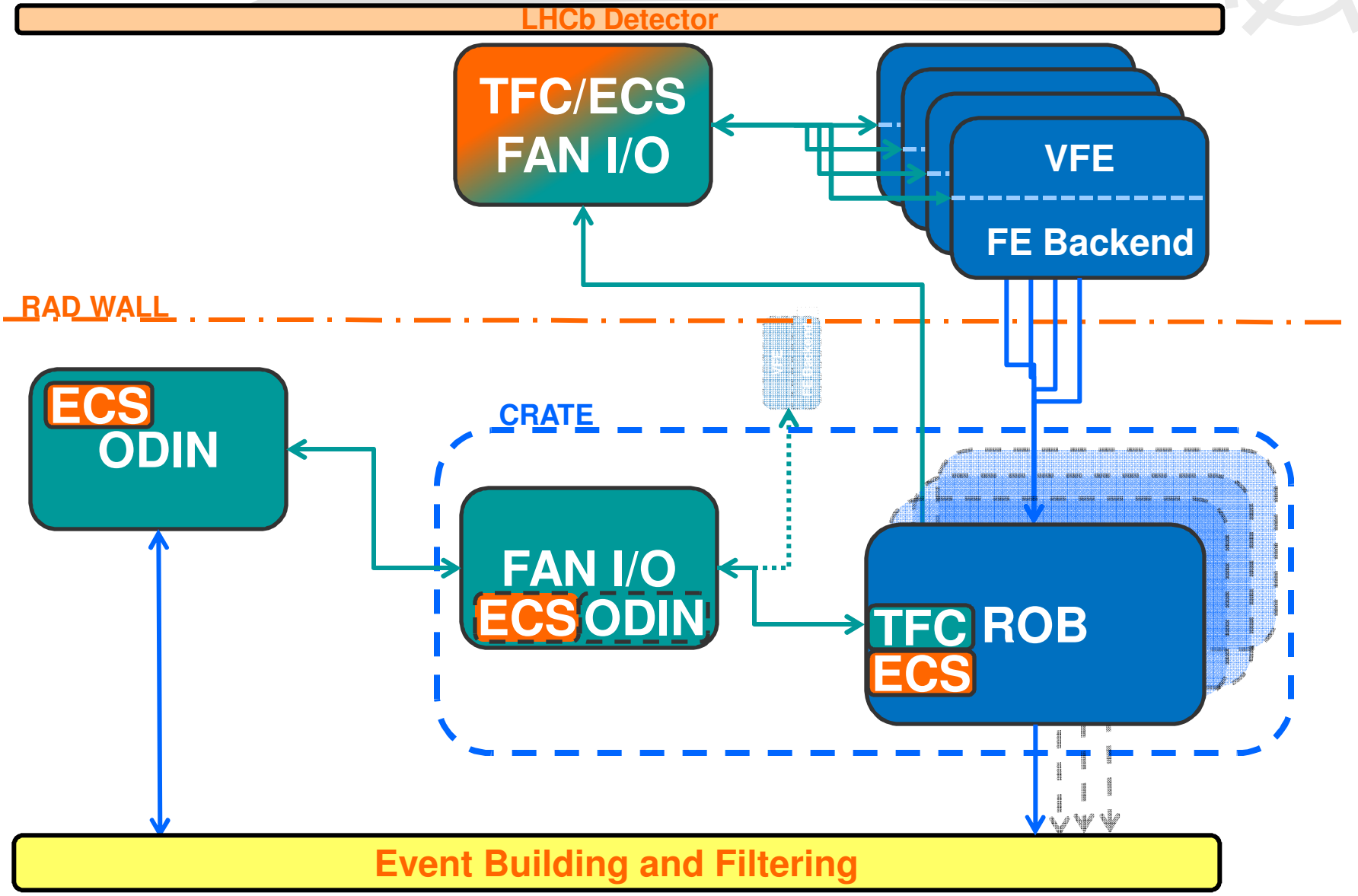
ECS interface based on DIM on NIOS with PCI-X and any other medium if needed

Event Building and Filtering

Our view of the Global Concepts

1. Single internally partionable ODIN
2. Commercial bidirectional FPGA links to ROB crates – latency/phase control solved
3. Intelligent fan-out/in board in each ROB crate
   - Used as local lab ODIN and ECS interface to early FE test benches
   - Not far from available thanks to Marseille hardware and CERN firmware development
4. TFC plug'n'play firmware block – relay of TFC to FE and ECS to/from FE
5. ROB is ECS interface for FE – common approach allow making it available now
6. One optical link to batch of FE corresponding to ROB per ROB
7. Common TFC/ECS fan-out/in board at FE
   - Distribution medium may have individual solutions
8. ECS interface based on DIM on NIOS with PCI-X and any other medium if needed
9. Distributed and hierarchical ECS
   - Not because of bandwidth of performance requirements on onboard ECS interface but
   - Because of the scalability of the control nodes and the global experimental control and its partitionability
10. Nail this down, incorporate a trigger
    - Procedure: Don't care what is "*in principle possible not to need it*", get a flexible and simple solution and integrate it

Readout Slice - Global Concepts



Prerequisits to go ahead

- Ken great job in collecting detector reqs - #links, data size etc
  - Generating discussion on ZS – we have decided it!, …or,… did we?
  - We need a document to ultimately check against when reviewing designs, reviews soon!
- List of functionality on which we have to settle on the specs now
  - (Mare's)dream of infinite buffers to handle a world of parallel schemes in FE is utopia
- Boils down to specify the following mechanisms and model back-end of FE
  - VFE (almost) full flexibility for individual solutions but timing boundaries
  - Synchronization
  - Latency limits and limits on asynchronicity
  - Truncation
  - Calibration
  - NZS data
  - Header formats (id,error flags, data type)
  - Throttling
  - Trigger
  - We need to clearly outline and incorporate what we use of old system
  - Control interfaces
  - ….
  - To most of these there are clear proposals but it is not enough – chose, write down and sign
- Availability of plug'n'play TFC and ECS interface for test benches is vital now