Tile Rear Extension (TREX) module for the Phase-I upgrade of the L1Calo Trigger

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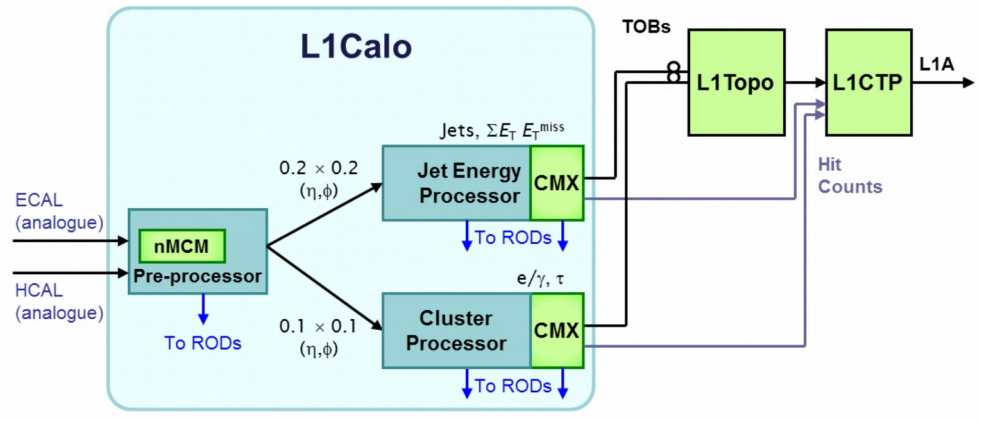
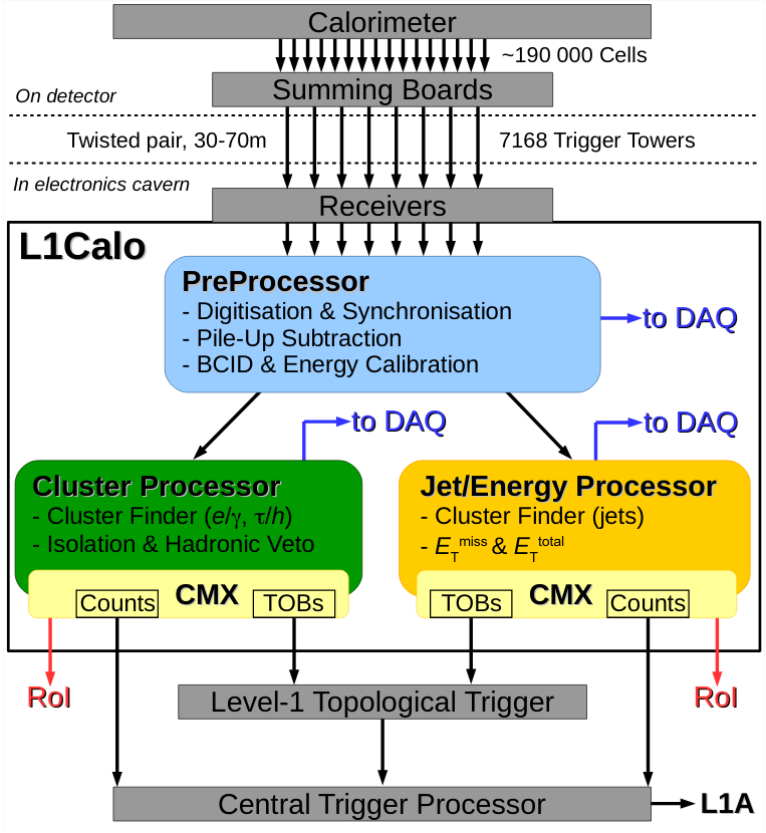
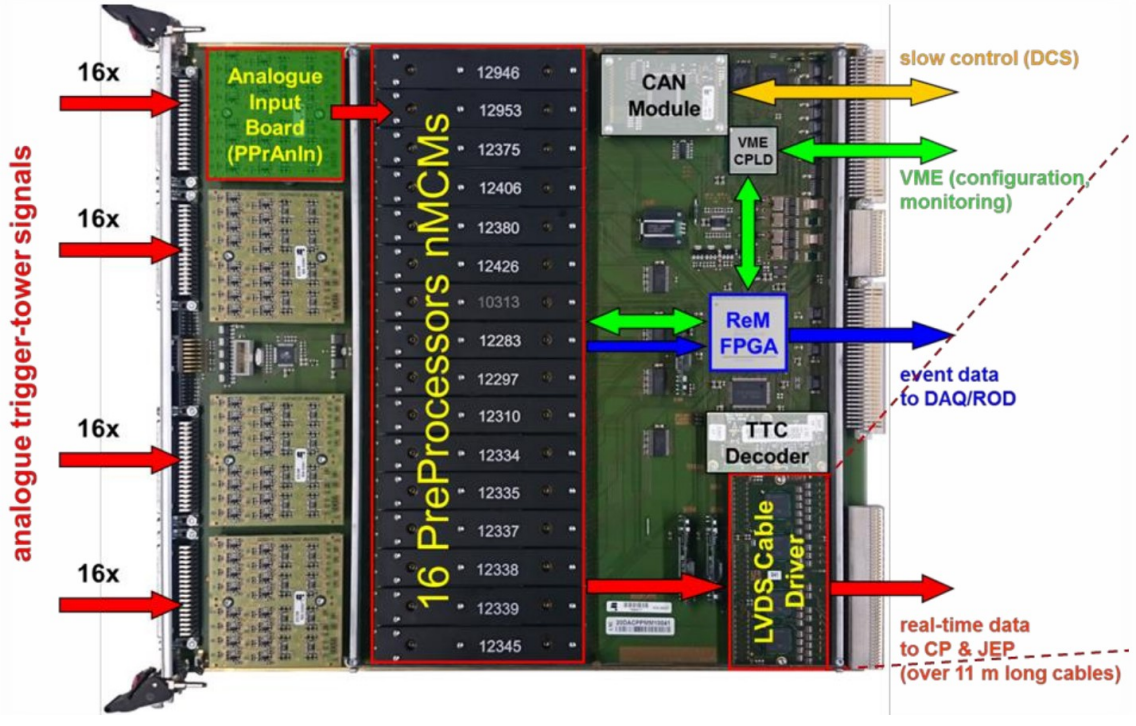
L1Calo system architecture Run2





- Sum up calorimeter data to trigger towers
- PreProcessor (PPM)
- Transmission to Cluster and Jet processor
- Find interesting events and provide the information to the CTP
- Find interesting event topologies through L1Topo
- Positive final trigger decision L1A

PreProcessor module (PPM)



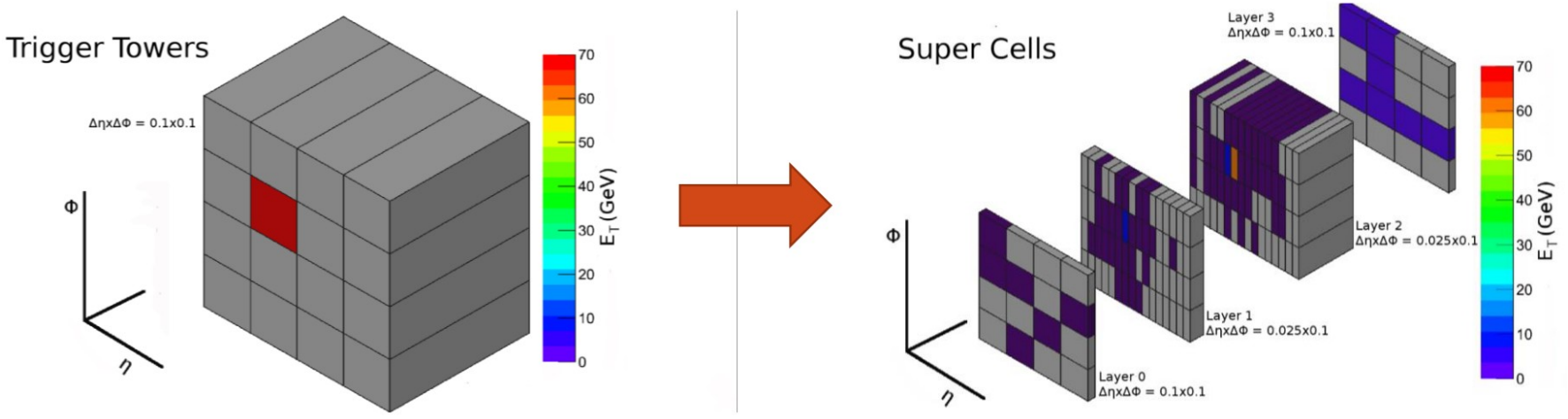
- 64 incoming analogue trigger tower signals
- nMCMs: Digitisation, synchronisation, pile-up suppression, bunch crossing identification and calibration
- ReM FPGA: Readout, VME configuration and monitoring
- CAN module: Slow control (DCS)
- LCD: Duplicates signals for CP & JEP and drives all signals over LVDS cables

L1Calo Preprocessor In USA15

- 8 VME crates [6 LAr and 2 Tile]
- 496 analogue cables into 8 crates
  [4 cables on front of one 9U module]

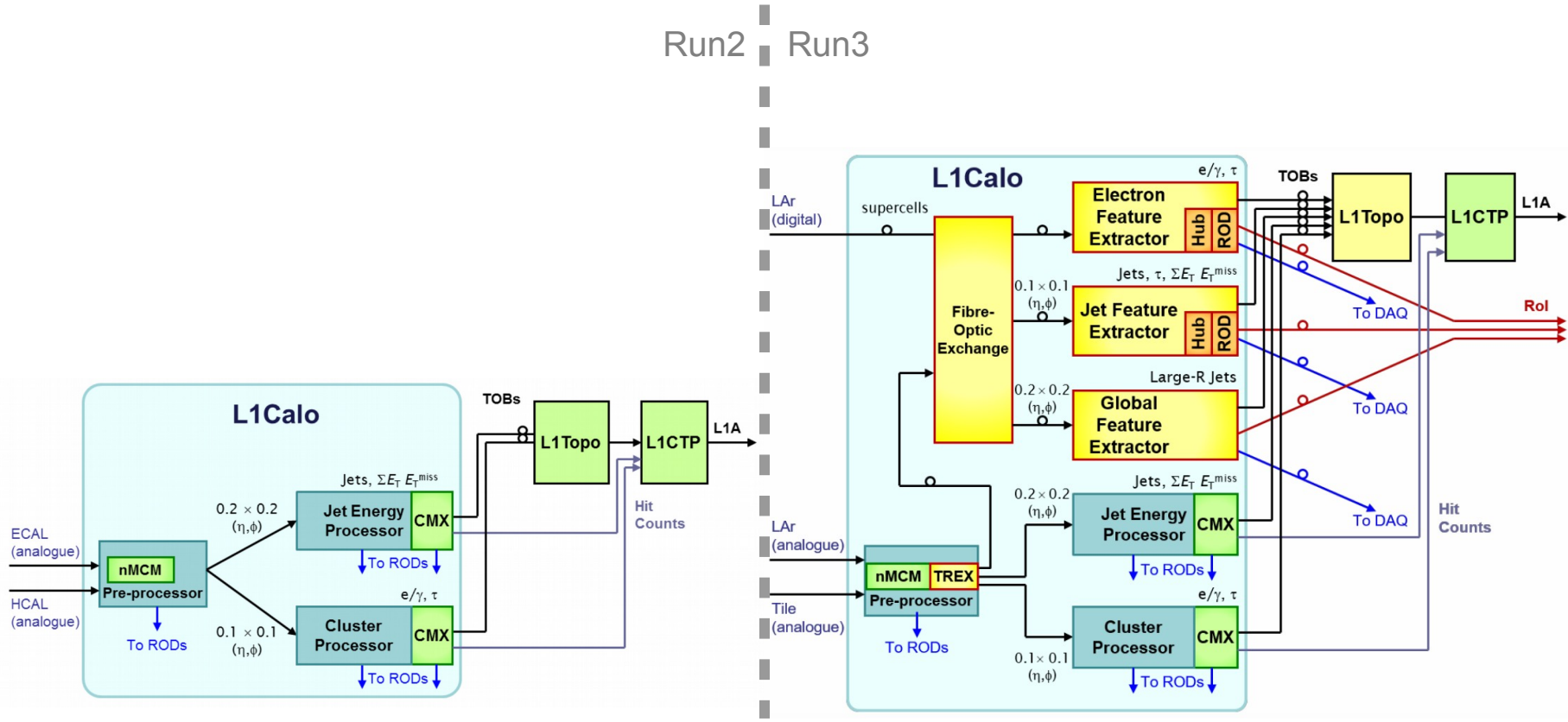
- 124 PPMs in total,
  [~16 PPMs per crate]
- Dense digital cabling
  at backside of crates
  [LVDS to CP/JEP]

LAr Phase-I Upgrade



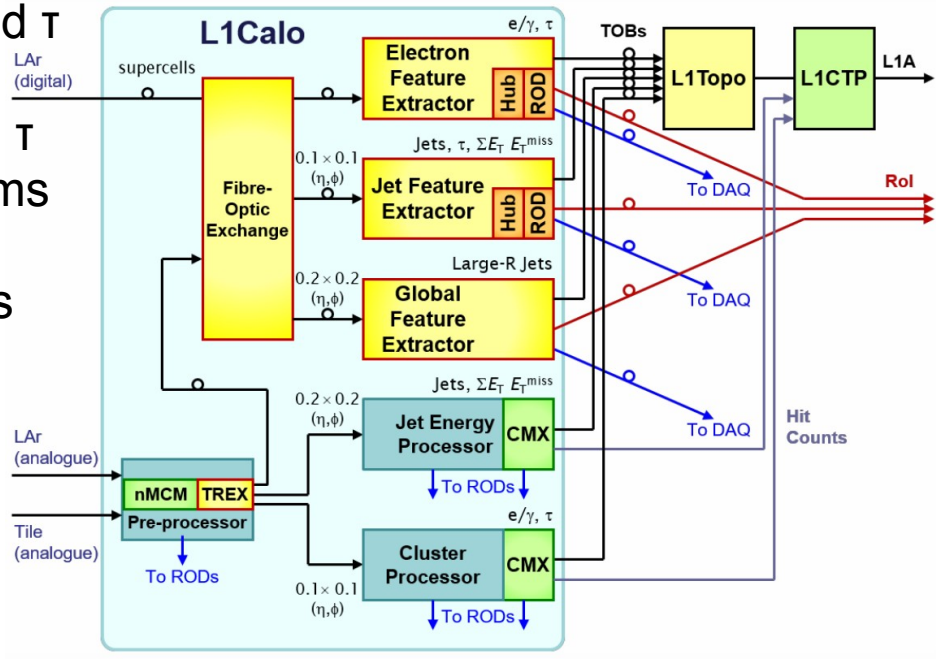
- Shower shape information lost in trigger towers
- Super Cells: Increase granularity and access to longitudinal shower shapes
- Additionally fine-granularity digital information via optical fibers

L1Calo system architecture

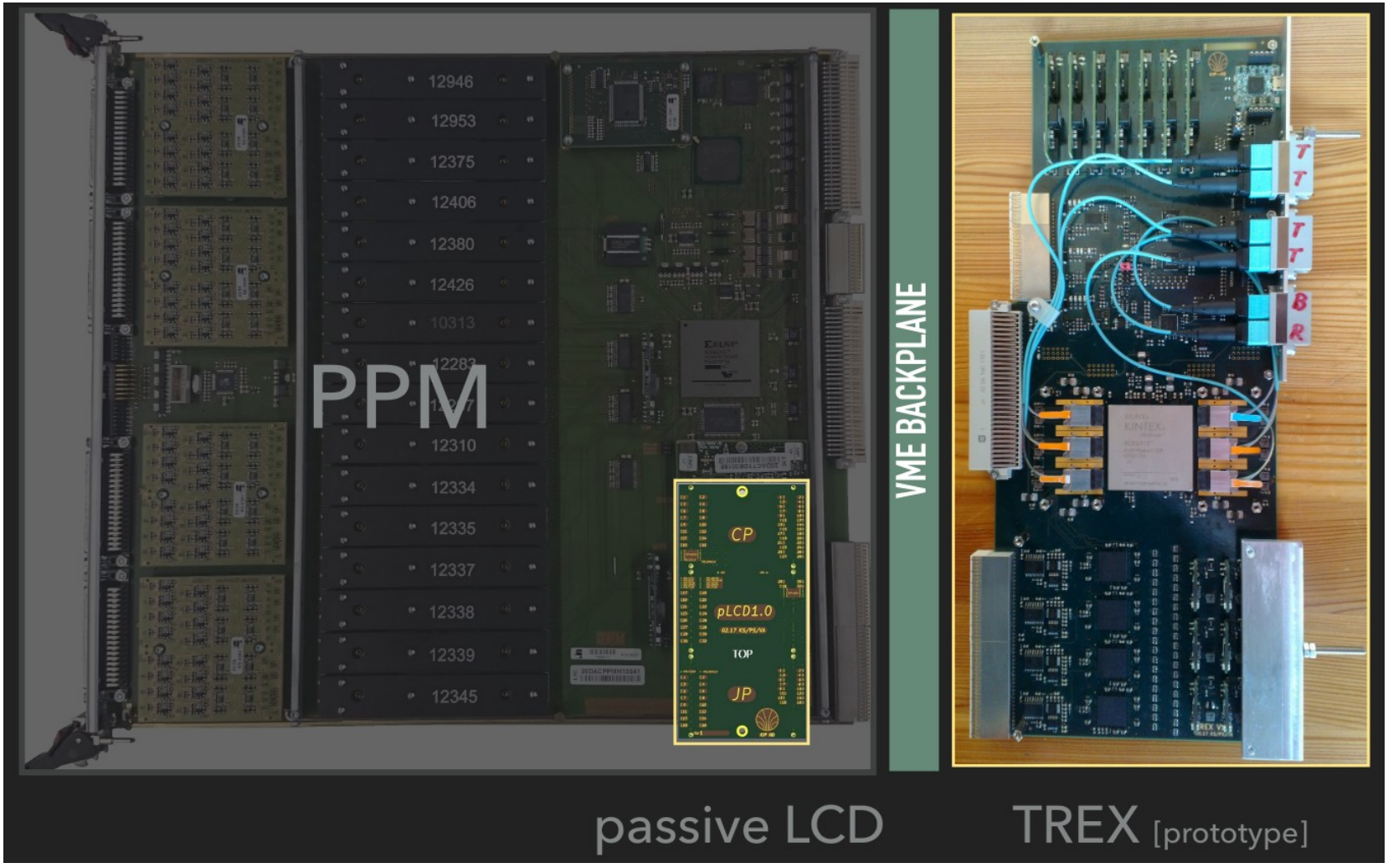


L1Calo system architecture Run3

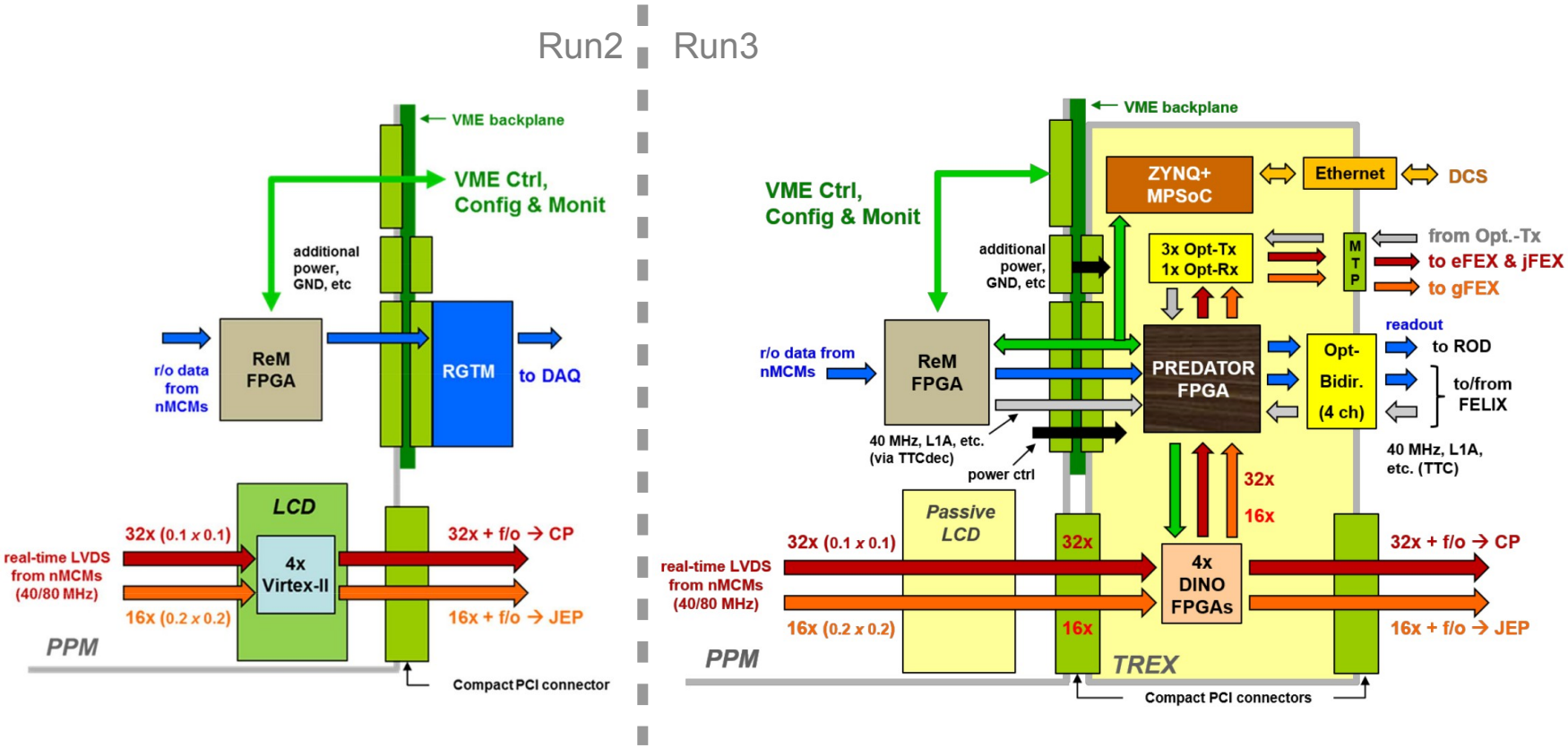
- Three new feature identification subsystems:
  - eFEX: Identification of isolated e/γ and τ
  - jFEX: Identification of energetic jets, τ and computation of energy sums
  - gFEX: Identification of trigger features requiring the complete data
- Fibre-Optic Exchange (FOX)
- New readout interface: FELIX
- Tile Rear Extension Module (TREX)



PPM and TREX

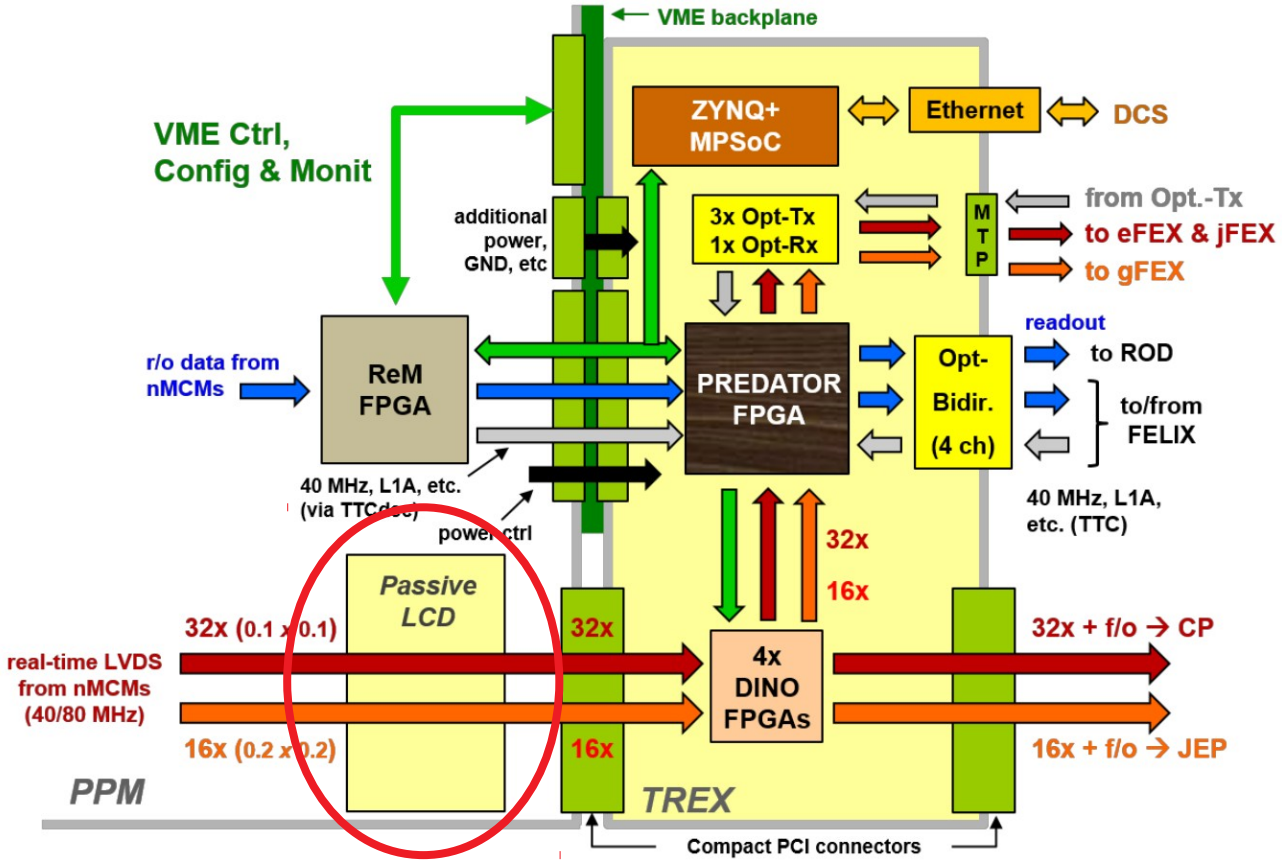

12946
12953
12375
12406
12380
12426
10313
12283
12310
12334
12335
12337
12338
12339
12345
PPM
CP
pLCD1.0
TOP
JP
VME BACKPLANE
T
T
T
T
B
R
passive LCD
TREX [prototype]

Functional Overview



Functional Overview Run3

- **pLCD**
- DINO FPGAs
- PREDATOR FPGA
- FireFlys
- ZYNQ+ MPSoC

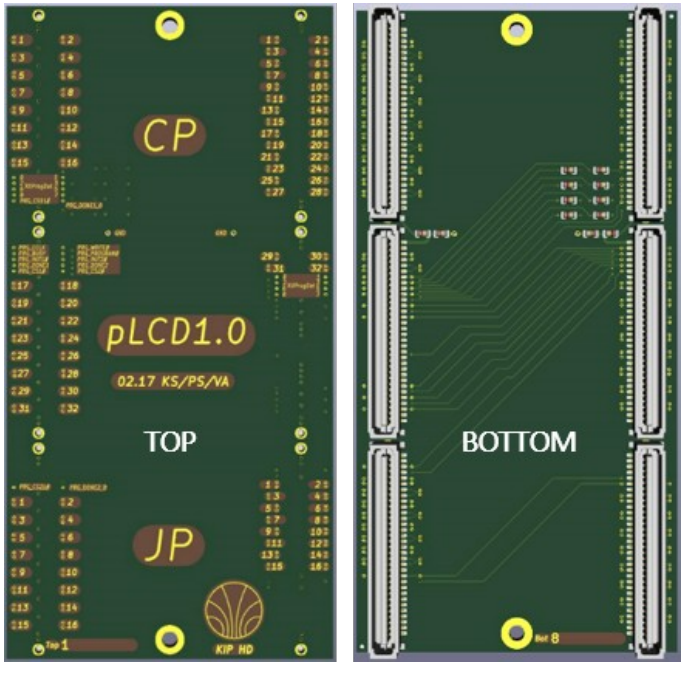


pLCD

- In Run 2: Duplication and transmission to CP/JEP on the LCD card

- In Run 3: Duplication and transmission to CP/JEP and FEXs on the TREX module
  - Possibility to double the data rate to 960 MB/s (after decommissioning of CP/JEP)
  - LCD not capable of this speed!

- Passive LCD card (pLCD)
  - Simple PCB as a passive bridge
  - Extension of the VME programming interface



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- **DINO FPGAs**
- PREDATOR FPGA
- FireFlys
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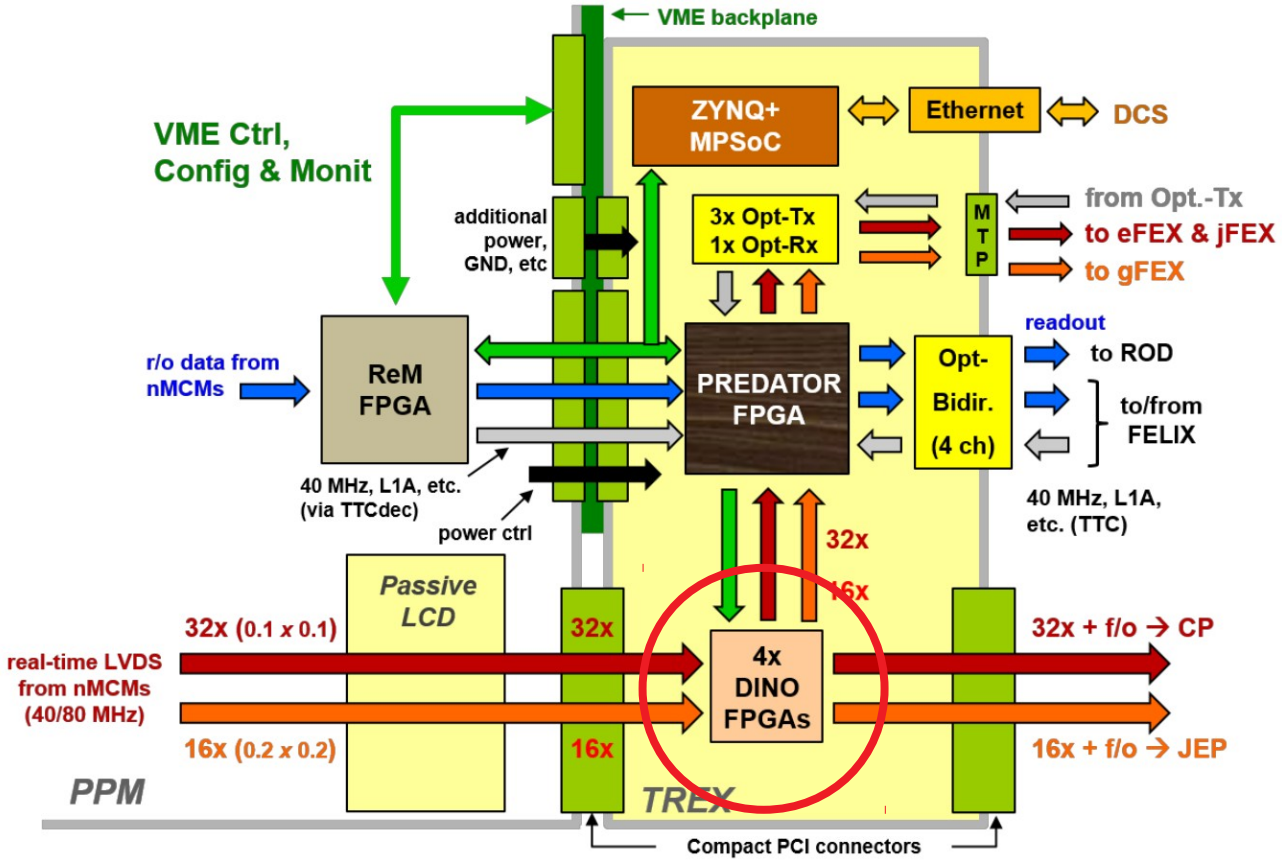
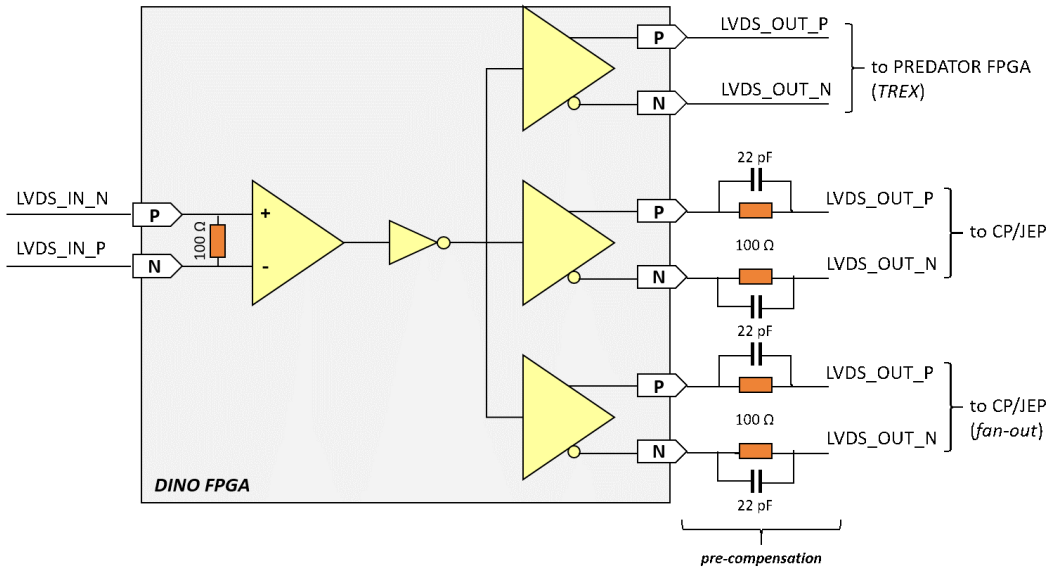
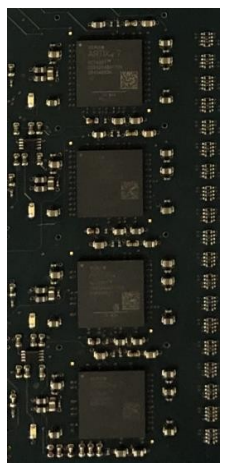


DINOs

- “LVDS **D**ata **In**-**O**ut”
- Xilinx Artix-7 XC7A35T
- Main task:
  Duplication and transmission to CP/JEP & new system
  - 48 diff. input signals
  - 121 diff. output signals
    - 40 to CP
    - 33 to JEP
    - 48 to new system

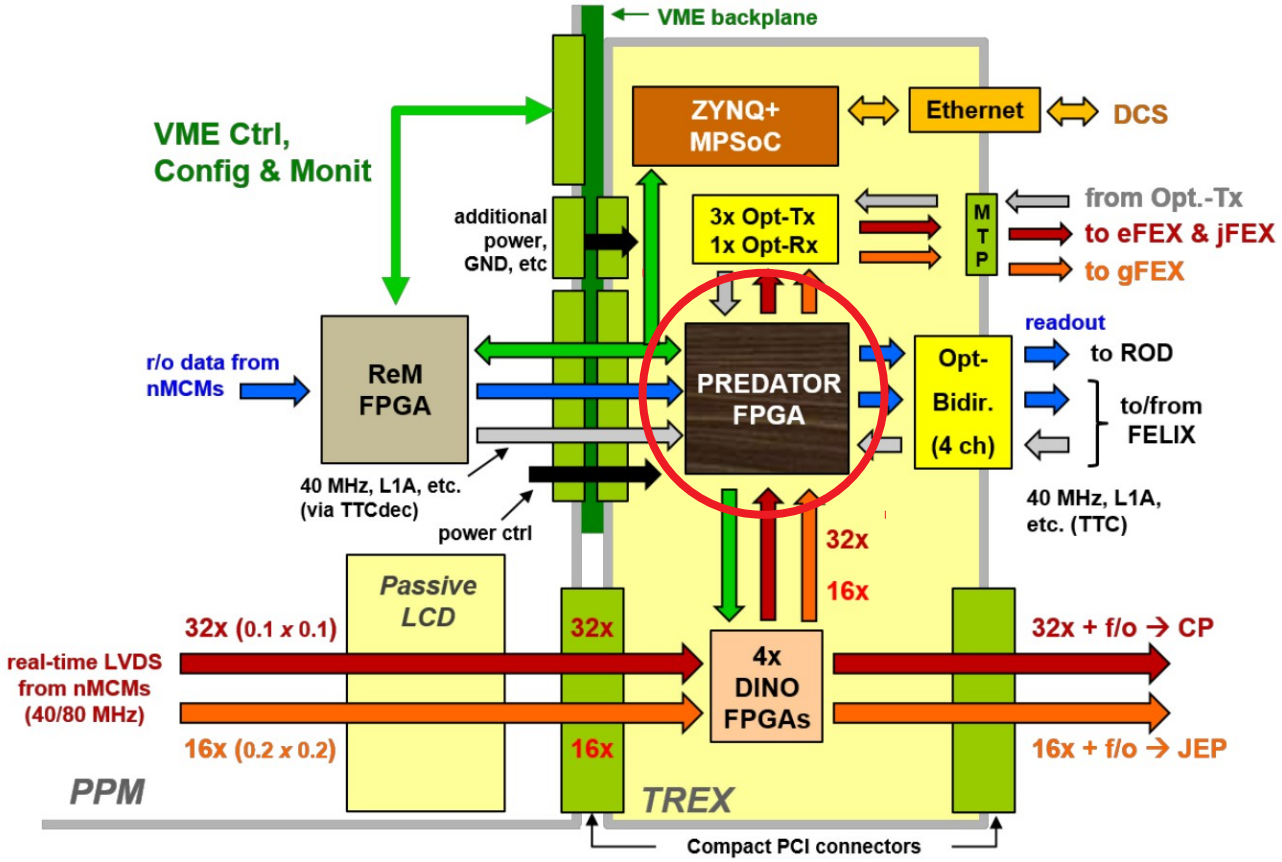


- Pre-Compensation of the signal losses due transmission
- Transmission via 11m long electrical cables to the legacy system



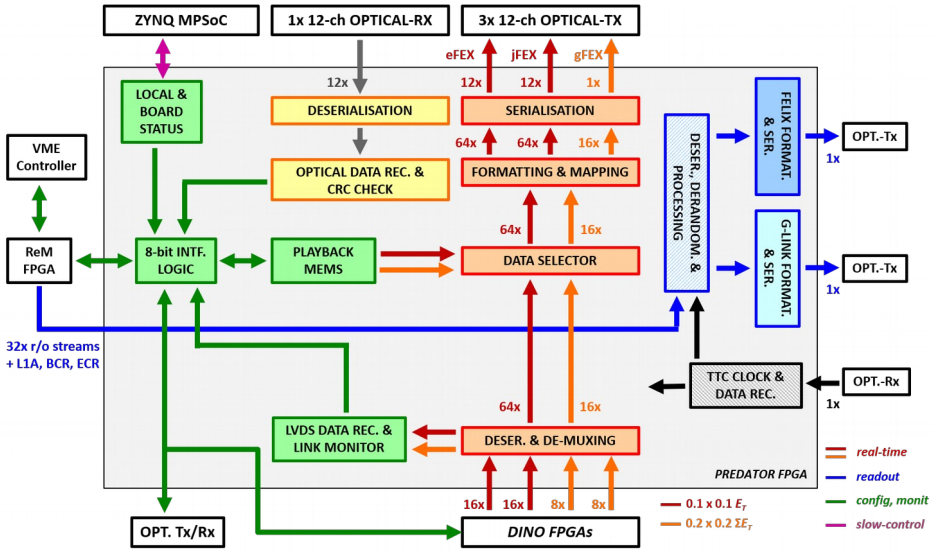
Functional Overview Run3

- pLCD
- DINO FPGAs
- **PREDATOR FPGA**
- FireFlys
- ZYNQ+ MPSoC



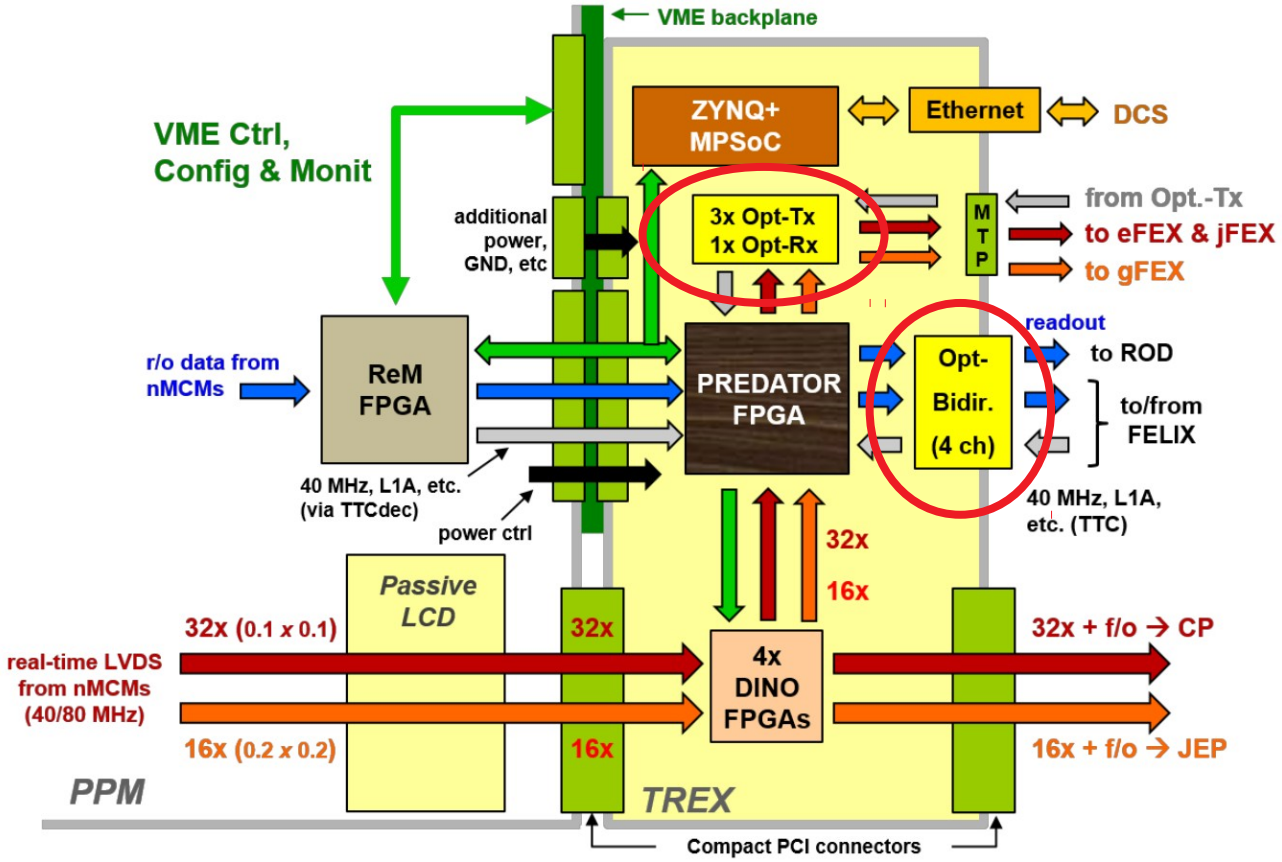
PREDATOR

- “**Pre**Processor **Data** Collect**or**”
- Xilinx Kintex UltraScale XCKU085
- Central processing unit on TREX
- Real-Time Data Path:
  - 48 diff. input signals from DINO
  - Convertion of diff. signals to single-ended format
  - Deserialization, duplication & formatting
  - Serialization & transmission to each FEX system via optical fibres
- Readout Data Path:
  - 32 serial links from nMCMs
  - Deserialization, buffering & formatting
  - Transmission to ROD & FELIX via optical fibres



Functional Overview Run3

- pLCD
- DINO FPGAs
- PREDATOR FPGA
- **FireFlys**
- ZYNQ+ MPSoC



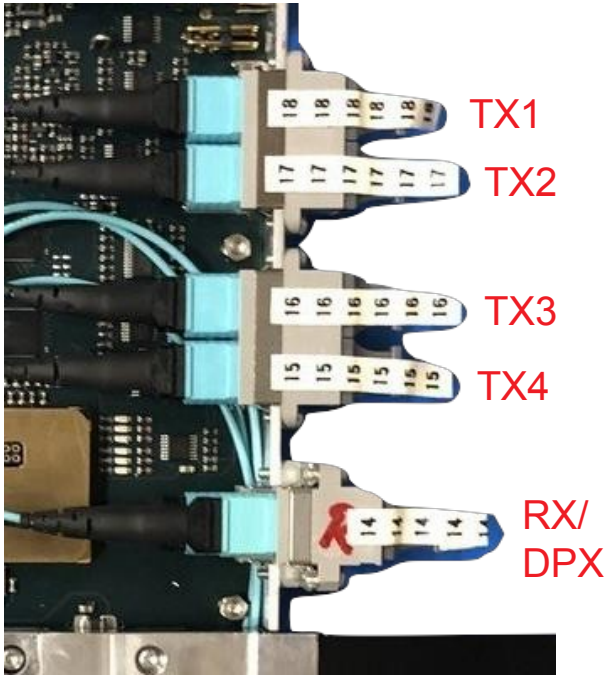
FireFlys

- FireFly modules coupled to 12-way male MTP connector

- Optical Transceivers (6x)
  - Samtec FireFly ECUO
  - (4x) 12-channel transmitters
  - (1x) 4-channel Duplex transceiver
  - (1x) 12-channel receiver (only for tests)

- FireFlys:
  - Realtime: Transmitter to FEXes
  - Readout: Transceiver to FELIX & ROD

Label	FireFly Device	Used Links	Link Rate (Gbps)	Destination	Source
Tx1	12-ch transmitter	12	11.2	eFEX	-
Tx2	12-ch transmitter	12	11.2	jFEX	-
Tx3	12-ch transmitter	1	11.2	gFEX	-
Tx4	12-ch transmitter	-	11.2	e/j/gFEX	-
Rx	12-ch receiver	12	11.2	-	TREX
DPX	4-ch transmitter	1	0.8	ROD	-
		1	9.6	FELIX	-
	4-ch receiver	1	4.8	-	FELIX



Functional Overview Run3

- pLCD
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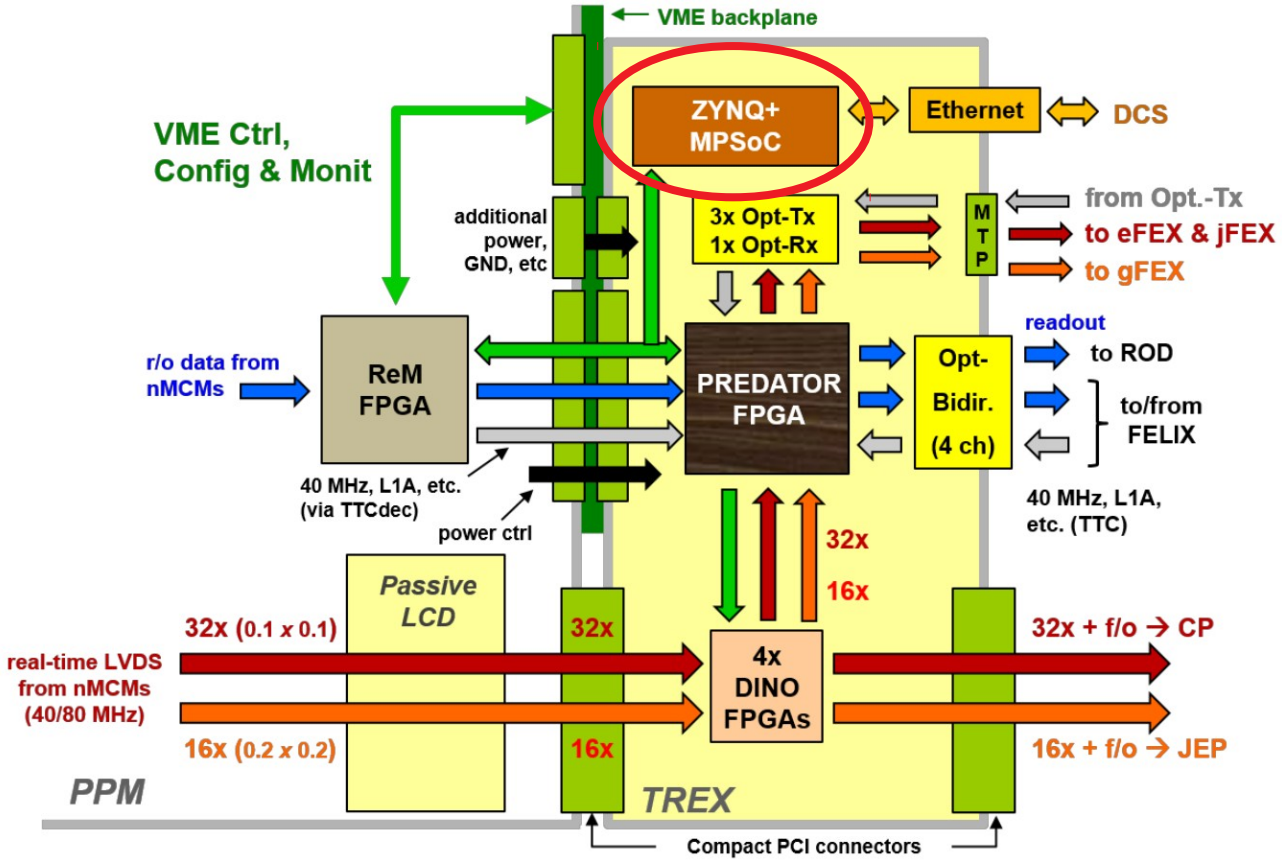
- FireFlys
- **ZYNQ+ MPSoC**

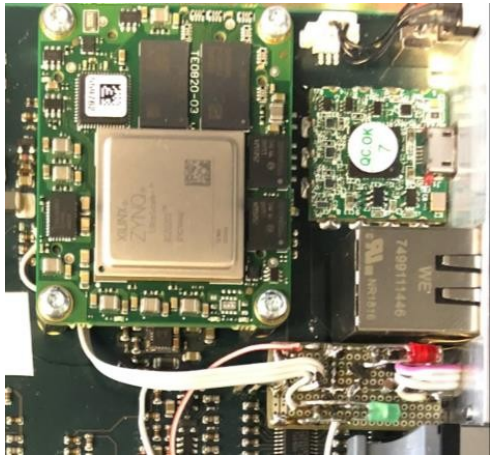


ZYNQ Ultrascale+

- Xilinx Zynq UltraScale+ (ZU3CG-1SFVC784E) MPSoC device

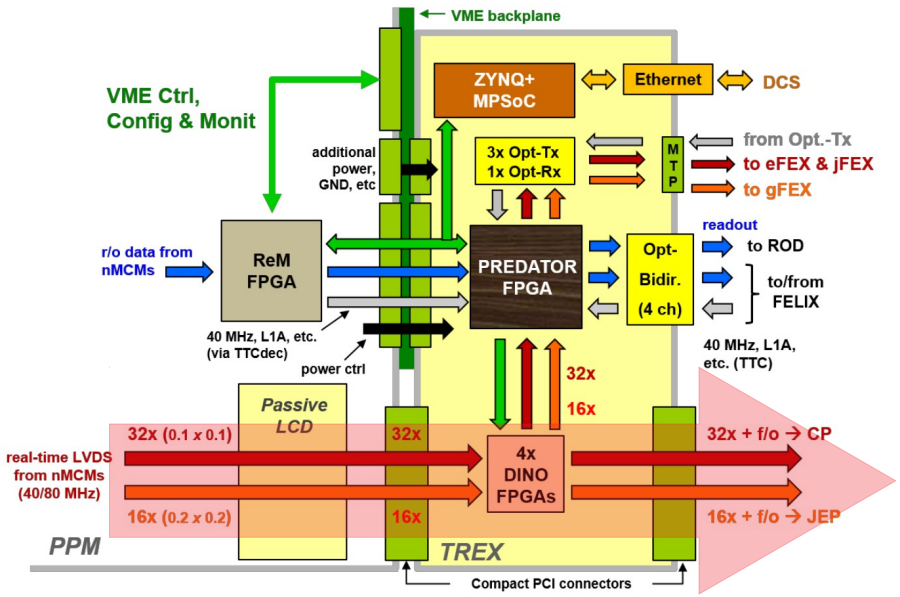
- Commercial pluggable module from Trenz Electronics

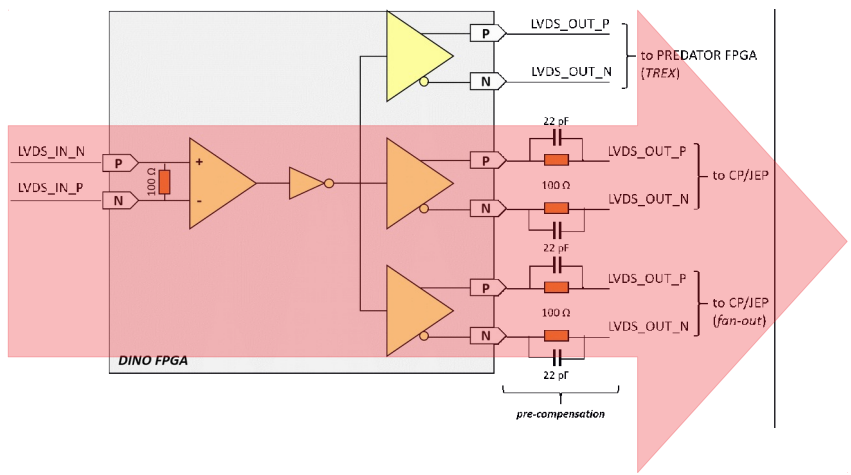
- Task: Slow control (DCS)
  - Collection of periodically environmental parameters from various locations on the TREX via I2C (e.g. temperatures, voltages, currents, etc.)
  - Is being implemented in both the Programmable Logic (PL) and Processing System (PS)
  - Connection to DCS via Ethernet



Real-Time Data Path to CP/JEP

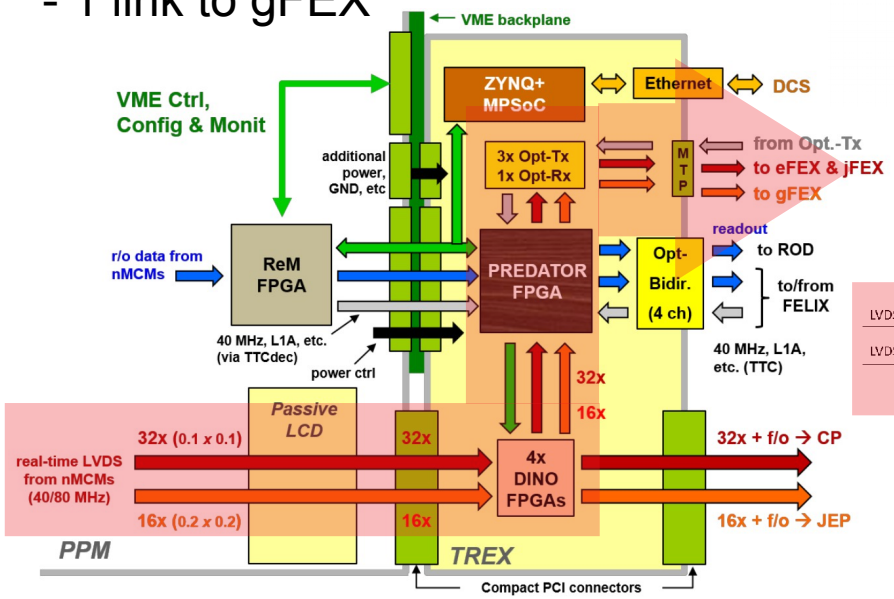
- 48 input LVDS signals
  - 32 signals: 0.1 x 0.1 E_T values
  - 16 signals: 0.2 x 0.2 jet sums
- DINO: Duplication & Transmission
  - 40 signals to CP
    (32 E_T values, 8 Fan-out E_T values)
  - 33 signals to JEP
    (16 jet sums, 17 Fan-out jet sums)

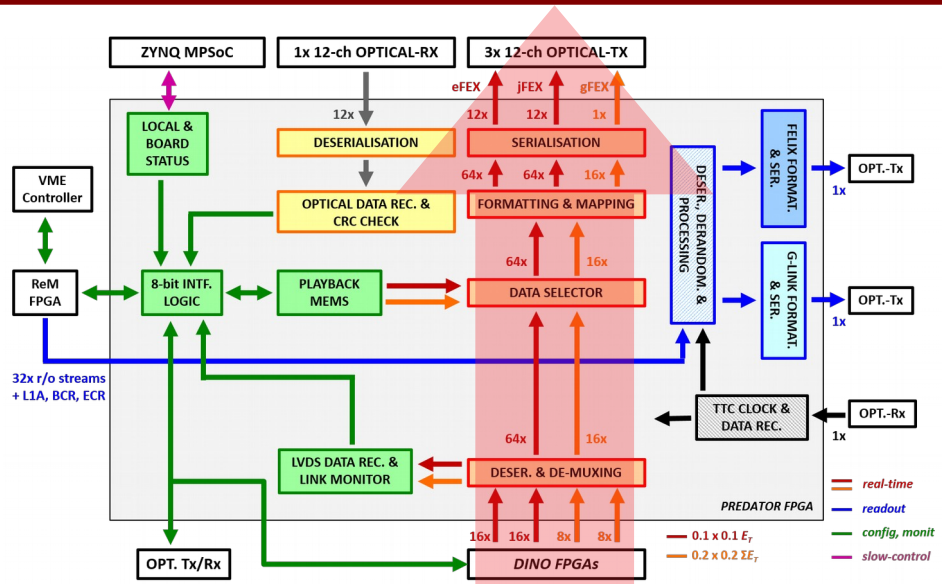


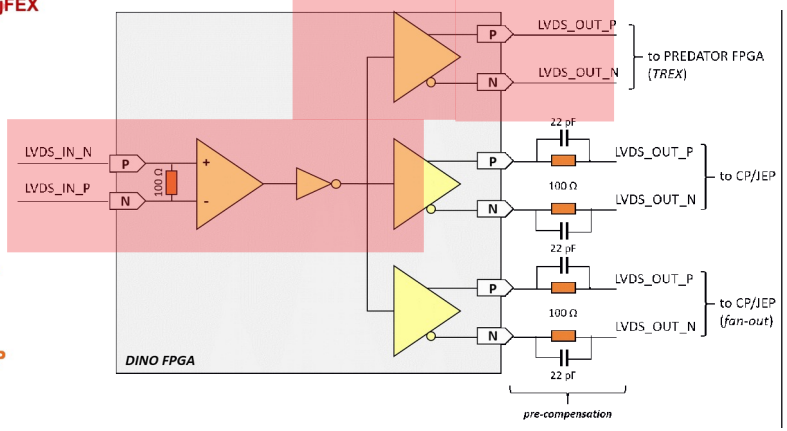


Real-Time Data Path to FEXs

- 48 input LVDS signals
  - 32 signals: 0.1 x 0.1 E_T values
  - 16 signals: 0.2 x 0.2 jet sums
- DINO: Duplication & Transmission
  - 48 signals to PREDATOR
- PREDATOR: Data Formatting
- FireFlys: Transmission at 11.2 Gb/s
  - 12 links to eFEX & jFEX
  - 1 link to gFEX

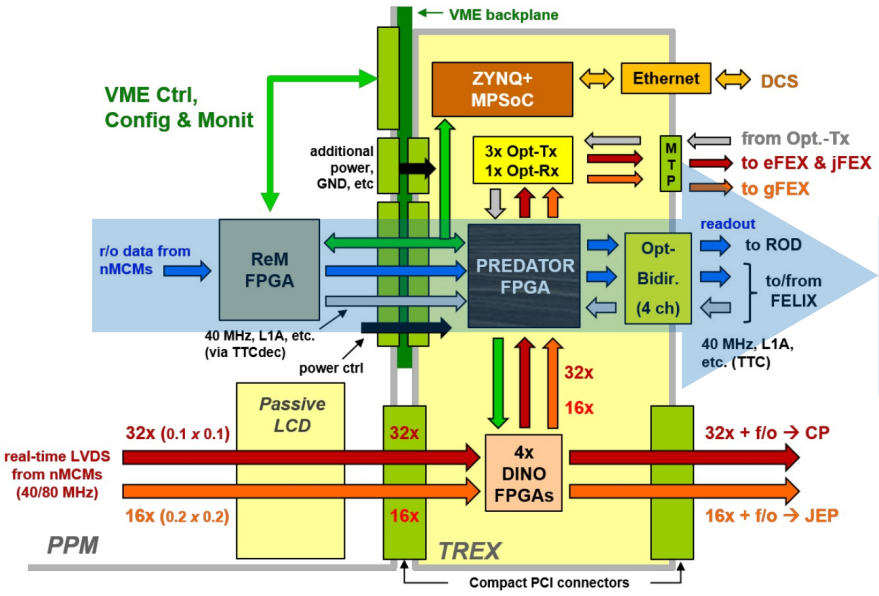


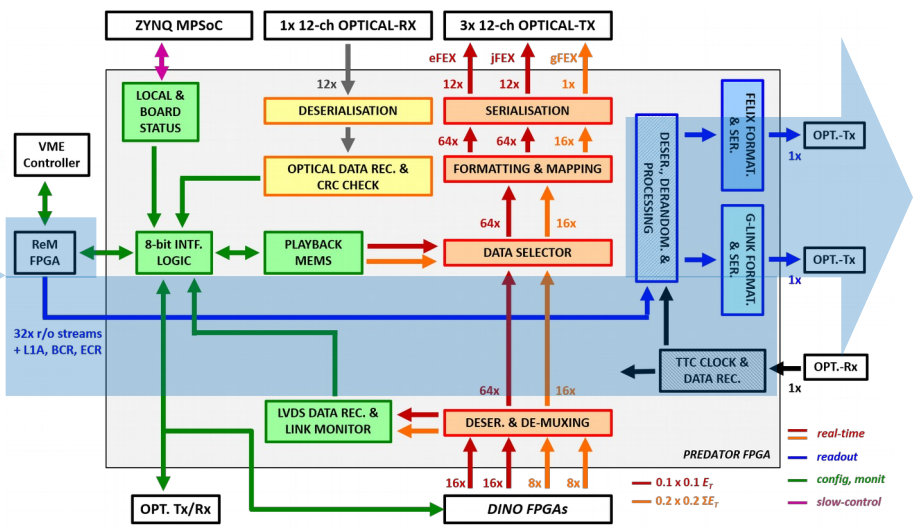




Readout Data Path

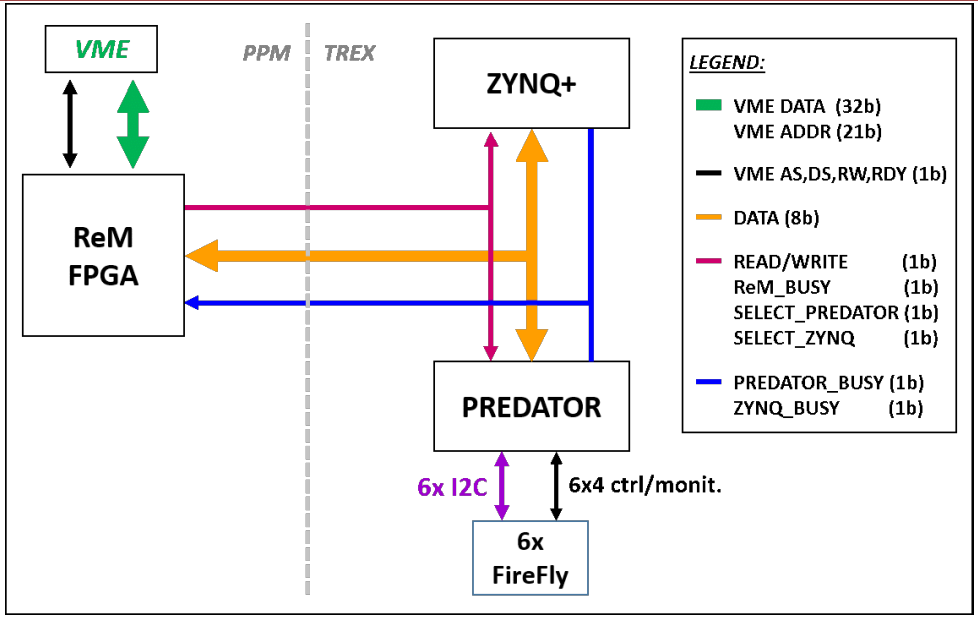
- nMCM data from the ReM FPGA through the VME backplane over 32 serial links
- TTC information (BC clock, L1A, etc.) from ReM FPGA or FELIX
- PREDATOR: Processing & Formatting
- FireFlys: Transmission
  - One link running at 800 Mb/s to ROD
  - One link running at 9.6 Gb/s to FELIX

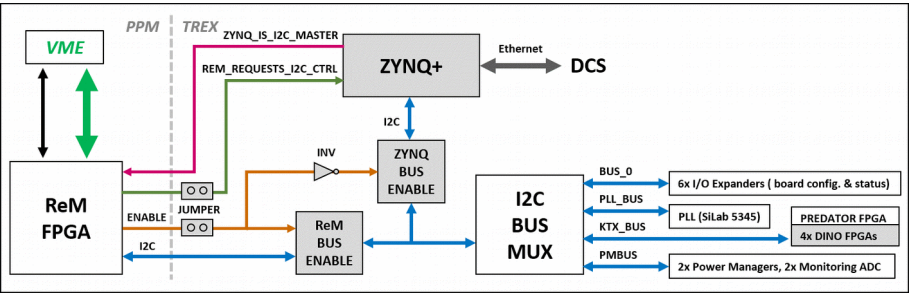




Control & Monitoring

- 8-bit Configuration Interface:
  - 8-bit bidirectional data bus
  - Six control signals for the communication
  - Between ReM and PREDATOR/ZYNQ

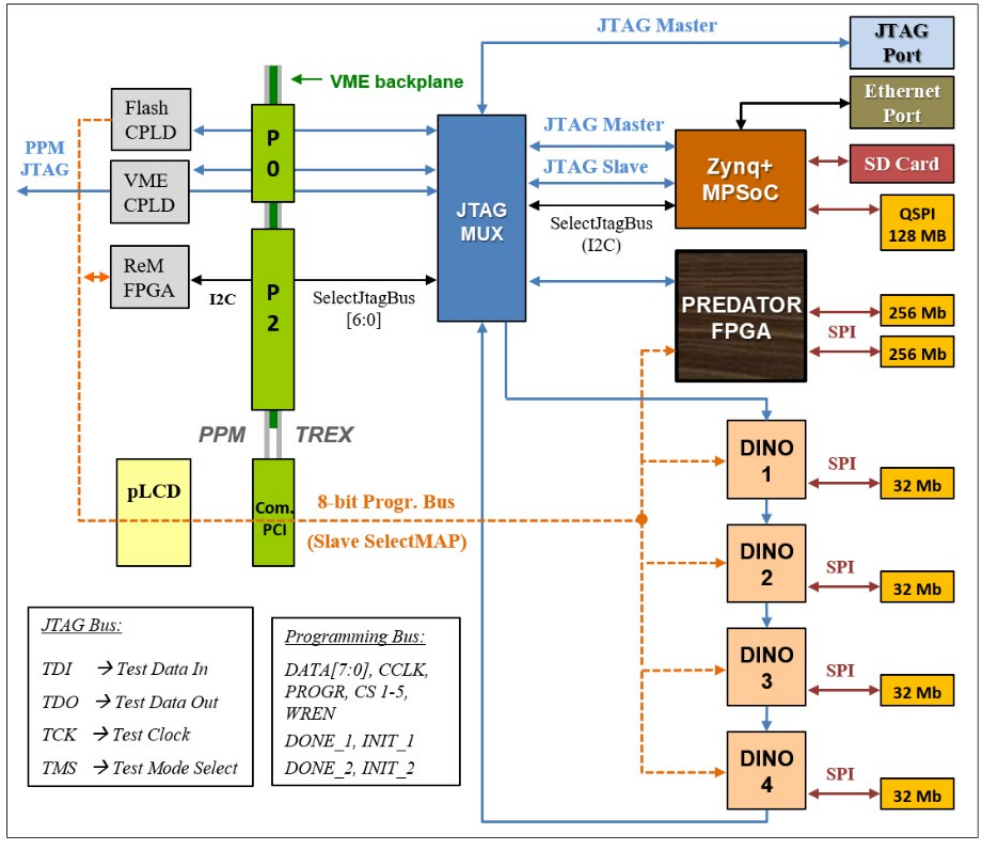




- I2C Interface:
  - Between ReM/ZYNQ and I2C devices
  - ZYNQ is master by default
  - ReM can request master via VME
  - I2C results from ZYNQ to ReM via 8-bit config interface

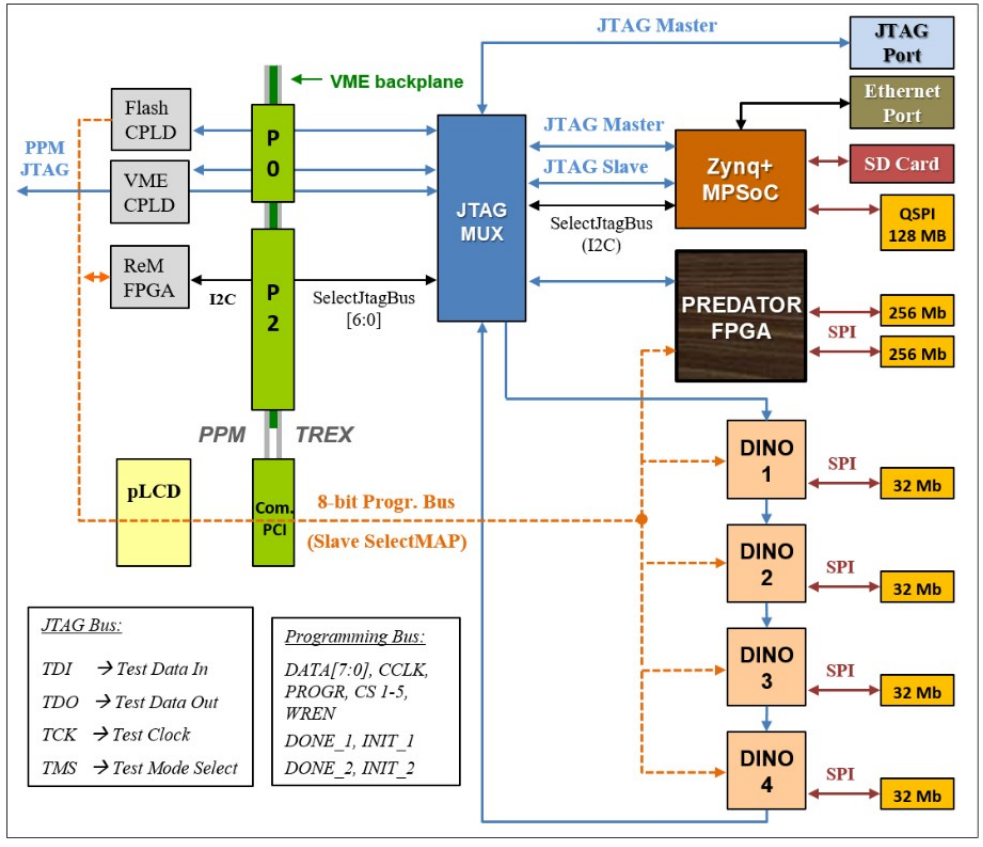
FPGA configuration

- Configuration with a bitfile
- 3 methods of configuration
  - JTAG Method
  - Slave SelectMAP Method
  - Master SPI Method



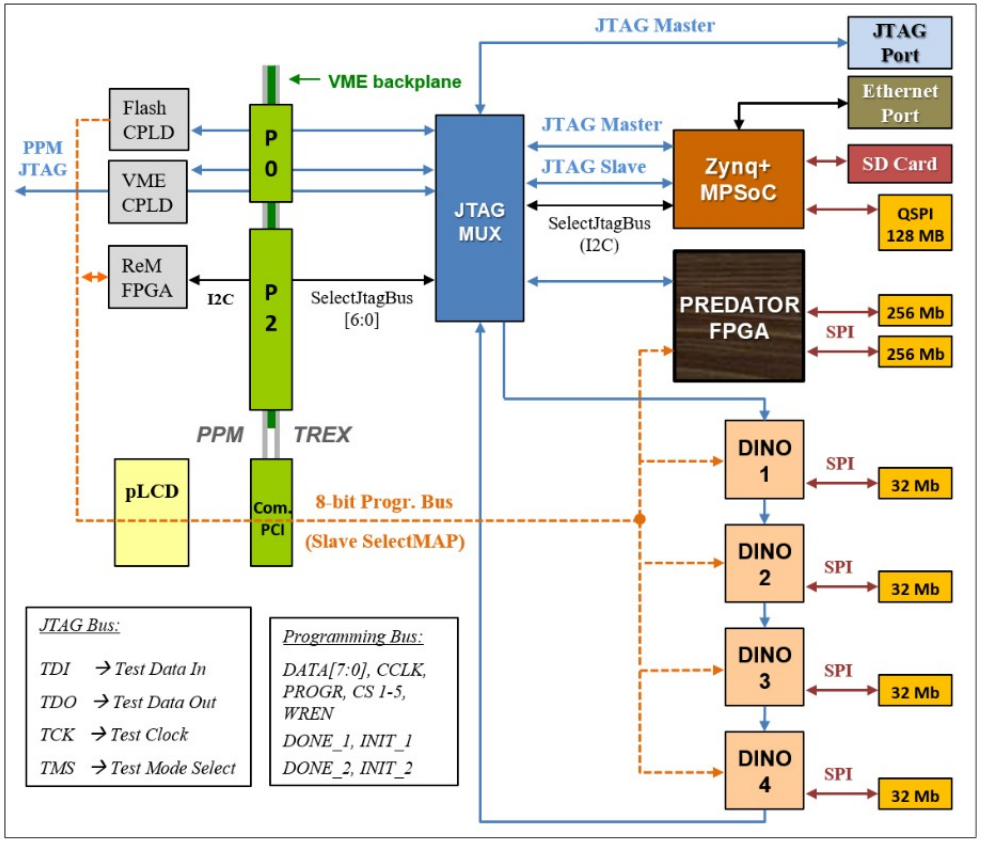
JTAG Method

- Access via micro-USB connector
- For use in the test-rig
- Fast configuration of FPGAs and SPI memories
- Debugging purposes



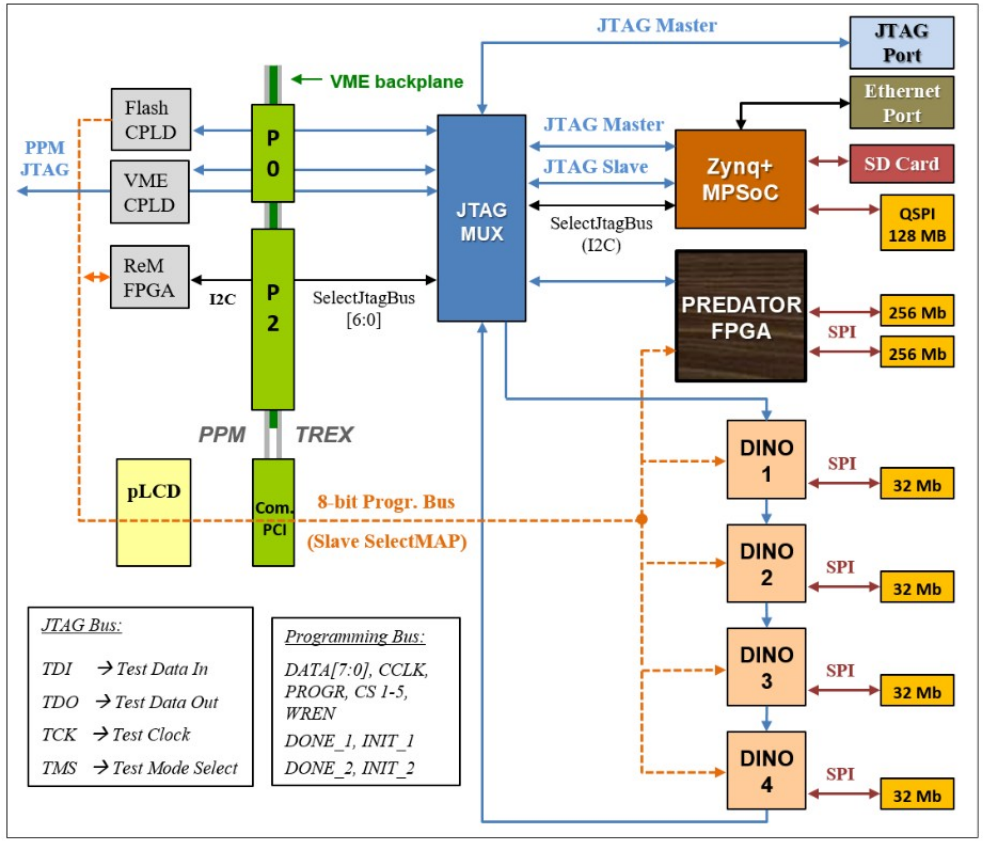
Slave SelectMAP Method (File Mode)

- Access via VME
- For use in test-rig and USA15
- 8-bit programming interface
- Routed through PPM



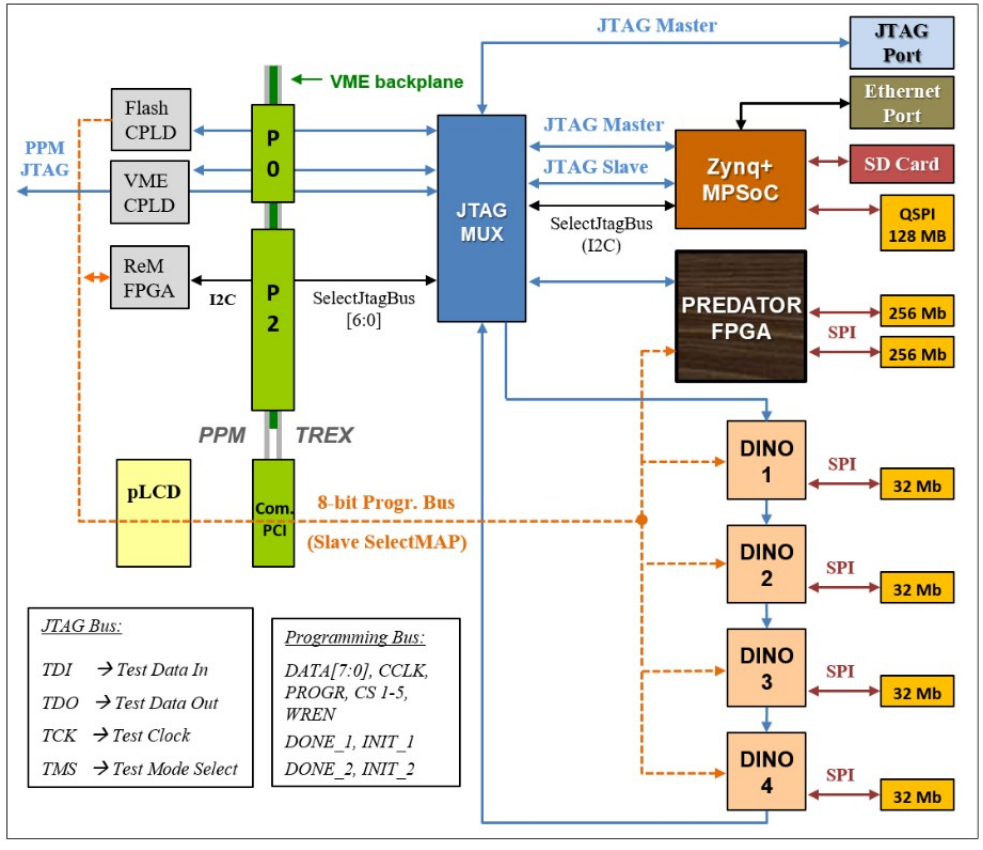
Master SPI Method (Flash Mode)

- Activation via VME
- For use in test-rig and USA15
- Fast configuration of FPGAs with binaries stored in SPI memories
- Target method
- Configuration of SPI memories only via JTAG possible



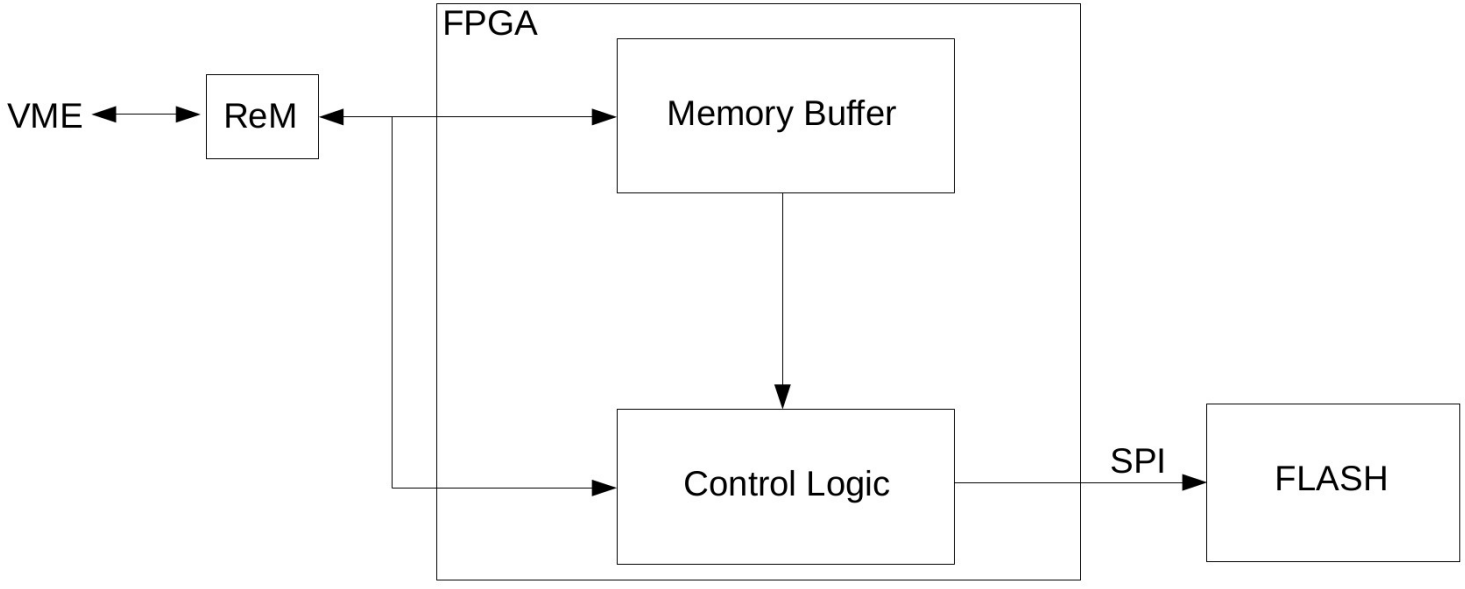
Qualification task: VME config of the SPI memories

- Use Slave SelectMAP method to update SPI memories
- Important to use Master SPI method in USA15



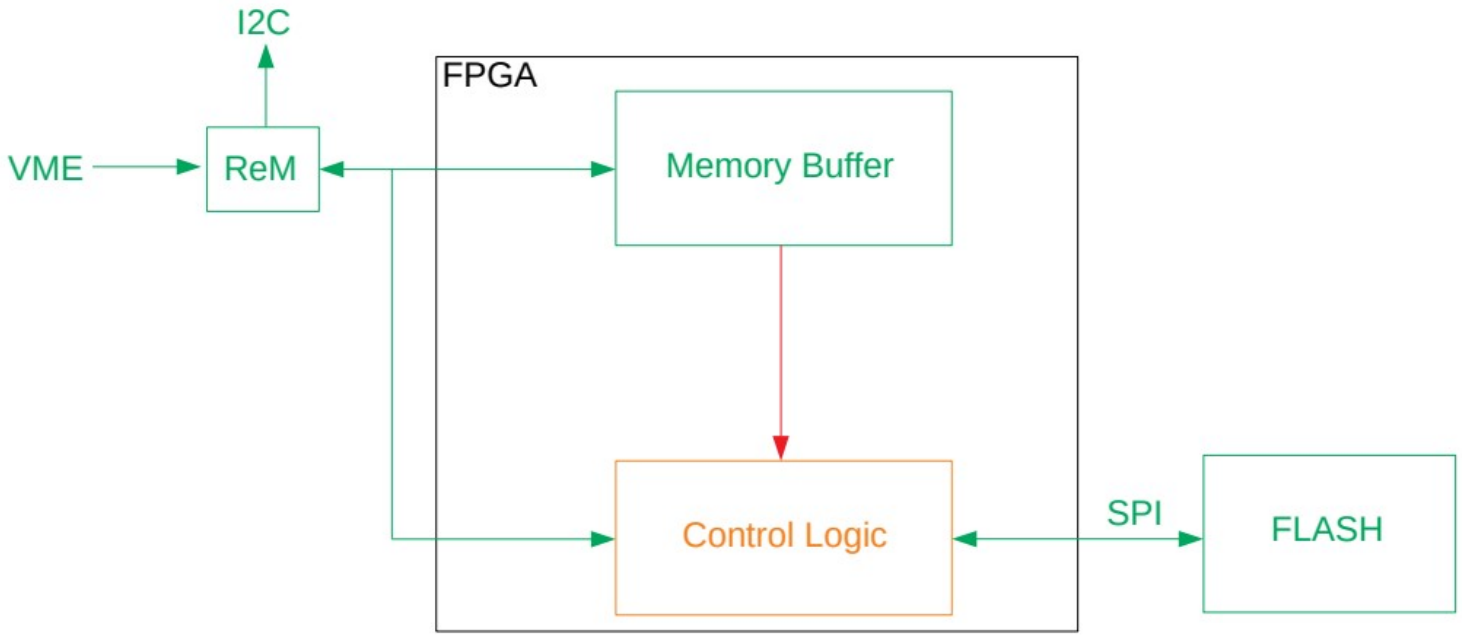
Qualification task: Firmware design idea

- Write bytewise into memory buffer module
- Send read command to control logic
- Write into FLASH
- Adapt the firmware code from the CALIPPR firmware design



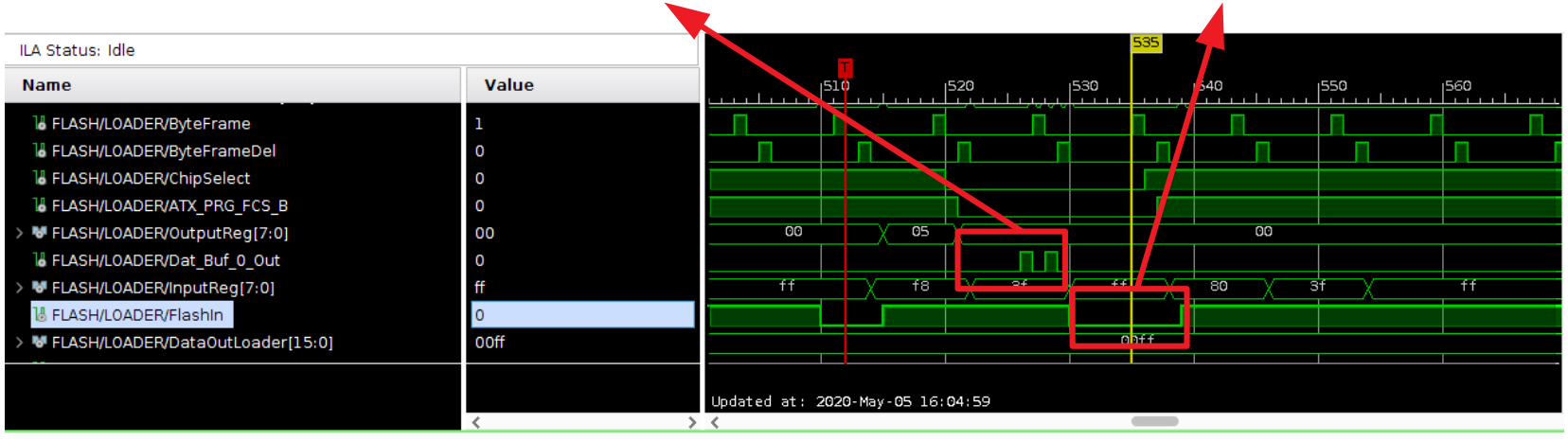
Qualification task: Current development status

- Memory buffer module implemented into DINO design
- I2C readout instead of VME
- Tested succesfully with SW
- Implementation of write & read of WriteEnable status bit

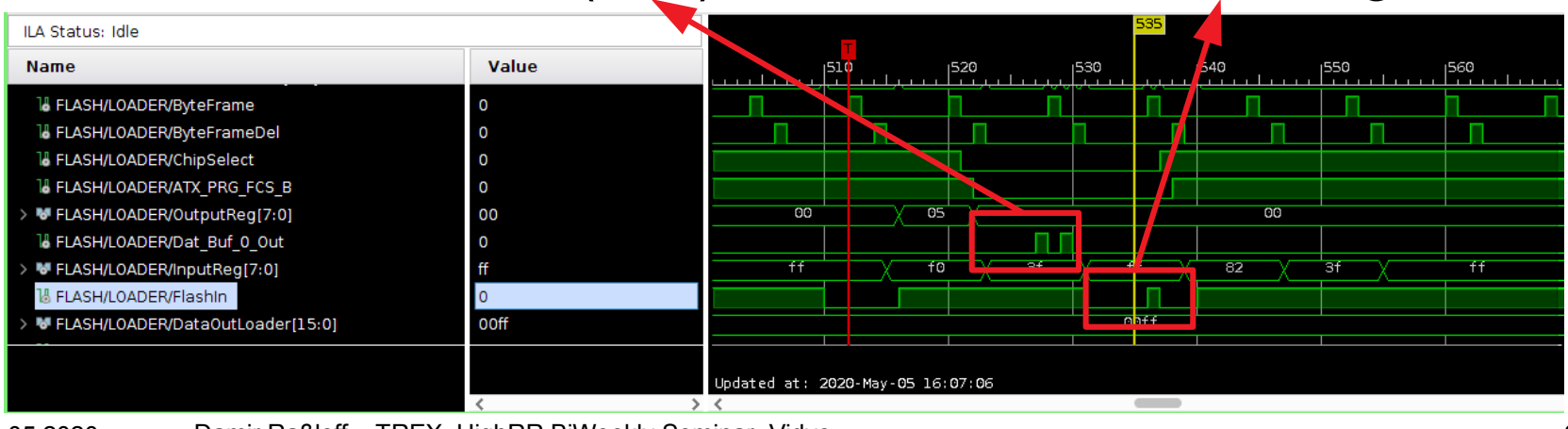


Qualification task: Write & Read WriteEnable Status bit

Command Read: 0x05 (101) WriteEnable Status Register = 0

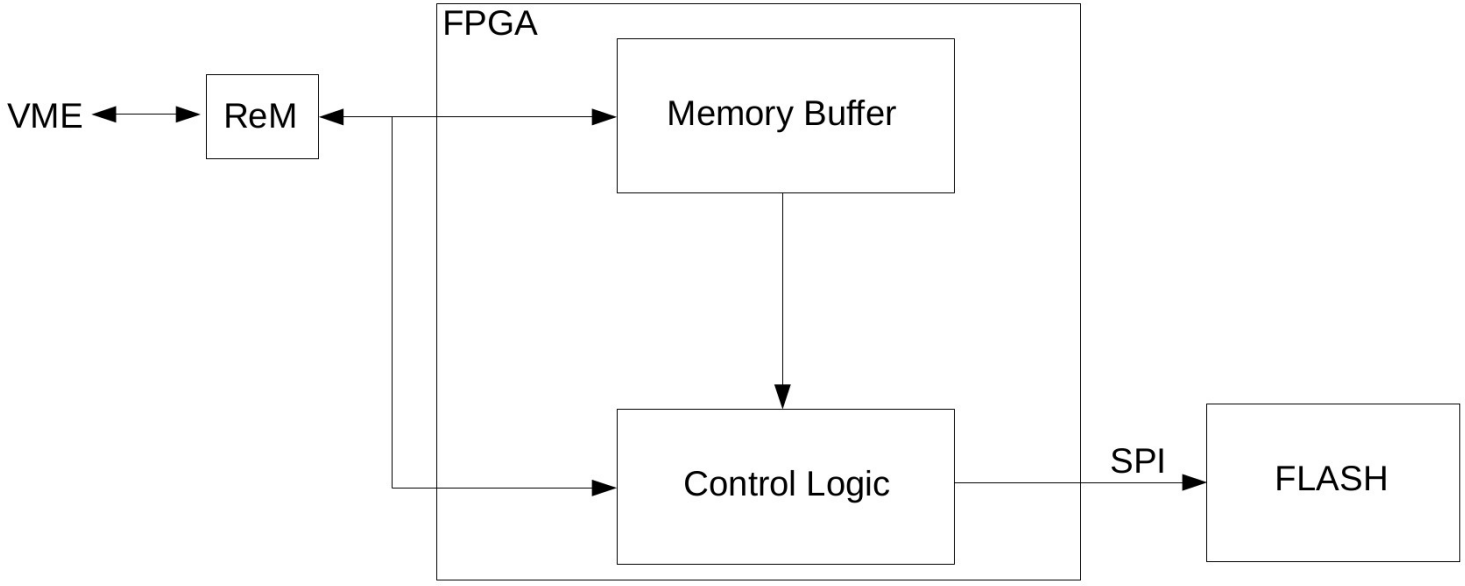


Command Read: 0x05 (101) WriteEnable Status Register = 1



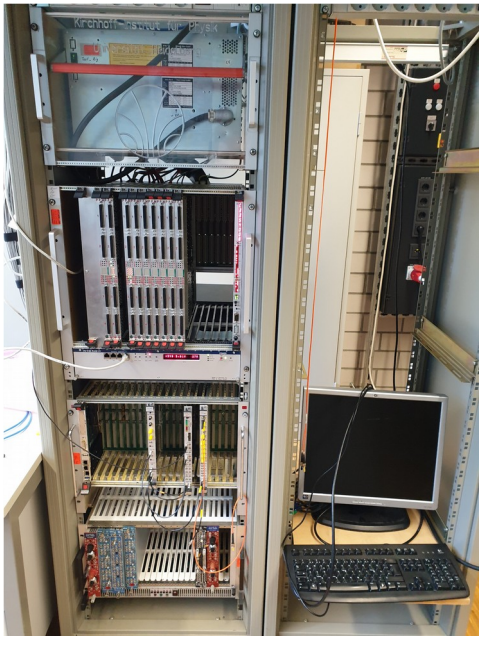
Qualification task: Next steps

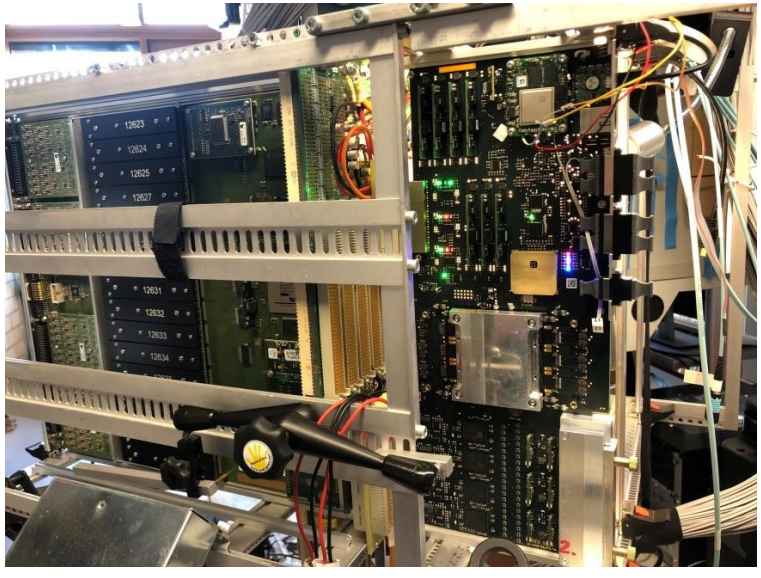
- Development & tests of the control logic
- Tests with the whole design
- Implementation for the other FPGAs



Tests at Heidelberg

- Single-board testbench:
  - Custom VME crate
  - Homebrew VME crate controller (i7 CPU, Universe-II)
  - Initial tests and power-up (e.g. LVDS transmission)

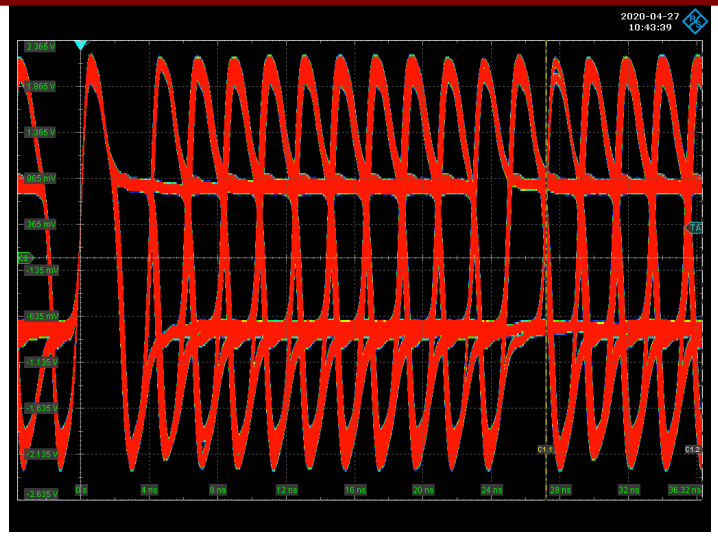




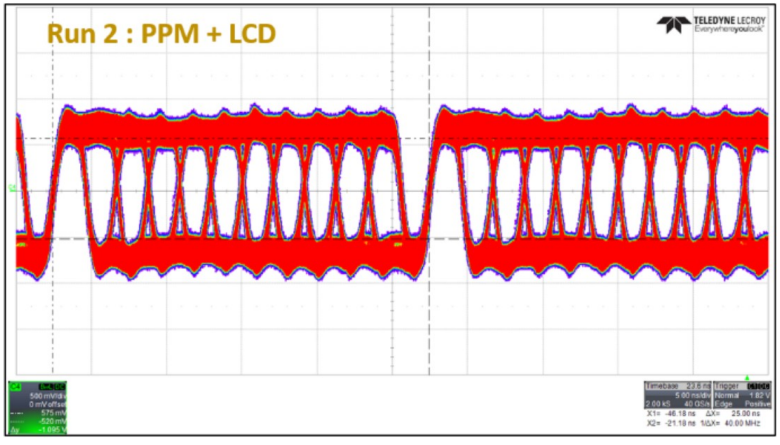
- Multi-board testbench:
  - Wiener crate with TREX modifications
  - Concurrent Technologies VME crate controller
  - Emulates crate setup at CERN
  - Long-term tests (e.g. Thermal test)

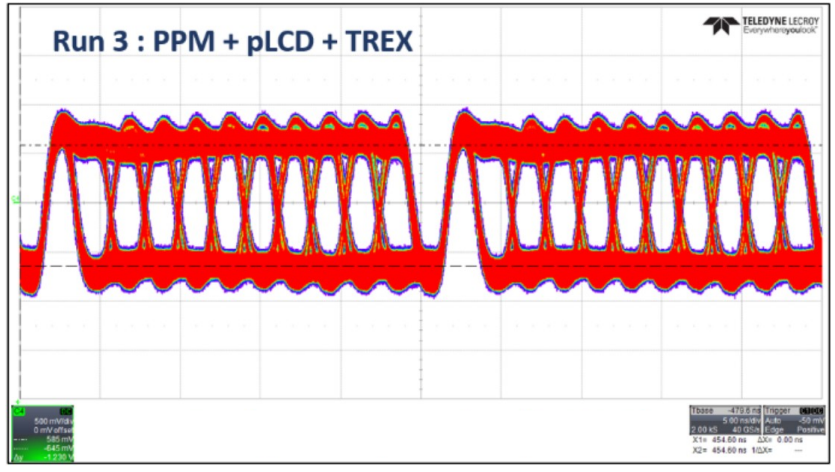
LVDS transmission to CP/JEP

- LVDS signal quality check before and after a 15m cable (in USA15 around 11m) using an oscilloscope
- Good results on prototype and pre-production module
- Similar results with Run2 system



Test results provided by Tigran Mkrtchyan (KIP)

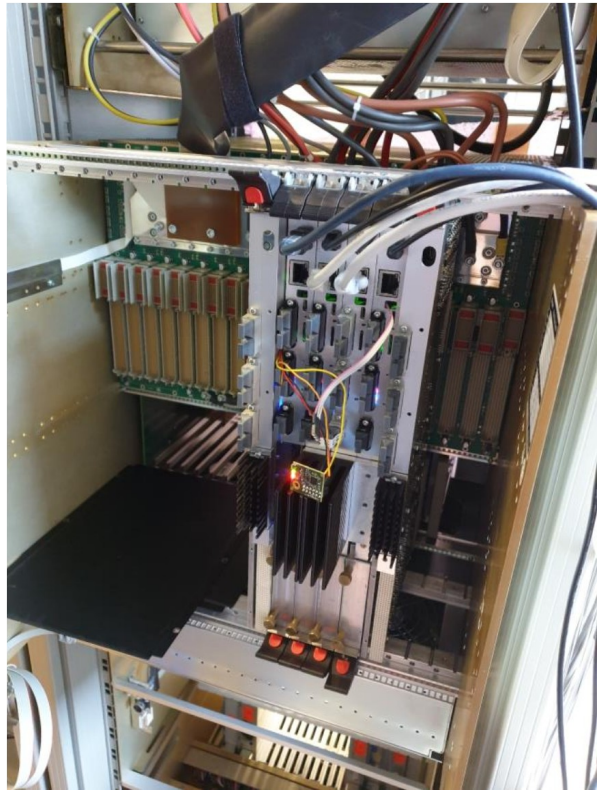




Thermal Test

- 4 active TREX modules & PPMs
  - Additional 6 passive PPMs and 2 TREX modules

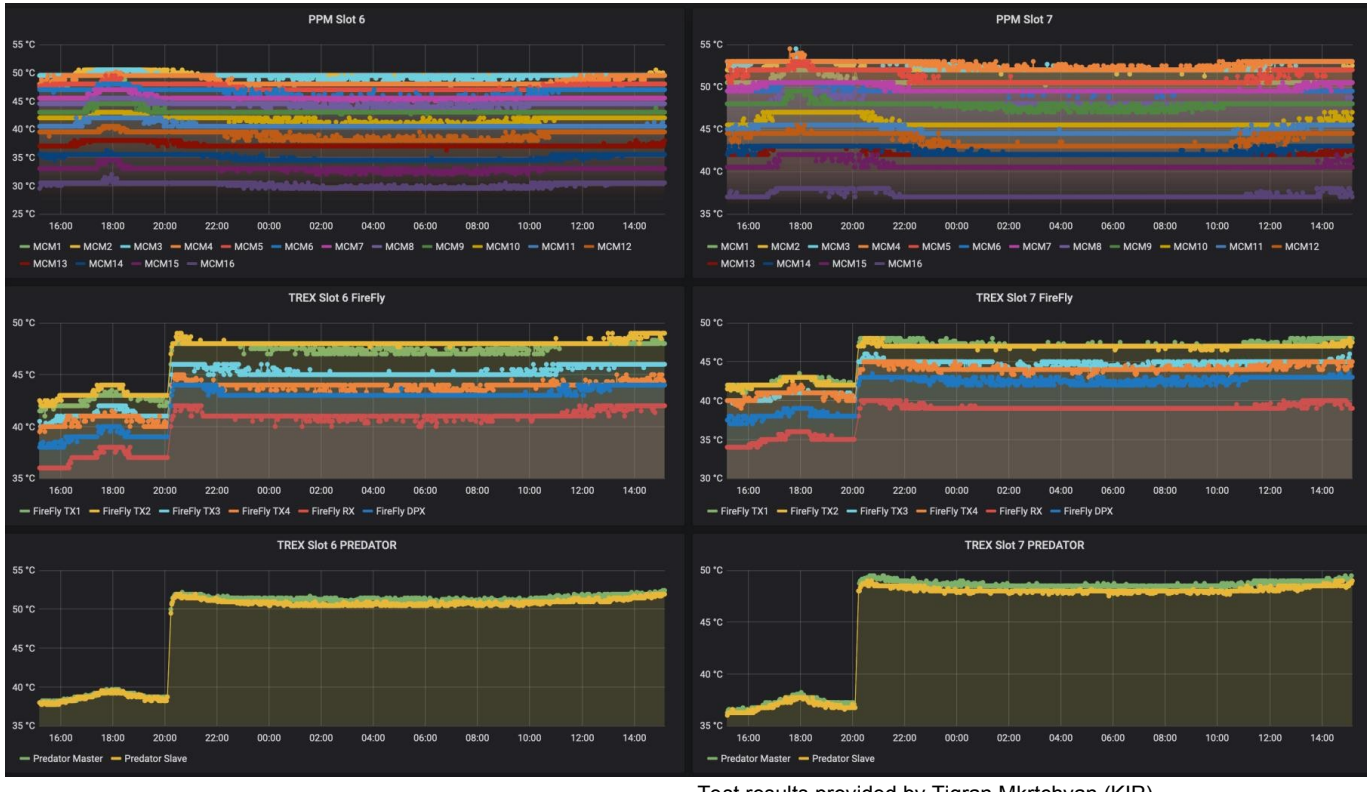
- Test duration of multiple days
  - Temperature captured every 30 seconds
  - Stored in a time series database
  - Visualization via Grafana



- Test with two PREDATOR FW designs
  - Full-load
  - Current design

Thermal Test: Results

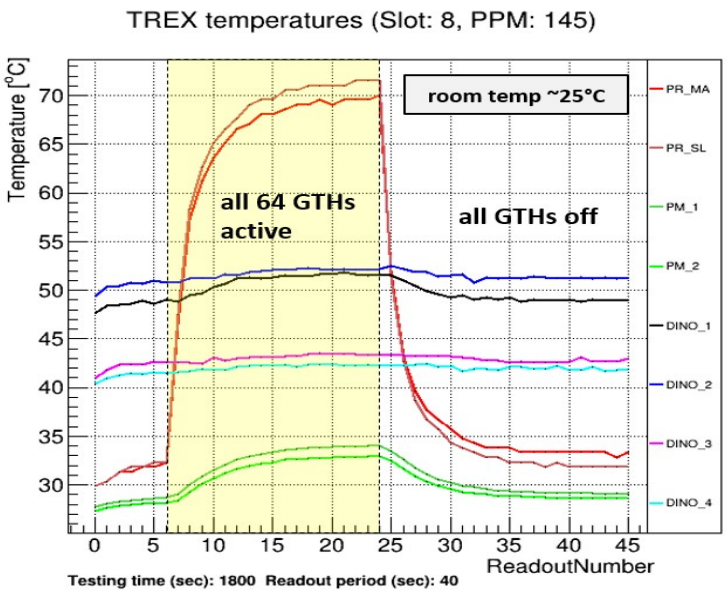
- Temperature increase during the change to the full-load FW design
- Hottest devices nMCMs on the PPM ~54°C

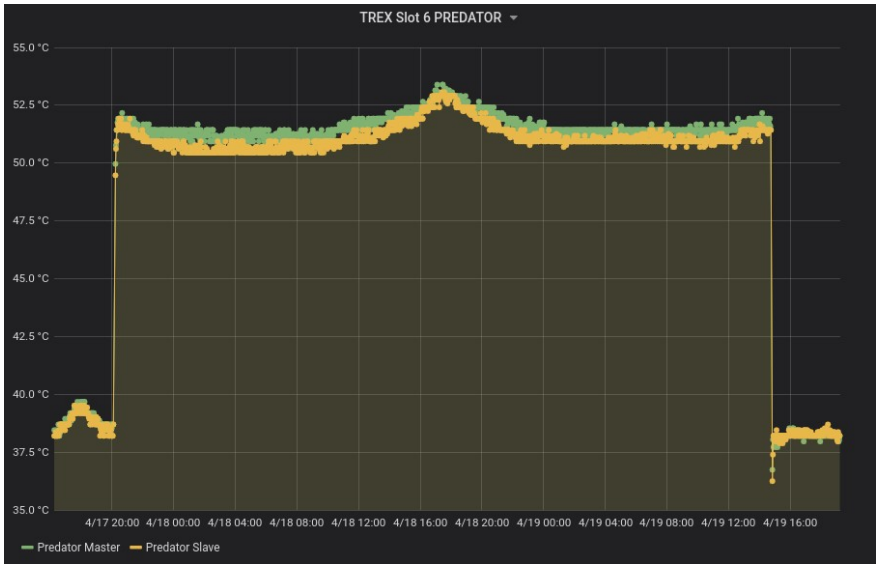


Test results provided by Tigran Mkrtchyan (KIP)

Thermal Test: Results

- PREDATOR temperature peak at < 54°C
- Comparison between prototype and pre-production: ~18°C difference
  - Improved heat sink
  - “Slimmer” FPGA (less GTHs)



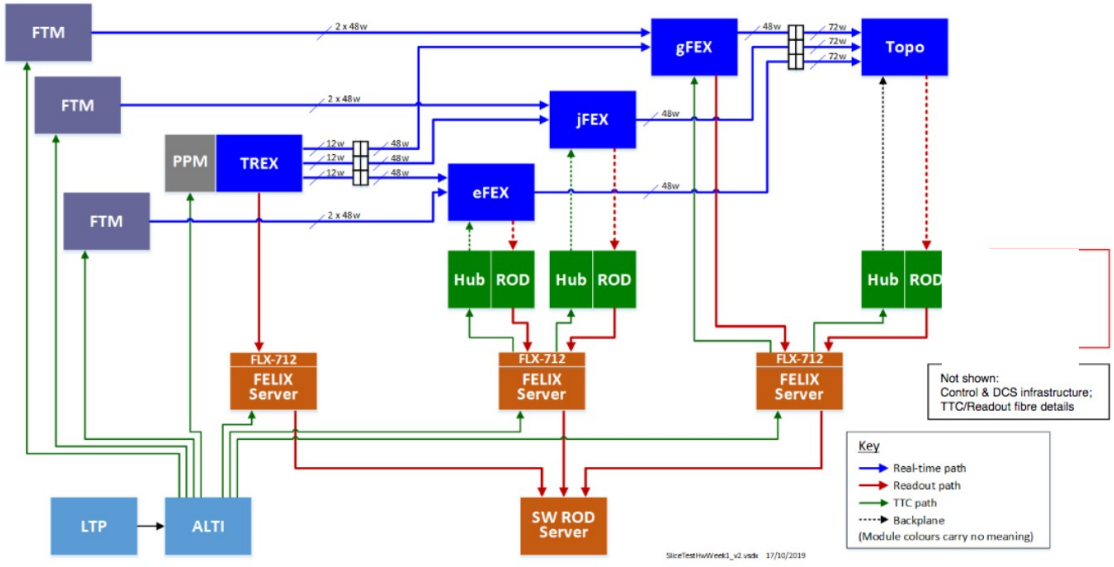


Test results provided by Tigran Mkrtchyan (KIP)

Integration tests at L1Calo Surface Test Facility (STF)

- System currently powered down

- Tests with prototype (v1) and pre-production (v2) module



- Readout path:
  - TREX (v1 & v2) to FELIX: Data transmission achieved, decoding and verification succesful

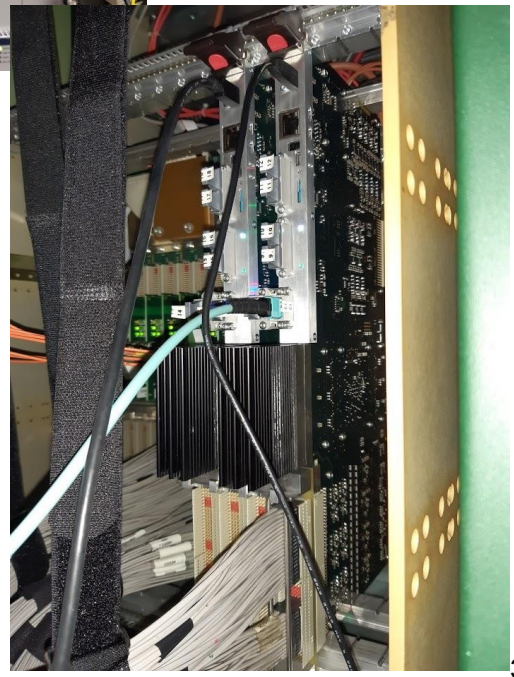
- Realtime path:
  - TREX (v1) to eFEX: Data transmission verified, no errors
  - TREX (v1 & v2) to jFEX: Data transmission verified, no errors
  - TREX (v1) to gFEX: Data transmission verified, some errors (cross-check with jFEX)

Integration tests at B. 104 (Legacy System)

- System currently powered down

- Legacy system integration tests with pre-production (v2) module

- Readout path:
  - TREX (v2) to ROD:
    - Established a stable link to the ROD
    - Data incorrect, to be investigated



- Realtime path:
  - TREX (v2) to JEP:
    - Configuration of playback data via Online SW
    - Successfully detected on JEM
  - TREX (v2) to CP:
    - To be tested

Current Status

- Production Readiness Review (PRR) last thursday (07th of May)
- HW design finished (wait for outcome of PRR)
- FW development almost done (FLASH programming, minor functions of PREDATOR, debugging & ZYNQ)
- Essential tests done with the TREX prototype (v1) & pre-production module (v2); wait for CERN power up

TREX Production & Installation Timeline			DURATION
START DATE	END DATE	DESCRIPTION	(days)
07/05/2020	08/05/2020	PRR	1
08/05/2020	22/05/2020	Preparation for Production	14
22/05/2020	12/07/2020	PCB Production	50
12/07/2020	26/07/2020	Initial board assembly [~5pcs]	14
26/07/2020	03/08/2020	Testing of initial boards	7
03/08/2020	17/08/2020	Assembly of remaining boards	14
17/08/2020	30/11/2020	Validation/QA @ KIP	103
14/10/2020	21/10/2020	Installation of the 1st batch [16 pcs] @ CERN	7
21/10/2020	31/12/2020	Testing @ CERN	70
01/12/2020	08/12/2020	Installation of the 2nd batch [16 pcs] @ CERN	7