Superconducting Electronics

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Superconducting Electronics

- **SQUIDs**
- **Voltage Standards**
- **Digital Circuits**
- **Radiation Detectors**

The International System of Units

- SI-Units -

SI: Systeme Internationale d´Unités
International System of Units:
Meter-Kilogram-Second-Ampere MKSA
(+ mol, cd, and K)

Kilogram
The PtIr Kilogram at the BIPM

Meter
Length of the path travelled by light in vacuum during
a time interval of 1/299792458 of a second

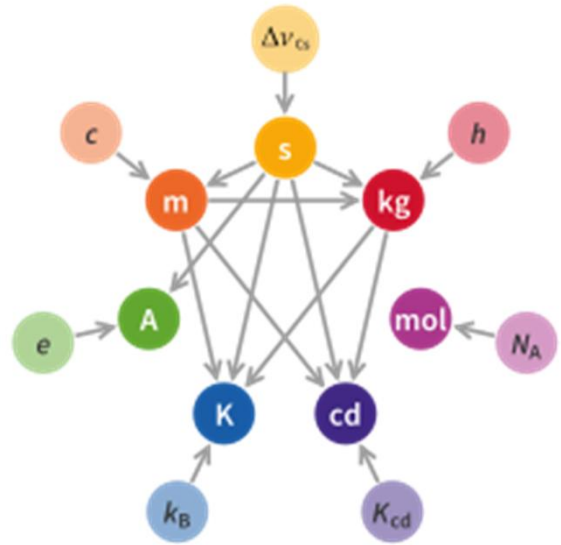
Second
9192631770 times the period of the hyperfine-structure radiation of ^{133}Cs

Voltage
Connected to SI via the voltage balance: 0.3 ppm

Current
Connected to SI via the current balance : 0.3 ppm
or traced back to Volt, Second, Meter via the calculable capacitor $I = dQ/dt = CdU/dt$

Resistance
Connected to SI via calculable capacitor $(1/\omega C)$: 0.045 ppm

New SI



The goal is to define the units through fixed universal constants
Last revision 2018

Connecting the electrical quantities

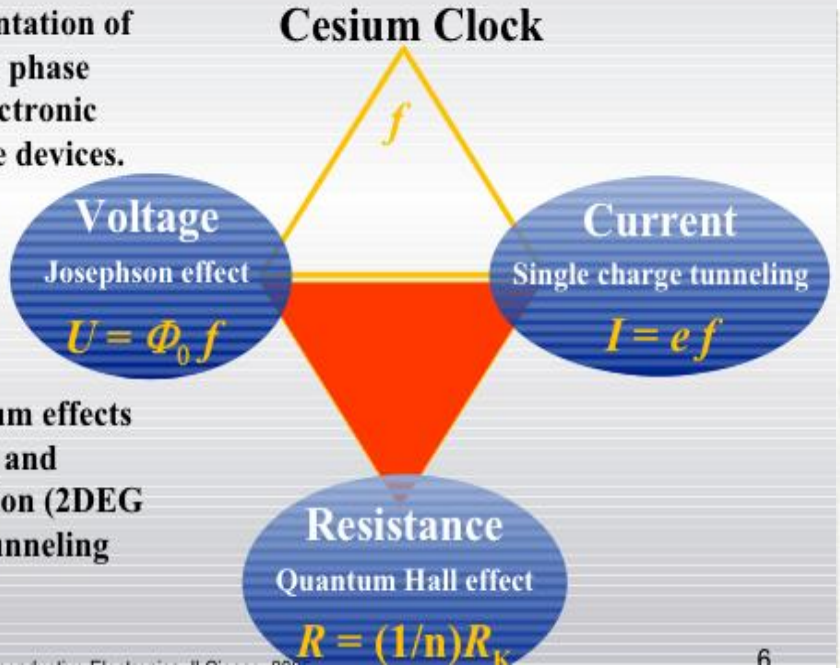
Metrological Triangle

$\Phi_0 = h/2e$: Flux Quantum; 2,06783461x10^{-15} Vs

e : Charge Quantum; 1,60217733x10^{-19} C

$R_K = h/e^2$: Resistance Quantum; 25812,8056 Ω

A quantum representation of Ohm´s law requires phase coherence of the electronic wave function in the devices.



obtained by:

macroscopic quantum effects (superconductivity) and dimensional reduction (2DEG and single charge tunneling devices)

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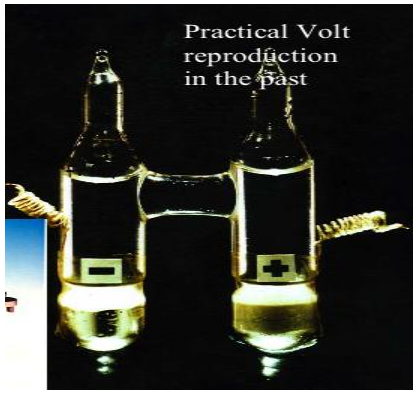
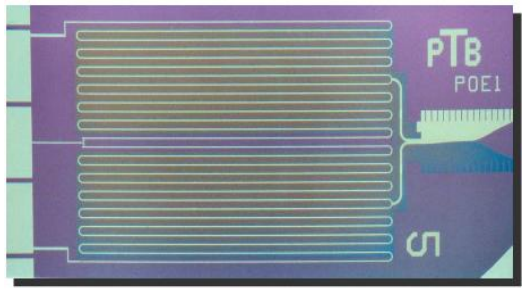
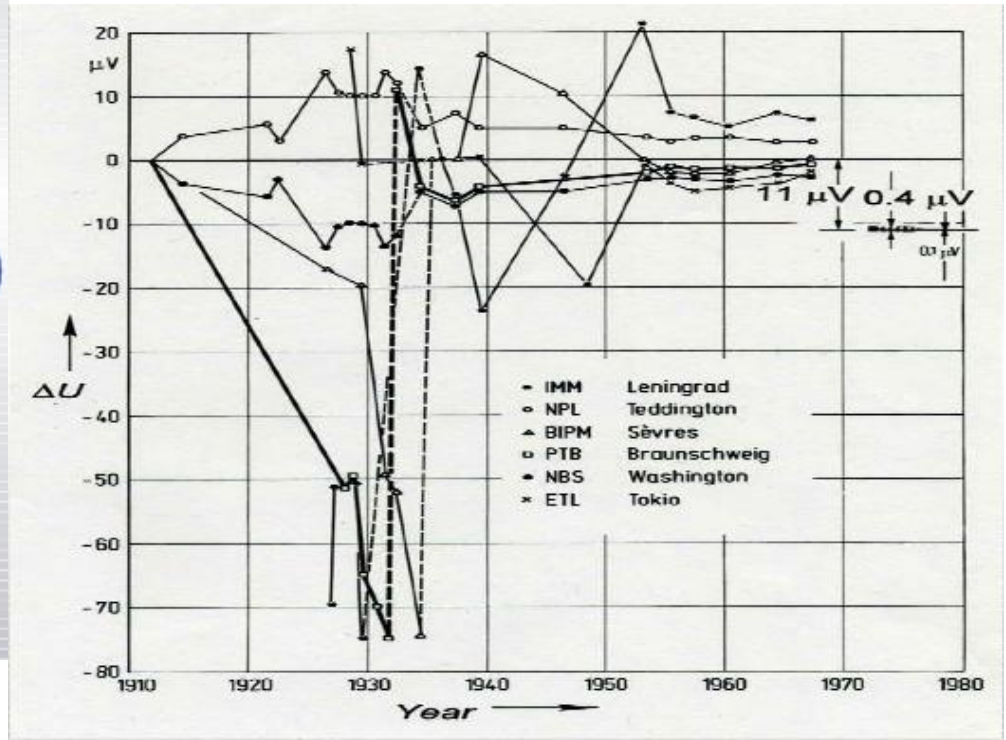
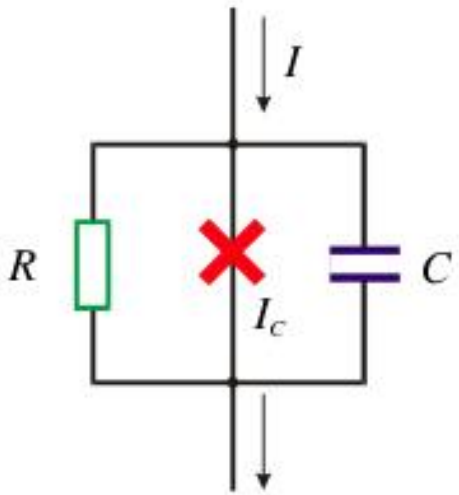






precision of voltage standard

The resistively shunted model RSJ of a Josephson junction

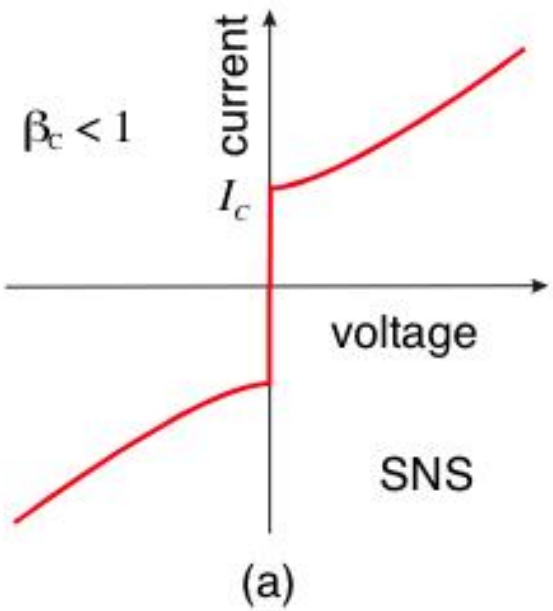


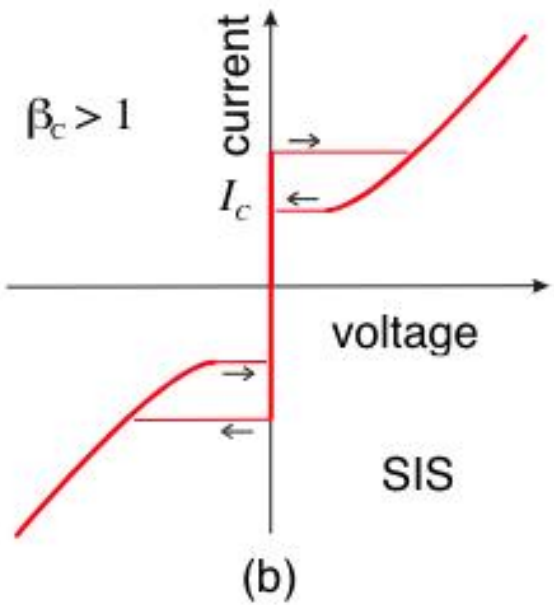
$$I = I_c \sin\varphi + \frac{V}{R} + C\frac{dV}{dt} \qquad \frac{d\varphi}{dt} \equiv \dot{\varphi} = \frac{2\pi}{\Phi_0}V$$

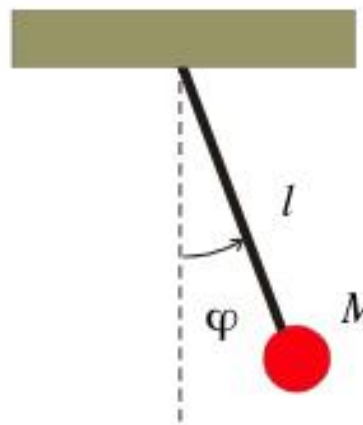
$$I = I_c \sin\varphi + \frac{\Phi_0}{2\pi R}\dot{\varphi} + \frac{\Phi_0 C}{2\pi}\ddot{\varphi} \qquad i \equiv \frac{I}{I_c}\,,\quad \tau = \frac{2\pi I_c R}{\Phi_0}t$$

$$\beta_c \frac{d^2\varphi}{d\tau^2} + \frac{d\varphi}{d\tau} + \sin\varphi = i \qquad \beta_c = \frac{2\pi I_c R^2 C}{\Phi_0}$$

McCumber parameter







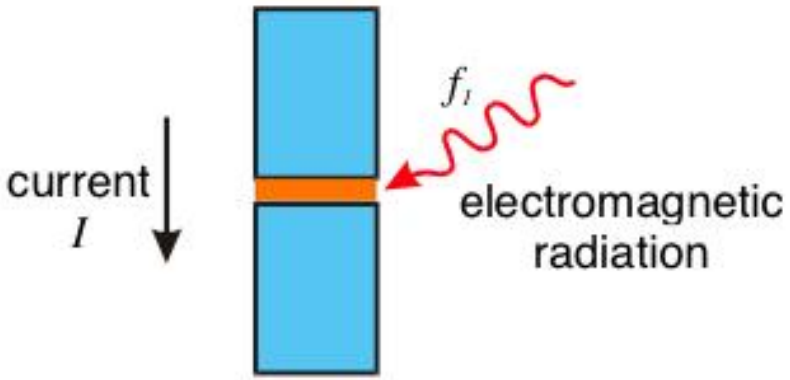
$$T = Mgl\sin\varphi + \chi\dot{\varphi} + \Theta\ddot{\varphi}$$

RF effects: Shapiro steps

$$V = V_0 + V_1 \cos(2\pi f_1 t)$$

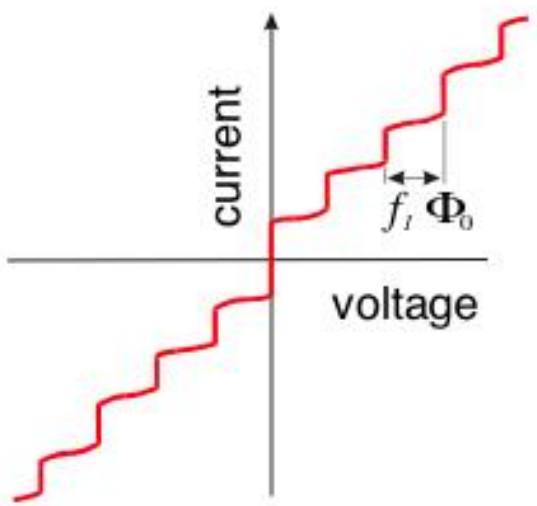
$$\varphi = \int \frac{2\pi}{\Phi_0} V dt = \varphi_0 + \frac{2\pi}{\Phi_0} V_0 t + \frac{V_1}{\Phi_0 f_1} \cos(2\pi f_1 t)$$

$$I_s = I_c \sum_{n=0}^{\infty} (-1)^n J_n\left(\frac{V_1}{\Phi_0 f_1}\right) \sin[\varphi_0 + \frac{2\pi}{\Phi_0} V_0 t - 2\pi n f_1 t]$$

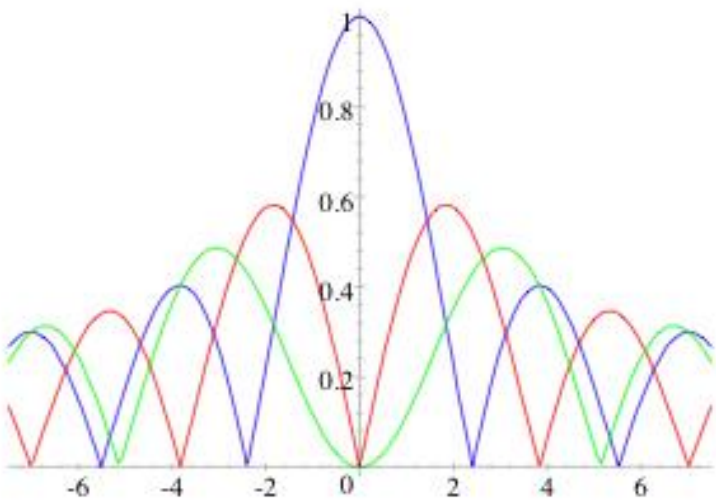


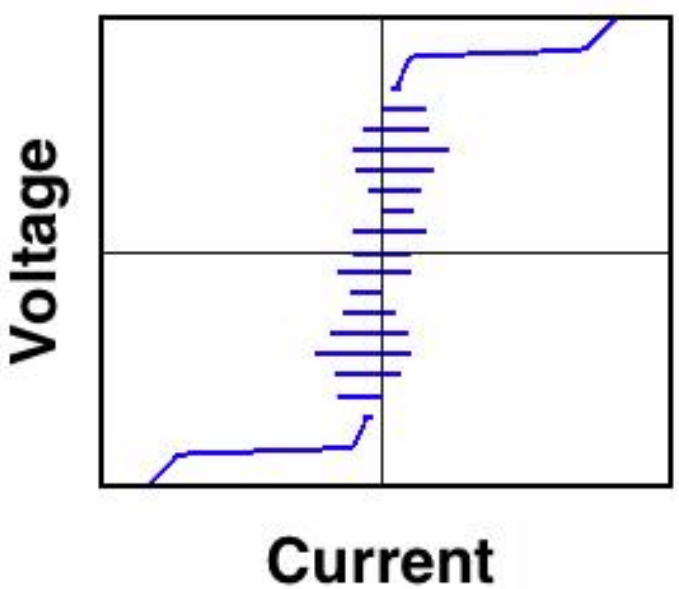
$$\Delta I_n \simeq I_c J_n\left(\frac{V_1}{\Phi_0 f_1}\right) \qquad V_0 = n f_1 \Phi_0,\ n = 0, \pm 1, \pm 2, \ldots$$

The current-voltage characteristic shows current steps at **constant** voltage with accuracy determined only by frequency precision and universal constants



$$\frac{2\pi}{\Phi_0} V_0 = 2\pi n f_1$$

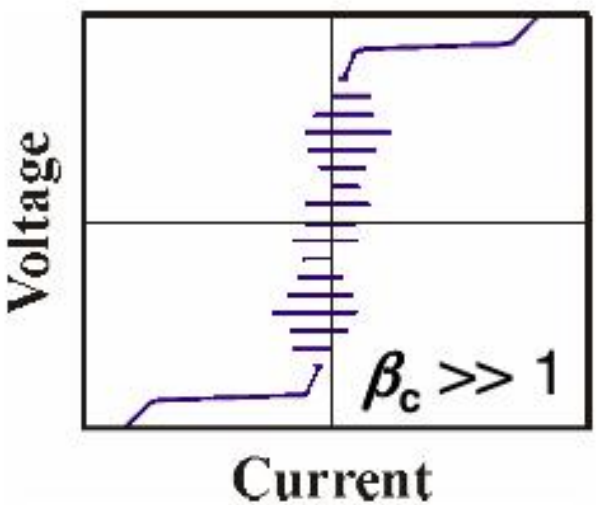


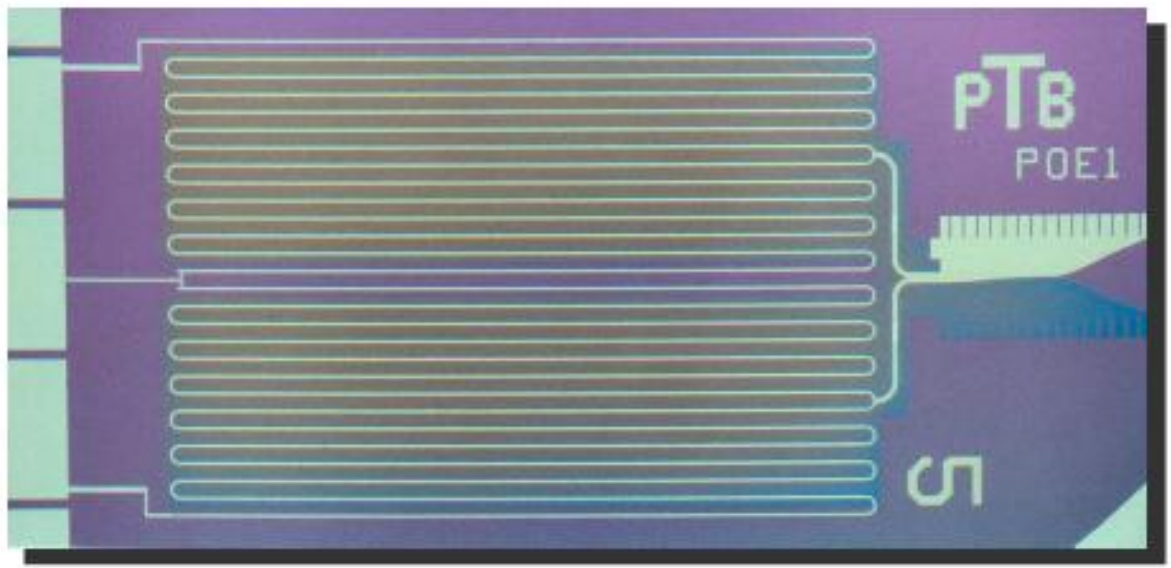


if the frequency ***f* = 70 Ghz → U_n = *n* 0.145 mV** , ***n*** is limited to few units → **need for arrays**

Steps of constant voltage: $U_n = n \cdot (h/2e) \cdot f$

Conventional
(underdamped junctions)





10-V Josephson voltage standard
(13 920 SIS junctions)

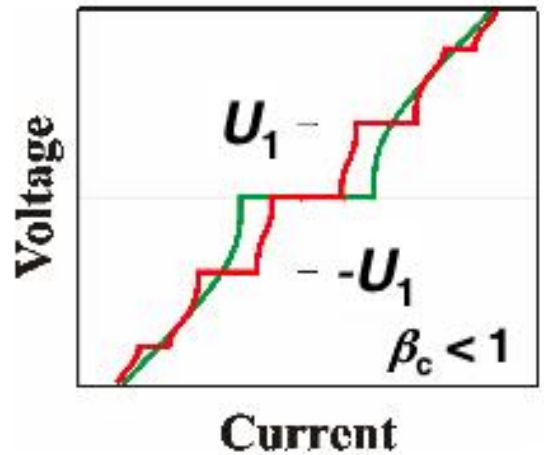
- **Hysteretic IVC**
- **Semistable steps**
- **Voltage hardly adjustable**

used by more than 50 labs world-wide
commercially available from IPHT, Hypres

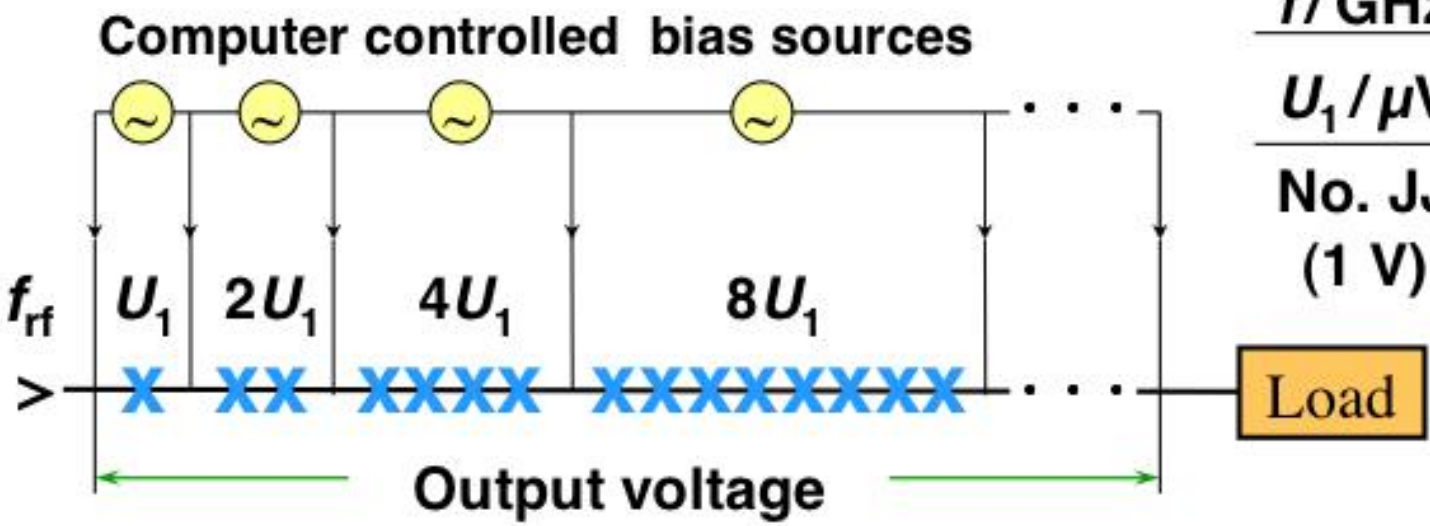
Programmable voltage standards

Overdamped Josephson junctions ($\beta_c < 1$):

- SNS junctions
- S-Sc-S junctions
- SINIS junctions
- shunted SIS junctions



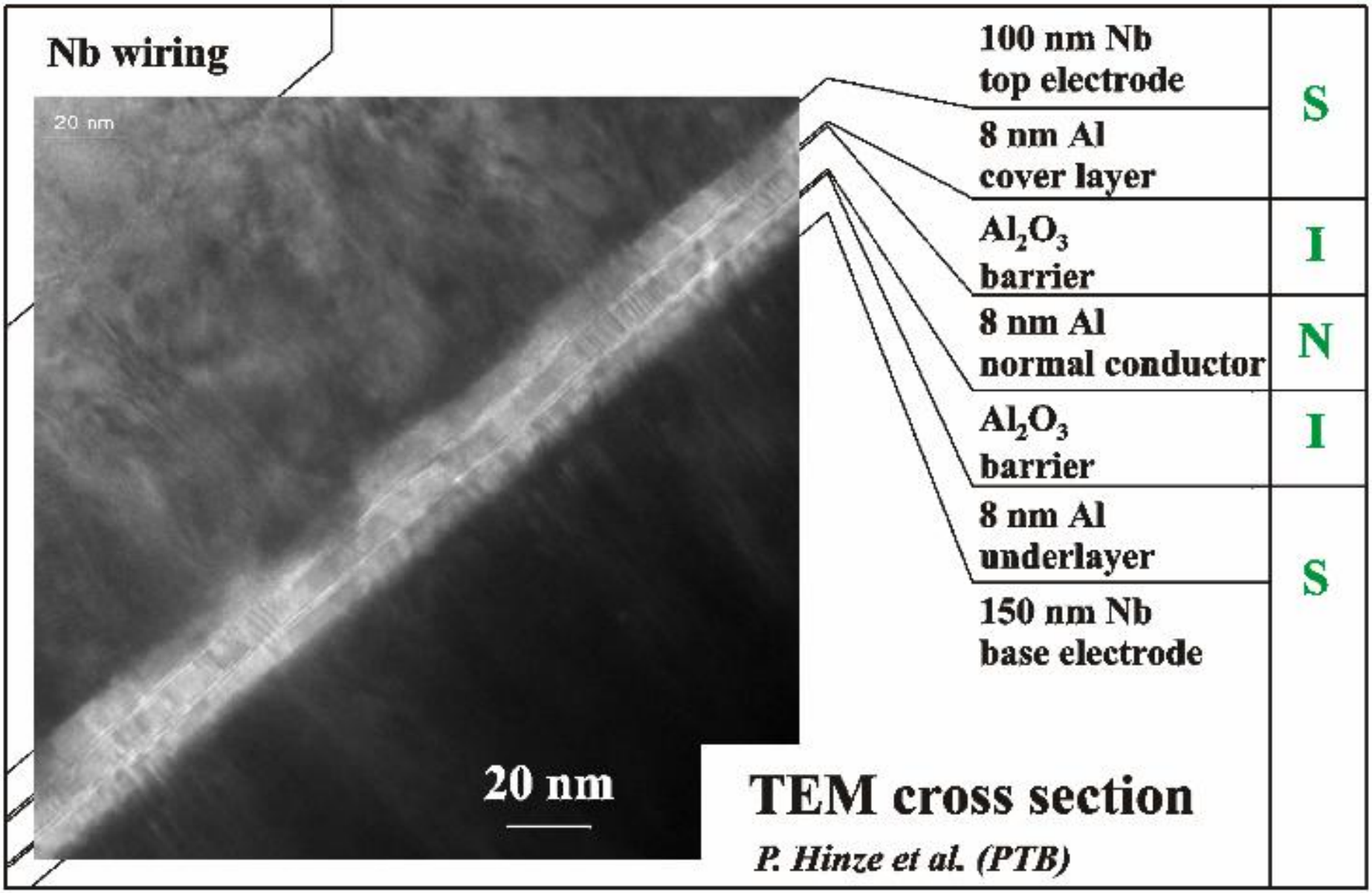
Binary divided series array

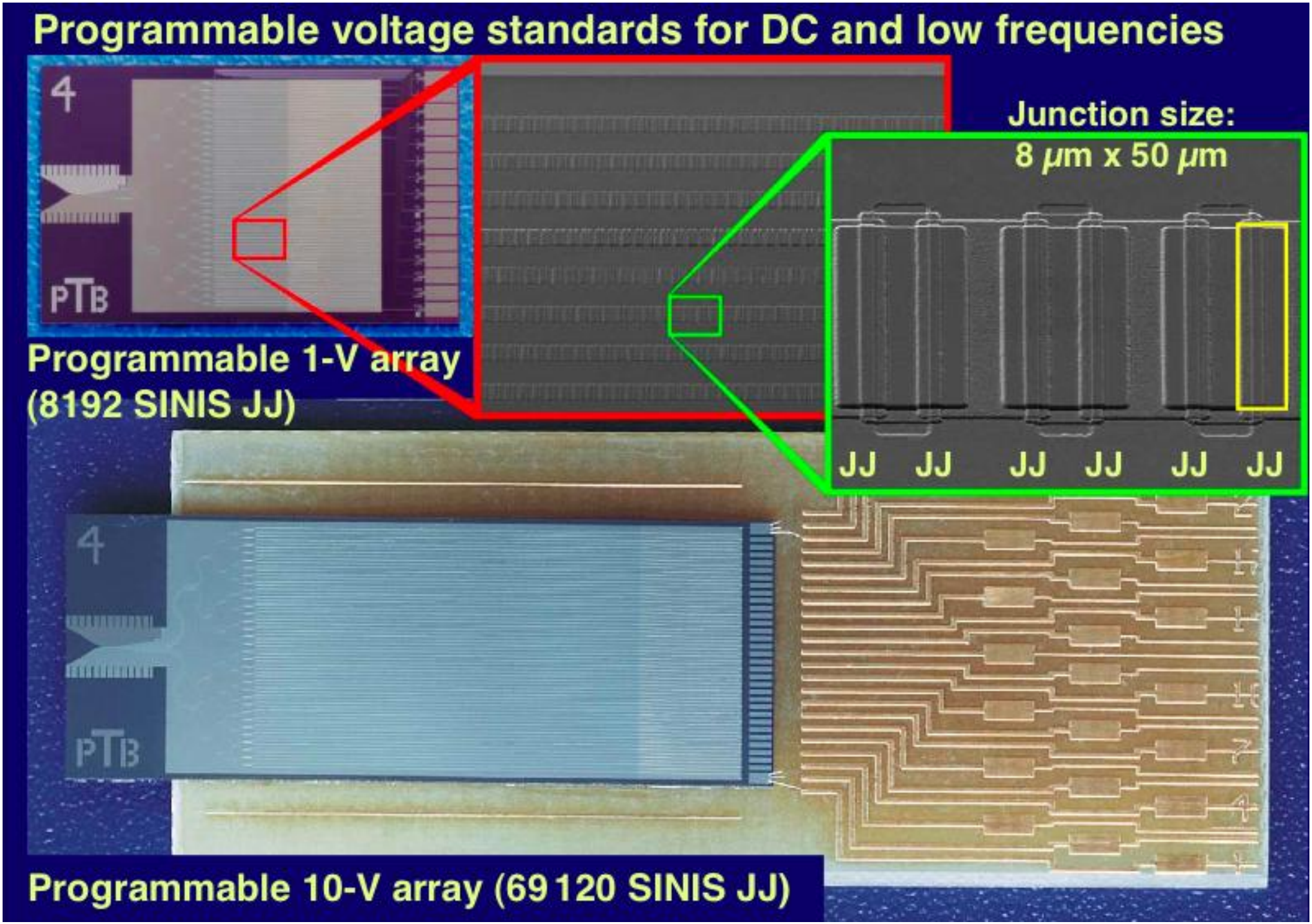


f / GHz	15	70
U_1 / μV	30	145
No. JJ (1 V)	33 000 SNS	7 000 SINIS

Application: D/A converter with fundamental accuracy

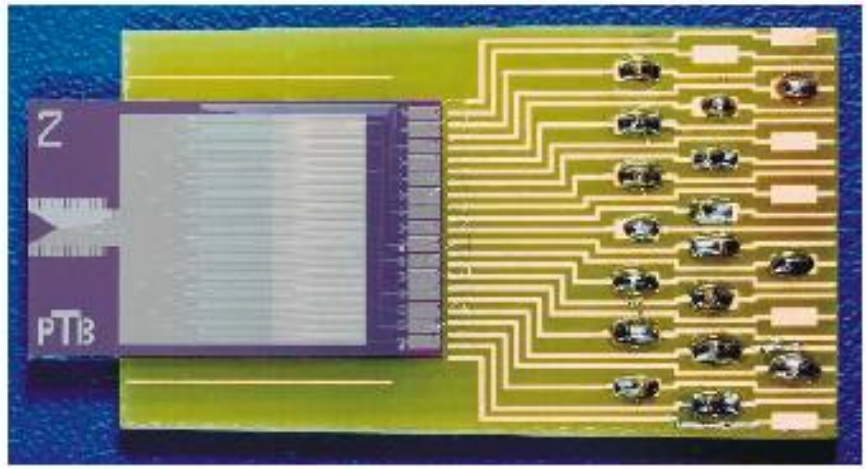
SINIS Josephson junction



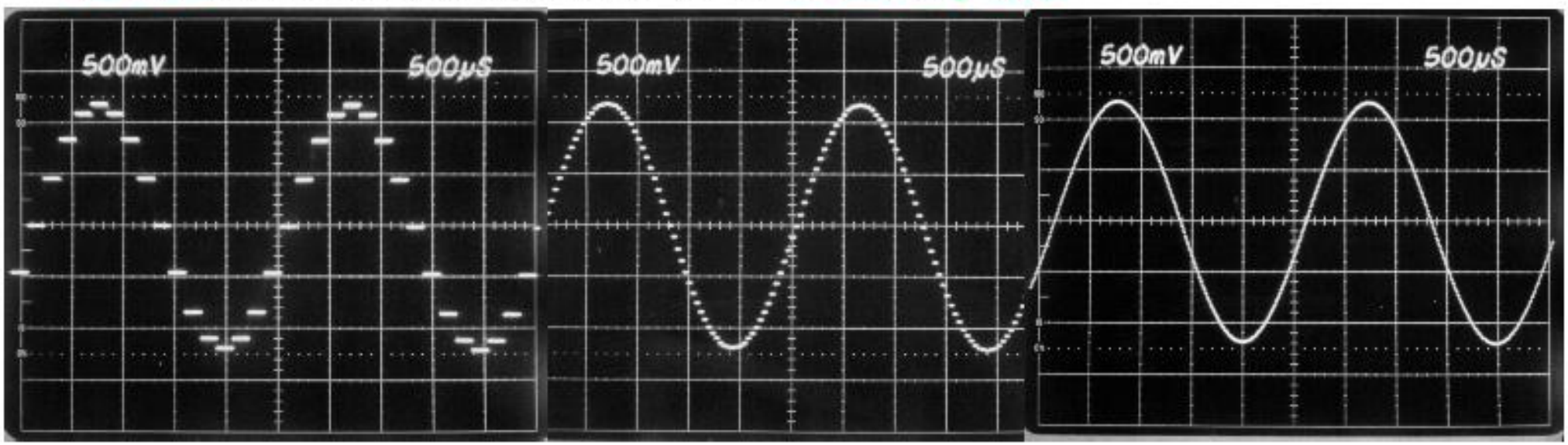

Programmable voltage standards for DC and low frequencies
Junction size:
8 μm x 50 μm
JJ JJ JJ JJ JJ JJ
Programmable 1-V array
(8192 SINIS JJ)
Programmable 10-V array (69 120 SINIS JJ)

Synthesized waveforms

- 1-V array (8192 SINIS-JJ) microwave frequency: 70 GHz
- Maximum voltage: 1,188 V (corresponds to an rms of 0,840 V for a sine wave)



400-Hz sine wave generated with 13 binary bits



16 samples 64 samples 256 samples

NIST - USA

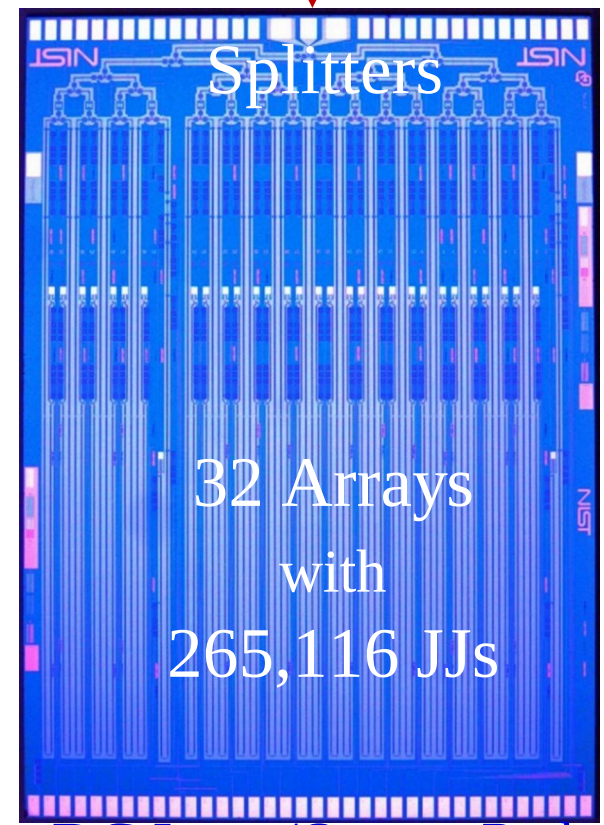
Fabrication & Design of Superconducting Circuits

- Boulder Micro-Fabrication Facility

- Superconducting integrated circuits
  - Uniform junctions, barrier materials, low-defect fabrication
- Microwave circuit design
  - Lumped element inductors & capacitors, power splitters, coplanar waveguides, simulation & modelling

(12 x 17) mm^2 PJVS Chip

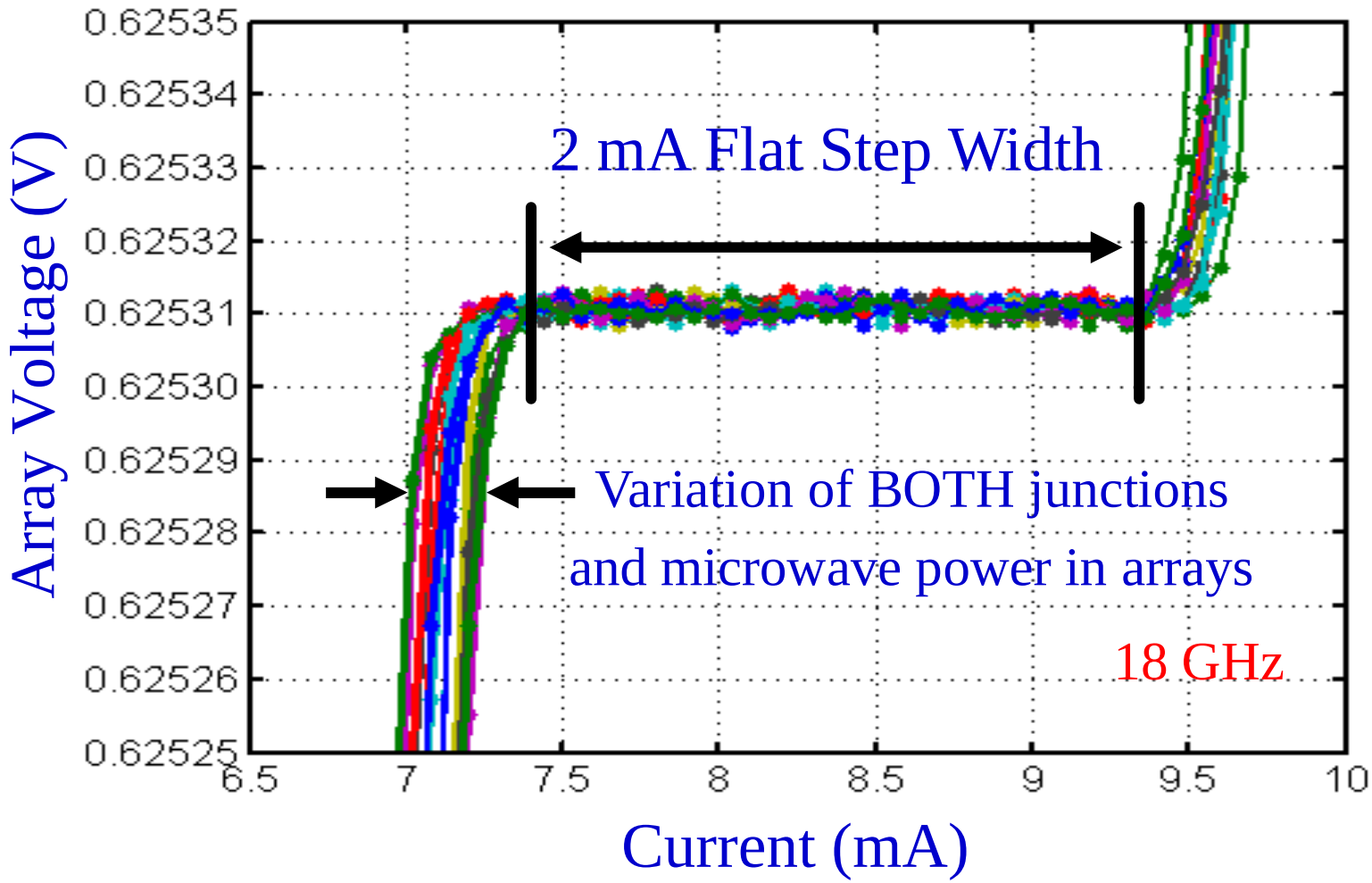
Microwave Input



DC Input/Output Pads

from P. Dresselhaus' talk, ISEC2017

Flat Spots of 16 Arrays with 16800 Junctions



Uniform junctions and microwaves

13

from P. Dresselhaus' talk, ISEC2017

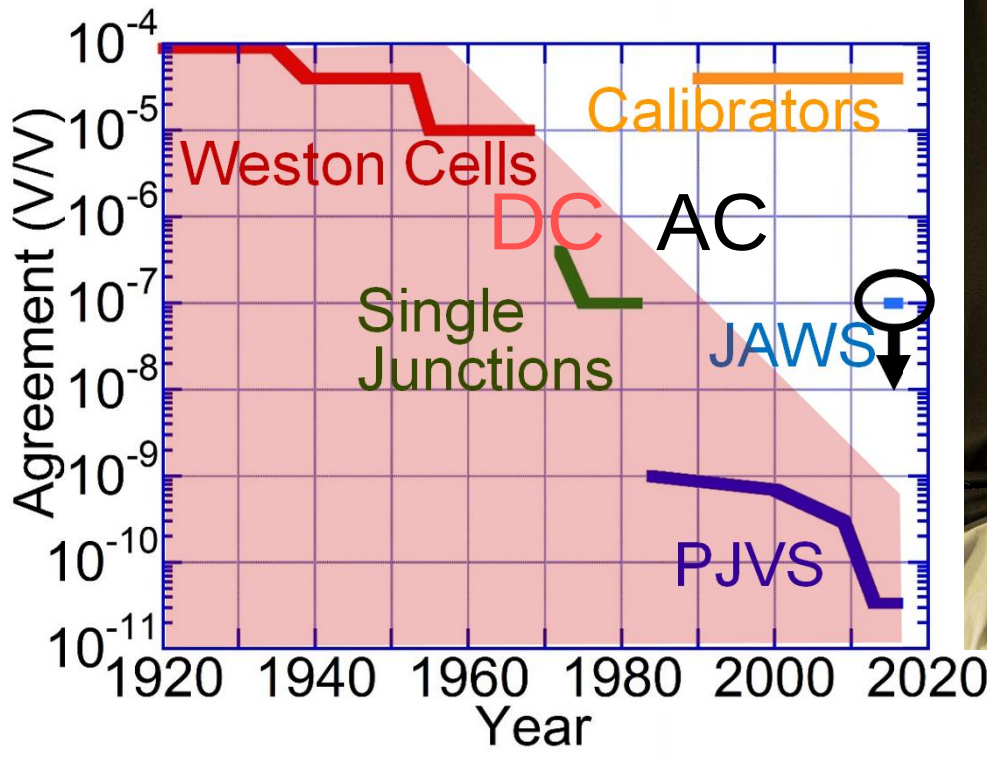
NIST Cryocooled PJVS System

- Integrated system
  - Bias electronics DC & MW
  - Cryogenics
  - Superconducting devices
  - Turn-key integrated system
  - Automation software
    - Optimize & check quantum states, flat spots
    - Performs measurements
- Specific measurement techniques needed for different applications

from P. Dresselhaus' talk, ISEC2017

First Comparisons of 1 V AC Josephson Voltage Standard Sources

Commercial Voltage Calibrators



1 V JAWS

- Statistical uncertainty of first intercomparisons of 1 V AC JAWS voltages are now below 0.1 μV/V
- Systematic errors are ~1 μV/V for kilohertz frequencies

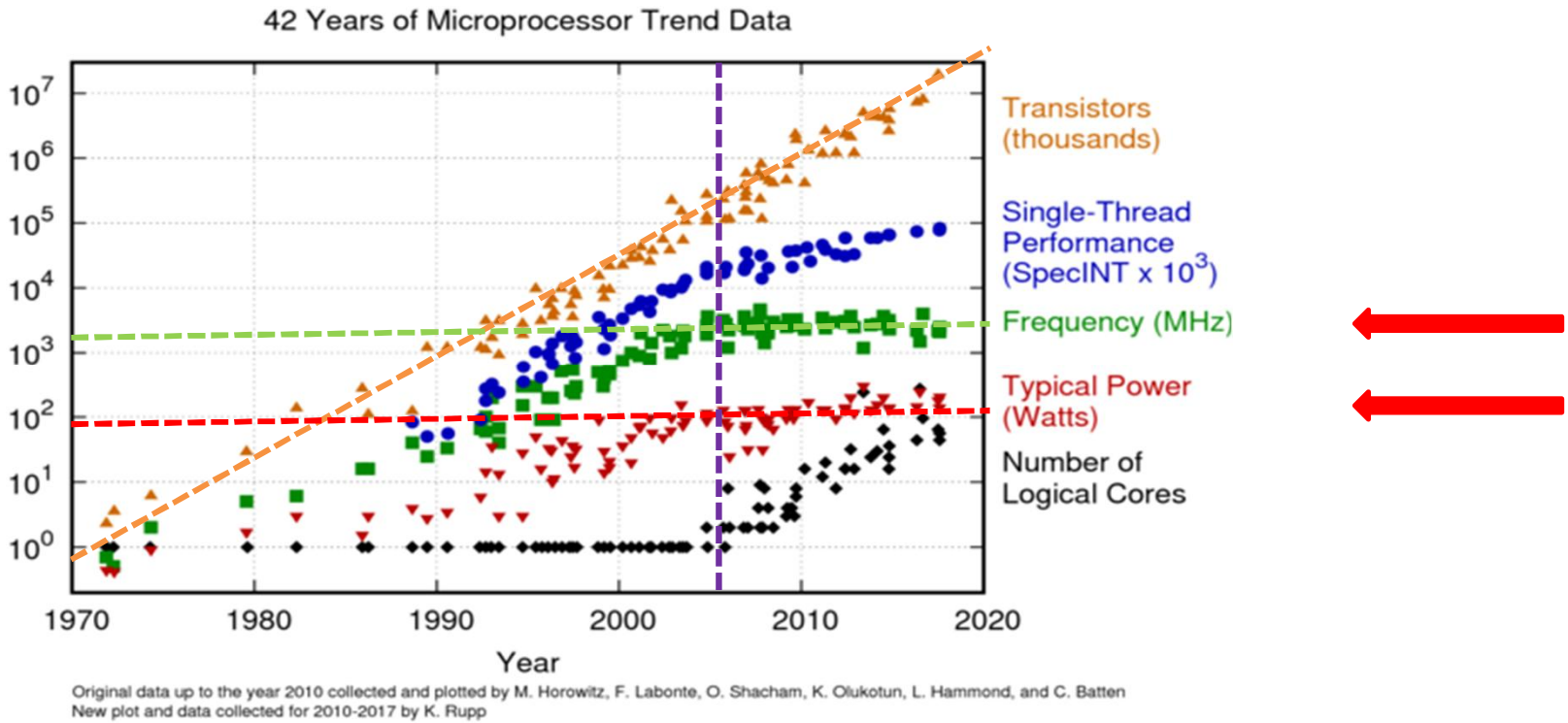
from P. Dresselhaus' talk, ISEC2017

Superconducting Electronics:

- **SQUIDs**
- **Voltage Standards**
- **Digital Circuits**
- **Radiation Detectors**

The End of the Moore's Law in Digital Electronics

The exponential growth of energy consumption by computing and network systems has become an increasingly important issue.
During the last fifty years the **density of integration** has followed an almost exponential increase and **promises to continue** for about another decade before reaching the technology physical limits. However **a large integration level comes with a large energy dissipation**, that has reached the level of **100 W/cm^2**. Such level of energy dissipation already limits the maximum clock frequency to about 4 GHz and poses severe limitation to the number of active elements in a chip that can be powered at any time.



From https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/

The End of the Moore's Law in Digital Electronics

Rank	System	Cores	Rmax (TFlop/s)	Rpeak (TFlop/s)	Power (kW)
1	**Sunway TaihuLight** - Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway , NRCPC National Supercomputing Center in Wuxi China	10,649,600	93,014.6	125,435.9	15,371
2	**Tianhe-2 (MilkyWay-2)** - TH-IVB-FEP Cluster, Intel Xeon E5-2692 12C 2.200GHz, TH Express-2, Intel Xeon Phi 31S1P , NUDT National Super Computer Center in Guangzhou China	3,120,000	33,862.7	54,902.4	17,808
3	**Piz Daint** - Cray XC50, Xeon E5-2690v3 12C 2.6GHz, Aries interconnect , NVIDIA Tesla P100 , Cray Inc. Swiss National Supercomputing Centre (CSCS) Switzerland	361,760	19,590.0	25,326.3	2,272
4	**Gyoukou** - ZettaScaler-2.2 HPC system, Xeon D-1571 16C 1.3GHz, Infiniband EDR, PEZY-SC2 700Mhz , ExaScaler Japan Agency for Marine-Earth Science and Technology Japan	19,860,000	19,135.8	28,192.0	1,350

www.top500.org *(as on November 2017)*

This is a particularly important problem for **high performance computing**.

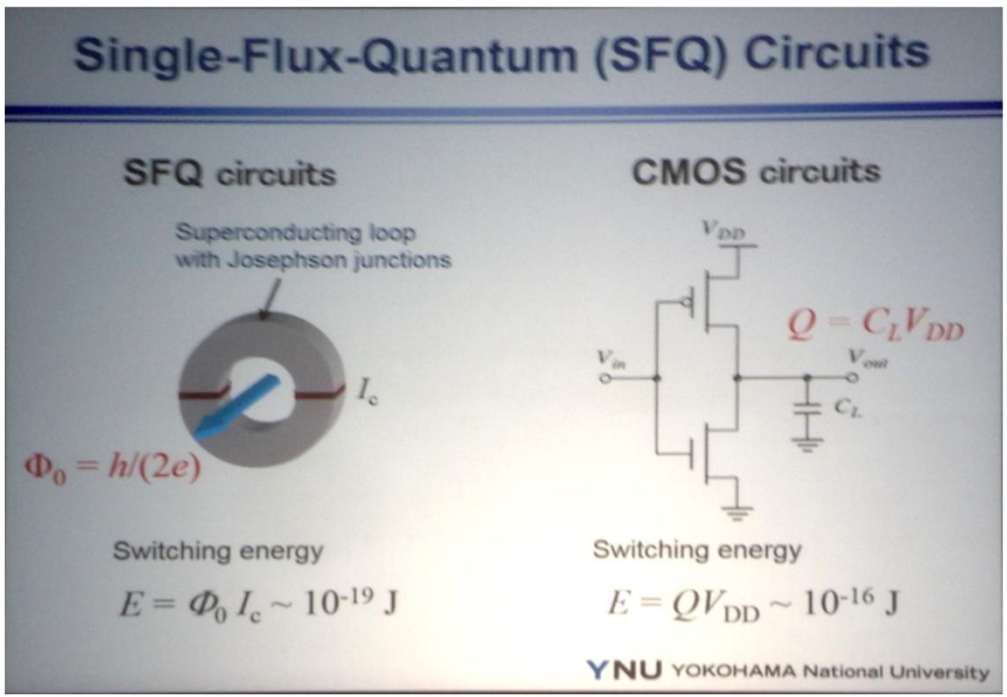
The top performing Chinese **Sunway TaihuLight: 10 Million cores, 10^{20} Flop/s,** has a power requirement close to **15 MW**, **one third** of which is used for cooling.

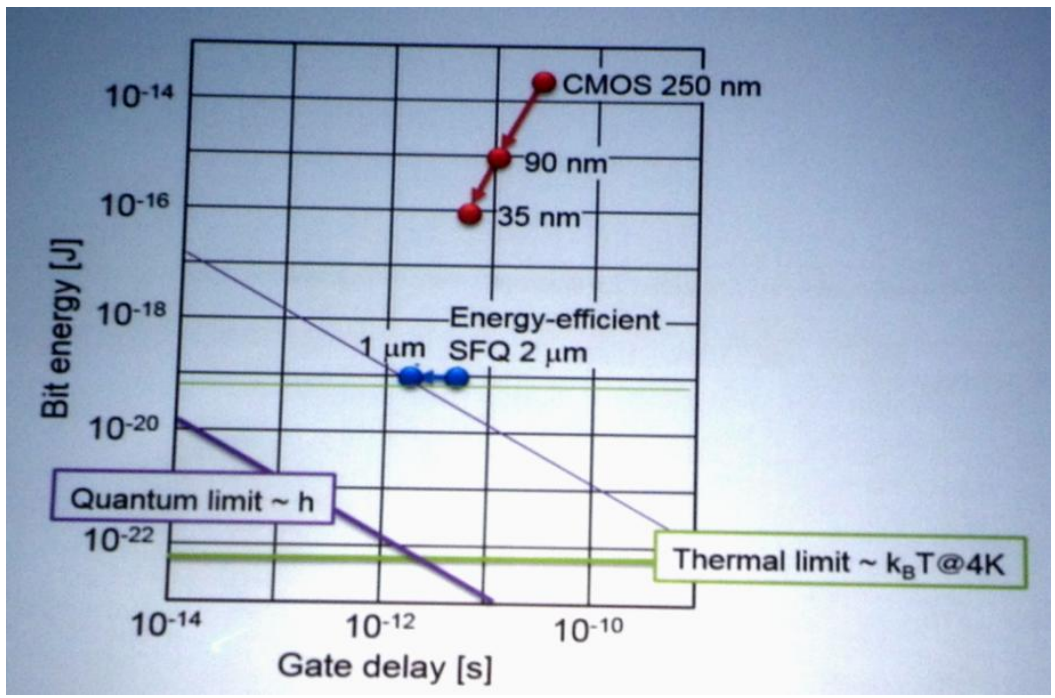
Electricity consumption is a growing issue also for large Data Centers

In 2013, U.S. data centers consumed an estimated **91 billion kilowatt-hours of electricity**, equivalent to the annual output of **34 large (500-megawatt) coal-fired power plants**. Data center electricity consumption is projected to increase to roughly **140 billion kilowatt-hours** annually by **2020**, the equivalent annual output of 50 power plants, costing American businesses $13 billion annually in electricity bills and emitting nearly 100 million metric tons of carbon pollution per year.

Why superconducting digital electronics?

Josephson junction based **superconducting electronics** has been proposed as a possible solution for high performance computing because of the possibility to reach much higher clock frequencies (**up to 200 GHz**) and great **energy efficiency**.





A brief history of Josephson digital circuits development

First efforts at IBM in 1967

Voltage-state projects at IBM, Sperry, TRW, Berkeley MITI project in Japan, some in Europe

Early 1980's
Important fabrication developments (full refractory material)

1985
First publication on rapid single flux quantum (RSFQ) circuits

1991 – 2010
RSFQ is adopted as main digital technology

2010-present
Development of Energy-Efficient superconducting digital families

Distinguishing Features of Superconducting Digital Circuits

- Need a large numbers of devices (many thousands for useful circuits)

- Need CAD tools (some tools made for semiconductors are usable, but others need modification)

- Small margins (allowed variation of power supply level)

- No gain (unlike transistor circuits)

- Lack of adequate memory (4-kbit memory demonstrated)

- Layout for flux management (1 cm^2 chip has 500 flux quanta if B = 0.1 mG . Circuits must be protected.)

Choosing a Technology

LTS Interconnections

Most interconnections are in microstrip configuration

Prior to 1985 **---Pb alloy** (basis of the 1967-1983 IBM project and early Japanese projects)

Currently **niobium** is the "workhorse" for large circuits; operation at 4-5 K. (Key inventions were AlO*x* grown barriers and the whole wafer process with subtractive etching.)
Microstrip Inductance per square for Nb L ~ 0.50 pH/ square

NbN technology based on NbN/MgO/NbN L ~ 0.75 pH/ square
Advantage over Nb: Tc ~ 15 K so operation temperature ~ 8-10 K
Disadvantage: Large and variable penetration depth and inductance/square

MgB2 technology

In some cases Tc = 40 K, so potentially usable with simple refrigerator
Early state of development, only a small number of junctions have been demonstrated; none at 40 K.

Choosing a Technology

High Tc materials

Most developed candidate is YBa2Cu3O with Tc = 90 K

The usual rule of operating 0.5 - 0.7 of Tc suggests operating at 45 K – 63 K
But noise currents and voltages increase with temperature.

Excessive error rates if T > 30 K.

Critical current spread: $\sigma = 6\%$ ($6\sigma = 36\%$)

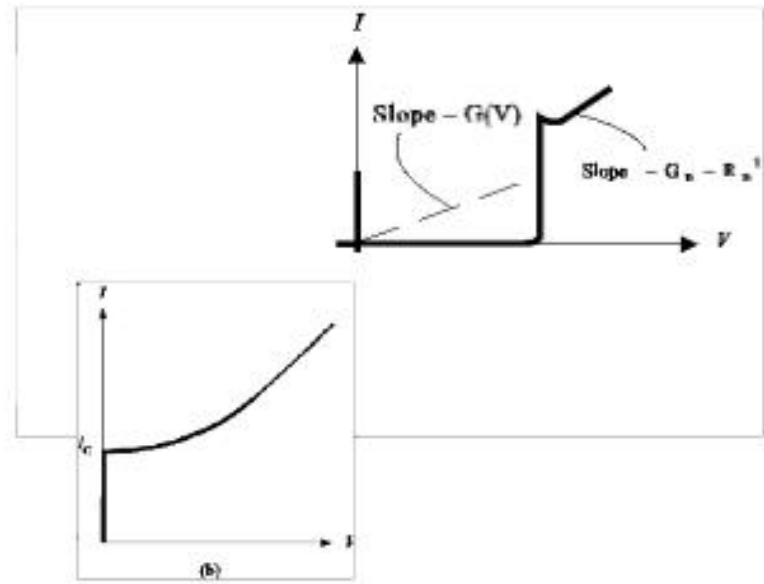
Too large for digital circuits, except small demonstration gates.

Need a breakthrough—a new controllable way to make Josephson junctions.

Niobium Josephson Junctions for Digital Circuits

The only JJ technology for circuits with large numbers of junctions with sufficient control is the Nb/AlO_x/Nb tunnel junction.

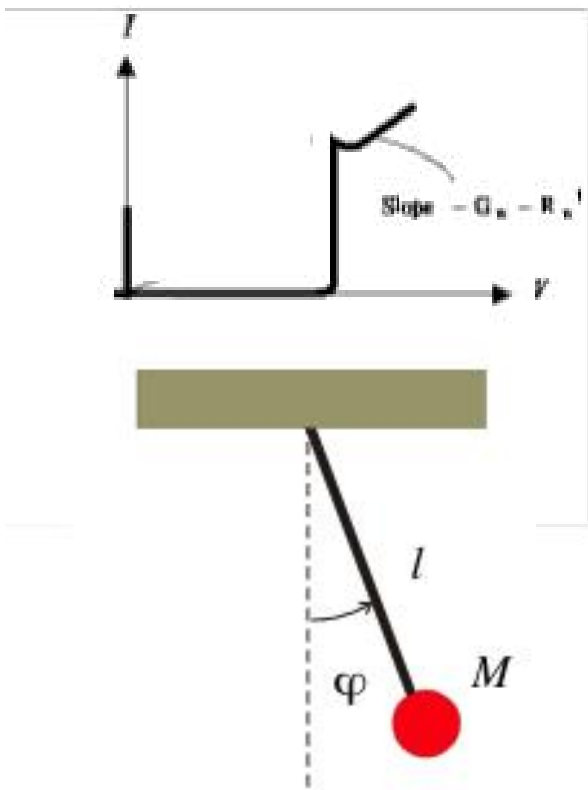
Typical I-V of a high-quality tunnel junction

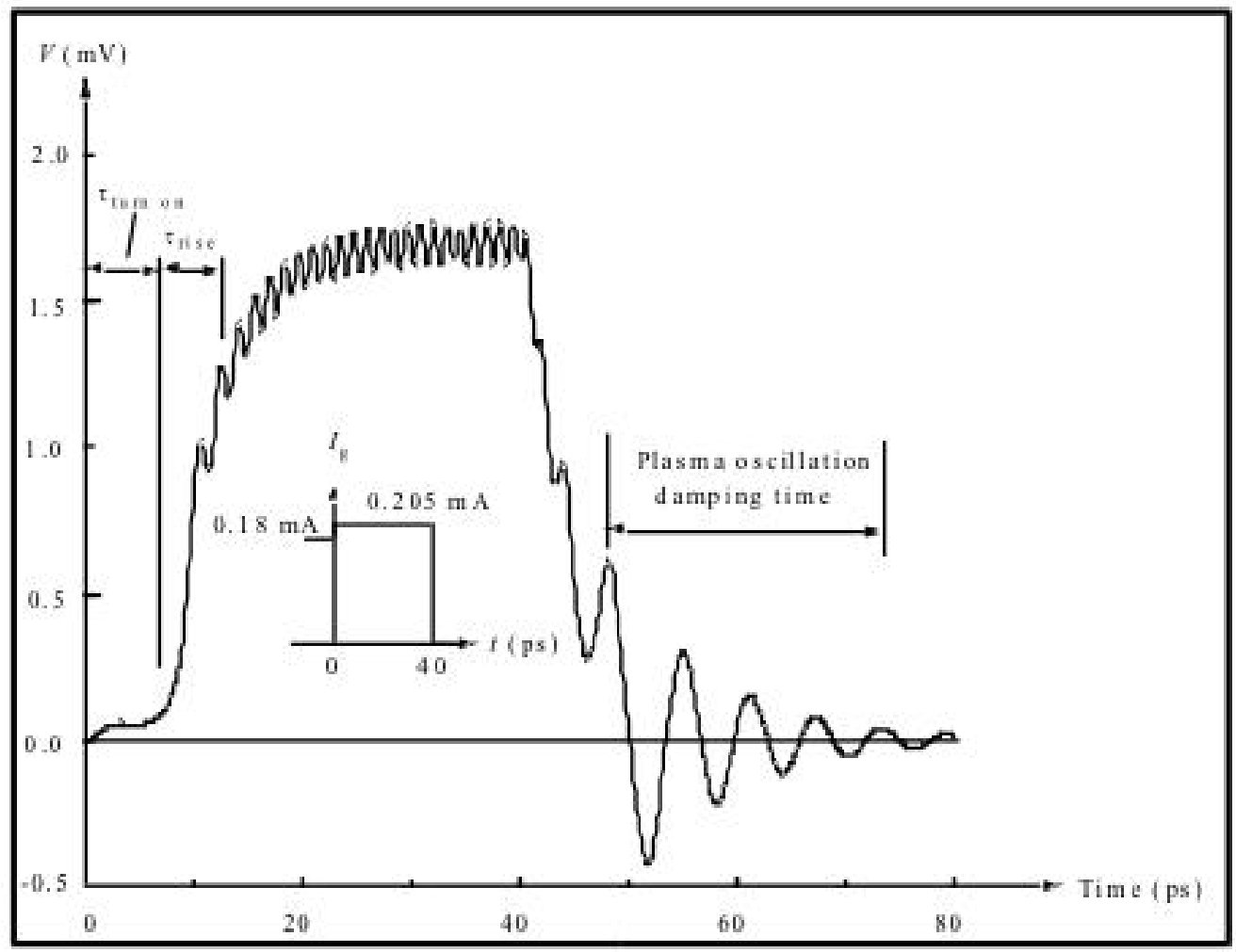


Predominant type of digital circuit is the Rapid Single Flux Quantum (RSFQ) logic family, which requires nearly non-hysteretic I-V.

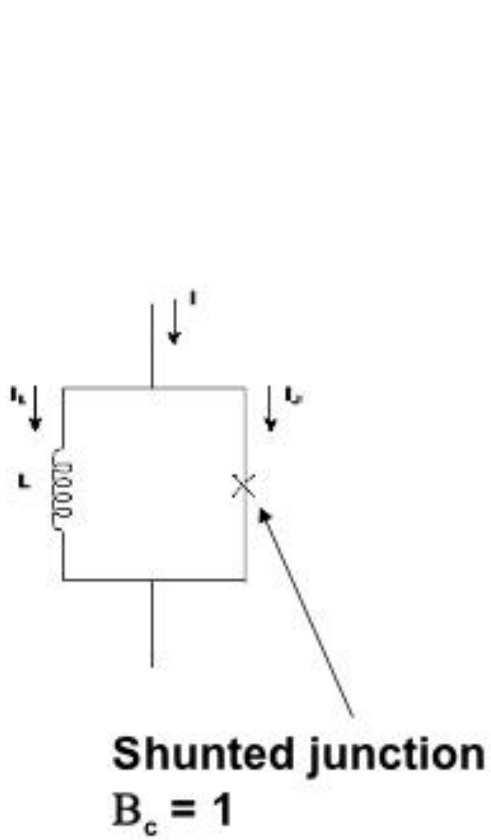
To achieve the non-hysteretic form of I-V, a resistor R is connected in shunt with the tunnel junctions to make $\beta c \sim 1-2$

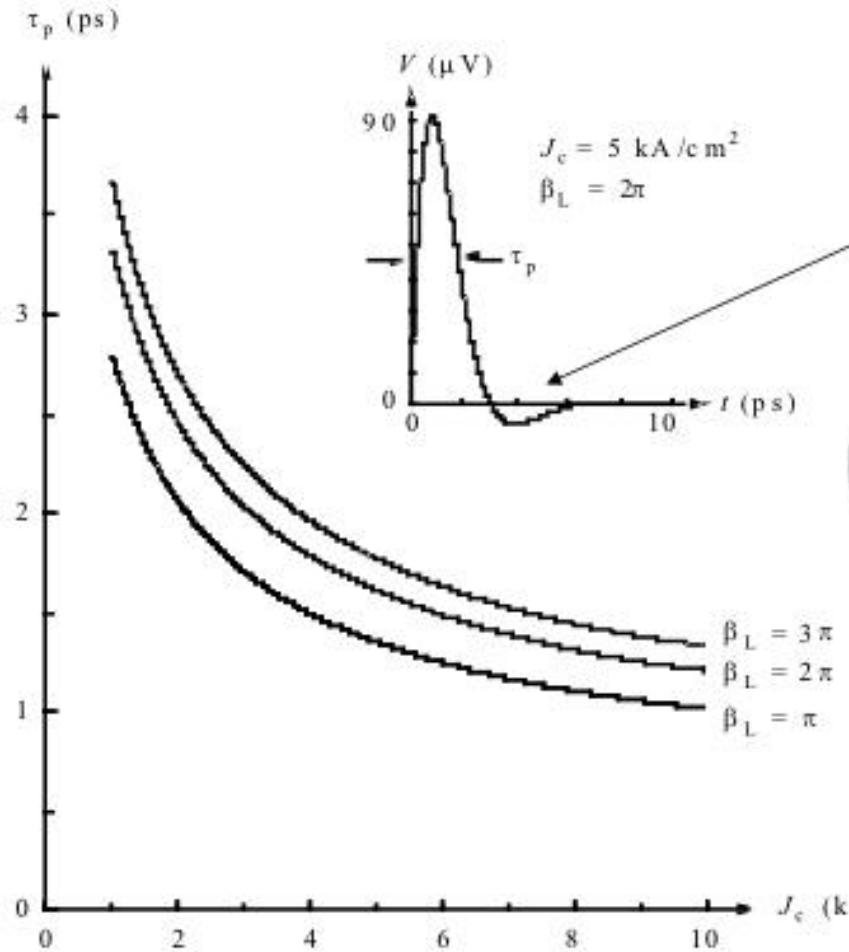
Switching time of a hysteretic Josephson junction → ns scale

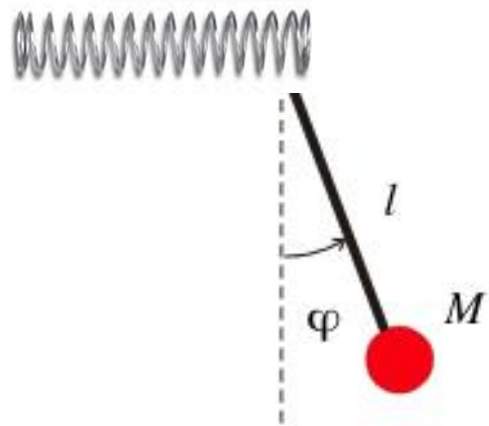




Switching time of a shunted junction (1 junction SQUID) → ps scale







SFQ and Flux Quantization

Quantization of Magnetic Flux

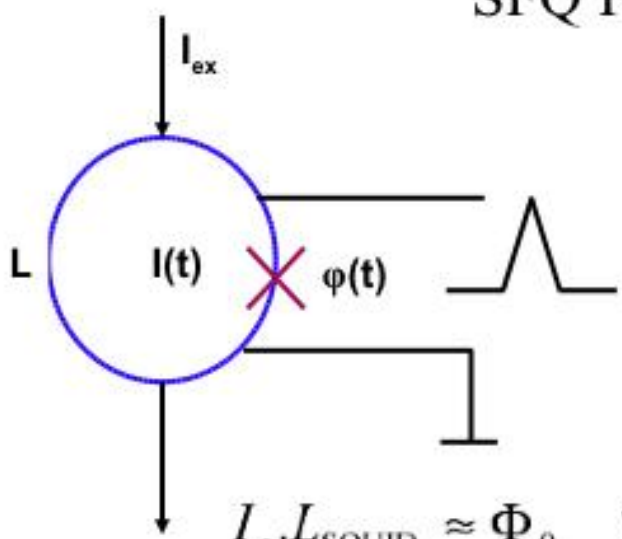
Flux through the Superconductive loop = $n\Phi_0$

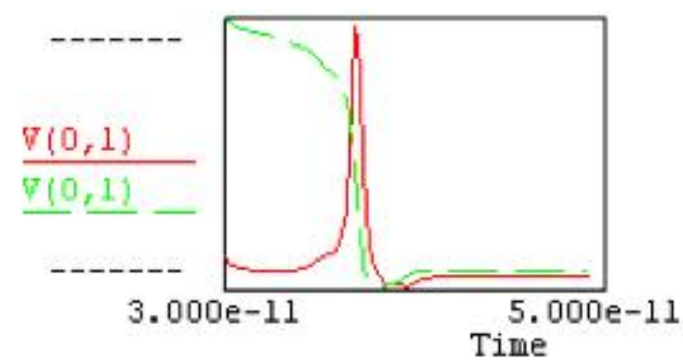
n=0 : "0"
n=1 : "1"

(multiples of flux quantum)

$\Phi_0 = 2.07 * 10^{-15}$ Weber

SFQ Pulse Generation



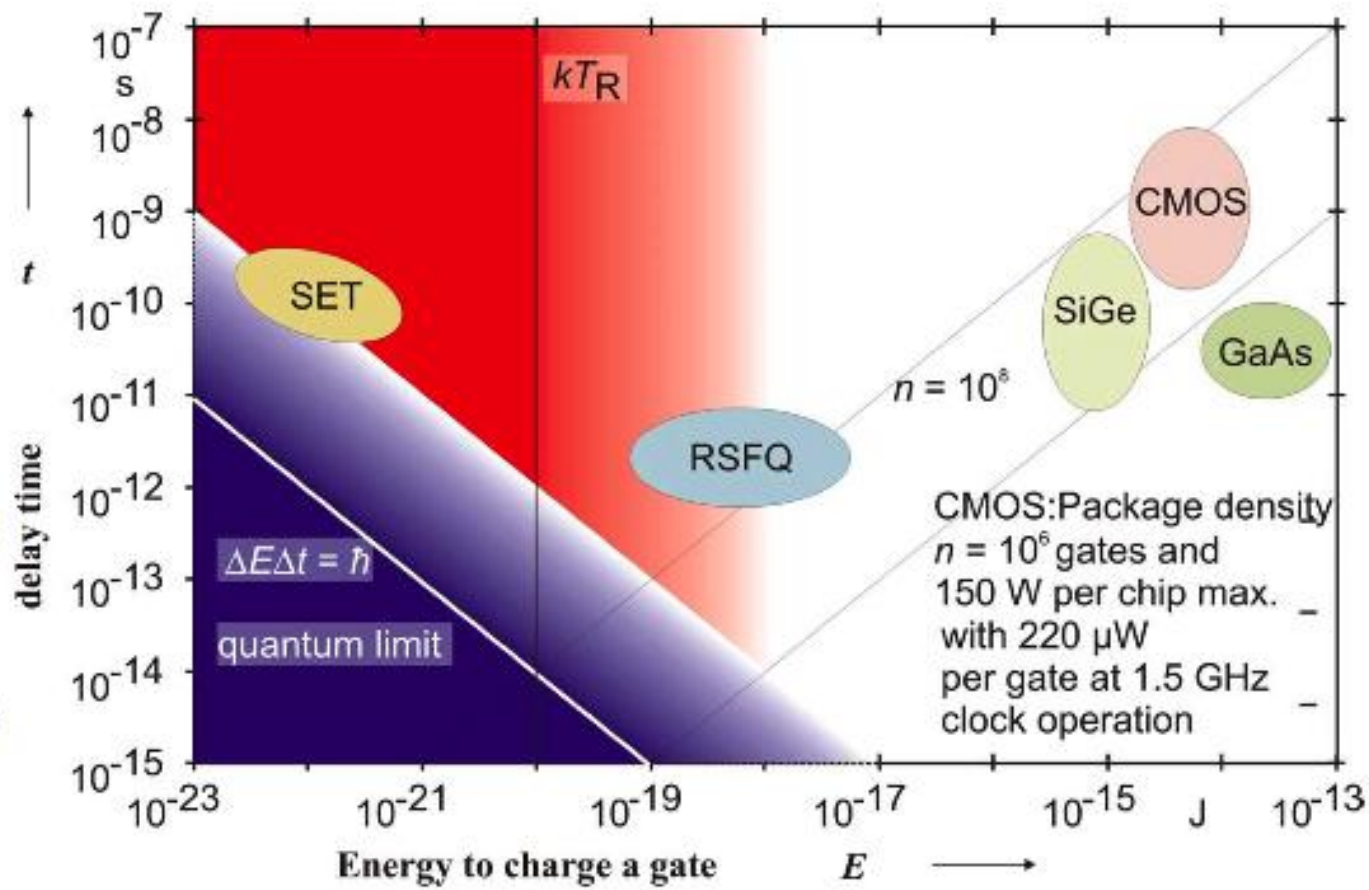


$I_c . L_{SQUID} \approx \Phi_0$ **V=dΦ/dt** $\int V dt = \Phi_0 = h/2e \sim 2.07$ mV.ps

Fundamental Limits for Integrated Electronics

SFQ:
0.1 μW per gate
at 100 GHz
and for 1μm
linewidth

but with standard
Nb technology
minimum
linewidth 0.2 μm



SFQ Circuit Elements

Current biased Josephson junction

Ideal: $I = I_c \sin$,

$V(t) = (\Phi_0/\pi) d\varphi/dt$

φ phase difference

I_c critical current

R_n normal state resistance

$\Phi_0 = h/2e = 2.0679 \times 10^{-15}$ Wb

The junction can act as:

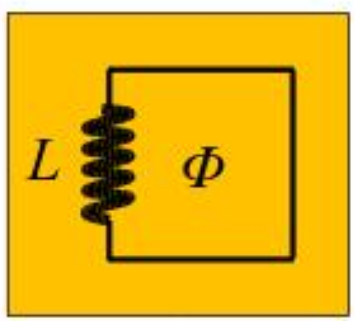
- **SFQ transfer element:**

a 2π phase slippage generates a voltage pulse $\int V(t)\, dt = \Phi_0$ in the 1- 4 ps range

- **Oscillator:**

$V_{DC} = \Phi_0 f$; $V_c = I_c R_n$ defines the maximum operation speed

e.g. 145 μV → 70 GHz



Superconducting ring

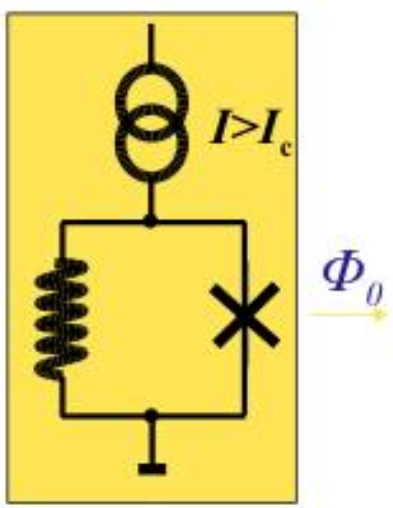
Stores Single Flux Quanta

$\Phi = n \Phi_0$

L loop inductance

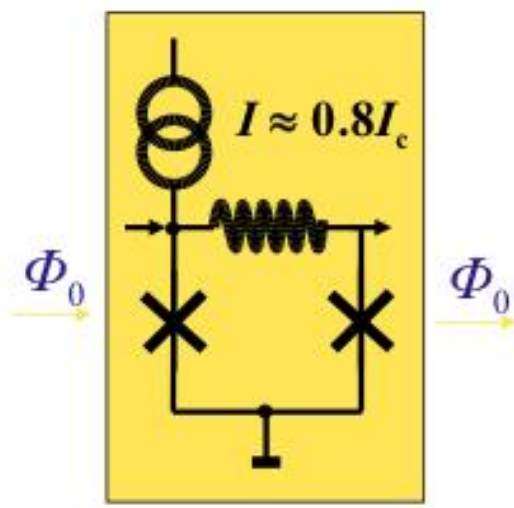
Both circuit elements can be combined to complex logic circuits

Basic SFQ Circuits

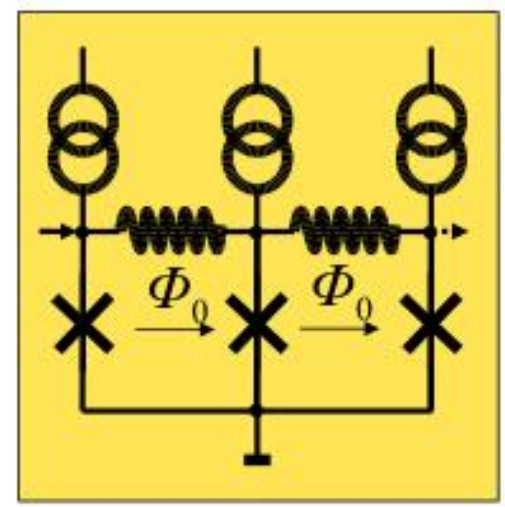


DC/SFQ converter

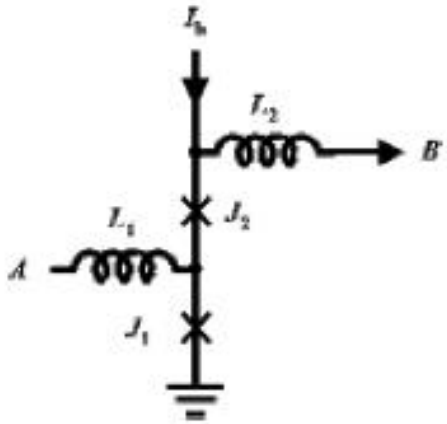
$L\,I_c \approx \Phi_0$



SFQ flip-flop

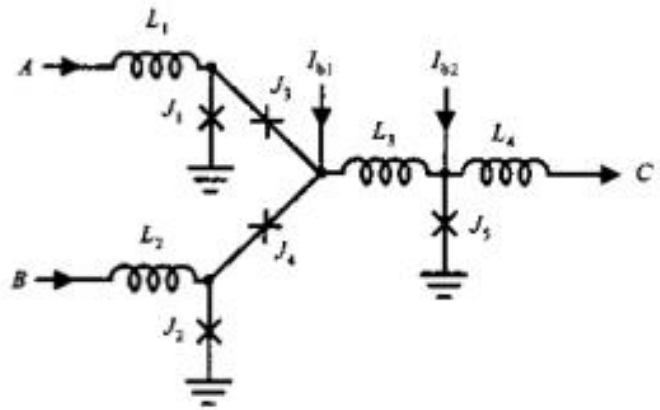


SFQ transmission line



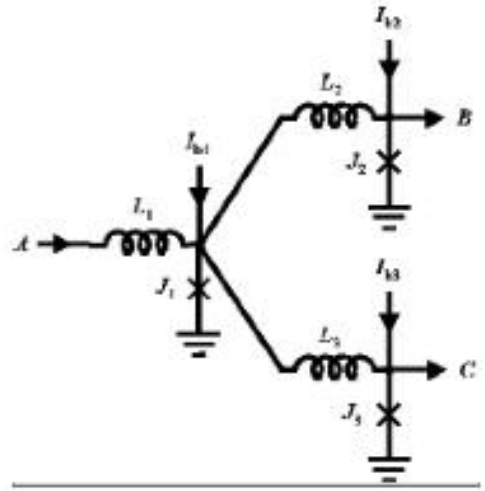
Buffer

One-way transmission



Confluence Buffer

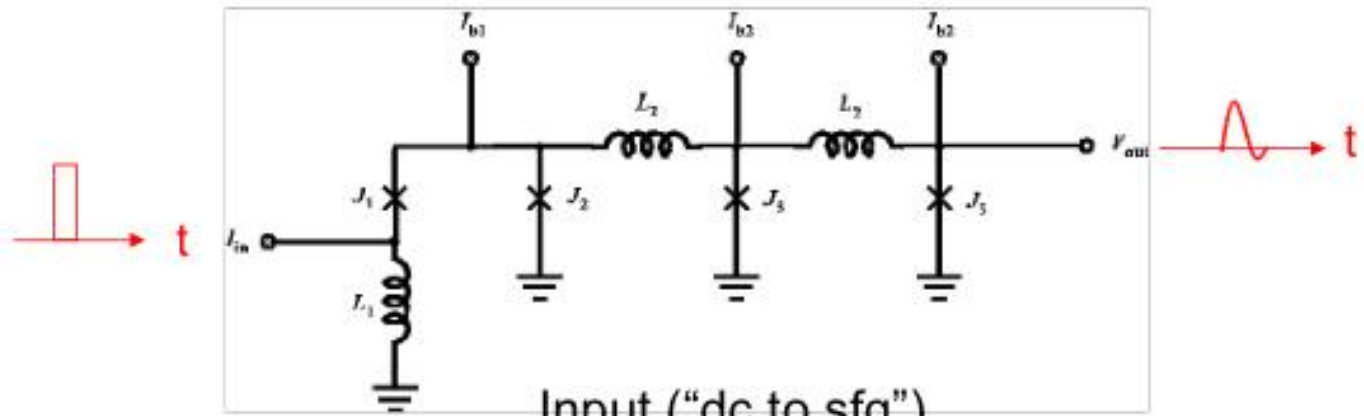
Combines inputs ("fan-in")

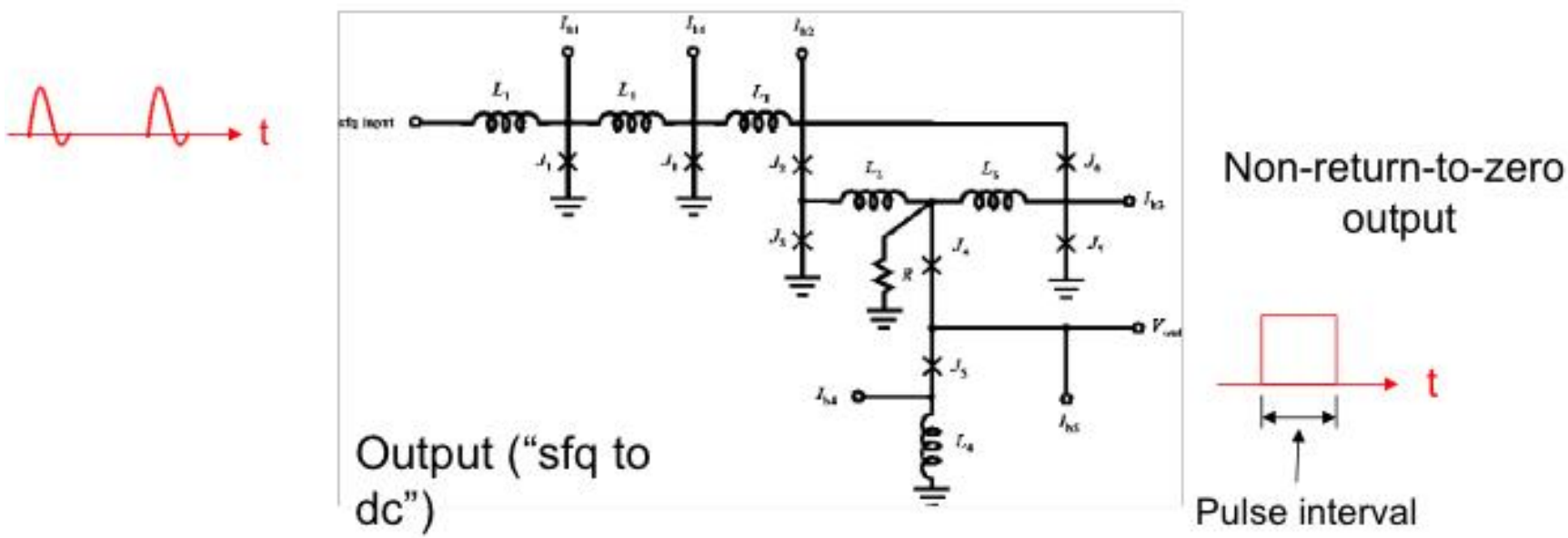


Pulse Splitter

Provides "fan-out"

SFQ pulses are too fast for semiconducting eletronics need for interface circuits

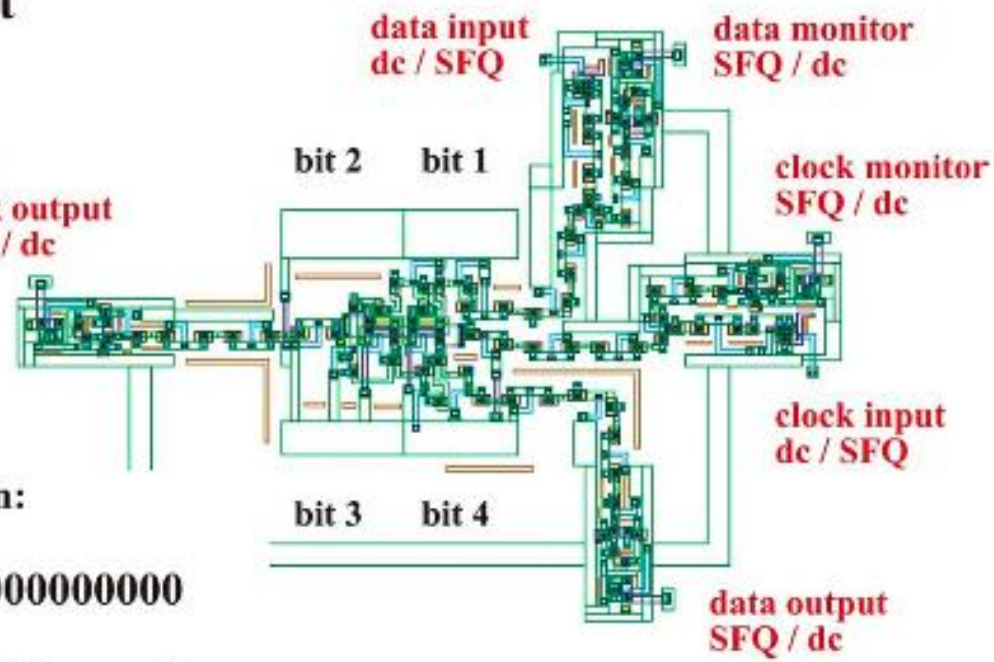


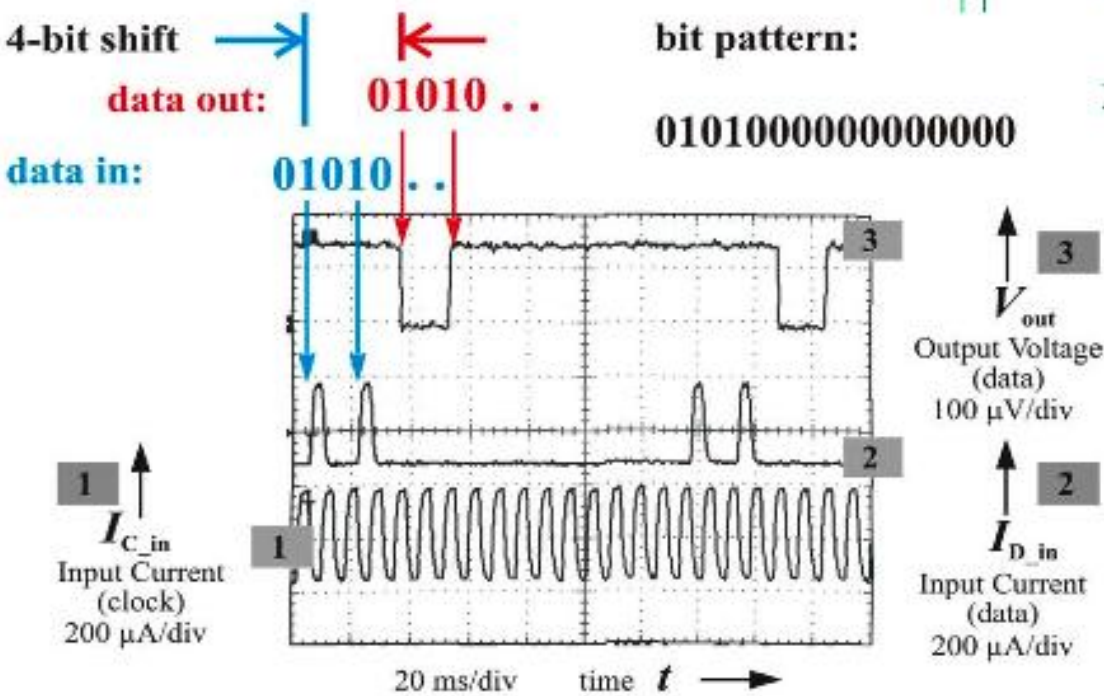


Typical SFQ Circuit

RSFQ 4 Bit Circular Shift Register: Test and Layout
SINIS technology

layout





PTB Braunschweig67

Figures of Merit

Linewidth (μm)	*3.5*	*1.5*	*0.8*
cells per cm²	10^4	$3x10^4$	10^5
Speed of large scale circuits (GHz)	10 - 40	40 - 80	70 - 130
Minimum power (μW per cell)	0.03	0.06	0.1

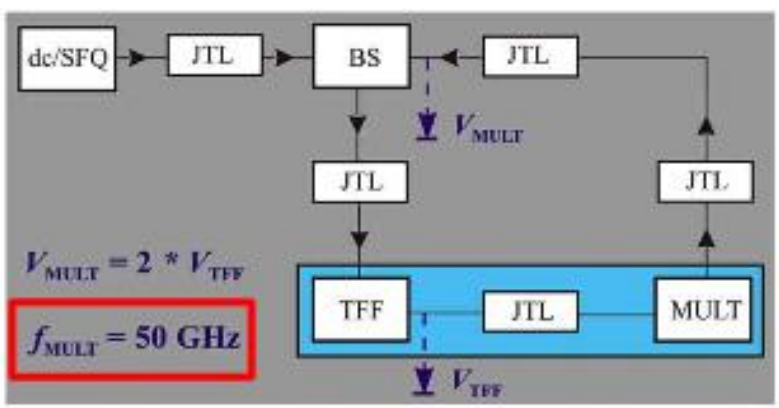
K.K. Likharev et al.

- Very low energy dissipation
- High speed operation (700 GHz for small circuits demonstrated)
- Dispersion free pulse propagation

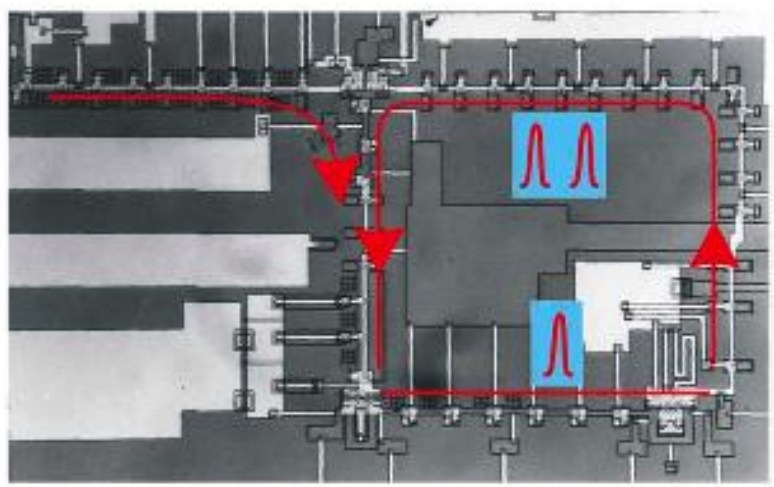
+

−

- Low operation temperatures
- Linewidth > 200 nm for conventional Nb technology
- larger junction number requires smaller parameter spread



Generation and maintenance of permanent SFQ pulse circulation
Reliability of circuit operation: $BER < 10^{-16}$



8

Application Potential

Application	Junction count	Market Size
integrated SIS receivers with correlator	10^6	Small
digital multichannel SQUID arrays	10^5	Medium
DC voltage standards	10^4	Small
AC voltage standards, digital synthesiser	10^5	Medium
A/D converters	10^4	Large
D/A converters	10^3	Medium
dc/ac quantum voltmeters	10^5	Large
time-digital converters	10^3	Medium
digital SFQ test circuits for rf metrology	10^3	Medium
coding/decoding systems for secure communications	10^3	Medium
frequency dividers, digital frequency meters	500	Medium
transient recorders	10^4	Medium
samplers	10	Medium
digital beam forming microwave antennas	?	??
read-out for multipixel focal plane array imagers	?	??
TeraFLOPS workstation	10^6	Medium
PetaFLOPS computer	1000×10^6	??

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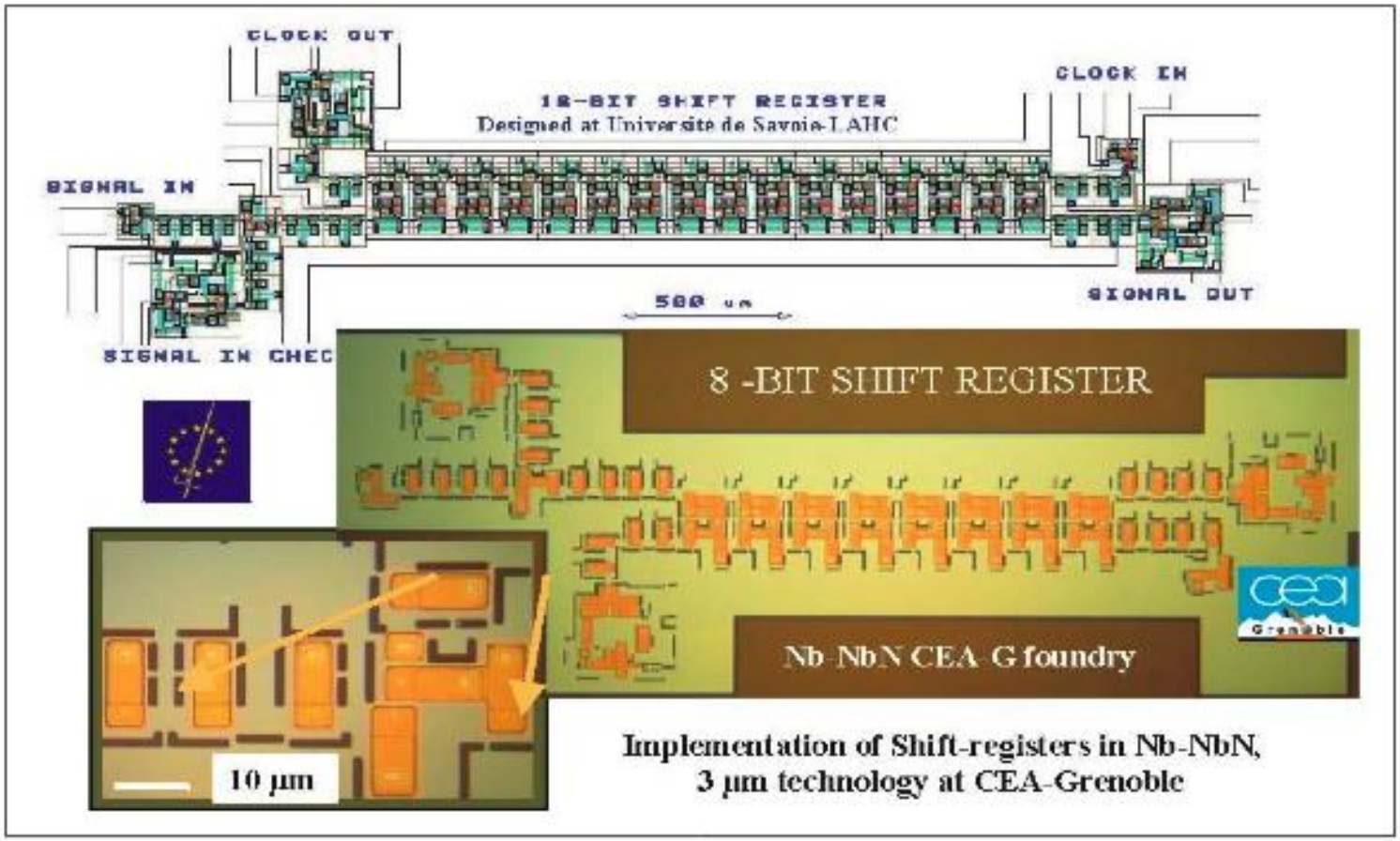
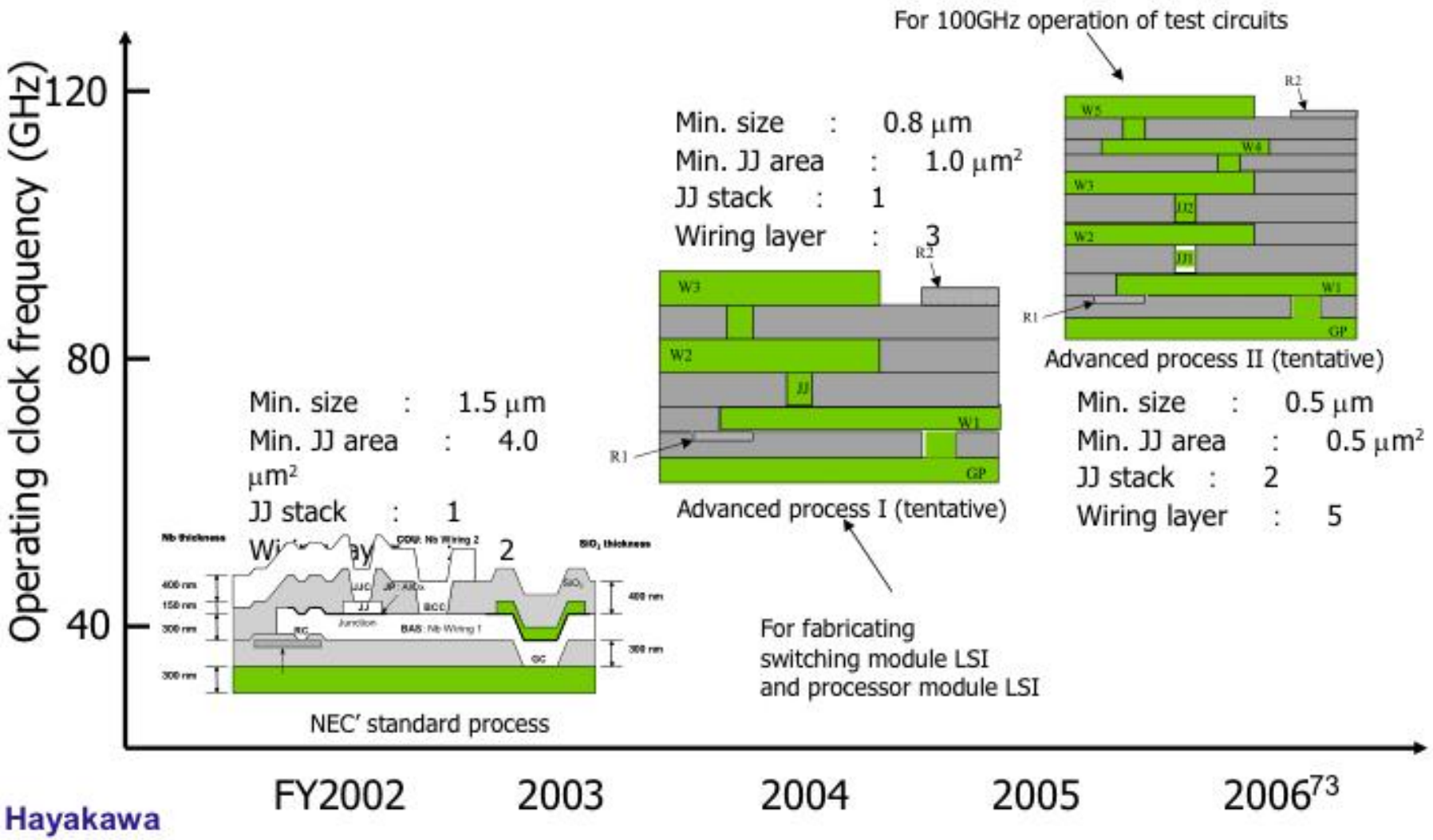
SCENET Roadmap for superconducting digital electronics

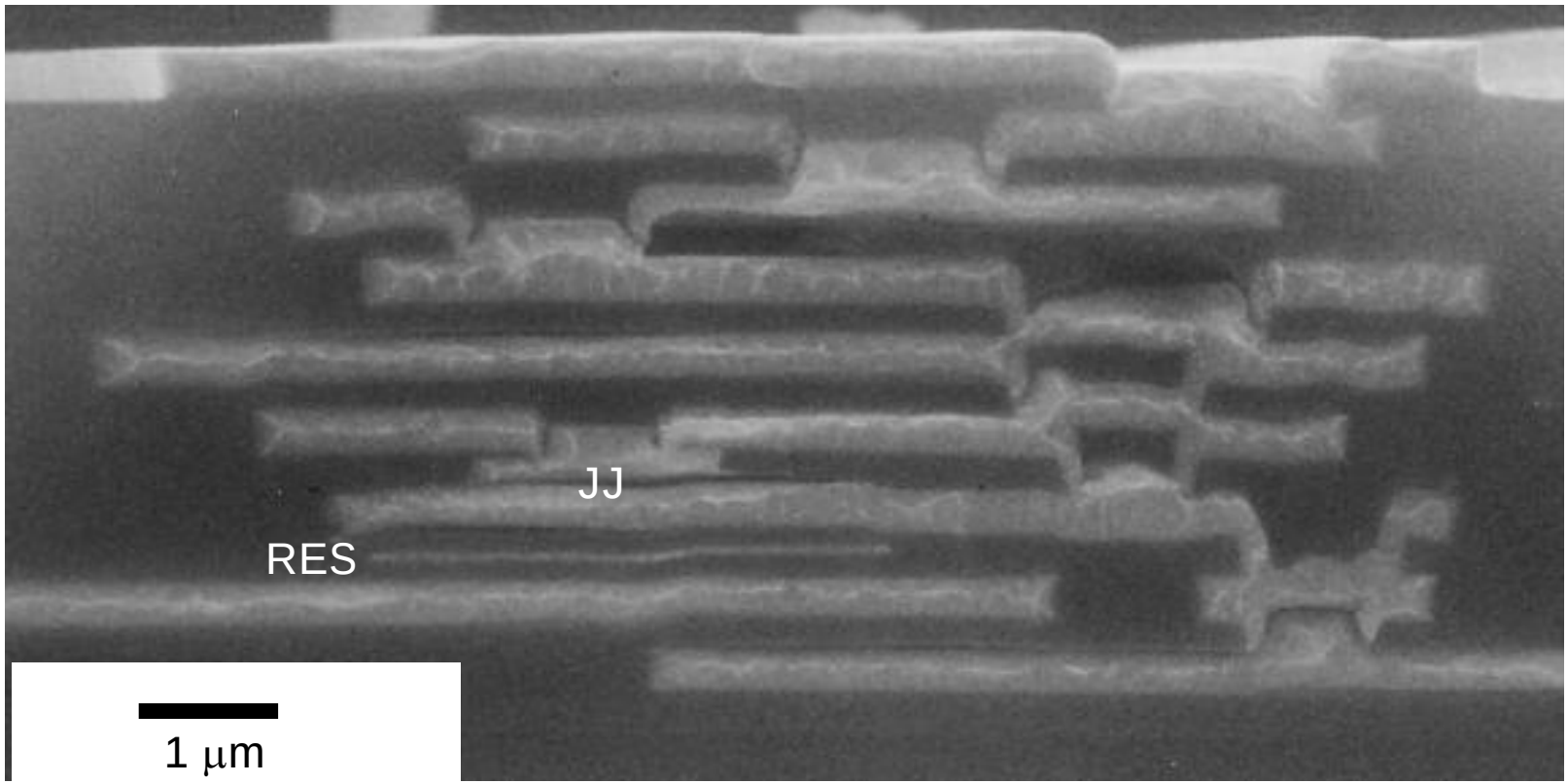
Nb-NbN 3µm technology



Implementation of a 8 bit shift register circuit with a new Nb-NbN 3µm technology developed at CEA-Grenoble MTS-Foundry; (the design of a similar 16-bit shift register done by University of Savoie is represented in the upper part of the figure).

Fabrication process (NEC Japan)



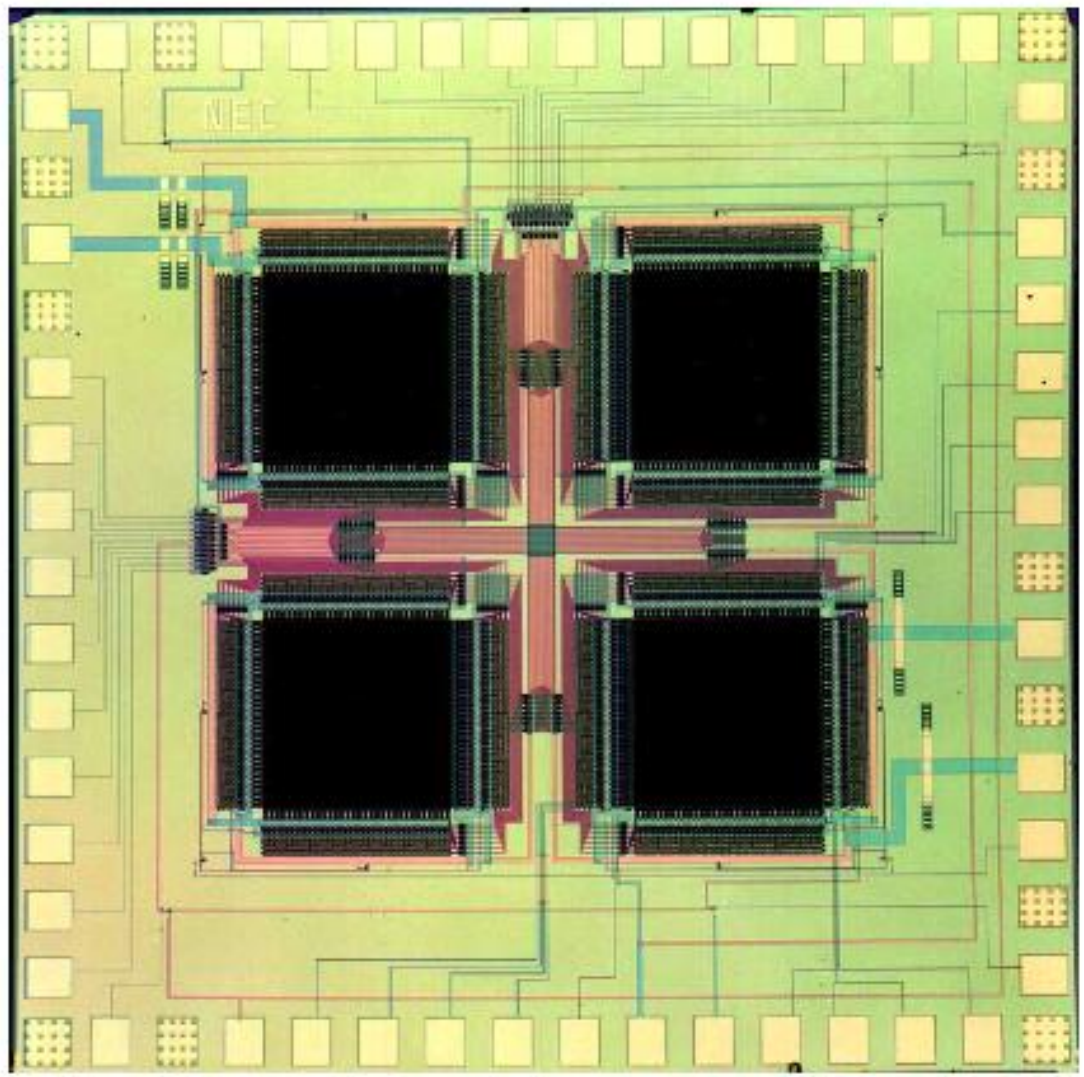


Features

- 9 Nb layers with planarized SiO_2.
- Nb/AlOx/Nb JJs with J_c of 10 kA/cm^2.
- Reduced feature size to 0.8 μm.

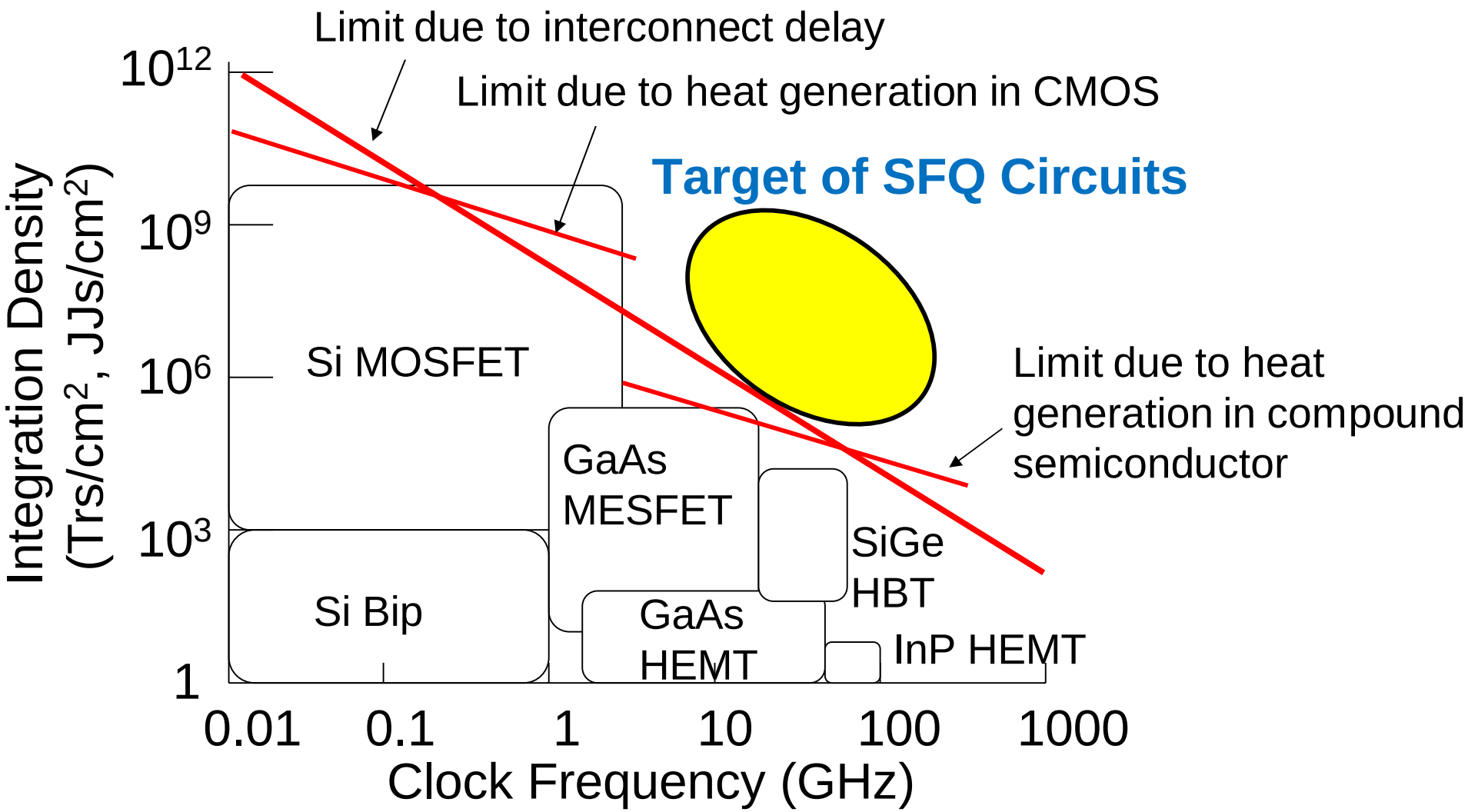
High Yield
High Speed
High Density

16kbit memory



NEC

Superconducting vs Semiconducting Digital Electronics



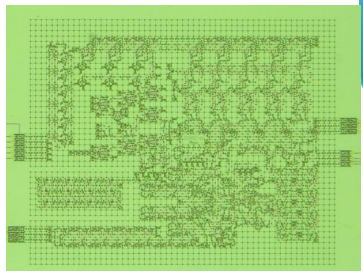
RSFQ CPU development

Bit-Serial Architecture (Complexity-Reduced)

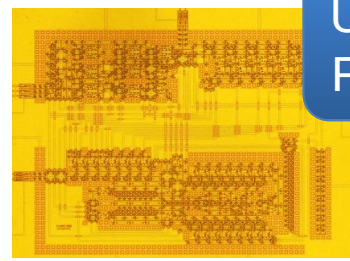
Bit-Slice/Parallel Architecture

Energy-efficiency

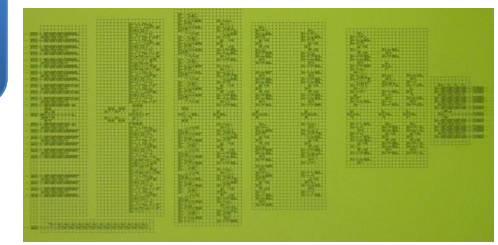
Ultra High-Frequency



CORE1α LV (2013)
3869 JJs, 35 GHz
400 MIPS, 0.23 mW

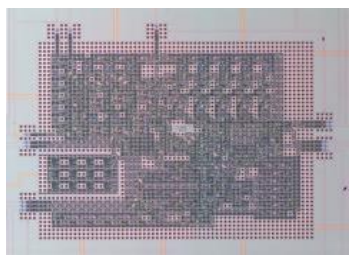


CORE100 MPU (2015)
Bit-serial μP no memory
100 GHz, 3073 JJs 3073 JJs
800 MIPS 1.0 mW 800
GIPS/W

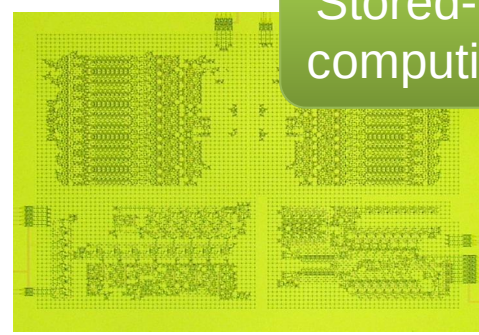


Bit-Parallel μP 50 GHz ALU
8b bit-parallel ALU (2017)
50 GHz, 4868 JJs
1.4 mW 36000 GIPS/W
Gate-Level Pipelining

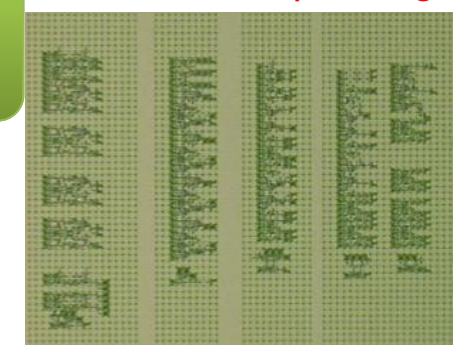
Stored-program computing demo



CORE1α MPU (2003)
15 GHz, 4999 JJs
167 MIPS, 1.6 mW



CORE e2 MPU (2014–2016)
Bit-serial μP Memory Embedded
50 GHz, 10000–20000+ JJs
500 MIPS 2.4 mW 210 GIPS/W

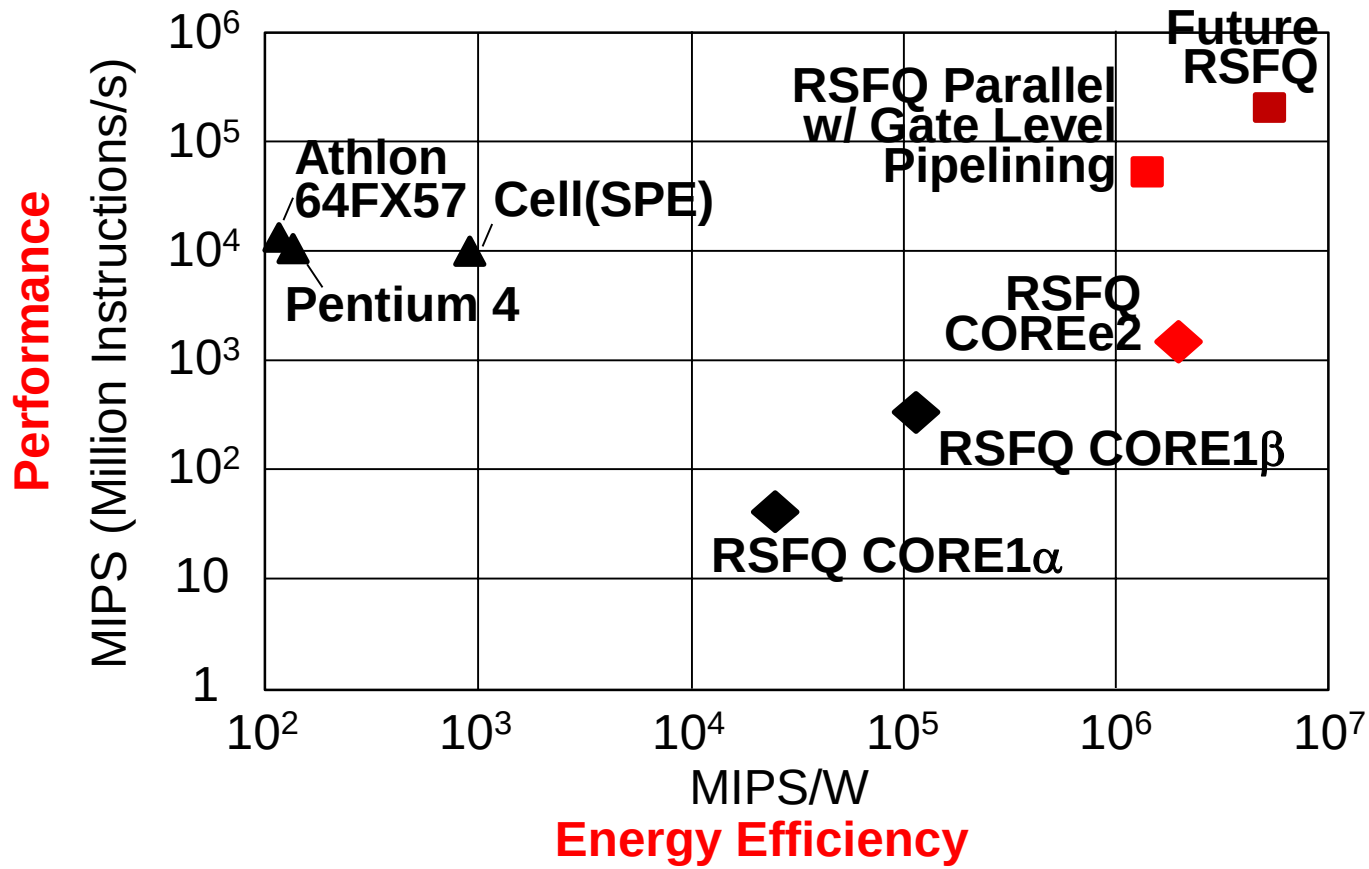


bit-slice ALU (2015)
50 GHz, 3481 JJs

NAGOYA UNIVERSITY · YOKOHAMA National University · 京都大学 KYOTO UNIVERSITY · KYUSHU UNIVERSITY · CRAVITY AIST

Masamitsu Tanaka et al. High-Throughput Bit-Parallel Arithmetic Logic Unit Using Rapid Single-Flux-Quantum Logic, IEEE TAS 2017

Superconducting vs Semiconducting Digital Electronics



Estimation of performances of a 32-bit single-core microprocessor based on the experiments

Main Issues Left for Practical Applications

High-frequency operation of bit-parallel processing

Energy-efficient SFQ circuits

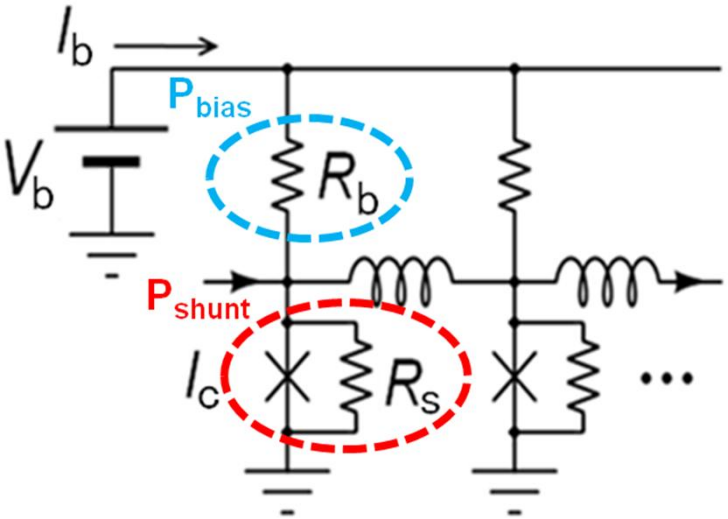
Energy-efficient power supply for dc-powered SFQ circuits

Large capacity **memory**

Interfacing between SFQ circuits and room temperature electronics

Large scale integration

Issue for Energy-Efficiency



R_b is used for providing a constant current to each Josephson junction.

Power consumption at R_b
(Static power consumption)

$$P_{\text{bias}} = \frac{V_b^2}{R_b} \approx 0.7 I_c V_b$$

Example: DFF
$P_{\text{bias}} = 1.8\mu\text{W}$

Power consumption at R_s
(Dynamic power consumption)

$$P_{\text{shunt}} = f I_c \Phi_0$$

f: operating frequency

Example: DFF
$P_{\text{shunt}} = 36n\text{W}$

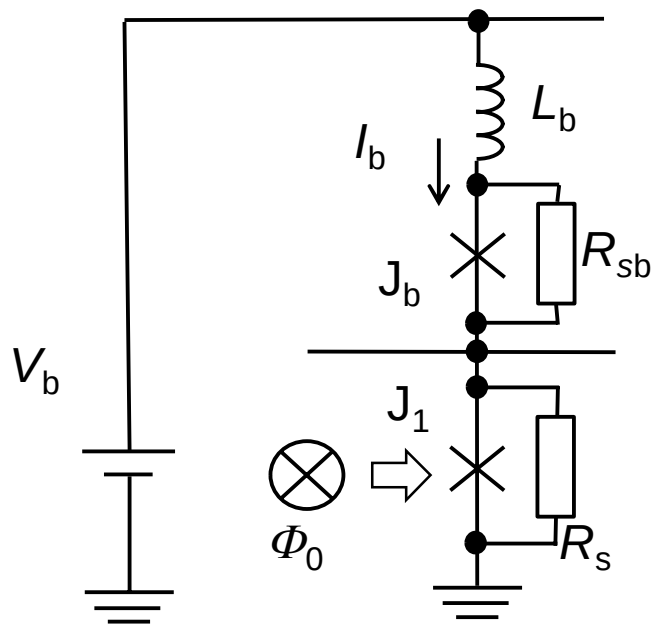
Typically, $I_c \Phi_0 \approx 2 \times 10^{-19} (J)$

Necessity for eliminating static power consumption.

DC-Powered Energy-Efficient SFQ Circuits

Bias resistors are replaced with inductors and junctions.

ERSFQ circuit (Hypres)



D. E. Kirichenko, et al., IEEE Trans. Appl. Supercond., **21**, 776(2011).

Advantage

- The base of design has been established because resources obtained from the RSFQ circuits can be used.
- PTLs can be used as interconnects.
- Possibly suitable to higher density because no mutual coupling is used.

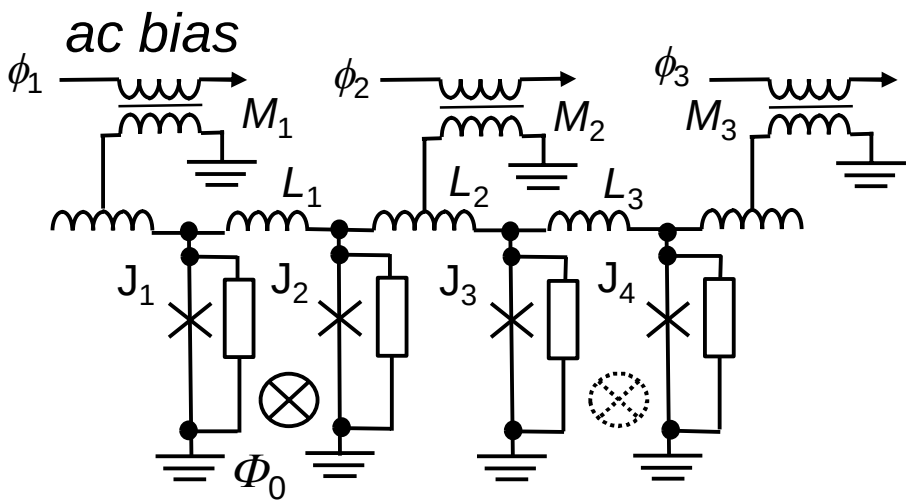
Disadvantage

- Difficult to make energy-efficient voltage supply around 0.1 mV.

AC-Powered Energy-Efficient SFQ Circuits

Circuits are driven by AC currents provided via transformers.

Example
Reciprocal Quantum Logic
(Northrop Grumman)



Q. P. Herr, et al., J. Appl. Phys., **109**, 103903 (2011).

Advantage

- Provided AC currents are used as clock signals.
- NOT logic is easy to be made.
- The above means the RQL can be made up of smaller number of junctions.

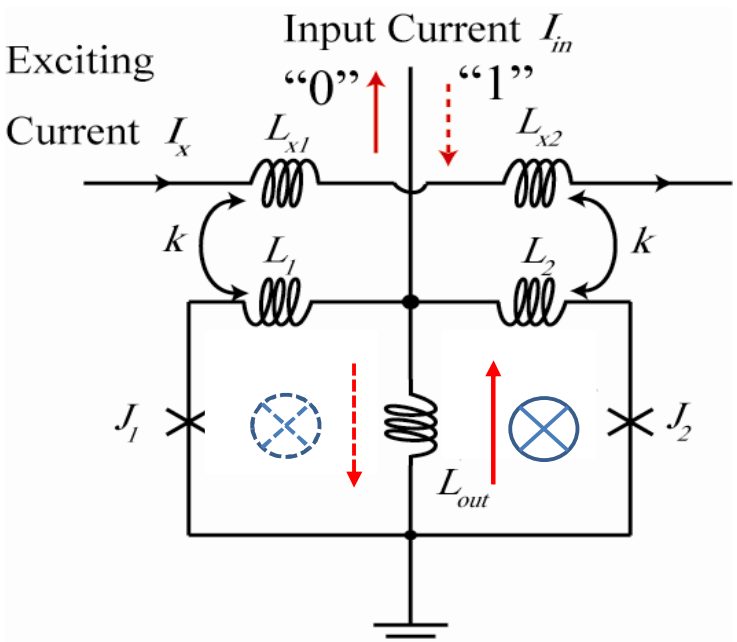
Disadvantage

- Transformers are needed for all the gates, indicating downsizing to sub-micron scale is difficult.
- High-frequency design technique is essential for operation.

AC-Powered Energy-Efficient SFQ Circuits

Circuits are driven by AC currents provided via transformers.

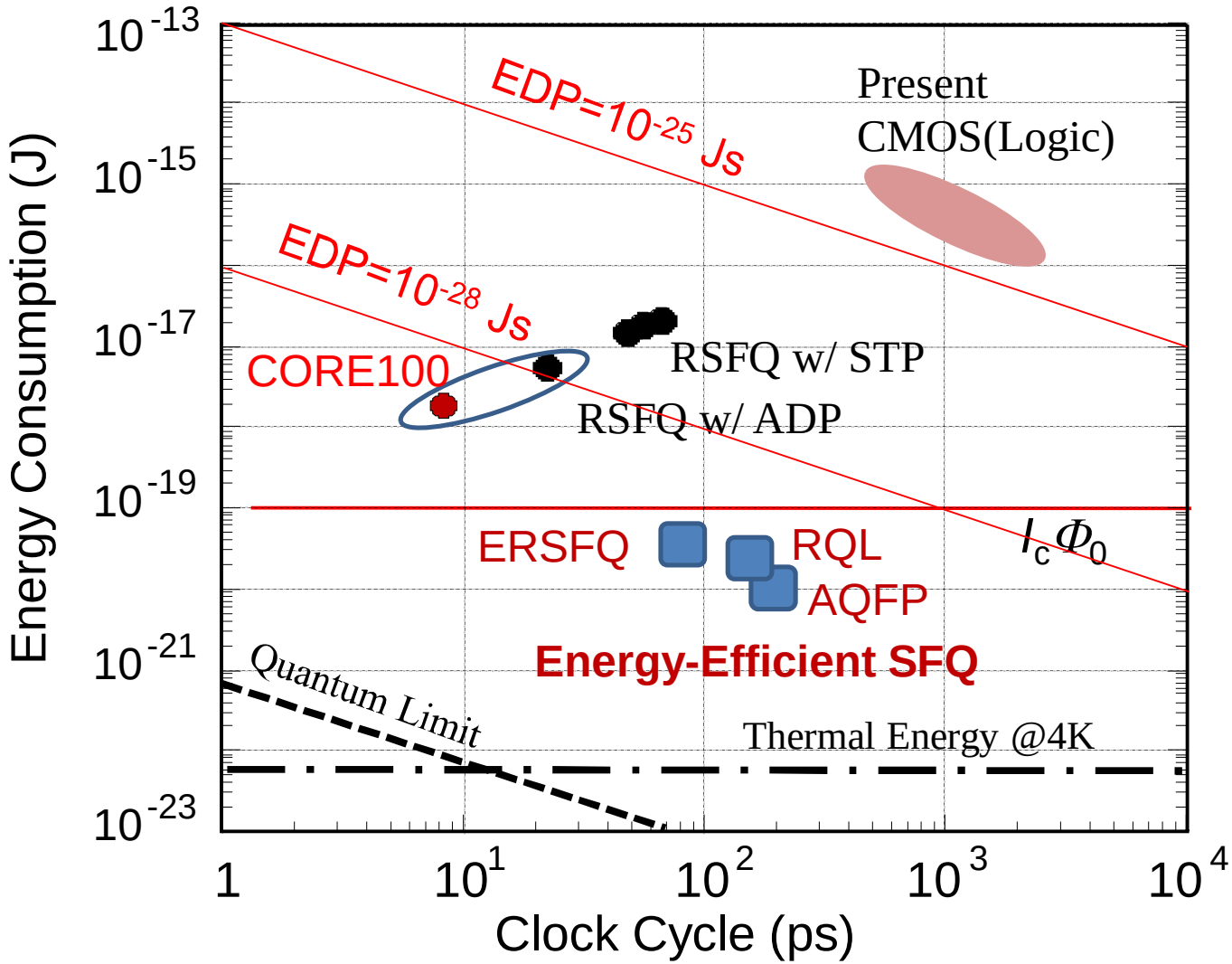
Example
Adiabatic Quantum Flux Parametron
(Yokohama Nat'l Univ.)



Advantage
- Very small energy consumption because of no phase jump in switching.
- All the logic operations are achieved based on a single 'majority' gate, leading to the robustness to the process variation.

Disadvantage
- Operating frequency is relatively low.
- Difficult to make long interconnects.
- DC offset currents are needed for operation.

Energy-Efficiency in Superconducting Digital Circuits

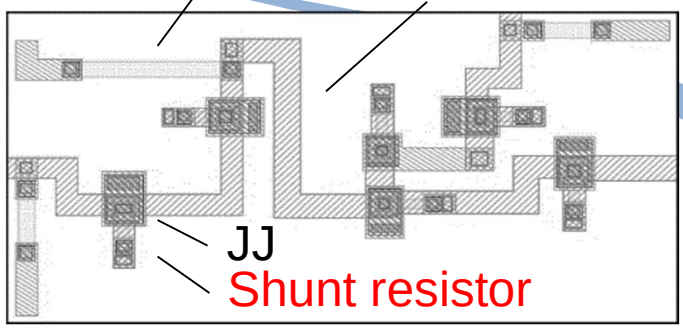


$$\text{Energy Consumption} = \frac{\text{Total power x Clk cycle}}{\text{Number of devices}}$$

STP: AIST 2.5-kA/cm^2 Nb/AlO$_x$/Nb Standard Integrated Circuit Process.

ADP: AIST 10-kA/cm^2 Nb/AlO$_x$/Nb Advanced Integrated Circuit Process

Issues for Large Scale Integration

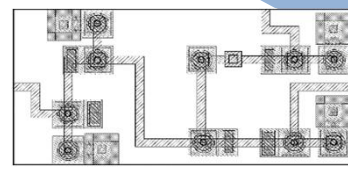


D Flip-Flop: 40 x 80 μm

(Assuming Min. I_c = 50 μA)

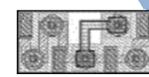
- Shunt-resistor-free JJs
- ERSFQ/eSFQ

(Elimination of resistors)



20 x 40 μm

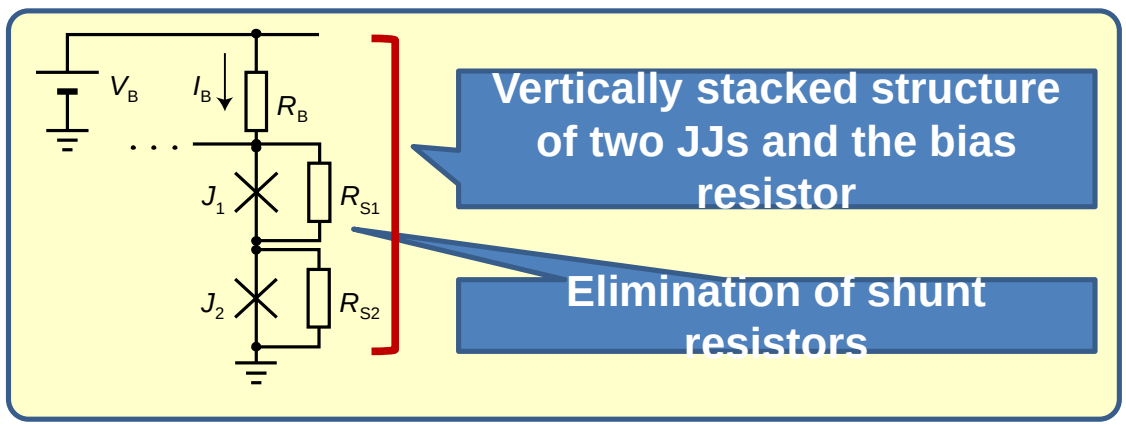
- High Sheet Inductance (NbN, etc.)
- JJ Stack



8 x 16 μm

- Equipment update

2 x 4 μm



Line and space: 1μm

0.25μm

The Memory issue

IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, VOL. 23, NO. 3, JUNE 2013

Energy-Efficient Superconducting Computing—Power Budgets and Requirements

D. Scott Holmes, *Senior Member, IEEE*, Andrew L. Ripple, and Marc A. Manheimer

available cryogenic refrigerators. The goal seems worthy and the technologies required to build such computers appear to be available or within reach with the notable exception of memory. If suitable memories become available, significant work remains in the areas of circuit density, computer architecture, fabrication, packaging, testing, and system integration.

A major difficulty for superconductive electronics is the low integration scale available today (about five orders of magnitude larger). In particular memory elements are currently based of flux quanta trapped in a superconducting loop and represent a critical point with their minimum cell size of the order of **15 μm × 15 μm**.

New proposals to build superconducting memories have been made, mostly employing **hybrid Josephson junction – CMOS RAM**, and **Magnetic Josephson Junctions (MJJ)**

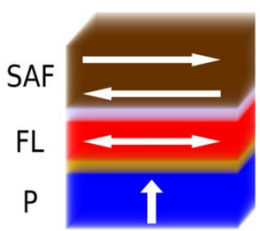
Cryogenic Magnetic Memories

Hybrid circuits with cryogenic magnetoresistive memory elements (JJ+metal spintronics)

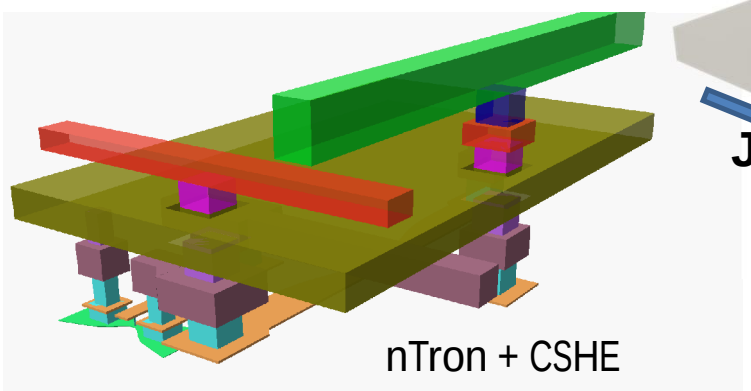
Memory cell based on spintronic elements with addition of JJs (for low impedance) or nanowire switches (for high impedance)

Memory devices:

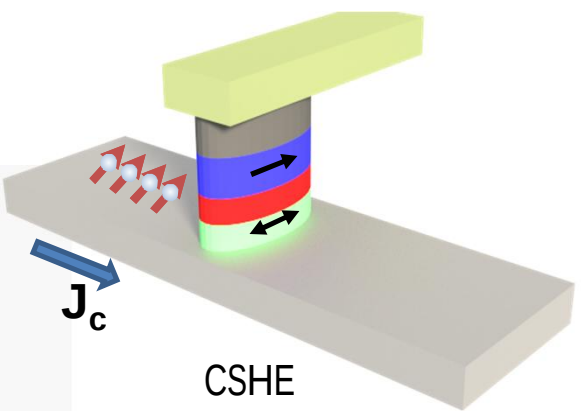
- Cryogenic Spin Torque transfer (CST)
- Cryogenic Spin Hall effect (CSHE) elements
- JJ periphery (address decoders, sense, etc.)



COST

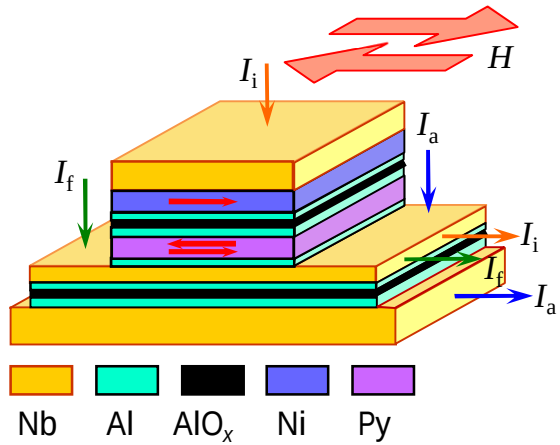


nTron + CSHE

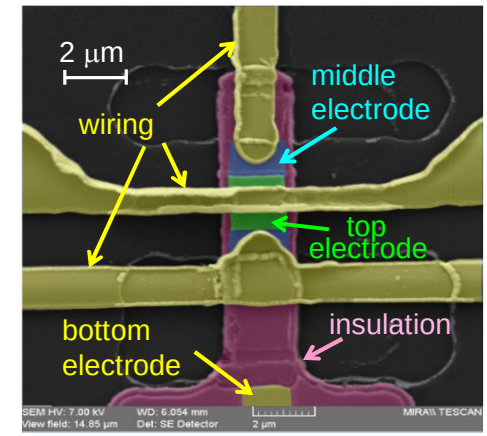


CSHE

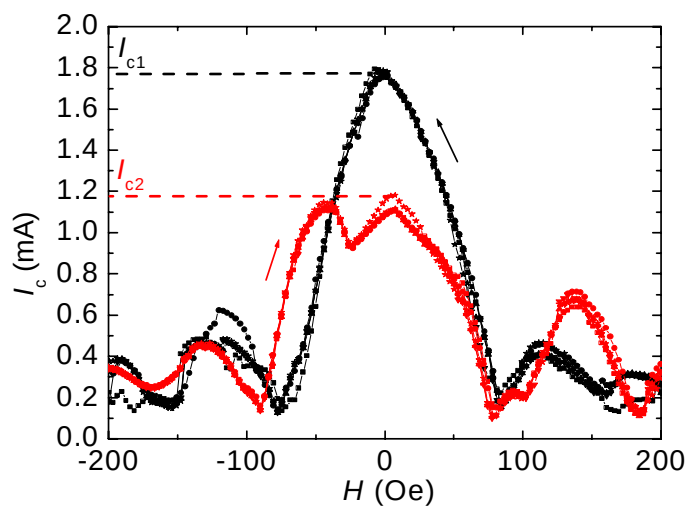
Cryogenic Magnetic Memories



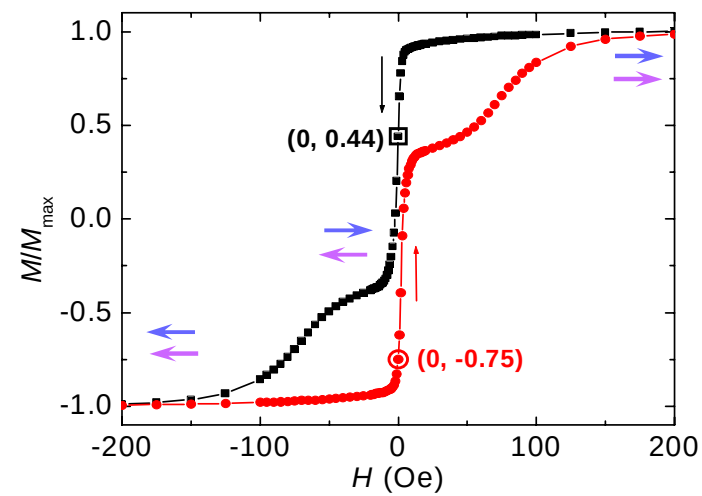
Schematic view of a four-terminal $SISF_1IF_2S$ device and its biasing



SEM micrograph of an actual $SISF_1IF_2S$ device



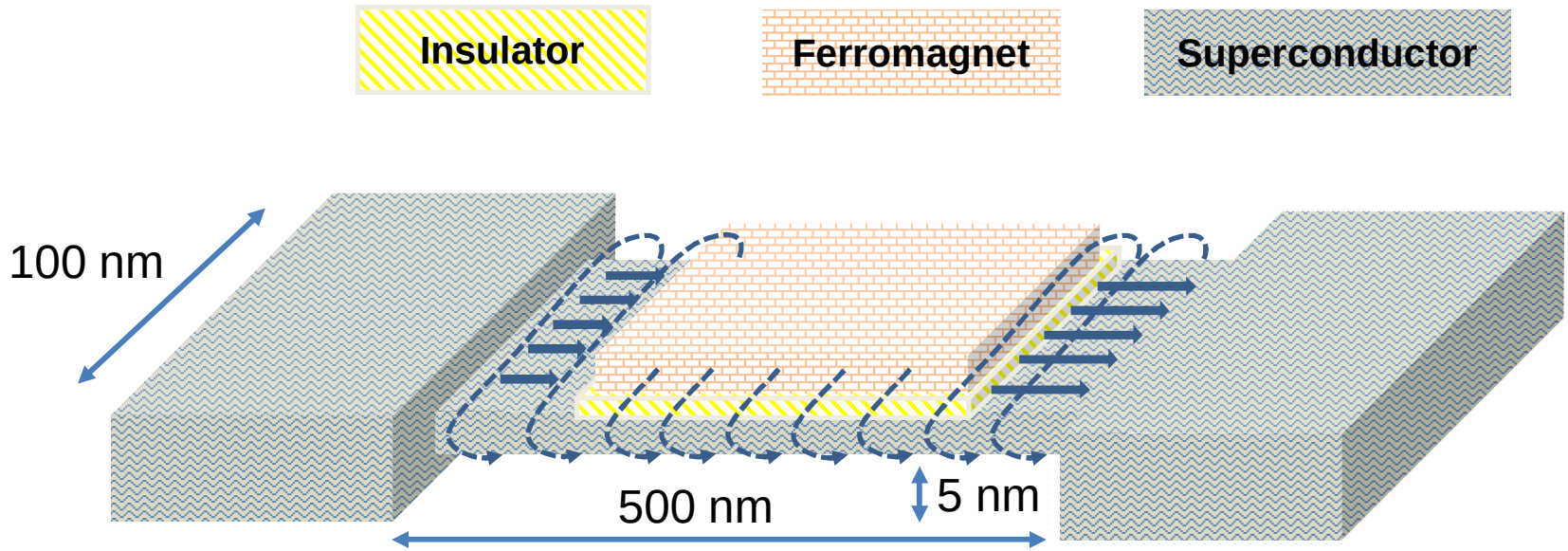
$I_c(H)$ dependence for the SIS junction while sweeping an external in-plane magnetic field in two opposite directions (five overlapped curves for five consecutive scans are shown).



$M(H)$ dependence at 10 K for 5 mm × 11 mm chip with unpatterned $SISF_1IF_2S$ multilayer used to fabricate the four-terminal devices. $|M/M_{max}|$ has two considerably different values at H=0, which correlates with the $I_c(H)$ dependence.

Ivan P. Nevirkovets et al., A multi-terminal superconducting-ferromagnetic device with magnetically-tunable supercurrent for memory application, IEEE TAS 2018

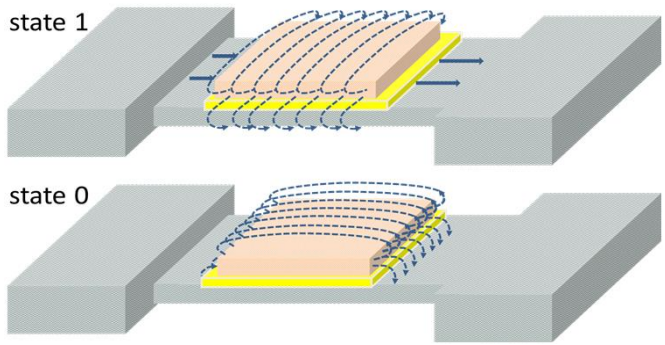
Superconducting Nanowire Memory device



The device is based on the **Heat Assisted Magnetic Recording**, a technique being explored for next generation hard disks. The idea is to heat a small magnetic volume and bring it above its Curie temperature for a short time. At the same time a magnetic field is applied that, although much smaller of the coercive field at the base temperature, can induce a magnetization in the affected volume while it is still cooling.

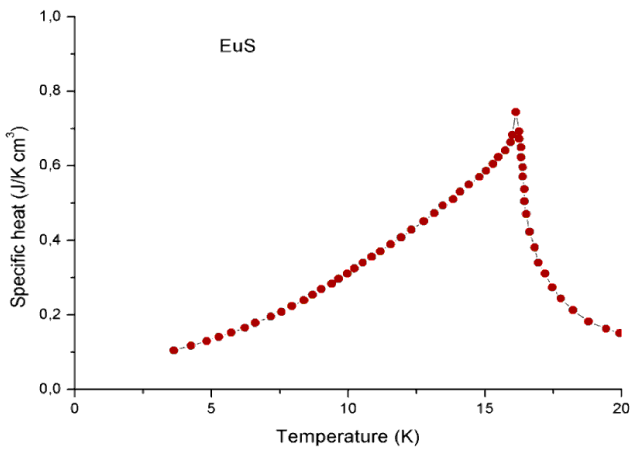
Advantages: sub-micrometer memory cell size, ns write and read operation, non destructive reading, static memory operation

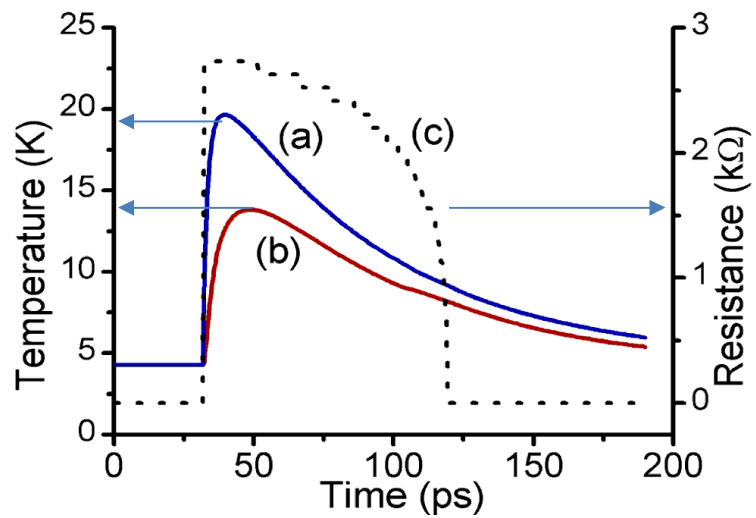
Issues: identify proper magnetic material (low Tcurie), optimize superconducting/ferromagnetic interface, develop proper digital read/write circuits

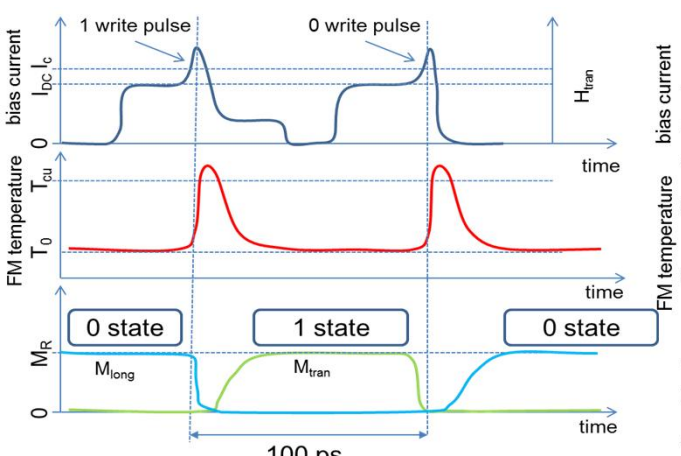


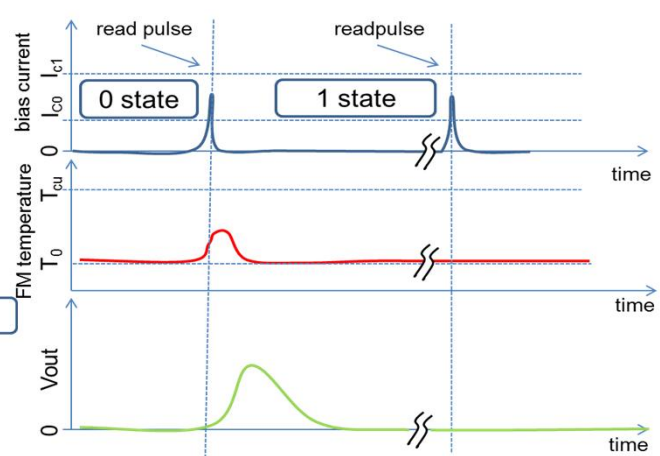
Logic state 1: residual magnetization perpendicular to current flow and with field lines not crossing the nanowire, **obtained by cooling the ferromagnet in presence of a small bias current**

Logic state 0: Residual magnetization parallel to current flow and with field lines crossing the nanowire, **obtained by cooling the ferromagnet in absence of bias current**









Few words on quantum computing

Universal fault-tolerant quantum computer

The holy grail of quantum information science. Allows one to run useful quantum algorithms which achieve exponential speed ups over their classical counterparts. However the overhead of quantum error correction estimates **1M-5M qubits**

Approximate quantum computer

A quantum device which does not need fault tolerance, with the goal of demonstrating a useful application by interacting with a classical computing system, e.g. quantum chemistry, optimization. Estimate **1K-5K qubits**

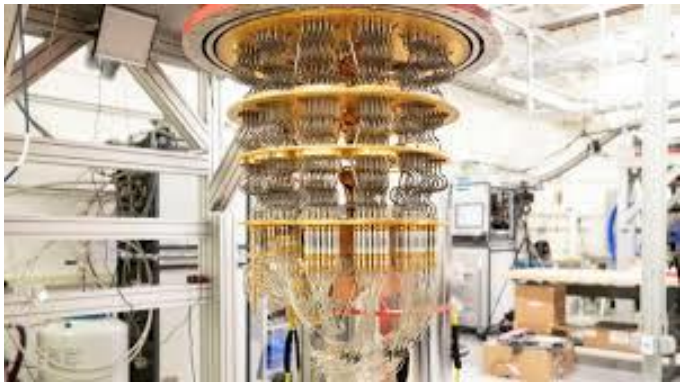
Quantum Advantage/Supremacy*

Quantum advantage is an idea that before any useful quantum computer is built it may be possible to demonstrate a special purpose application whose output cannot be simulated as fast using existing classical computers. Estimate **50-100 qubits**

*Arute, F., Arya, K., Babbush, R. et al. Quantum supremacy using a programmable superconducting processor. Nature 574, 505–510 (2019). 53 Qubits 200s instead of 10.000years (IBM claims 2.5days)

Superconducting digital logic for Quantum Computing

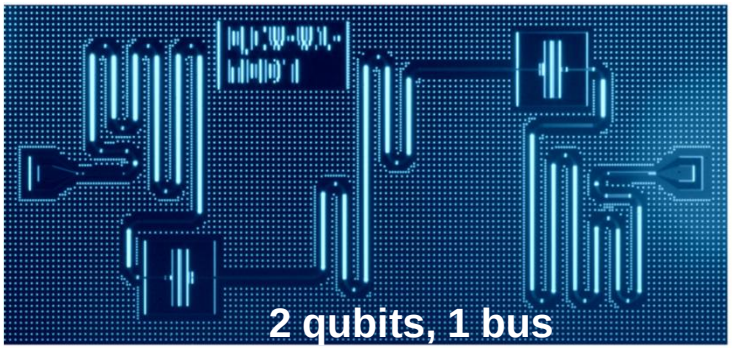
Today existing Quantum computers operate at very low temperatures (**10-20 mK**) and are **based on superconductors and Josephson junctions**

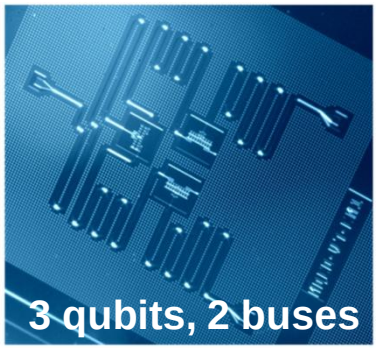


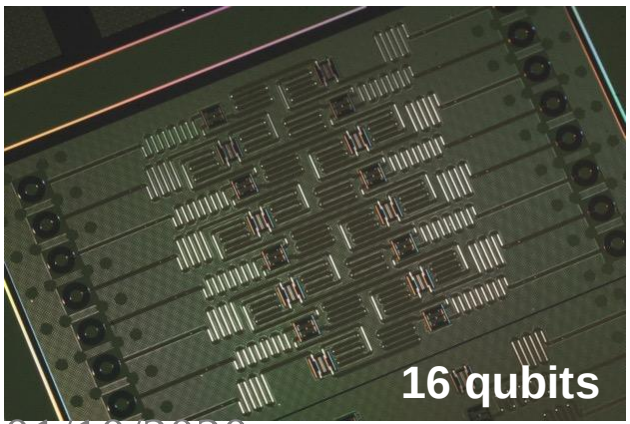
each Qubit requires interconnection to room other Qubits and to room temperature electronics to be programmed and read.

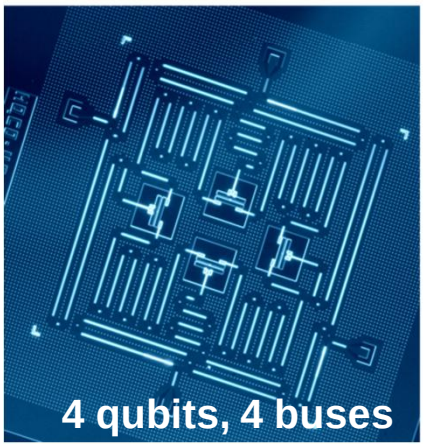
as the number of needed Qubits increases, there is a limit to the feasible number of connections from LT to RT

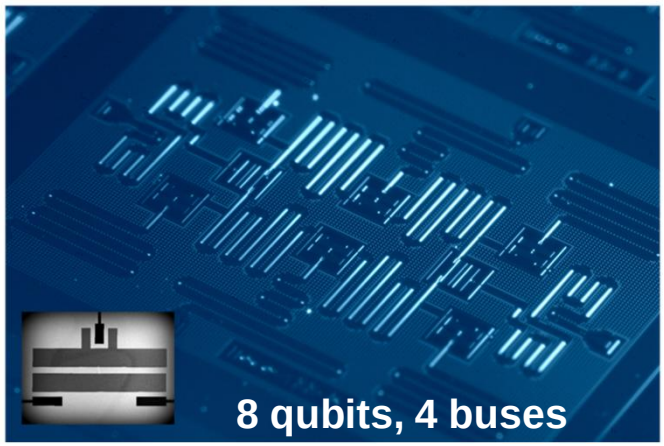
Local superconducting control electronics, already at LT although not at 20 mK, could overcome this difficulty and allow scaling up of number of Qubits



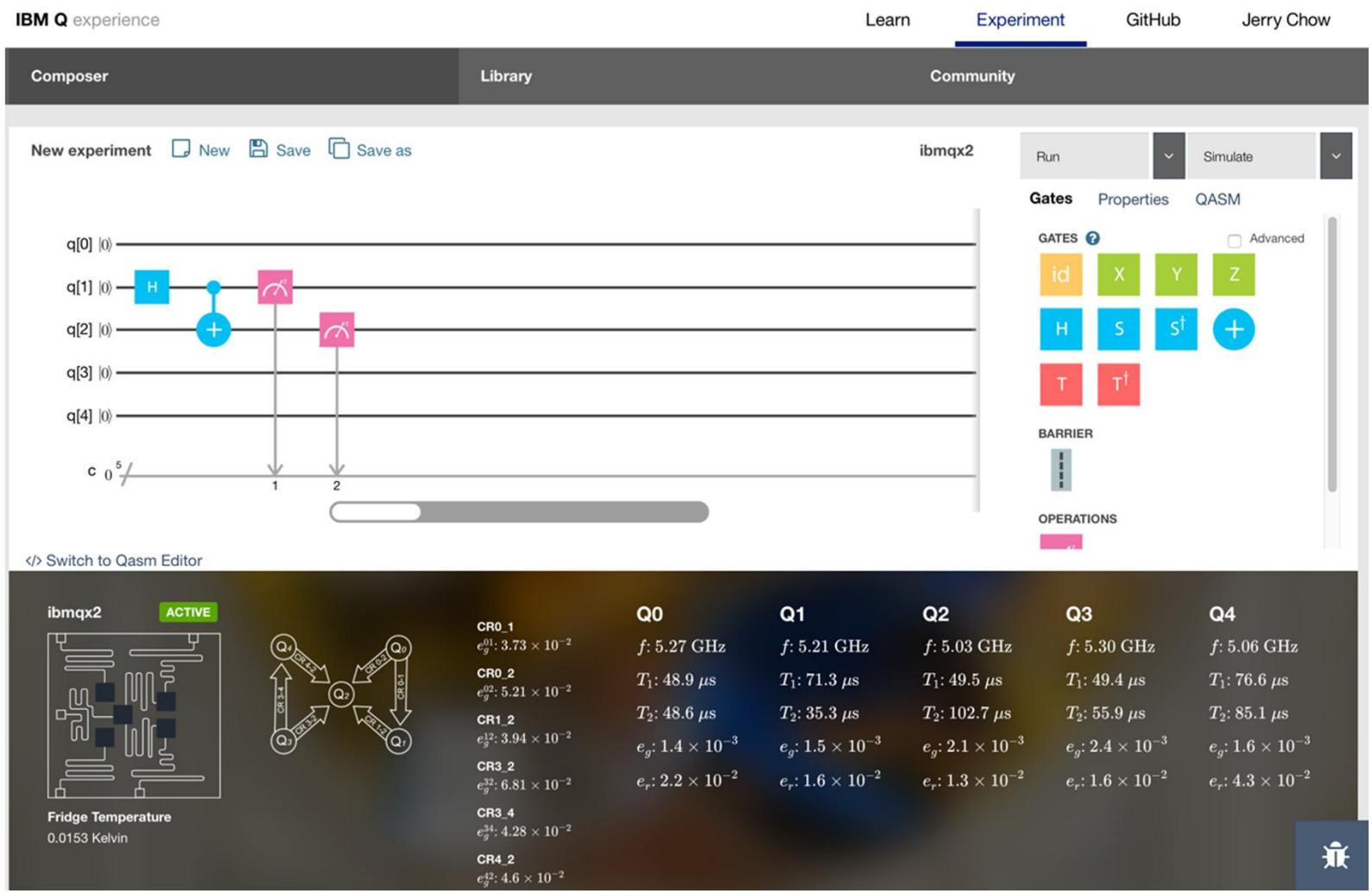








IBM Q experience



Launched May 2017

Program 5 qubit quantum processor from any web browser