

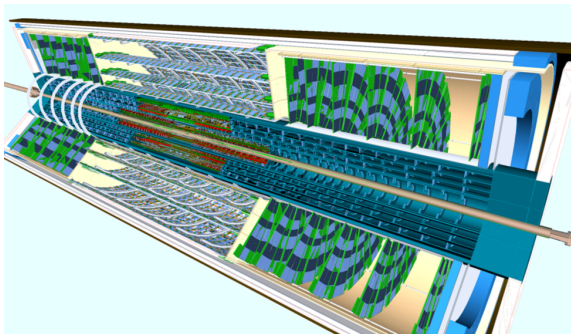
# Testing prototype ASICs setup for ATLAS ITk strips upgrade

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# ITk layout

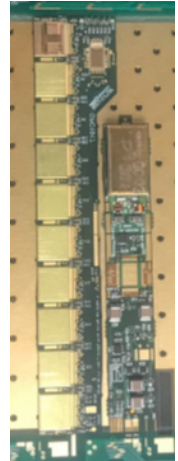
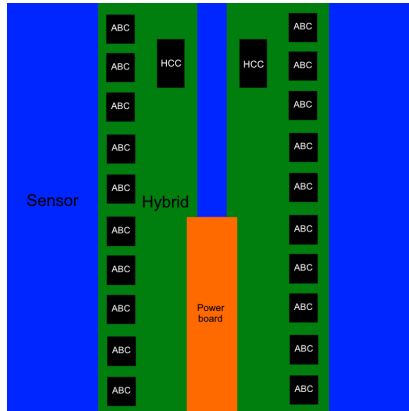
- Inner tracker consists of two sections: the ITk pixel detector (inner layer) and ITk strip detector (outer layer)
- ITk strip detector consists of four barrels and six disks in the endcap, covering  $\pm 2.5$  units of rapidity



LHCC-2017-005

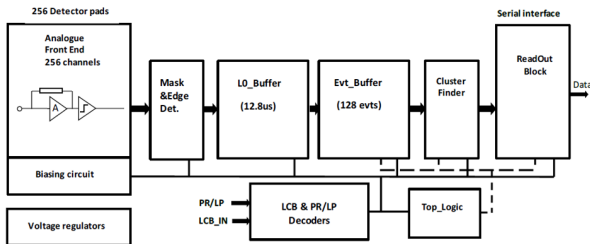
# ITk strip modules

- Barrels consist of staves, each with 28 modules
- Modules consist of sensor, two hybrids, and a power board



# ABCStar ASIC

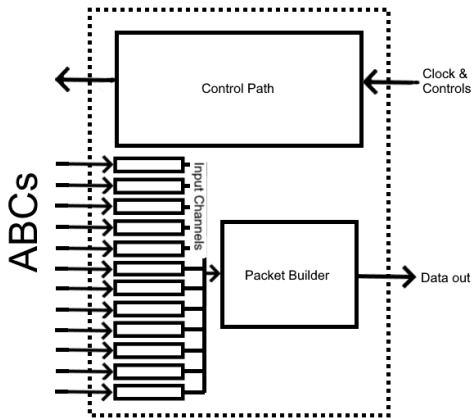
- ABCStar (ATLAS Binary Chip) processes signals from silicon strip detector
- Connects to 256 detector strips



*ABCStar Specification 7.66*

# HCCStar ASIC

- HCCStar (Hybrid Controller Chip) interfaces between front-end (ABCStar) and controller
- Receives BC clock, triggers and command input, sends to ABCStar
- Receives, packages, and outputs data from ABC chips in packets



*Adapted from HCCStar Specification 1.0e*

## ...and more

- AMAC (Autonomous Monitor And Control) chip monitors and controls voltages
- AMAC located on power board
- IpGPTx (low power GigaBit Transceiver) and VTRx+ (Versatile Transceiver) together convert commands from optical to electrical signal, and data from electrical to optical signal
- Not located on module, but on End of Substructure (EoS) card

# YARR: Yet Another Rapid Readout

YARR has 4 configurable components:

- 1 Scan engine sets parameters and sends triggers to ASICs setup, and receives data
- 2 Data processor reads raw data into events, associating hits with time
- 3 Histogrammer creates histograms for each event, as specified
- 4 Analysis produces output from histograms as desired



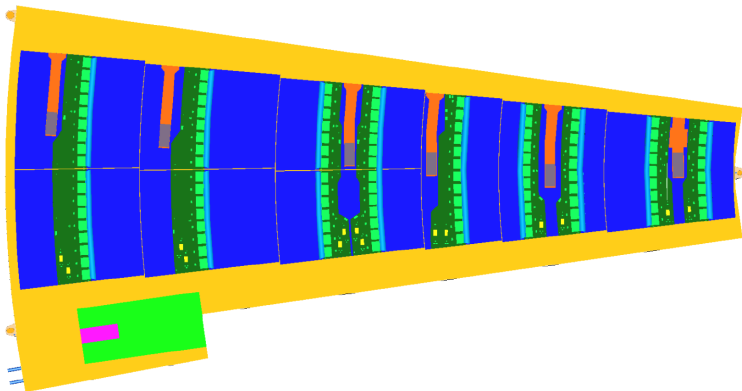
*YARR Gitlab*

# Examples

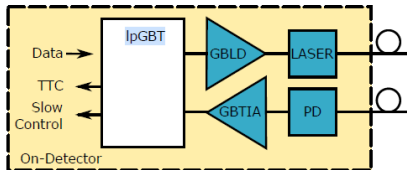
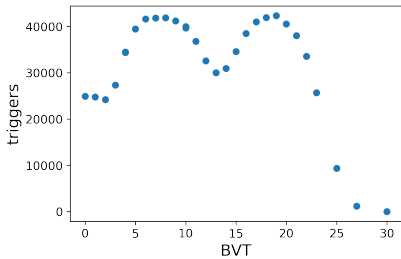
- Problems with YARR frequency handling
  - Specifying KHz trigger frequencies above single digits causes no increase in the number of packets received
  - Lower frequencies do not increase count linearly
  - Small bug in YARR with handling of frequency units explains cap, discrepancy between real time and “theoretical” trigger delays explains strange behavior
- BVT value
  - 8 bits in ABCStar register determine differential voltage offset in comparator stage of front-end
  - Ranges between 0 and -550 mV, not clear exactly how these values are determined







*ITk Strip Detector TDR*



*ITk Strip Detector TDR*