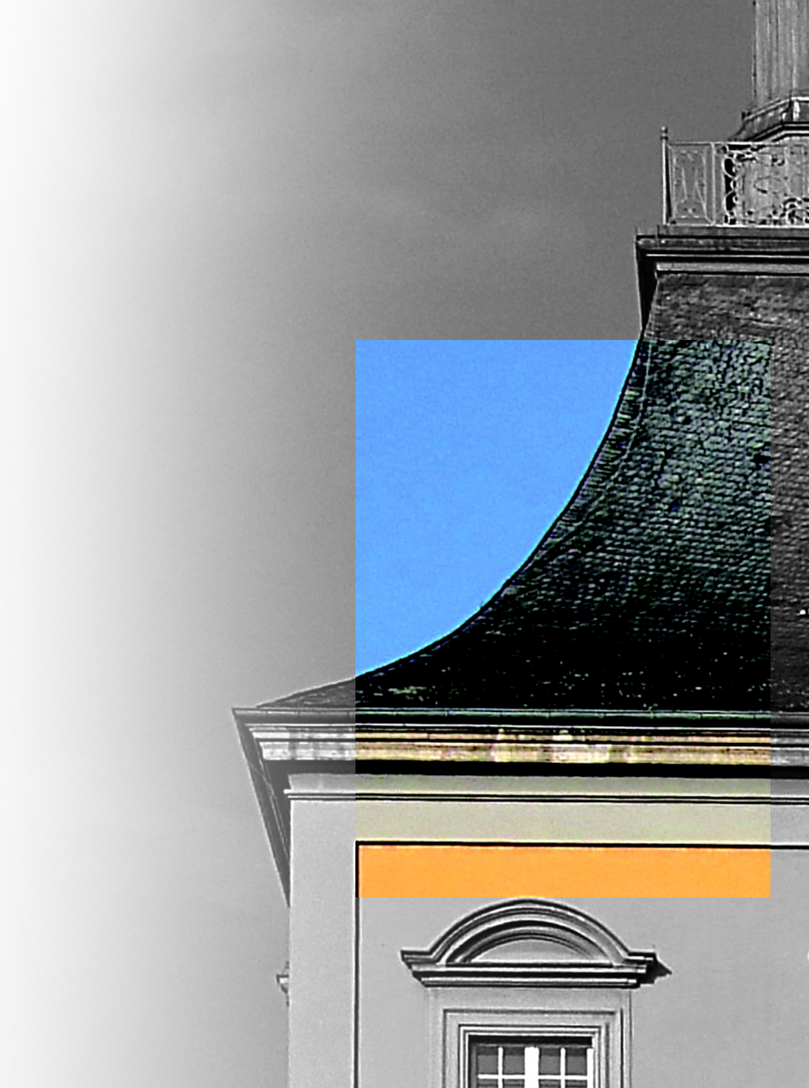
MONOPIX -
RADIATION HARD MONOLITHIC CMOS PIXEL DETECTORS

NORBERT WERMES (UNIVERSITY OF BONN)

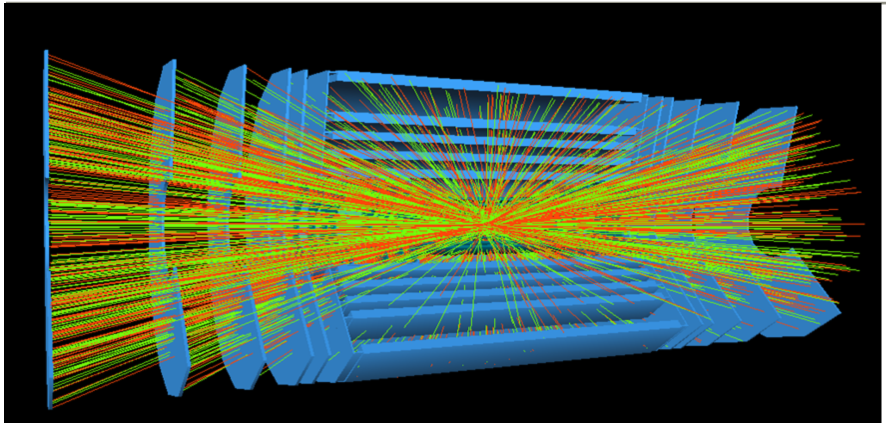


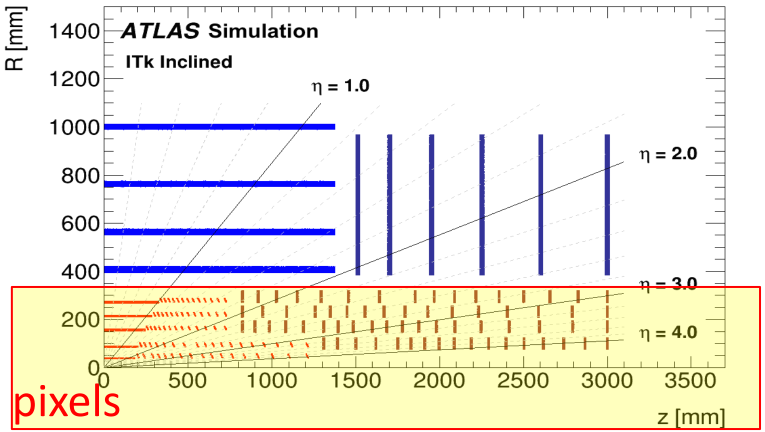
CERN, EP Detector Seminar, Feb. 07, 2020

OUTLINE

- Setting the stage
- The Monopix developments at UBonn (in coll. w/ CERN, CPPM, IRFU)
- Results on LF-Monopix1 and TJ-Monopix1
- The Monopix2's
- (Impressions on Bonn's new FTD)

TRACKER UPGRADES @ HL-LHC





- **2024/25++: Phase 2 ATLAS/CMS** completely replace their trackers to face the very fierce environment

- ATLAS:
  ~ 165 m^2 silicon strips
  ~ 12 m^2 silicon pixels (currently 2m^2)

- CMS:
  ~ 220 m^2 silicon strips
  ~ 5-6 m^2 silicon pixels (currently 2m^2)

FIERCE ENVIRONMENT AT THE HL-LHC (PP)

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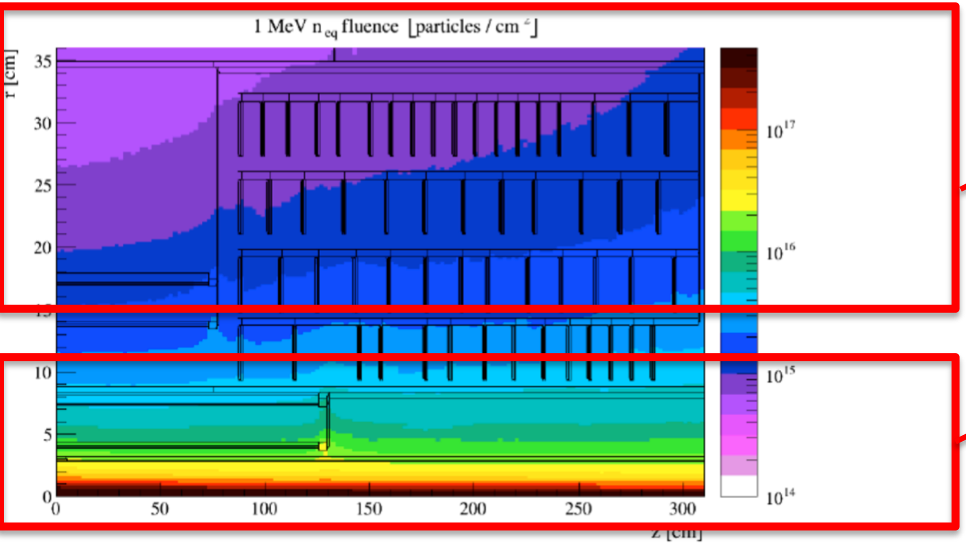
Solution: pixels as much as possible / affordable / buildable in time

Dominating objectives to meet:

Radiation levels, hit rates and 25 ns bunch structure



Strip layers

- NIEL ≈ 10^{14} n_{eq}/cm^2
- TID ≈ 10Mrad
- rate ≈ 30 MHz / cm^2
- Large area O(100m^2)

Outer pixel layer...

- NIEL ... cm^2
- TI...
- rate ... Hz / cm^2
- Large ... ea O(10m^2)

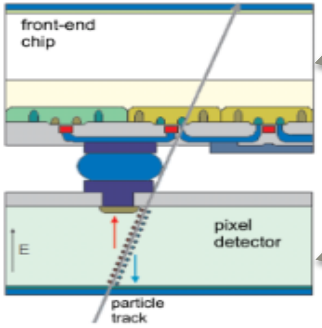
could be CMOS pixels -> DMAPS

Inner layers

- NIEL ≈ 5×10^{15} to 2×10^{16} n_{eq}/cm^2
- TID ≈ 1 Grad
- rate ≈ 3-4 GHz / cm^2
- Smaller area O(1m^2)

INTRODUCING DMAPS

<u>Hybrid detector</u>

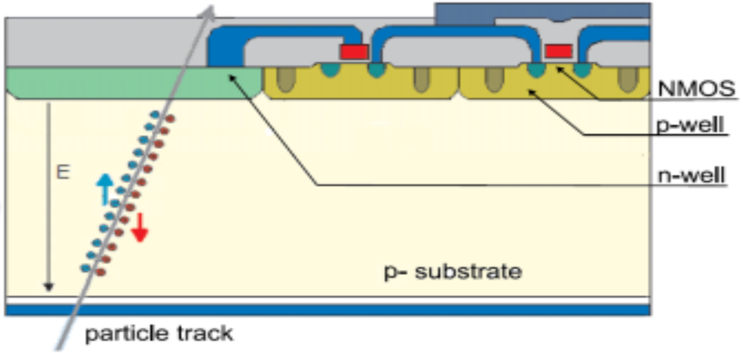


Readout

Sensor

<u>Depleted monolithic active pixel sensor (CMOS)</u>

Sensor & readout



No need for fine pitch bump bonding between sensor and readout circuitry.

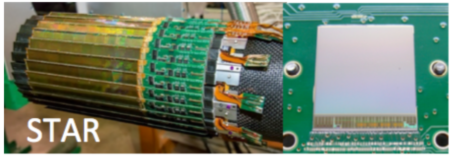
→ **Easier to produce and easier to test (one detector entity)**

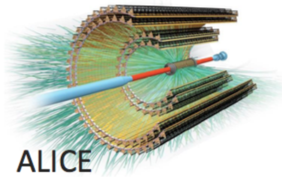
→ Large cost reduction: sensor + R/O chip + BB → one chip

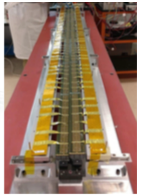
→ Plus all the advantages that large CMOS Fabs may offer, including fast turn around, large wafer sizes, large throughput

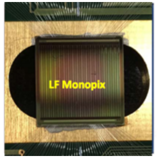
CMOS PIXEL DETECTORS

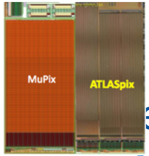
ARE THE FUTURE !
- for particle physics
- for high energy pp
- for pCT
- for imaging appl.
- other ...

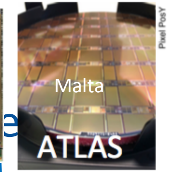












coming next: Belle II upgrade

	RHIC STAR	ALICE-LHC	ILC / CLIC	HL-LHC Outer	HL-LHC Inner
Req. time resolution [ns]	110	20 000	350 / 156	25	25
Particle Rate [MHz / cm^2]	0.4	< 10	< 3	100-200	2000
Fluence [n_{eq} / cm^2]	> 10^{12}	> 10^{13}	< 10^{12}	10^{15}	2 x 10^{16}
Ion. Dose [MRad]	0.2	< 3	< 1	80	> 1000

MAPS (e.g. ALPIDE)

Hybrid pixels -> DMAPS rejected

HL-LHC devm't: radhard (TID & NIEL) + fast response time + fast readout => Q coll. by drift & full R/O arch.

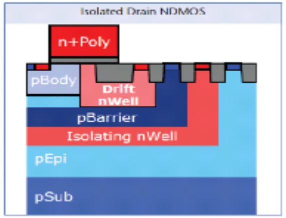
WHAT IS NEEDED TO REALISE (RADHARD) DEPLETED CMOS PIXELS?

$$d \sim \sqrt{\rho \cdot V}$$

1 **“High” Voltage add-ons to apply 50 – 200 V bias**

I. Peric, DOI: 10.1016/j.nima.2007.07.115

2 **“High” Resistivity Substrate (or epi) Wafers (100 Ωcm – kΩ cm)**



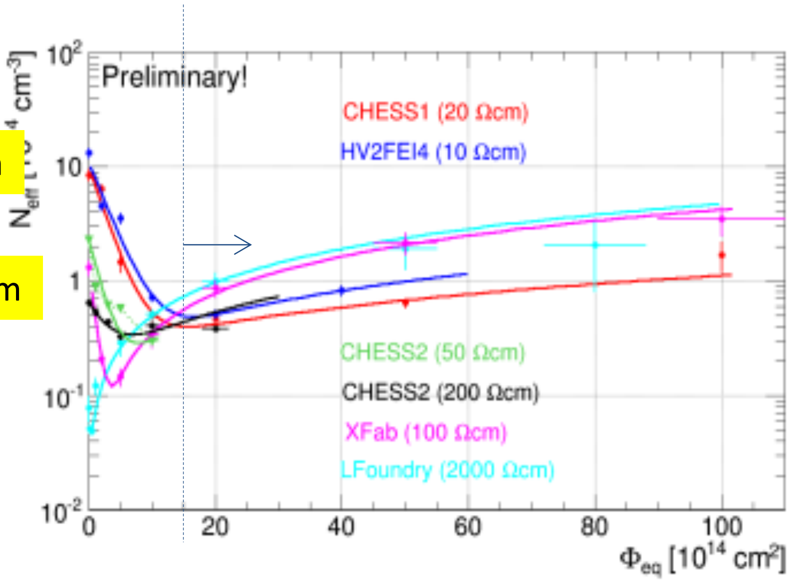
from: www.xfab.com

3 **Multiple (3-4) nested wells (for shielding and full CMOS)**

~10 Ωcm

~100 Ωcm

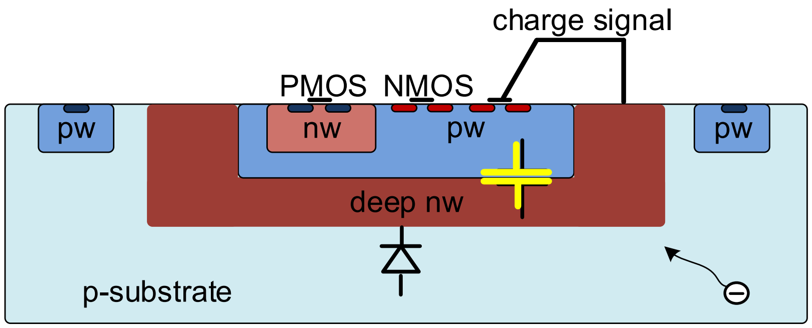
kΩcm

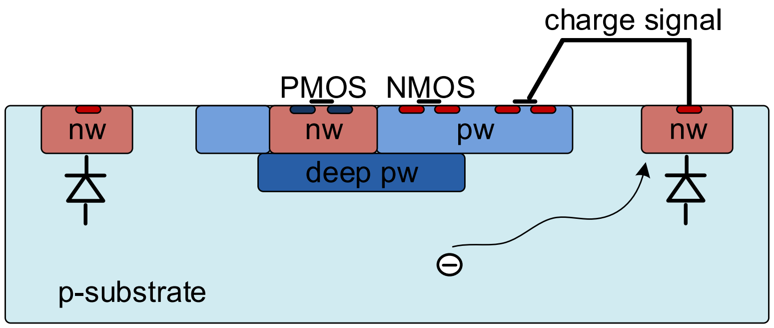


I. Mandic et al., JINST 12 (2017) no.02, P02021

4 **Backside Processing (for thin sensors and back side bias application)**

LARGE VERSUS SMALL COLLECTION ELECTRODE (FILL FACTOR)





Electronics **inside** charge collection well

- **large** collection electrode
  => little low field regions
  => on average **short(er) drift** paths
  => less trapping -> **radiation hard**
- **Larger** sensor **capacitance** (pw & dnw!)
  => noise & speed/power penalty
  => possible x-talk (digital to sensor)

Electronics **outside** charge collection well

- **small** electrode
  => **very small sensor capacitance (< 5fF)**
  => lower analog power budget (noise, speed)
  => less prone to x-talk
- on average long(er) drift distances and potentially low field regions
  → **radiation hardness needs process mods**

E.G. PROCESS MODIFICATION – TOWERJAZZ 180 NM CMOS

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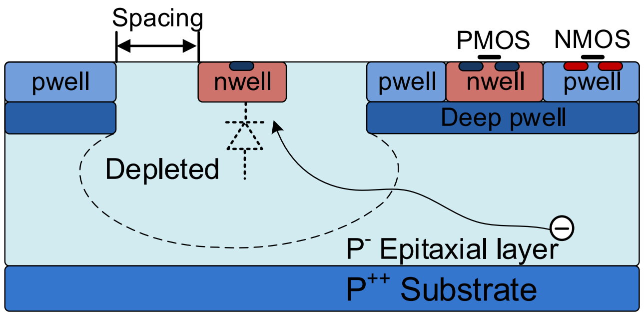
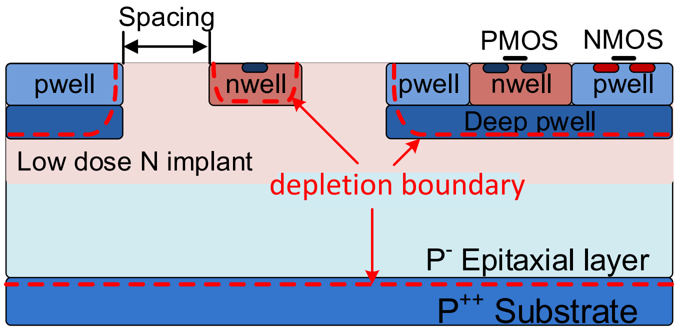


Standard process

- **ALICE ITS type**
- **High res.** **p**-type epi. (> 1 kΩ·cm)
  => thickness typ. **25 µm**
- Quadruple-well
  => deep pwell shields nwell => **full CMOS**
- **Reverse bias** typ. -6V
  => enhanced (but not yet full) depletion
  => some charge collected by diffusion only => slow



Modified process

- Additional planar medium dose **N implant**
  => depletion from two junction boundaries
  full volume can be depleted
  better charge collection in lateral direction
- Maintain small capacitance
- No significant circuit/layout changes

W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046

FOUNDRIES CONSIDERED & CHARACTERISED AT UBONN

XFAB MIXED-SIGNAL FOUNDRY EXPERTS

SOI 180 nm

epc espros photonics corporation

150 nm

LFOUNDRY A SMIC COMPANY

150 nm

TOSHIBA Leading Innovation

130 nm

(GLOBALFOUNDRIES)

130 nm

TOWERJAZZ

180 nm

all feature sizes ≥ 130 nm

LARGE WORLDWIDE INTEREST IN DEPLETED CMOS PIXELS

Institut "Jožef Stefan" Ljubljana, Slovenija

KIT Karlsruher Institut für Technologie

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

Lancaster University

u^b UNIVERSITÄT BERN AEC ALBERT EINSTEIN CENTER FOR FUNDAMENTAL PHYSICS

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

UiO University of Oslo

University of Tsukuba 筑波大学

CSIC Consejo Superior de Investigaciones Científicas

CERN

IFAE

UNIVERSITY OF OXFORD

AGH

design

UNIVERSITY OF BIRMINGHAM

UNIVERSITÉ DE GENÈVE FACULTÉ DES SCIENCES

University of Glasgow

BROOKHAVEN NATIONAL LABORATORY

UNIVERSITÄT BONN

INFN Istituto Nazionale di Fisica Nucleare

Irfu - CEA Saclay Institut de recherche sur les lois fondamentales de l'Univers

Argonne NATIONAL LABORATORY

Yale University

Università degli Studi di Milano; Alma Mater Studiorum A.D. 1088

KEK-JAPAN

UNIVERSITY OF LIVERPOOL

… and more

LF		TJ	
Bonn	CEA/IRFU	CERN	CPPM
large electrode		small electrode	

THE TWO DEVELOPMENT LINES

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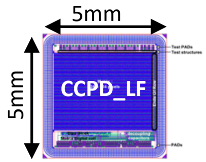
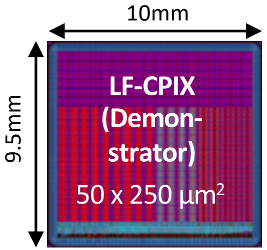


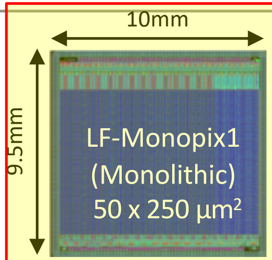
CCPD_LF

- *Subm. **Sep. 2014***
- *Fast R/O coupled to FE-I4*



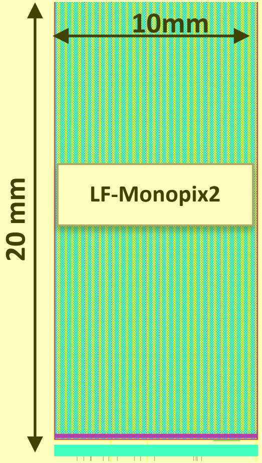
LF-CPIX (DEMO)

- *Subm. **Mar. 2016***
- *Fast R/O coupled to FE-I4*



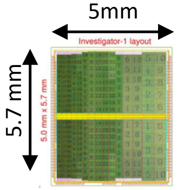
LF-Monopix1

- *Subm. **Aug. 2016***
- *Fast column drain R/O*



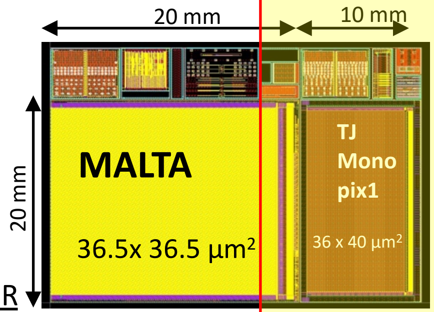
LF-Monopix2

- *subm. **April 2020***
- *50 x 150 μm² pixels*
- *Full height matrix*
- *Fast column drain R/O*



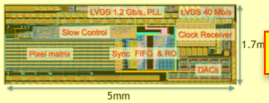
INVESTIGATOR

- ***2016***
- 8 x 8 pixel submatrices



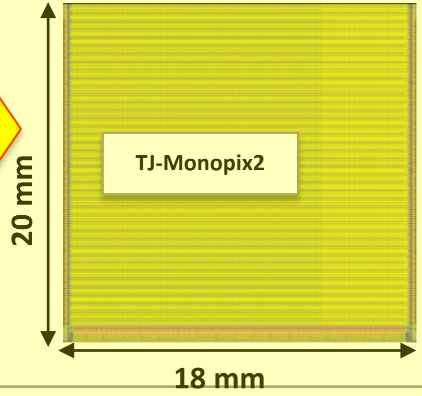
MALTA (asynchronous) & TJ-Monopix1 (column drain)

- subm. **2018**
- large matrices
- fast asynchr & col. drain R/O



miniMALTA

- subm. **2018**
- measures for rad. hardness



TJ-Monopix2

- *subm. **April 2020***
- *33 x 33 μm² pixels*
- *Full height matrix*
- *Fast column drain R/O*

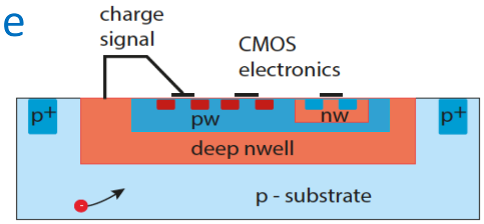
Different electrode (large/small) approaches lead to different

DMAPS

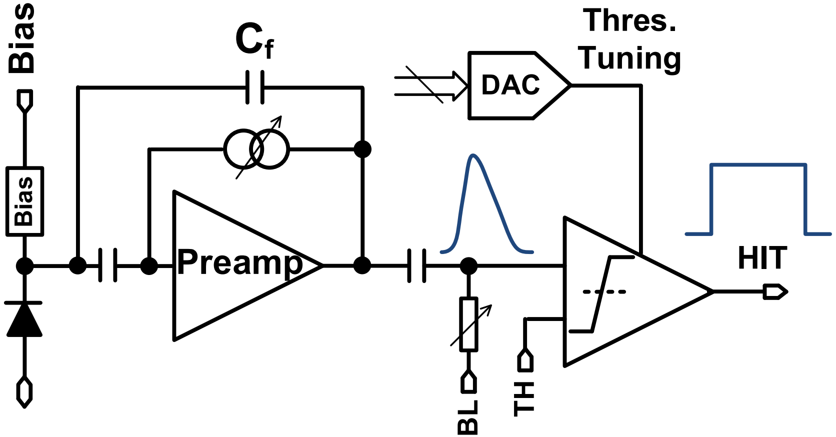
ANALOG FRONT END CHOICES

ANALOG FRONT-ENDS - CSA VS. VOLTAGE AMPLIFIER

- large electrode



(a) Large fill-factor



Charge Sensitive Amplifier

- Choice for large electrode design
- Gain (ideally) independent of C_D

  => G ~ $1/C_f$ (typ. C_f ~ 5 fF)

- $\tau_{CSA} \propto \frac{C_D}{g_m \cdot C_f}$, $ENC^2{}_{therm} \propto \frac{kT}{g_m} \frac{C_D^2}{\tau}$

  => requires larger g_m (power) for large C_D

  => typ. power 30 – 40 µW per pixel

- threshold trimming is advised and a standard in typical implementations

ANALOG FRONT-ENDS - CSA VS. VOLTAGE AMPLIFIER

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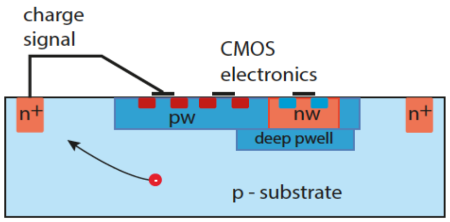
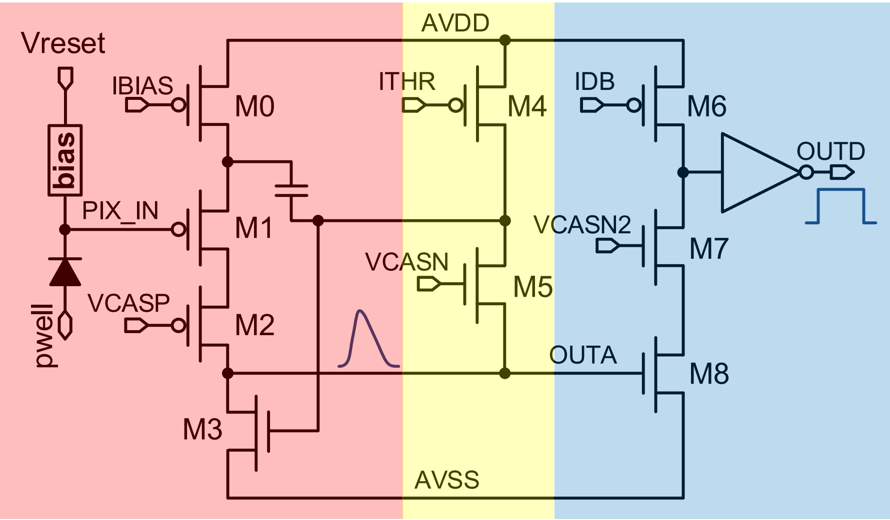
- small electrode



(b) Small fill-factor

W. Snoeys, DOI: 10.1016/j.nima.2013.05.073



D. Kim et al., doi 10.1088/1748-0221/11/02/C02042

Voltage amplifier (ALPIDE like)

- => Profit from small sensor capacitance
  => large voltage signal Q/C_D @ input node
- Very compact design
  => amplification + shaping in one stage
  => simple inverter as discriminator
  => no threshold trimming used (see later)
- Optimized power for required timing
  => ~1 µW/pixel for 25 ns peaking time

$$\frac{S}{N} \approx \frac{Q/C_D}{\sqrt{g_m}} \sim \frac{Q/C_D}{\sqrt[m]{P}}, \quad P \sim \left(\frac{Q}{C_D}\right)^{-m}$$

DMAPS

READOUT ARCHITECTURE CHOICES

wanted

- Small pixels
- High logic (memory) density
- Fast shaping
- High data transmission bandwidth

WE CHOSE A "COLUMN DRAIN" ARCHITECTURE

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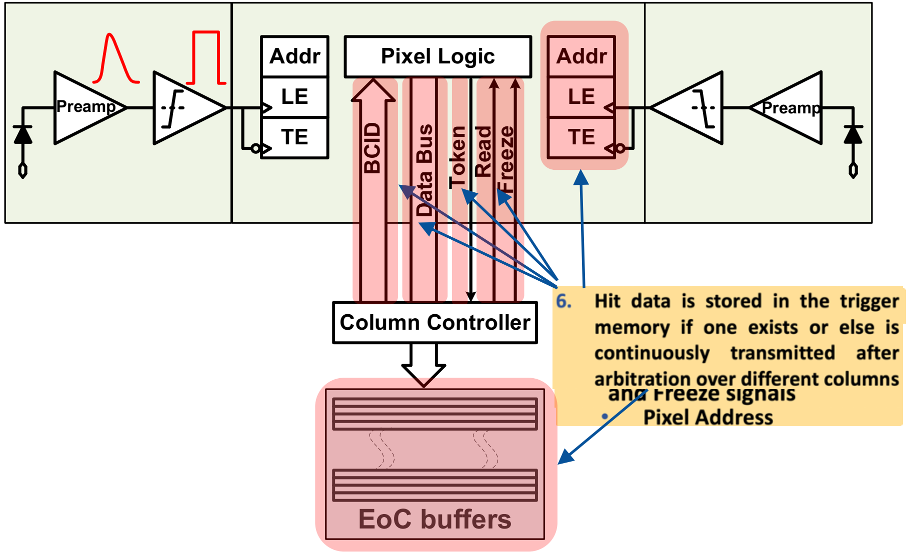
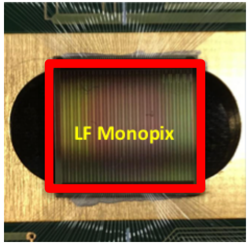
Synchronous readout => time stamping in matrix

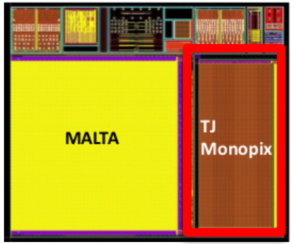


- BC ID (40 MHz) distributed in the column
- Hit timing stamped in pixel
  - LE: leading edge
  - TE: trailing edge

  => Time of arrival: LE

  => Ana. info. from ToT
- Hits read out sequentially, following a token passing scheme on a shared column bus

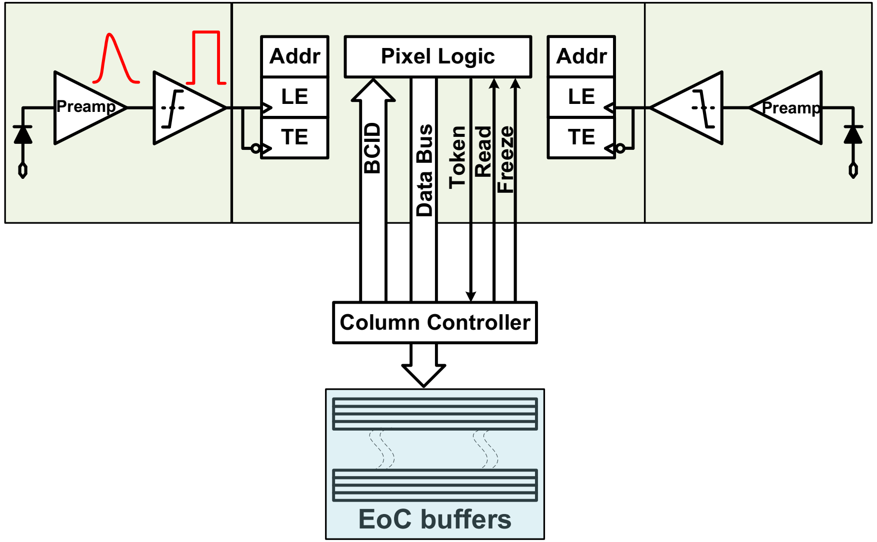




- Well established scheme in ATLAS – FE-I3 like (current pixel detector)
- Demonstrated rate capability for the addressed goal (ITk outer pixel layers)
- Affordable in-pixel logic (storage & digital R/O)
- Challenges: preventing digital cross talk, pixel size, C_D (for large electrode design)

WE CHOSE A “COLUMN DRAIN” ARCHITECTURE

Synchronous readout => time stamping in matrix



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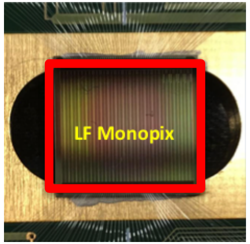
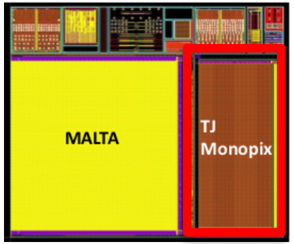
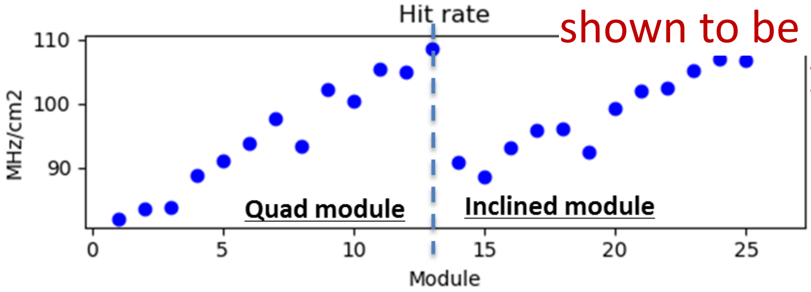
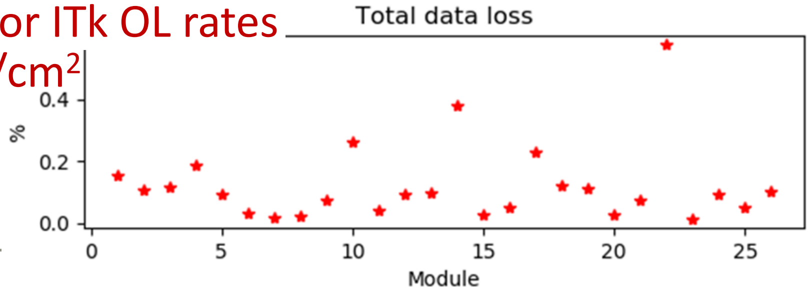




shown to be suitable for ITk OL rates

100 MHz/cm^2



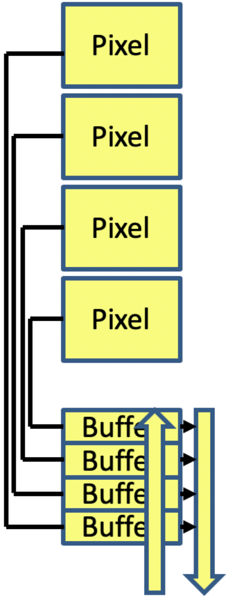


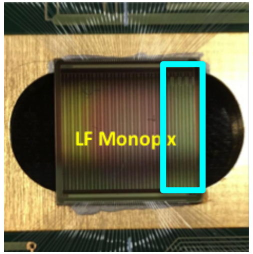
ALTERNATIVE: ASYNCHRONOUS READOUT SCHEMES

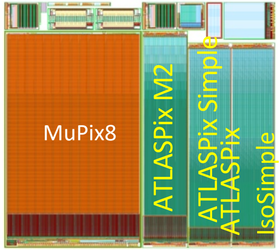
DMAPS with asynchronous matrix => time stamping at periphery

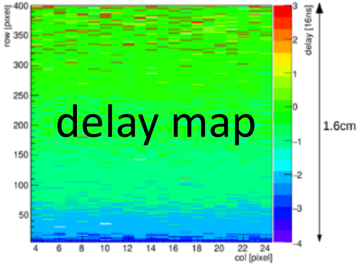
=> Hits transferred to periphery immediately => calls for massive parallelism

A) One to one connection



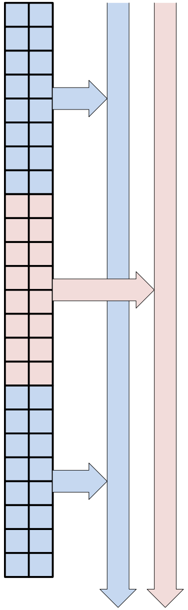


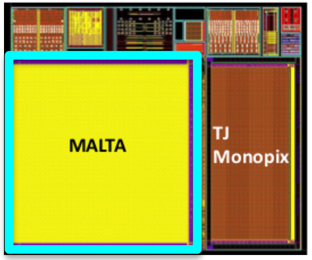




o(400) lines in two metal layers; larger periphery

B) Shared bus by pixel groups



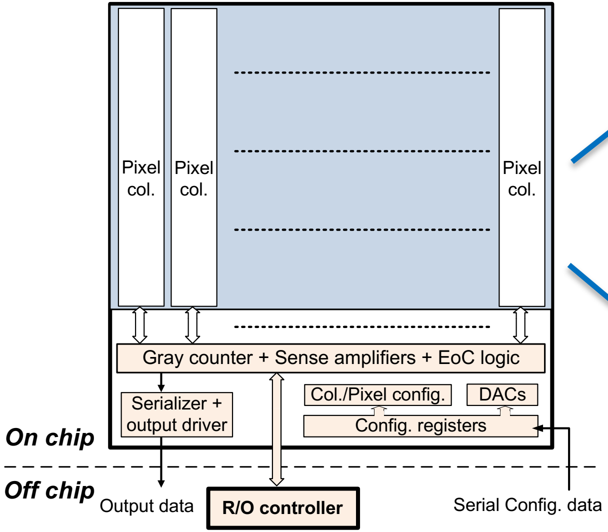


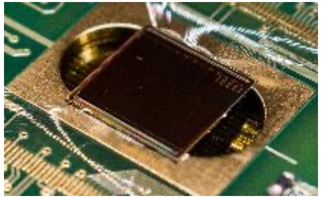
- Two high speed buses w/ short pulses (~1ns)
- Complicated balancing for multibit data to arrive simultaneously at bottom
- GHz synchronization needed

- Challenge: avoid data collisions

THE “MONOPIX1” CHIPS

- Two large scale DMAPS chips were developed targeting data rates and radiation levels expected at ATLAS ITk outer layers
  - Following both, large and small electrode sensor designs employing two CMOS technologies
  - and using the “column drain” architecture for the R/O **matrix**
    - Simplified “downstream” data processing, e.g. no data buffering & triggering, no Gbps-link



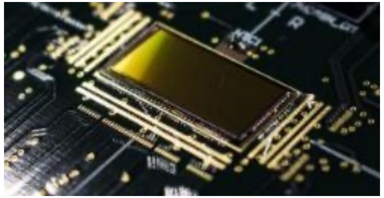


~1×1 cm^2

LF-Monopix1

$50 \times 250\ \mu m^2$ pixels

Designed by: UNIVERSITÄT BONN, CPPM, Irfu CEA Saclay



~1×2 cm^2

TJ-Monopix1

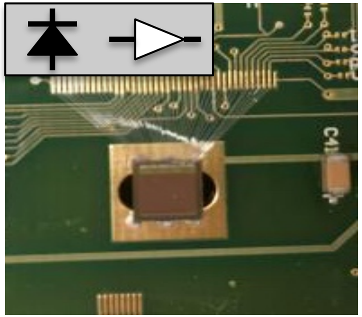
$36 \times 40\ \mu m^2$ pixels

Designed by: UNIVERSITÄT BONN, CERN

RESULTS ON

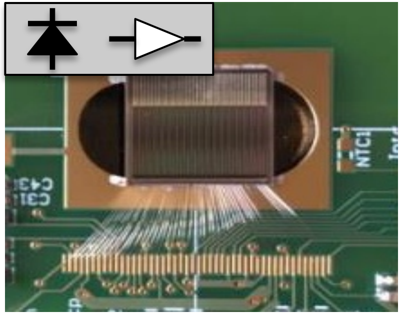
LFOUNDRY 150 NM DESIGNS

❑ CCPD_LF



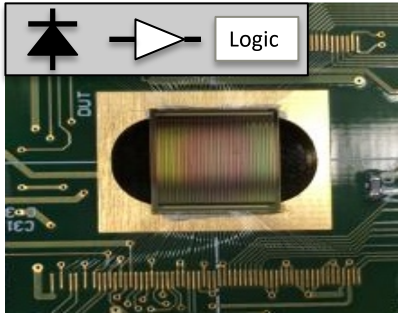
- Pixel size: 33 µm × 125 µm
- Chip size: 5 mm × 5 mm
- Fast R/O with FE-I4
- Thickness: 750/300/100 µm
- Design by Bonn/CPPM/KIT

❑ LF-CPIX



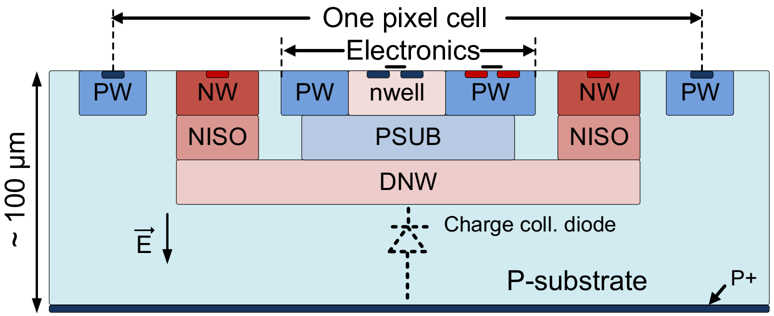
- Pixel size: 50 µm × 250 µm
- Chip size: 10 mm × 10 mm
- Fast R/O with FE-I4
- Thickness: 750/200/100 µm
- Design by Bonn/CPPM/IRFU

❑ LF_Monopix1



- Pixel size: 50 µm × 250 µm
- Chip size: 10 mm × 10 mm
- Integrated column drain R/O
- Thickness: 750/200/100 µm
- Design by Bonn/CPPM/IRFU

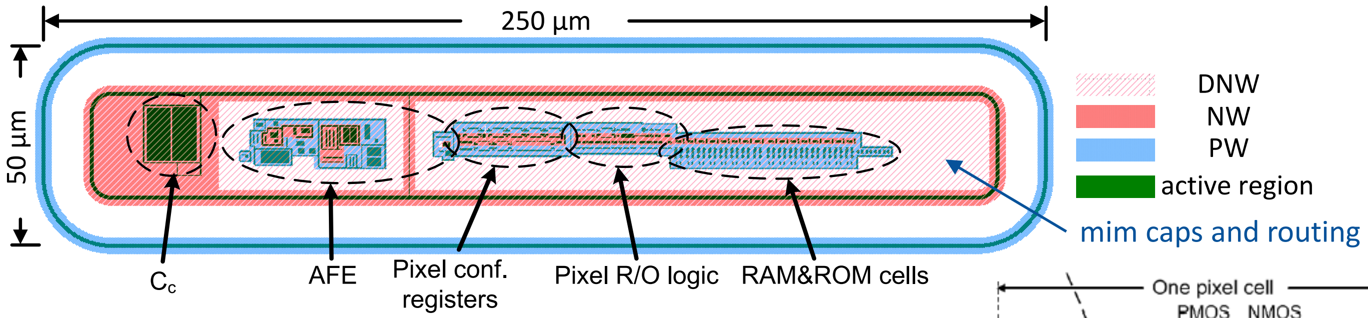
LFOUNDRY 150 NM
LARGE ELECTRODE (55% FF)

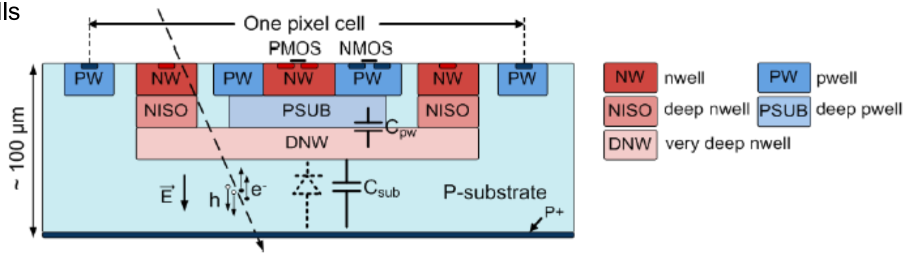


LFA150:

- LFoundry **150 nm** process (deep N-well/P-well)
- **Quadrupel** well
- 7 metal layers
- Resistivity **> 2 kΩ·cm**
- Backside processing
- Voltages > **350 V**

LF-MONOPIX1: PIXEL LAYOUT





- Pixel size 50 µm × 250 µm
  - ~ 55% of "fill factor"
  - "rounded" corner to minimize field
- Careful layout / precautions required to prevent cross talk from circuit layer to sensing electrode through psub/dnw capacitance
  1. Separated analog/digital power domains
  2. Digital "bulk" (in a separate pwell) is separated from digital ground
  3. Full custom in-pixel digital design, optimising transient signal switching

SENSOR IRRADIATION PERFORMANCE

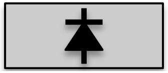
UNIVERSITÄT BONN

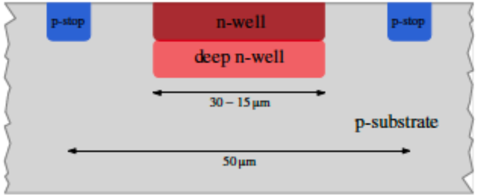
- Good radiation hardness of large electrode sensor proven in various prototypes

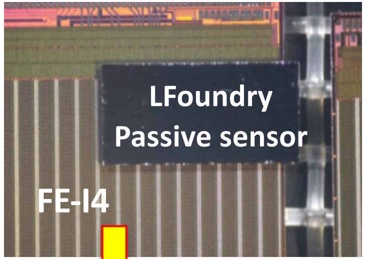
LFoundry 150 nm CMOS
P-substrate > 2 kΩ·cm
Bias 100 - 400 V
7 metal layers

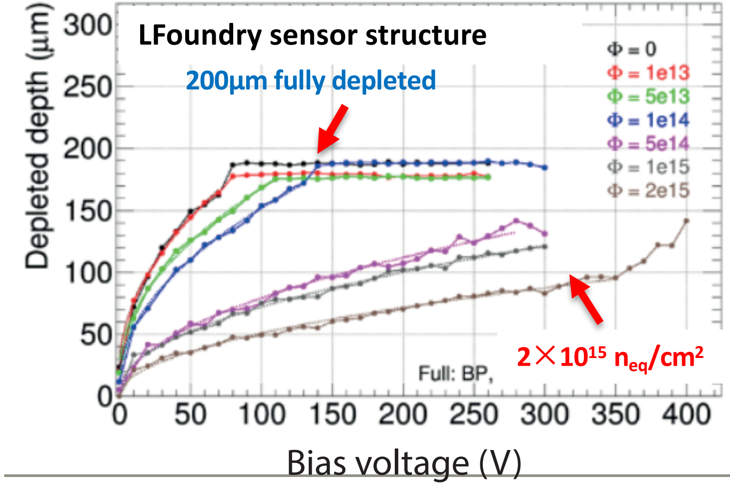
T. Hirono et al., DOI: 10.1016/j.nima.2016.01.088
P. Rymaszewski et al., DOI: 10.1088/1748-0221/11/02/C02045

Passive sensor

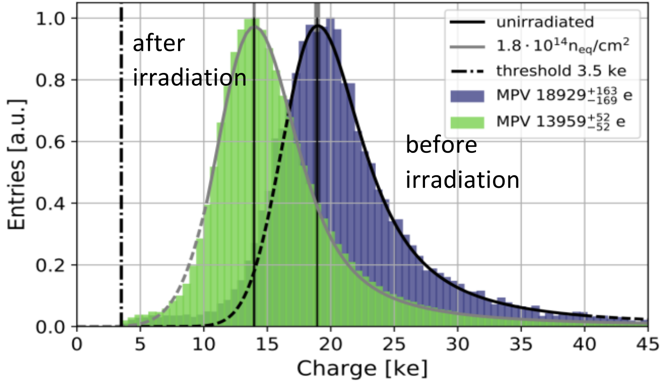








I.Mandić, et al.,
DOI:
10.1016/j.nima.2018.06.062



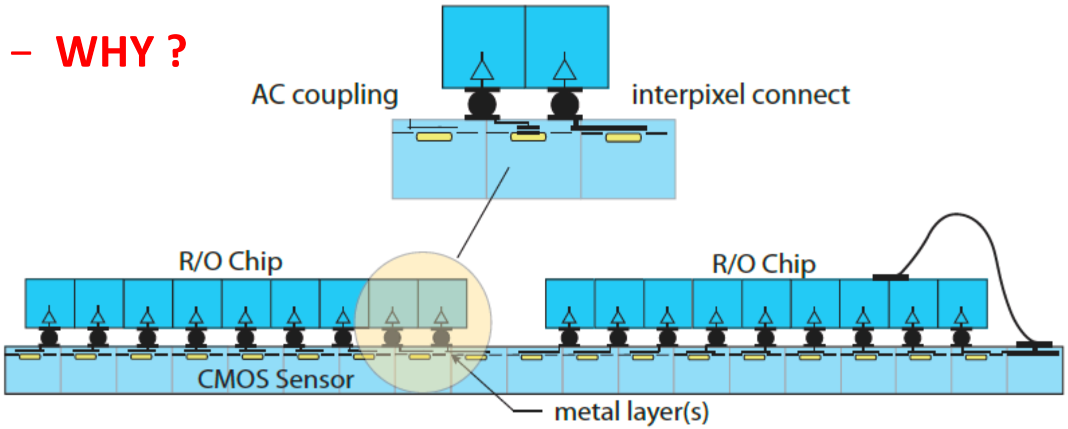
D.-L. Pohl et al., JINST 12 (2017) no. 06, P06020

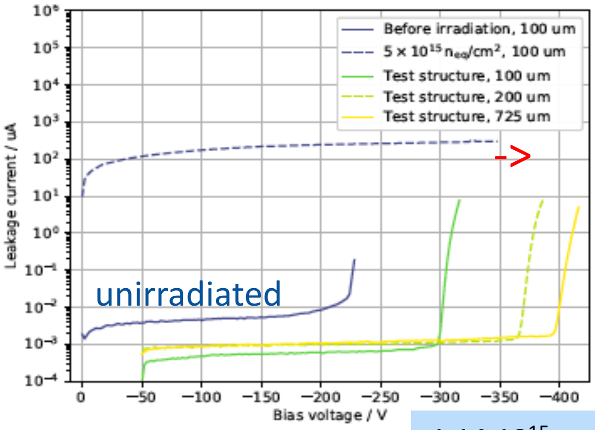
PASSIVE CMOS SENSORS

LFoundry 150 nm + FE-I4

UNIVERSITÄT BONN

– **WHY ?**

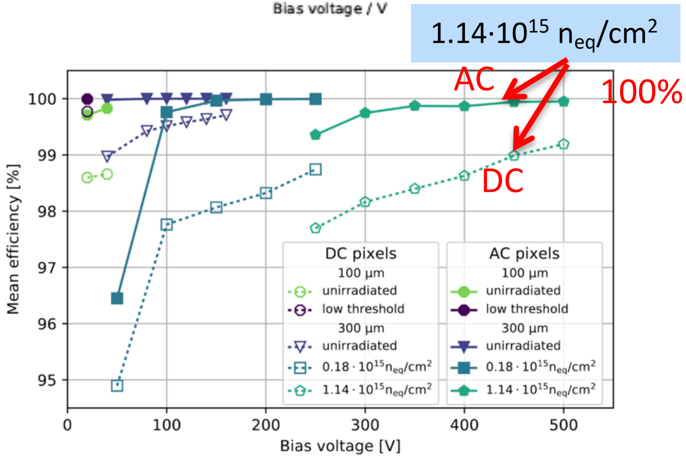




- Cheaper
- High wafer throughput
- Exploit metal layers for AC coupling and rerouting

Results

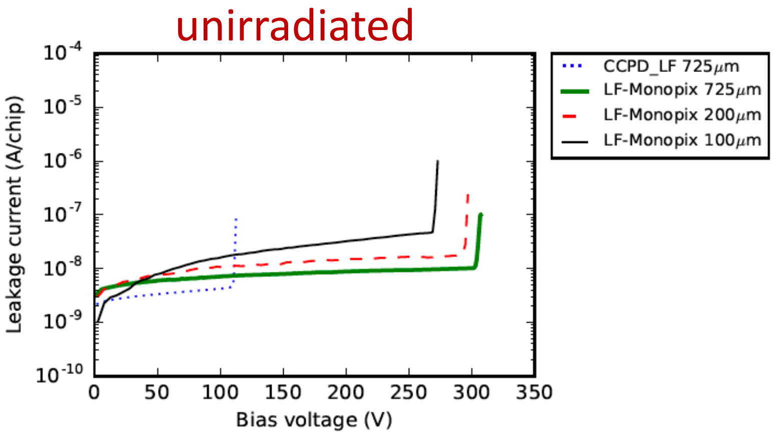
- **bias 120 V** -> up to 350 V
- **~220 µm** depletion depth
- same performance as standard planar sensors in terms of i_{leak} and noise
- **very high eff. after** $1x10^{15} n_{eq}/cm^2$
- in ATLAS ITk sensor market survey

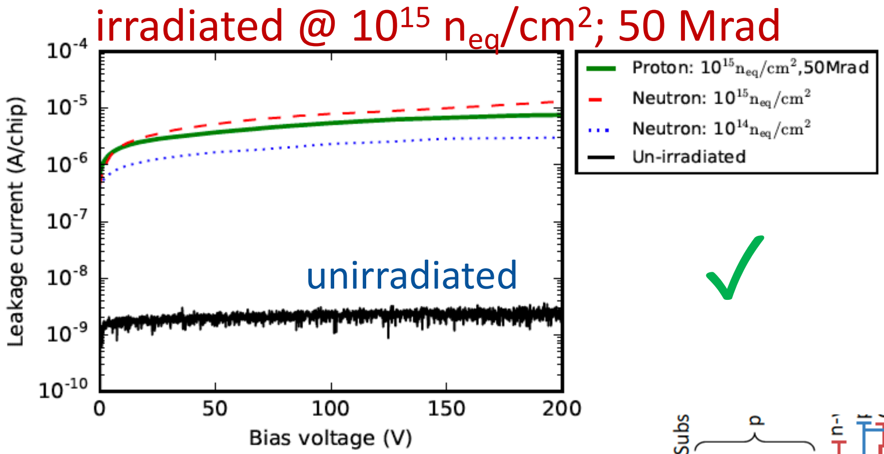


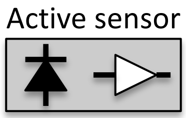
D.-L. Pohl et al., JINST 12 (2017) no. 06, P06020

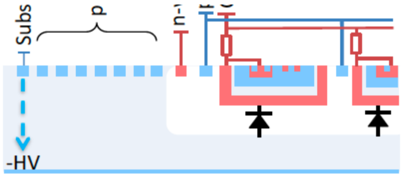
IRRADIATED ACTIVE SENSORS OF LF_MONOPIX1

UNIVERSITÄT BONN









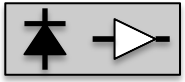
- Guard ring structure essential for high breakdown voltage (up to 300 V)
- Full depletion voltage **@ 100 µm:** unirr. V_{dep} = **7 V**, irradiated V_{dep} = **130 V**

TID PERFORMANCE

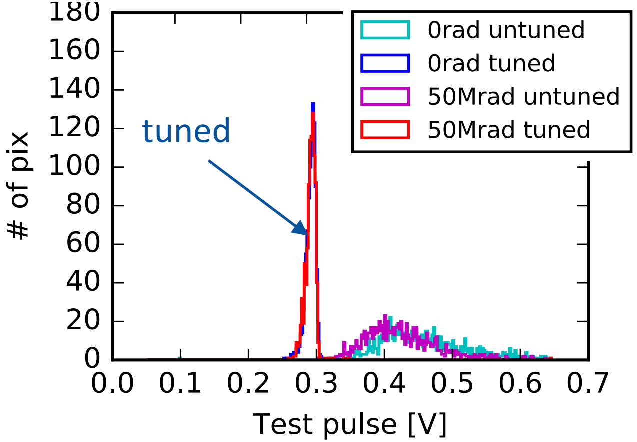
- LF-CPIX X-ray irradiated to 100 Mrad
  - Irradiated and measured at room temperature
  - Tunable thresholds with almost unchanged dispersion
  - **Gain degradation <5%**
  - **Noise increase ~25%**

    (probably largely due to i_{leak} increase after irrad.)

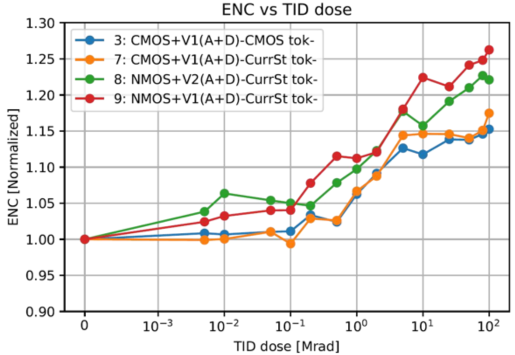
Active sensor

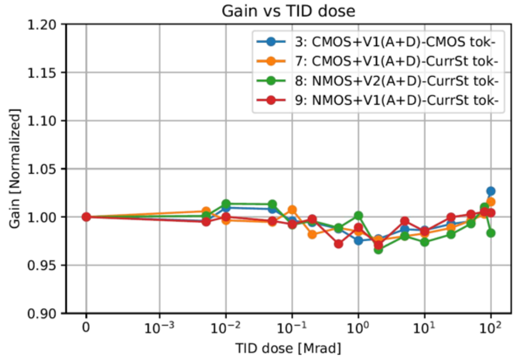


Threshold dispersion (LF-CPIX)



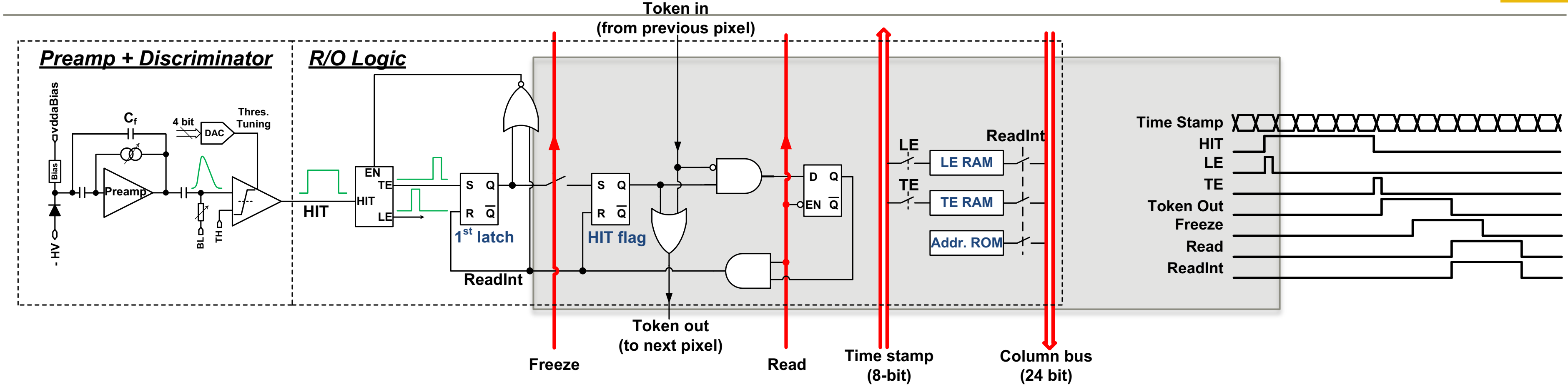
Normalized gain and ENC (LF-Monopix1)





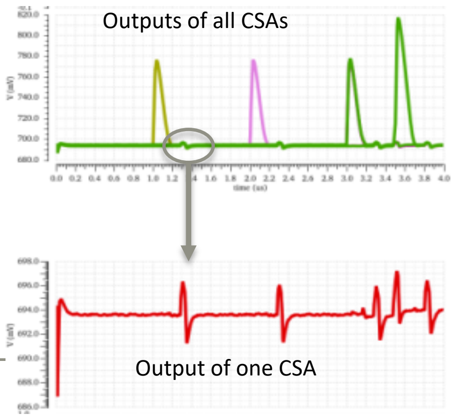
T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059

LF-MONOPIX1: IN-PIXEL DIGITAL LOGIC

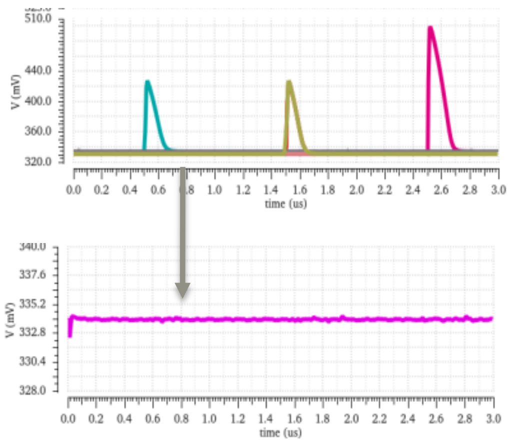


- 8-bit time stamp & ToT @ 40 MHz (gray encoded)
- Full-custom digital circuit

LF-Monopix1 full column post layout simulation



LF-Monopix2 full column post layout simulation



LF-MONOPIX1: EFFICIENCY

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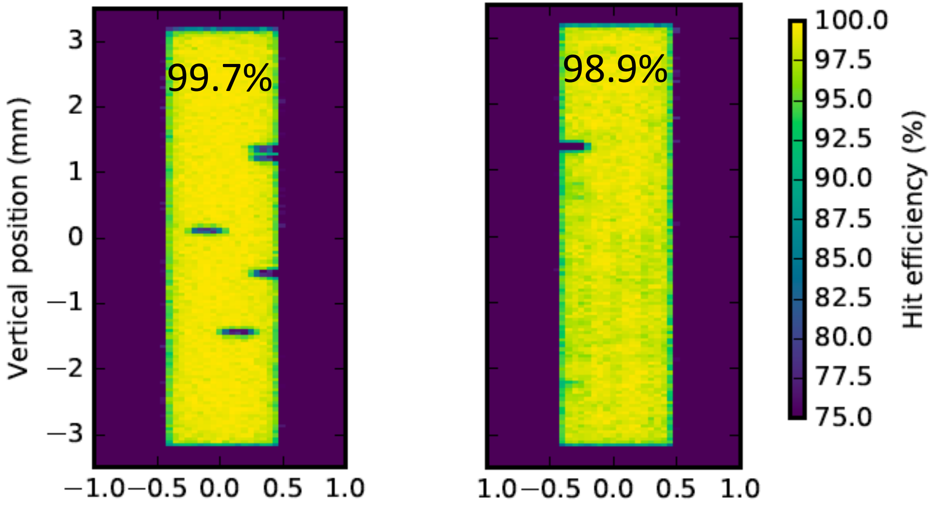
- High and uniform efficiency even after irradiation

Before irrad. | **After $10^{15} n_{eq}/cm^2$ (neutrons)**

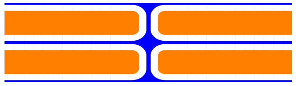
Before irradiation:

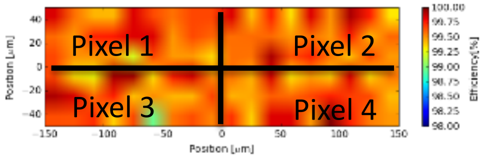
- Noise occ. < 1.2 Hz/pix
  < 10^{-7}/25 ns/pixel
- 1% masked pixels
- Dry ice cooling
- Bias -200 V
- Thres ~1800 e-
- **ε = 99.7 ± 0.1 %**

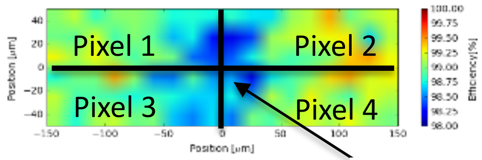


After irradiation:

- Noise occ. < 0.1 Hz/pix
  < 10^{-7}/25 ns/pixel
- 0.2% masked pixels
- Dry ice cooling
- Bias -130 V (this sensor!)
- Thres ~1700 e-
- **ε = 98.9 ± 0.1 %**





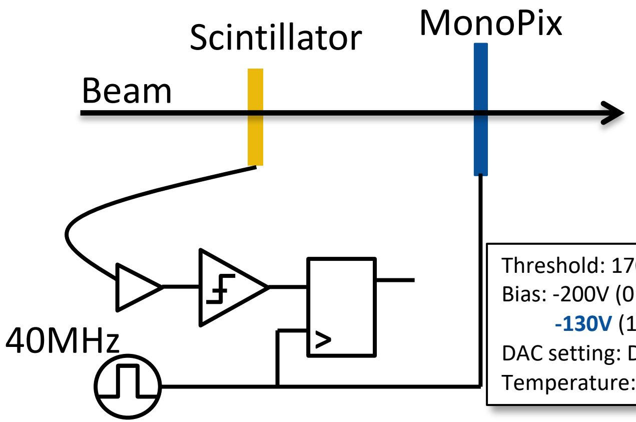


~ 98%

M. Barbero et al., arXiv:1911.01119, submitted to JINST

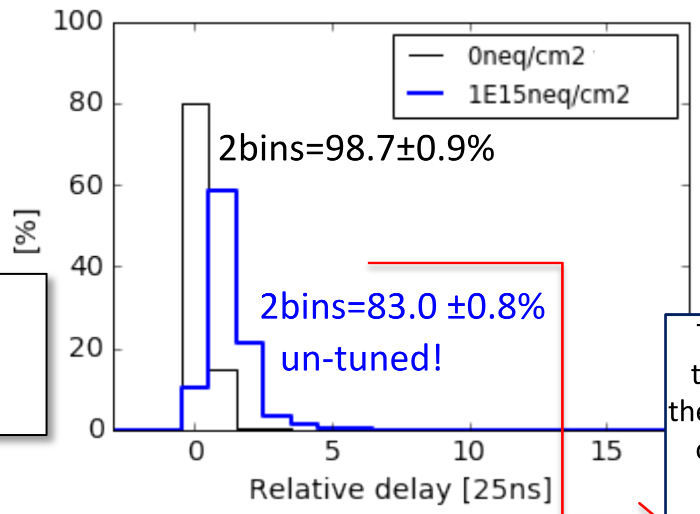
TIMING?

UNIVERSITÄT BONN



Threshold: 1700 e-
Bias: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
DAC setting: Default
Temperature: cooled by dry ice

Delay = (Scintillator LE) – (MonoPix LE)

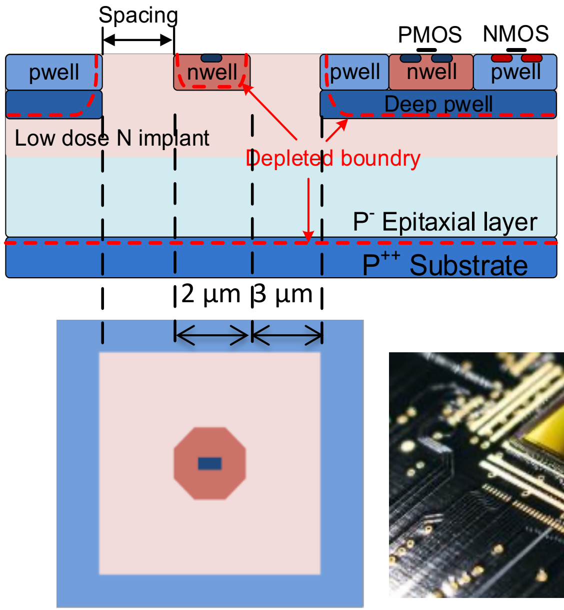


Two bins are "in-time" efficient, as the absolute position of the scintillator signal is random relative to the clock edge

- **>80% in-time efficient after** 1 x $10^{15} n_{eq}/cm^2$.
  Remarkable for C_D ~ 400 fF and promising for new design with smaller C_D
  There is still plenty of room for improvement by tuning for lower thresholds and faster response
  optimise CSA tune, discriminator settings, etc., ... higher bias voltage, backside bias

RESULTS ON

TOWER JAZZ 180 NM DESIGNS

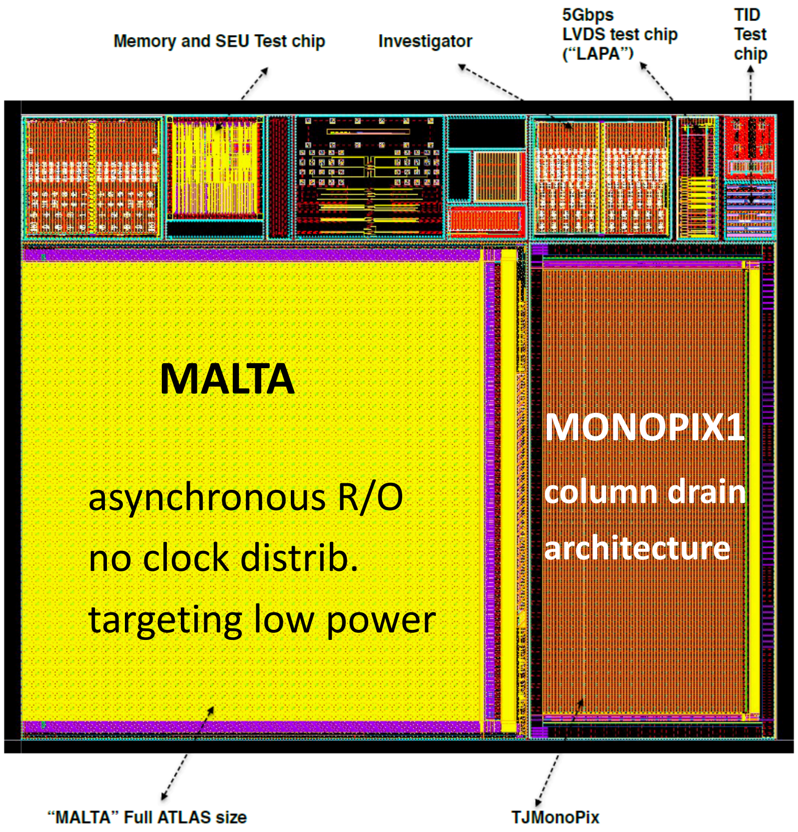


<u>**TowerJazz** 180 nm CMOS CIS</u>

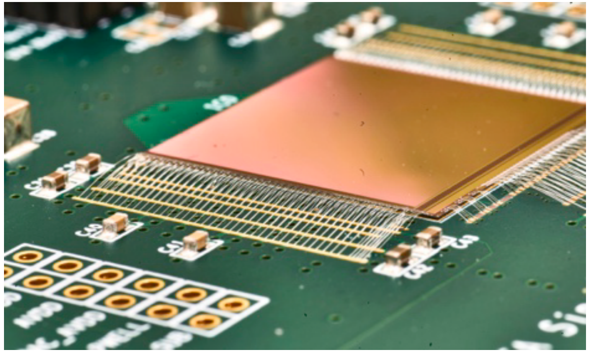
- Deep pwell allows full CMOS in pixel
- 6 metal layers
- High res. epi-layer: **1–8 kΩ·cm**
  => epi thickness: **18 - 40 µm**
- **Modified process** to improve lateral depletion

Derived from ALICE development (led by CERN)

TJ – MALTA AND TJ - MONOPIX



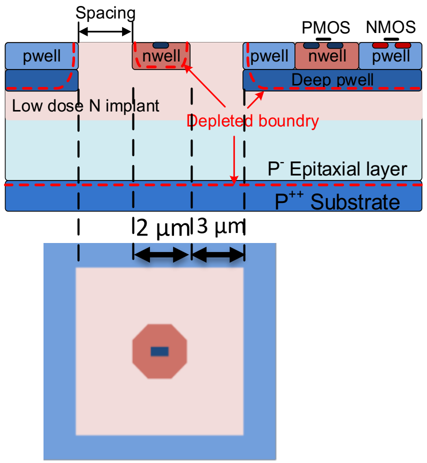
Small electrode designs

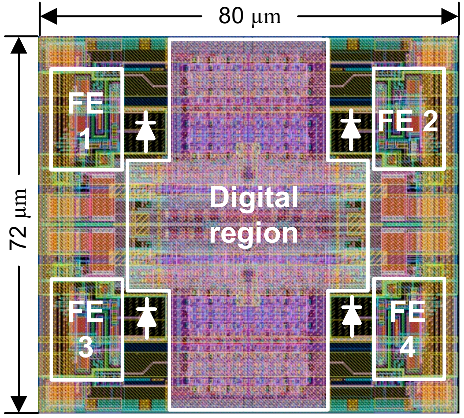


- Sensor design is identical
- Front ends similar (different biasing schemes)
- R/O architectures very different

TJ-MONOPIX1: PIXEL LAYOUT

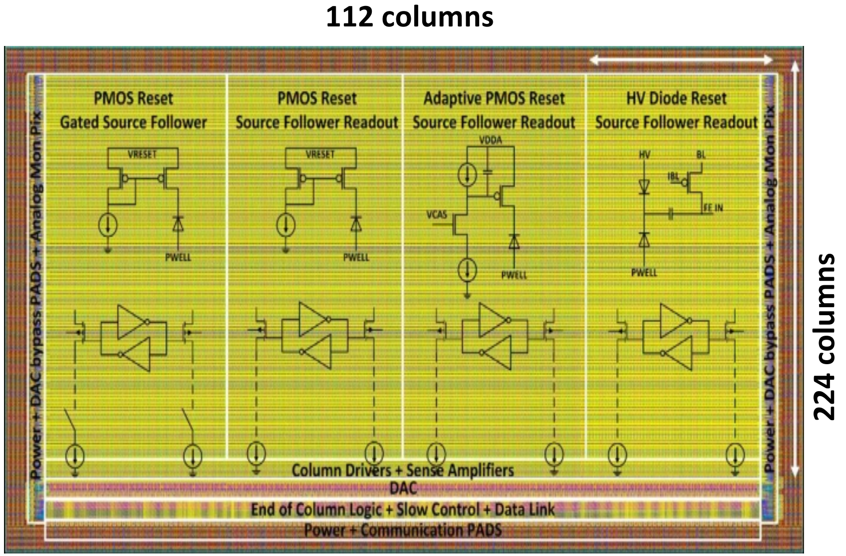
UNIVERSITÄT BONN





Four equal sectors with different pixel/periphery designs

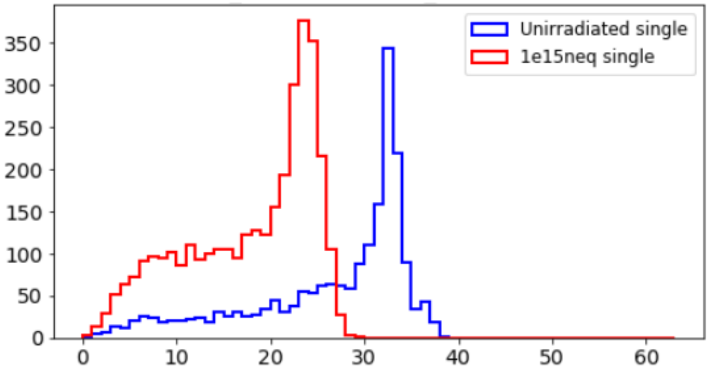
(4 × 224 × 112 pixels



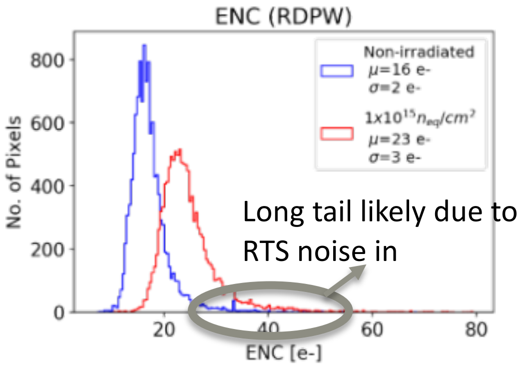
- Pixel size 36 × 40 µm²
- 2 µm collection diode + 3 µm spacing
- Separated digital & analog region, several
- Full-custom digital design
  - 6 bit ToA & ToT
  - Minimized area for small pixel size

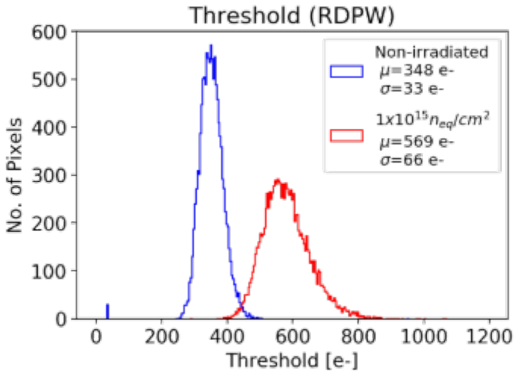
TJ-MONOPIX1 MEASUREMENTS (LAB & TESTBEAM)

- Good noise performance 10 - 15 e^-
  - -> Increased by ~10 e^- after 10^{15} n_{eq}/cm^2
- Thres. dispersion 30 - 40 e^-
  - -> 50 - 65 e^- after 10^{15} n_{eq}/cm^2



Better noise & threshold tuning needed !

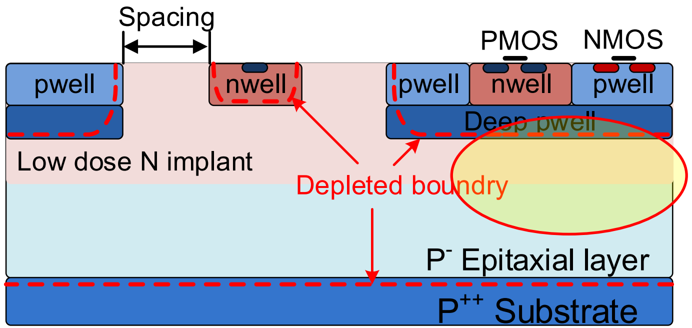


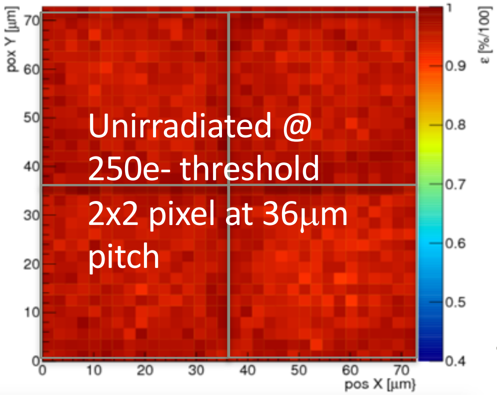


I. Caicedo et. al, DOI: 10.1088/1748-0221/14/06/C06006

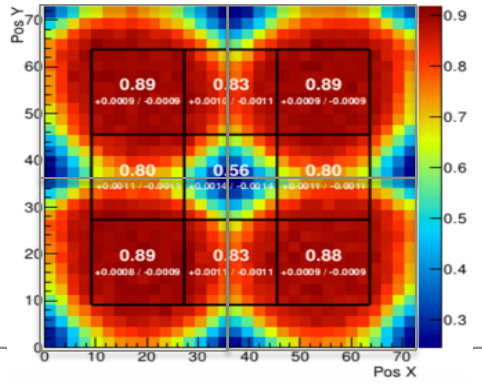
CHARGE COLLECTION WITH SMALL ELECTRODES

- Epi thickness 20-30 µm
- Field strength and shape under DPW in pixel corners is critical
  - Full depletion under the DPW
  - and operating at low threshold is essential
  - Transverse field components in corners essential for radiation hardness



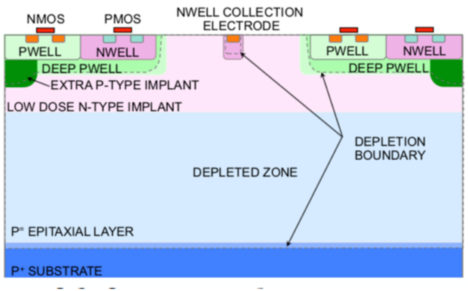


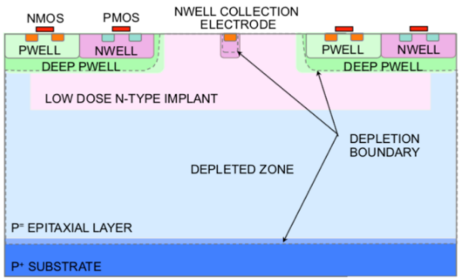
Irradiated 10^{15}n/cm^2 @ 350e- threshold
2x2 pixel at 36 µm pitch



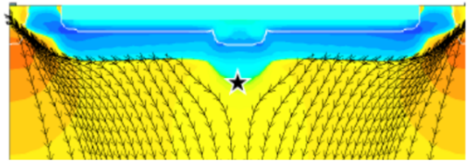
OPTIMATIONS FOR RADIATION HARDNESS

1. Structuring underneath dpw





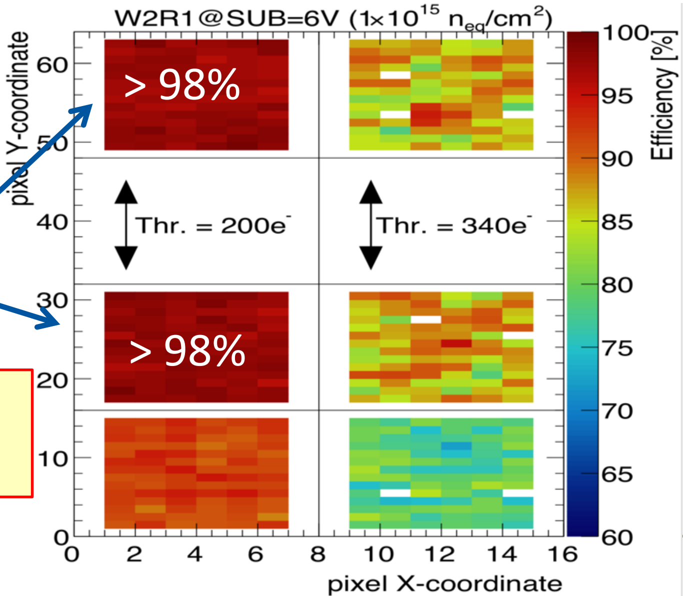
2. Lower thresholds and noise
   -> mods to analog electronics

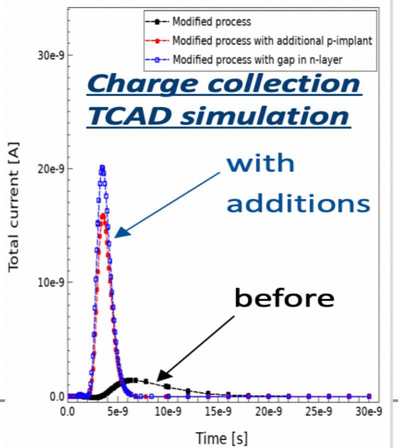


M. Dyndal et al., ArXiv:1909.11987

MiniMALTA test chip
36x36μm^2
after 10^{15} n_{eq}/cm^2

measures 1 plus 2



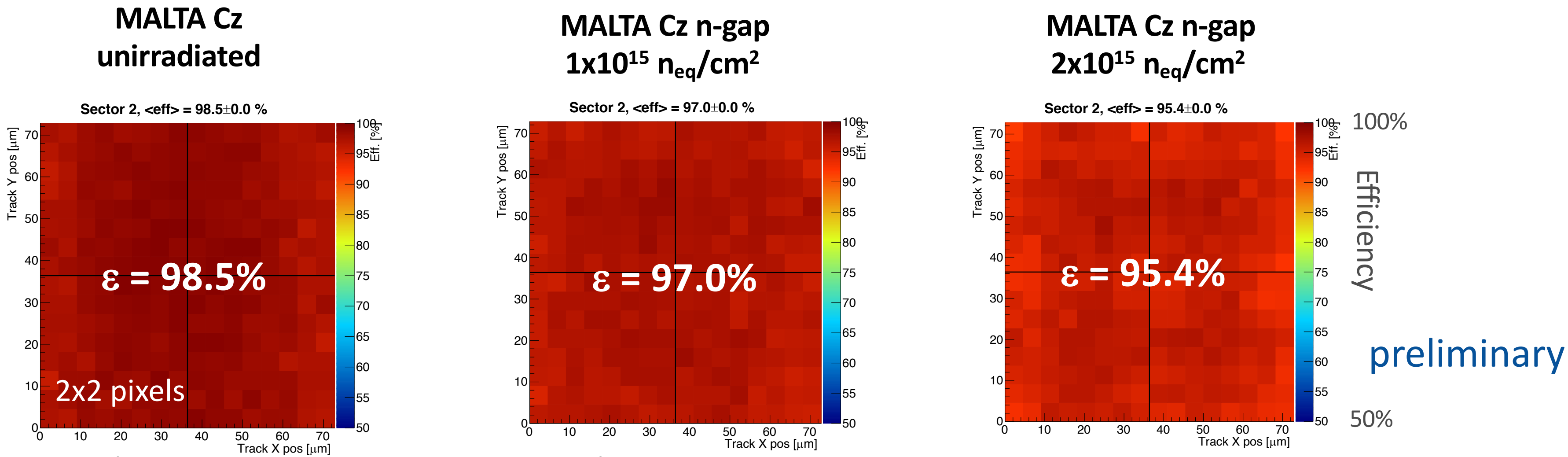


3. high resistivity substrate
   (pCz … next slide)

OPTIMIZATION FOR RADIATION HARDNESS

n-irradiated (IJS) to $2x10^{15}$ n_{eq}/cm^2 followed by DESY beam test

Full-size MALTA sensor with original front-end design on HR pCz (i.e. only measure no. 3)



Thres = 427e^- | Thres = 260 e^- | Thres = 226 e^-

ENC = 9.8 e^- | ENC = 12.7 e^- | ENC = 14 e^-

H. Pernegger, HSTD2019

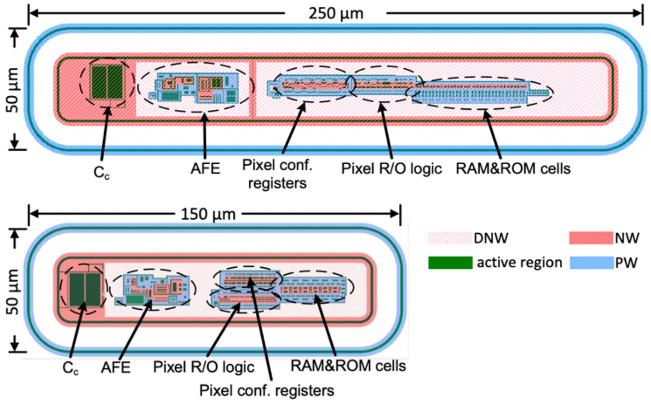
UNIVERSITÄT BONN

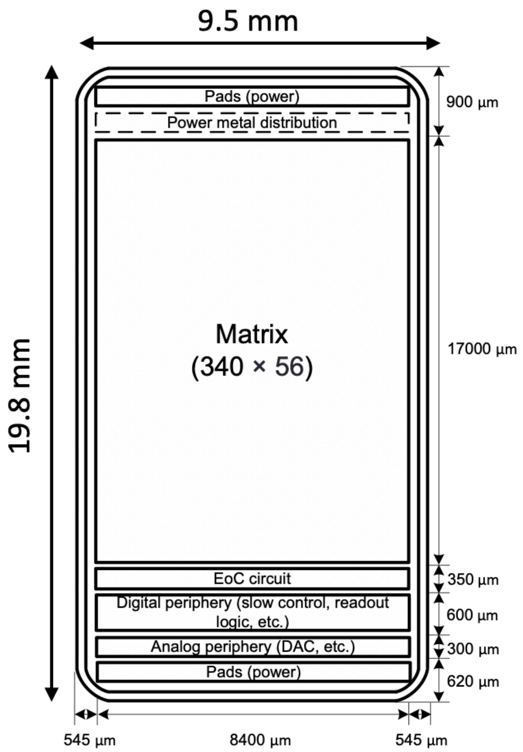
FROM MONOPIX1
TO MONOPIX2

GOALS LF-MONOPIX2

UNIVERSITÄT BONN

- Smaller cell size -> 50 × 150 μm²
- Reduce detector capacitance from 400 fF -> 250 – 300 fF
- Optimise digital design for minimum dig./ana. coupling
- New amplifier design (faster timing)
- Keep conservative and safe design (e.g. wide power metals, guard rings) to ensure high breakdown tolerance





- 340 × 56 pixels
- 50 × 150 μm²

LFOUNDRY MONOPIX2 (LARGE ELECTRODE DESIGN)

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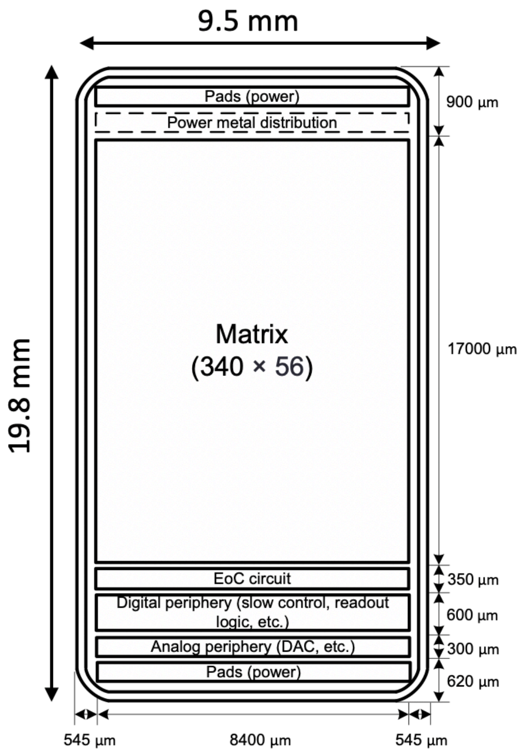
	LF-Monopix1	LF-Monopix2
Pixel size	50 × 250 μm²	**50 × 150 μm²**
Cd	~ 400 fF	250 – 300 fF
Analog power/pixel (CSA + Discri.)	15 μA + 5 μA = 20 μA	**10 μA + 2 μA = 12 μA**
Noise	~150 e⁻ - 200 e⁻	**100 ~150 e⁻**
LE/TE time stamp	8-bit	**6-bit**
ToT @ 6 ke⁻	---	**200 – 250 ns**
Max. ToT	---	**400 ns**
(rms) thres. dispersion	(~ 100 e⁻)	(80 e⁻)
Min. threshold	1500 e⁻	**1000 e⁻**
In-time threshold	~ 2000 e⁻	**1500 e⁻**



Tape out: April 2020

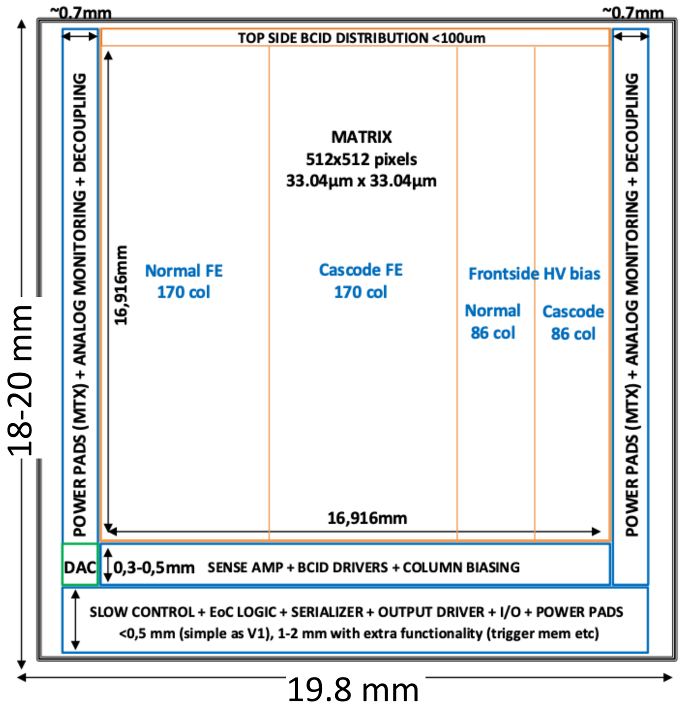
- 340 × 56 pixels
- 50 × 150 μm²

GOALS TJ-MONOPIX2

Large 2x2 cm2 sensor featuring

- Larger signal
  - high resistivity pCz material ?
- More efficient charge collection
  - modified sensor geometry (n-gap, extra dpw)
  - optimum (smaller) cell size for given electronics
- Lower noise and threshold operation
  - improved front end

    gain increase
    RTS noise reduced
    less threshold dispersion
    threshold trimming



- 512×512 pixels
- $33.04 \times 33.04\ \mu m^2$

TOWERJAZZ MONOPIX2 (SMALL ELECTRODE DESIGN)

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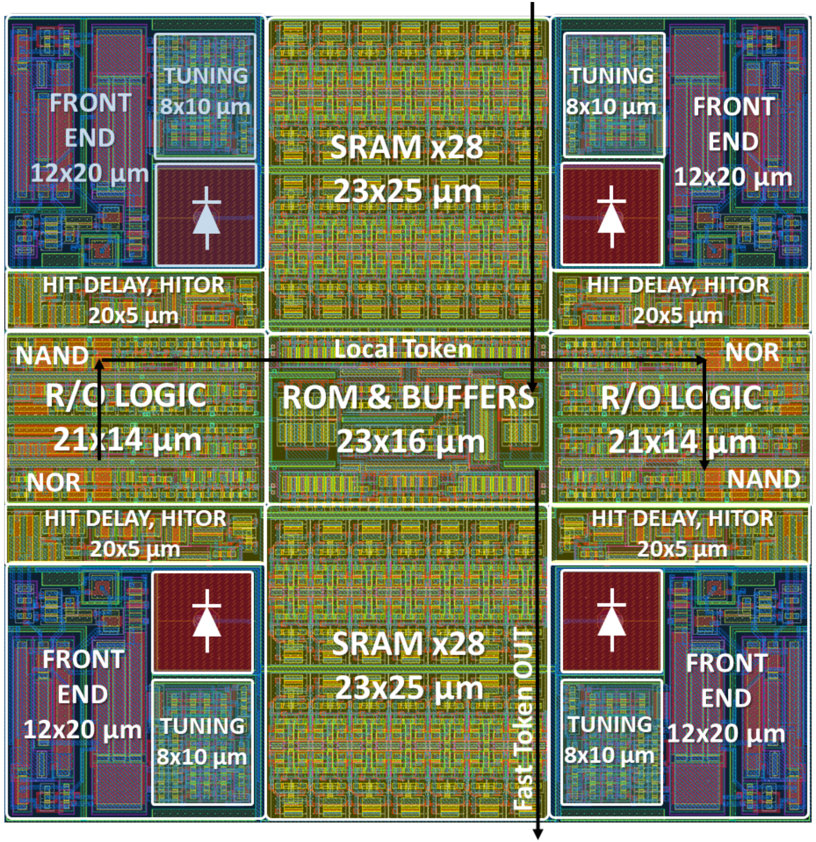
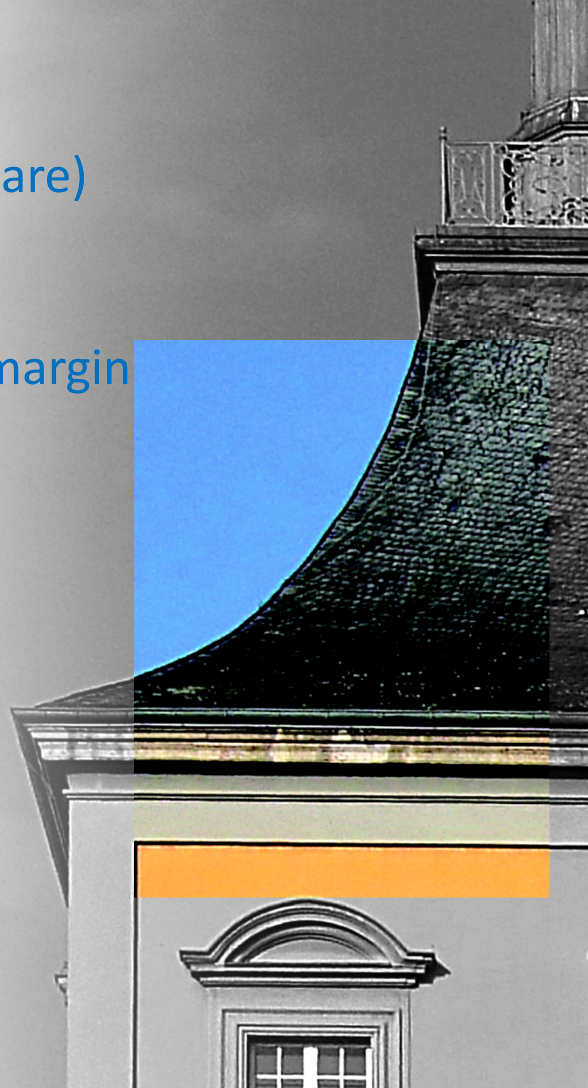


	TJ-Monopix1	TJ-Monopix2
Chip Size	1x2 cm^2 (224x448 pix)	2x2 cm^2 (512x512 pix)
Pixel size	36 × 40 µm^2	33.04 × 33.04 µm^2
Noise	≅11 e$^-$	< 10e$^-$ (improved FE)
LE/TE time stamp	6-bit	7-bit
Threshold Dispersion	≅ 30 e$^-$ rms	< 20 e$^-$ rms (improved FE + tuning)
Minimum threshold	≅ 300 e$^-$	<150 e$^-$
In-time threshold	≅ 400e$^-$	250 - 300 e$^-$
Efficiency	≅ 70 % (irradiated)	> 95% (irradiated)

Tape out: April 2020

CONCLUSIONS

- Development of DMAPS with full R/O needs time (and care)
- MONOPIX developments with large and small electrode can be considered as viable options for HL-LHC trackers
- Col-drain architecture meets Layer 4 rates with a (x10) margin
- Large electrode
  - high beak down voltage
  - large signal
  - high efficiency after 10^{15} n_{eq}/cm^2
- Small electrode
  - low capacitance, low noise
  - low power, large Q/C
  - ways towards radiation hardness identified
- Stay tuned for large MONOPIX2 chips




FTD BONN

FTD = RESEARCH & TECHNOLOGY CENTER FOR DETECTOR PHYSICS

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- hosts 10 Groups from 2 institutes from
  - High Energy & Hadron Physics
    - LHC: ALICE, ATLAS, LHCb
    - Belle II, COMPASS, Crystal Barrel, BGO-OD, ILC, PANDA
    - RD42, RD50, RD53
  - Photonics
- 2 local accelerators
  electron stretcher ring ELSA (3.5 GeV e-)
  cyclotron 15 MeV p (and ions)

FTD building

ELSA

cyclotron

FTD BUILDING

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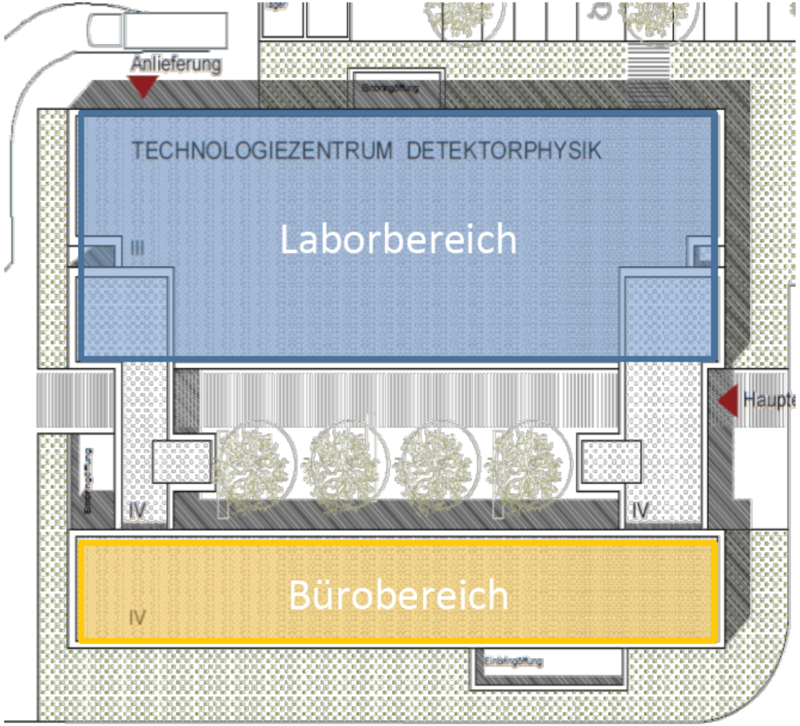
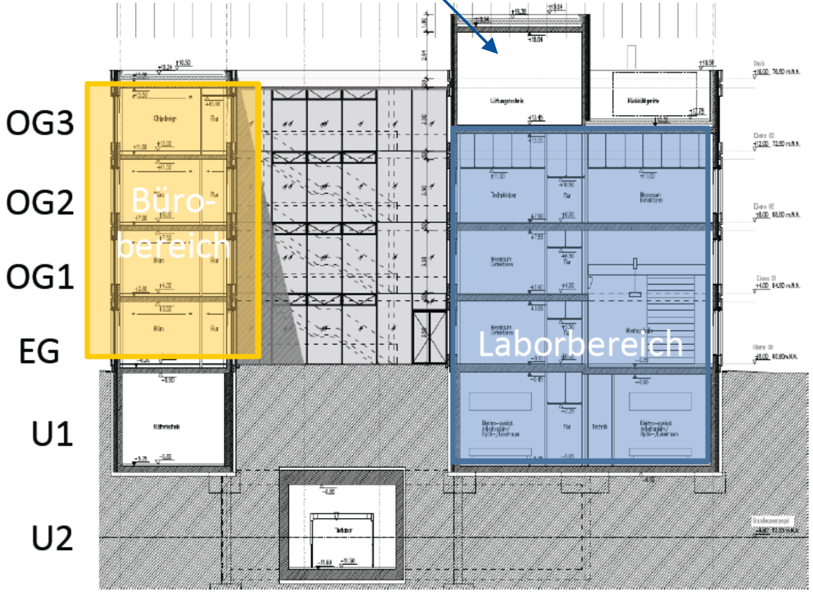
office area: 880 m^2 on 4 levels



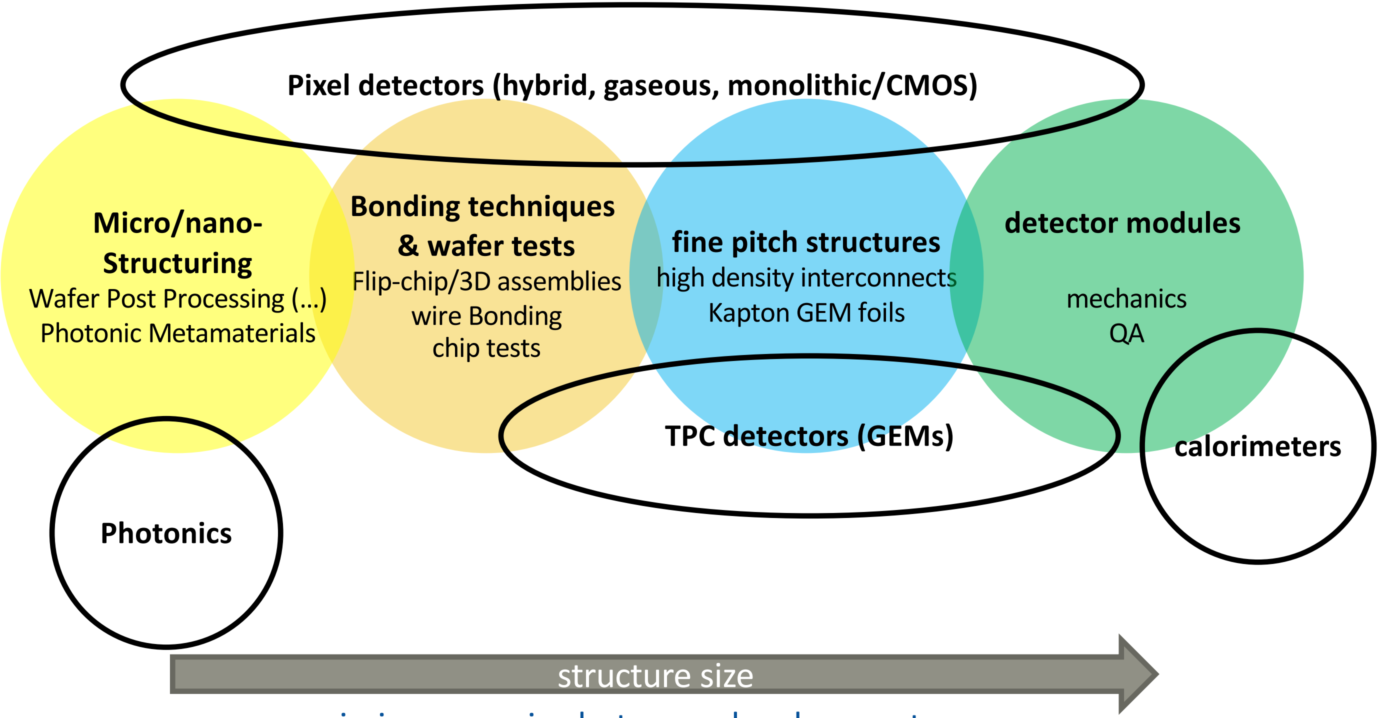
lab area: 2010 m^2

- 4 levels + underground laboratory
- 360 m^2 clean rooms (ISO 5 – 6)
- air flow / technique on upper most level



TARGET TECHNOLOGIES AND APPLICATIONS

clean room and lab area



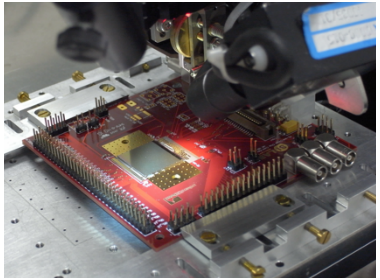
maximise synergies between development areas

EQUIPMENT

Existing equipment (standard for microlabs)

wire bonders (4)
wafer probers (2 x 8“ , 1 x 12“)
laser test systems
rad. source test benches
microscopes
electronics meas. equipment (scopes, logic analysers, function & pattern generators, network analyser, etc.)

... has been updated within FTD acquisition



Newly acquired (big) equipment for FTD

A) New for micro electronics and detectors
B) Micro structuring (to try things out ... simple structures at first)

NEW EQUIPMENT: MICRO ELECTRONICS AND DETECTORS

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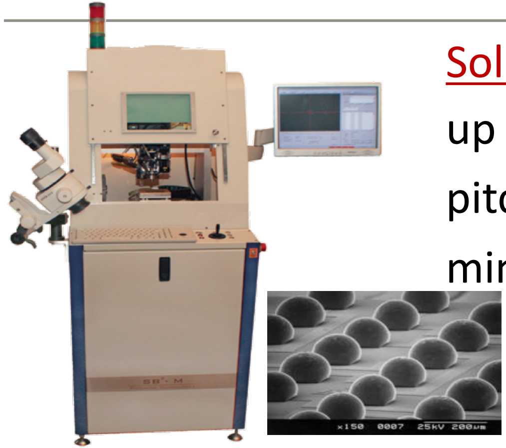


CR: PacTech

Solder ball placer

up to 8“ wafers

pitch $\lesssim$ 100 µm

min Ø = 40 µm

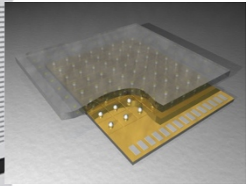
X-ray inspection

precision < 1µm

scan area (20cm^2)

CR: Nikon

wafers, ball-bonding and inspection



CR FineTech

Flip-chip bonder

can do 25 µm (→ 10 µm)

AgSn bumps with <1 µm accuracy

Wafer saw

12“ wafers

autom. step-cut dicing

CR DISCO

NEW EQUIPMENT: MICRO ELECTRONICS AND DETECTORS

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cyclotron

15 MeV p irradiation

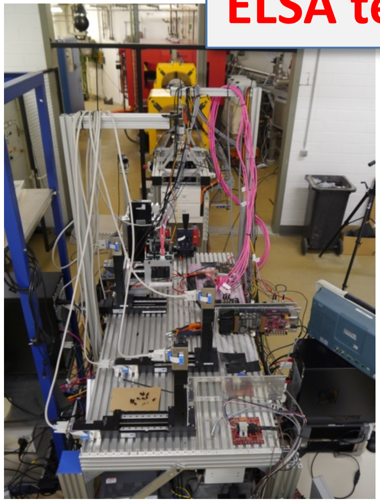
$10^{16}\ n_{eq}/cm^2$

in about 2 hrs

X-ray cabin for TID irradiation

100 kV, 2 Mrad / h

ELSA testbeam



irradiation and measurements

Marta CO2 cooling machine

3D measuring machine

laser-based tracker

contact-less

1 µm resolution

MICRO STRUCTURING / POSTPROCESSING

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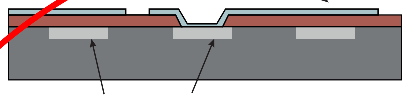
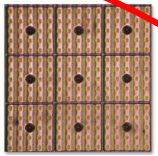
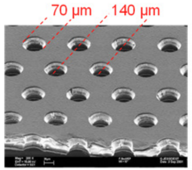
Plasma Etching

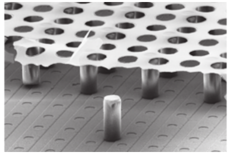


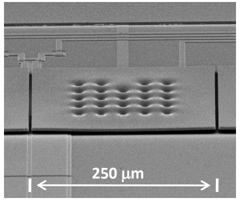




Structuring of flexible materials (e.g. Kapton/Cu, GEMs etc.)

CMOS surface post processing (e.g. pad enlargement, re-routing)





low-T sensors MMC, TES; SC structures, SQUIDS

Complex structures on top of CMOS chips (e.g. InGrid)

Sputtering

Ion Etching

Maskless Aligner

3 wet benches for chemistry (for GEMs & other)

and spin coating => to try things out (backside stuff, (D)RIE, TSVs)

IMPRESSIONS

move-in July 20