

## Progress with the wire interlocks for Run3

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Uythoven, J. Wenninger, D. Wollmann, M. Zerlauth.



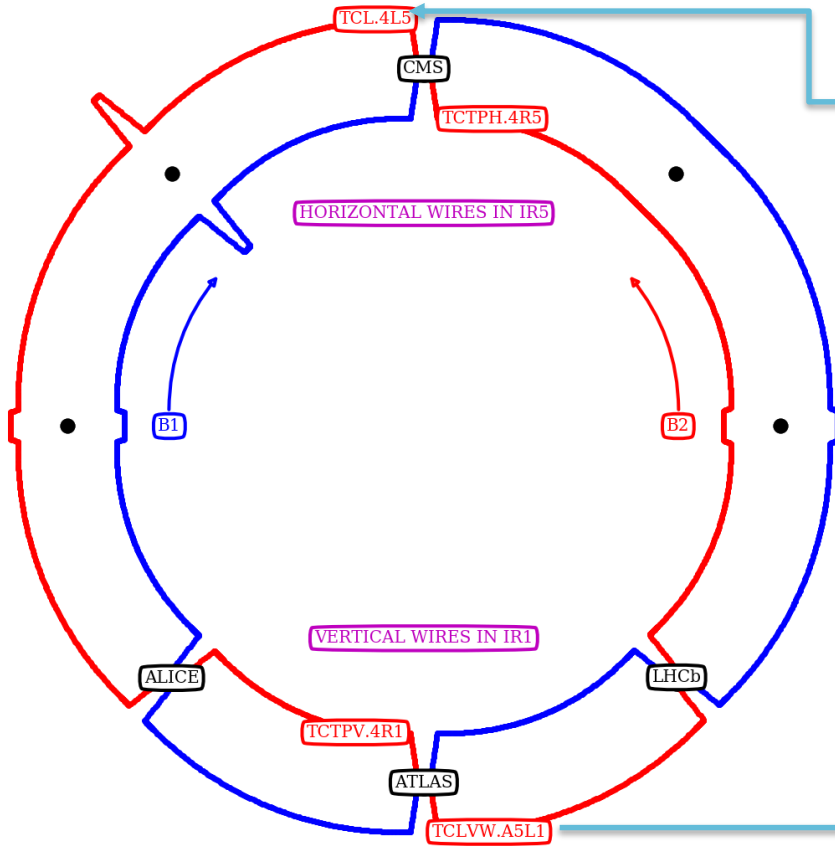
Beam-Beam and Luminosity Meeting on February 7th 2020

# Outline

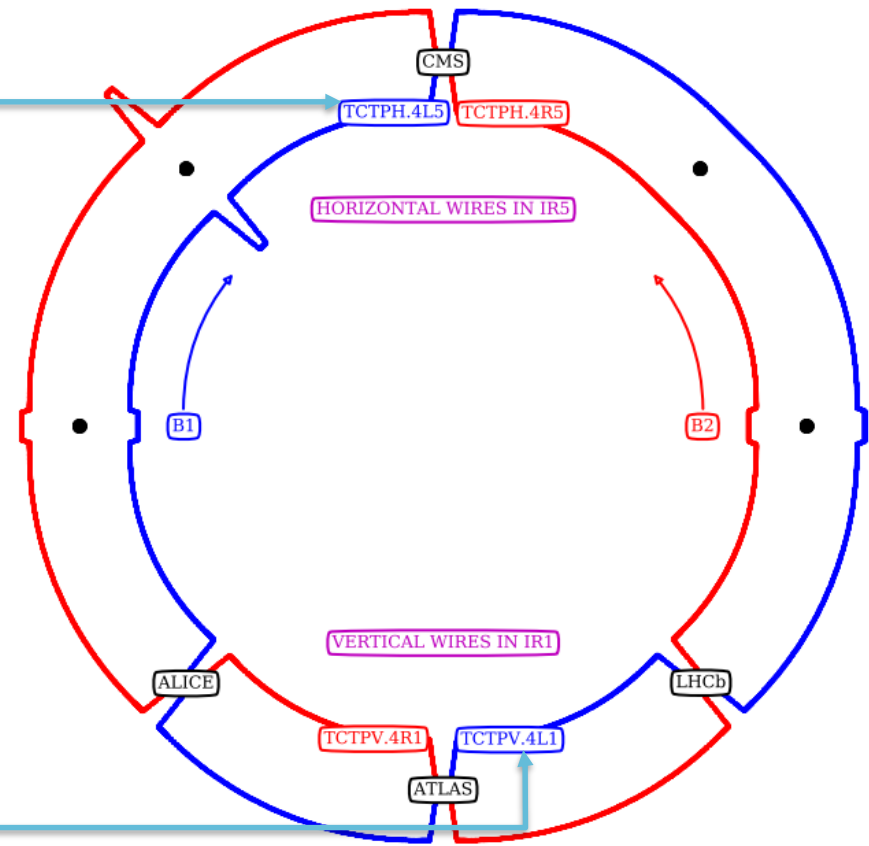
- New installation during LS2
- 2018 studies on effect of wire off (and Q4/5 trim on) on  $\beta$ -beating, tune shift and collimation hierarchy
- Power converter + circuit time constant
- Wire overheating
- Proposal for interlocks

# Changes during LS2

Before LS2



After LS2



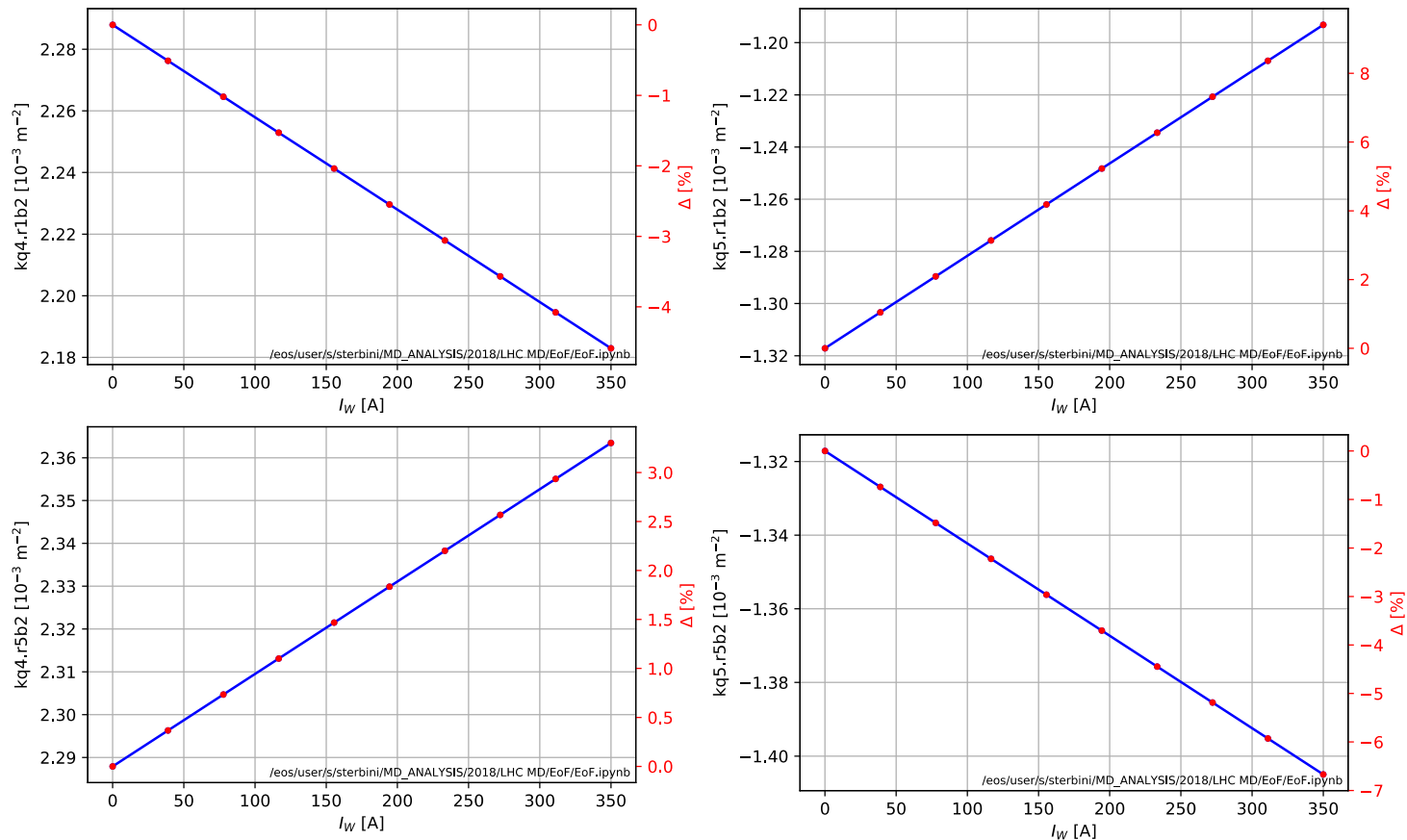
Courtesy of Guido Sterbini BE-ABP

/eos/user/s/sterbini/MD\_ANALYSIS/2018/LHC MD Optics/OpticsInjection.ipynb

Wire-in-jaw collimators have been moved to new position.  
Commissioning planned for Q4 of 2020

Beam-Beam and Luminosity Meeting on February 7th 2020

# Q4/5-feedforward on when wires on



When we trim a wire the Q4/5 close to the wire are trimmed to compensate as close as possible the quadrupolar perturbation of the wire.

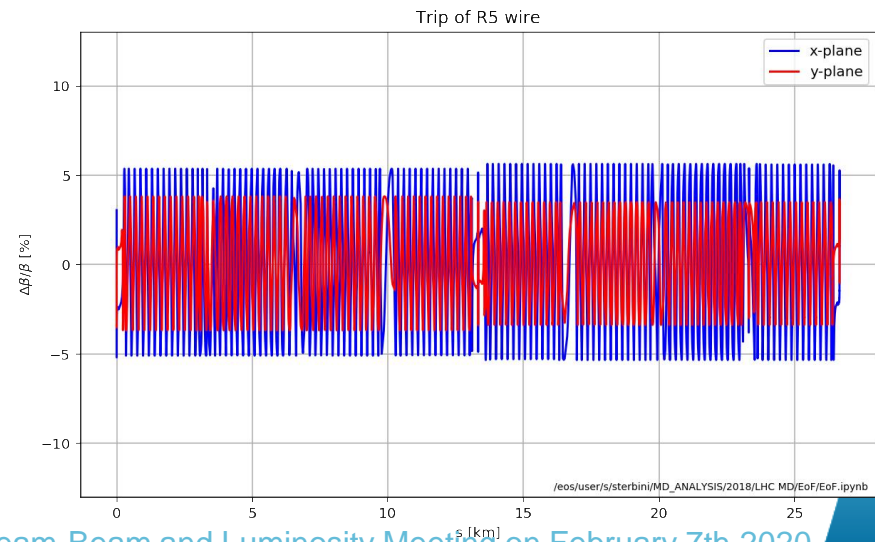
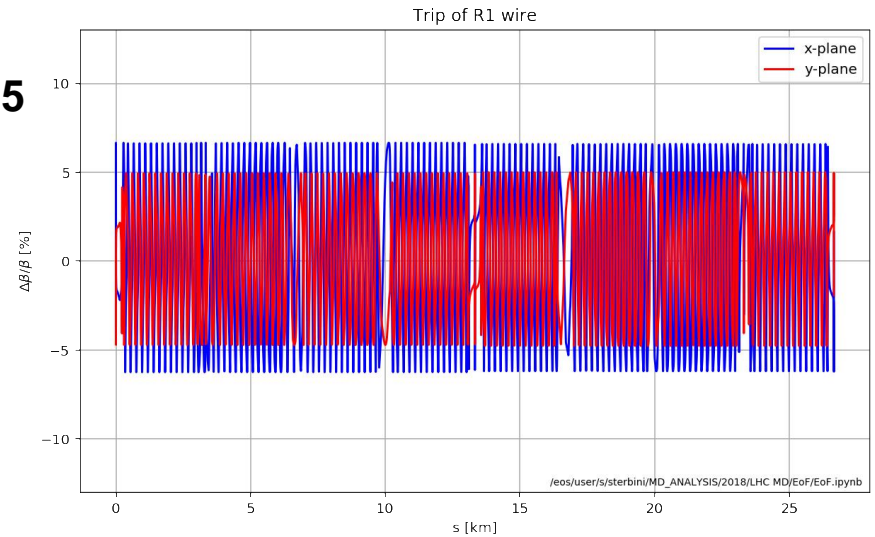
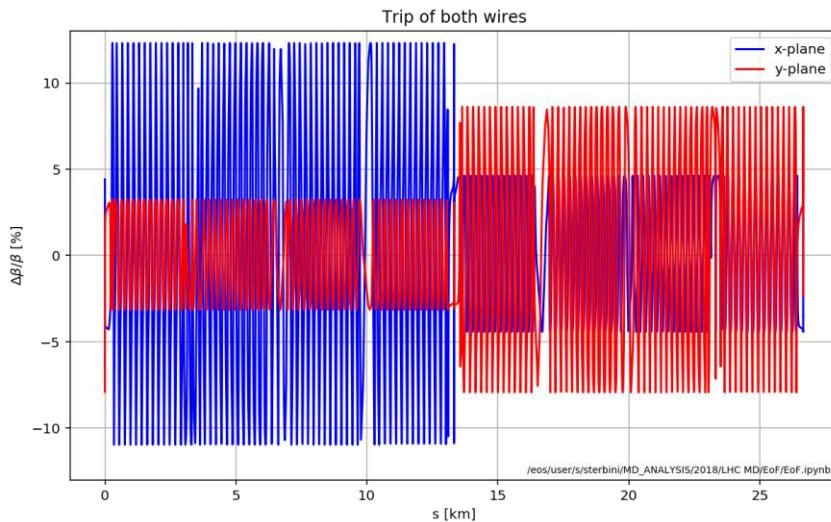
*G. Sterbini, M. Solfaroli*

# What if a wire PCs trips?

G. Sterbini

IF the wire PC trips, **AND** the beam is **NOT** automatically dumped: the Q4/5 trim will cause tune shift and  $\beta$ -beating.

Assuming we are using TCT4.R1 and TCT4.R5 at  $\beta^*=30$  cm and  $\theta c/2=130$  mrad



	$\Delta QH$	$\Delta QV$
<b>Trip on both wires</b>	-0.001788	0.002006
<b>Trip on R1 wire</b>	-0.009535	0.006858
<b>Trip on R5 wire</b>	0.008327	-0.005695

# Effect on collimation hierarchy (R. Bruce)

Studying effect on collimation hierarchy from  $\beta$ -beat due Q4/Q5 correction still running after wire trips on 2018 baseline optics

- Typically observing up to  $0.2 \sigma$  difference in effective collimator settings
  - Not expected to be critical for most collimators
  - No hierarchy breakage expected in IR7, unless  $\beta$ -beating from other effects comes on top
  - Up to  $0.7 \sigma$  difference in the worst case
- Most critical case: Effective  $\sigma$ -setting of dump protection and IR5 TCT

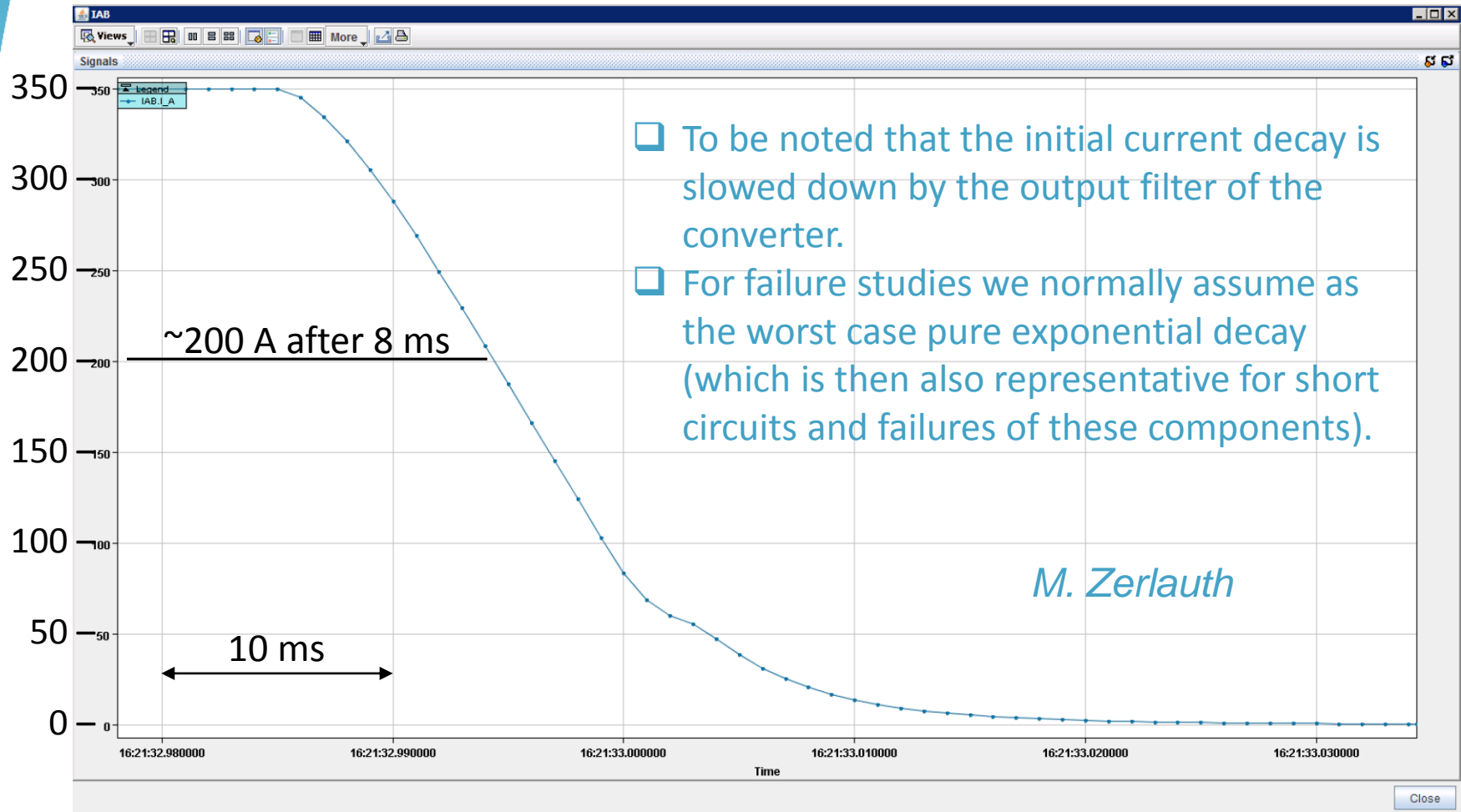
**30 cm**

**25 cm**

$\sigma$ -setting	Nominal	Trip IR5	$\sigma$ -setting	Nominal	Trip IR5
TCDQ.B4L6.B2	7.24	7.46	TCDQ.B4L6.B2	7.3	7.56
TCTPH.4R5.B2	8.5	8.43	TCTPH.4R5.B2	7.8	7.68

- At 25 cm, margin between TCDQ and TCT is reduced to about  $0.1 \sigma$ 
  - On top of other sources of  $\beta$ -beat, risk to be out of tolerance at 25 cm – discouraged running scenario
  - For regular operational use, preferable to do loss maps with wire off and compensation running
- Phase advance MKD-TCT shifts by 1-2 degrees and stays within tolerance – no issue expected
- For any operational use in Run 3, all studies should be repeated with final

# Wire current decay after converter fault



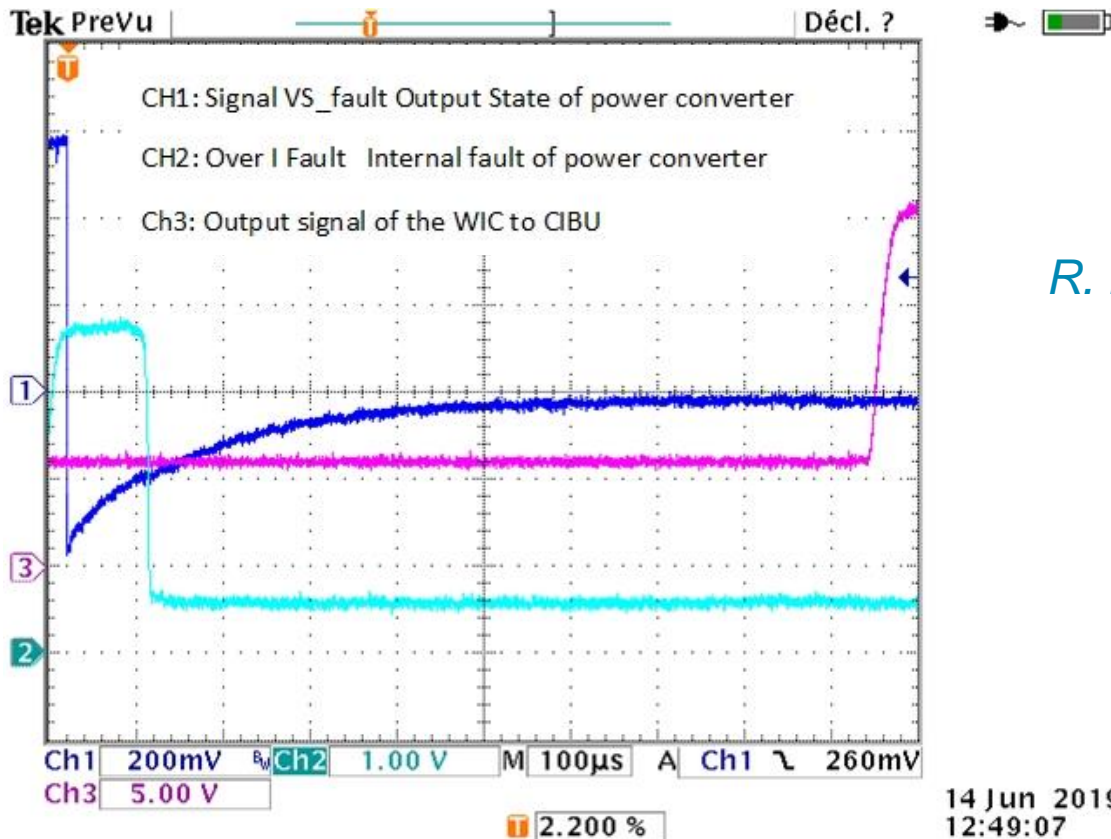
# Power converter failure, FPG and WIC

- There are 4 main reasons to generate POWERING\_FAILURE on the FGC2 (which is the one used for the BBCW) and the FGC3 (which is relevant for the RD1s, RD34s and in the future for newer converter installations):
  1. VSFAULT: Voltage source Internal Fault (fast power abort unsafe, over voltage, over current, aux PSU)
  2. VSEXTINTLK: Voltage source External Interlock (water, earth current, equipment stop button)
  3. DCCT faults
  4. FGCFAULT: which is used for remote testing as asserted from the software as well as the PIC2 tests.
- In the first 3 cases, the signal gets from the voltage source buffers to the FGC FPGA, via a relay to the WIC. Max reaction time = max. 350us (voltage source signal delay) + max. 10us (FPGA processing delay) + max. 3ms (relay reaction time) = **3.36ms**
- In the latter case, it depends on the software and might take from **~8ms** (FGC2, FGC3) to **20/40ms** (FGClite).

*M. Zerlauth*



- Very small overall delay between the occurrence of an internal converter failure until the beam dump to the BIS: 1.2ms for the latest FGC3 version, and 1ms for the FGC2



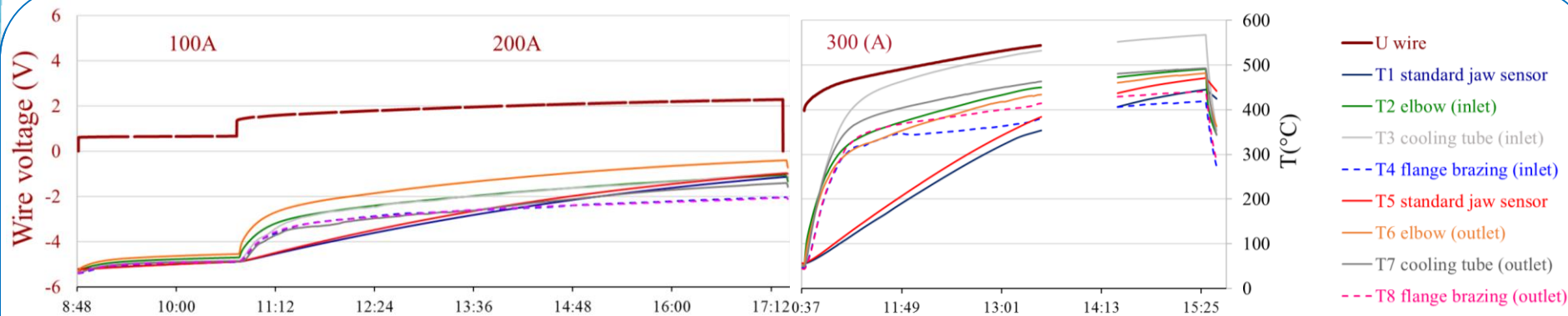
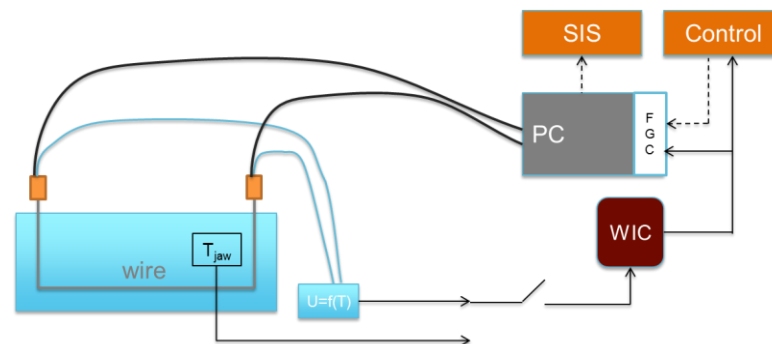
R. Mompo, L. Ceccone

FGC2

- Confirm (*M. Zerlauth*) WIC path sufficient interlock chain even for the most (time) critical failures of the wire compensator

# Wire overheating

- Wire resistivity  $f(T)$
- If wire voltage  $> 2.6V^*$   
= if hottest point @ 350A  
 $< 200^{\circ}C$ , WIC cuts the PC
- WIC could dump at the same time
- Long time constant of system**, no constraints on collimator HW



Tests performed on spare wire-in-jaw, under vacuum with no coolant

\*Note this also correspond to  $I_w=375A$

# Future work

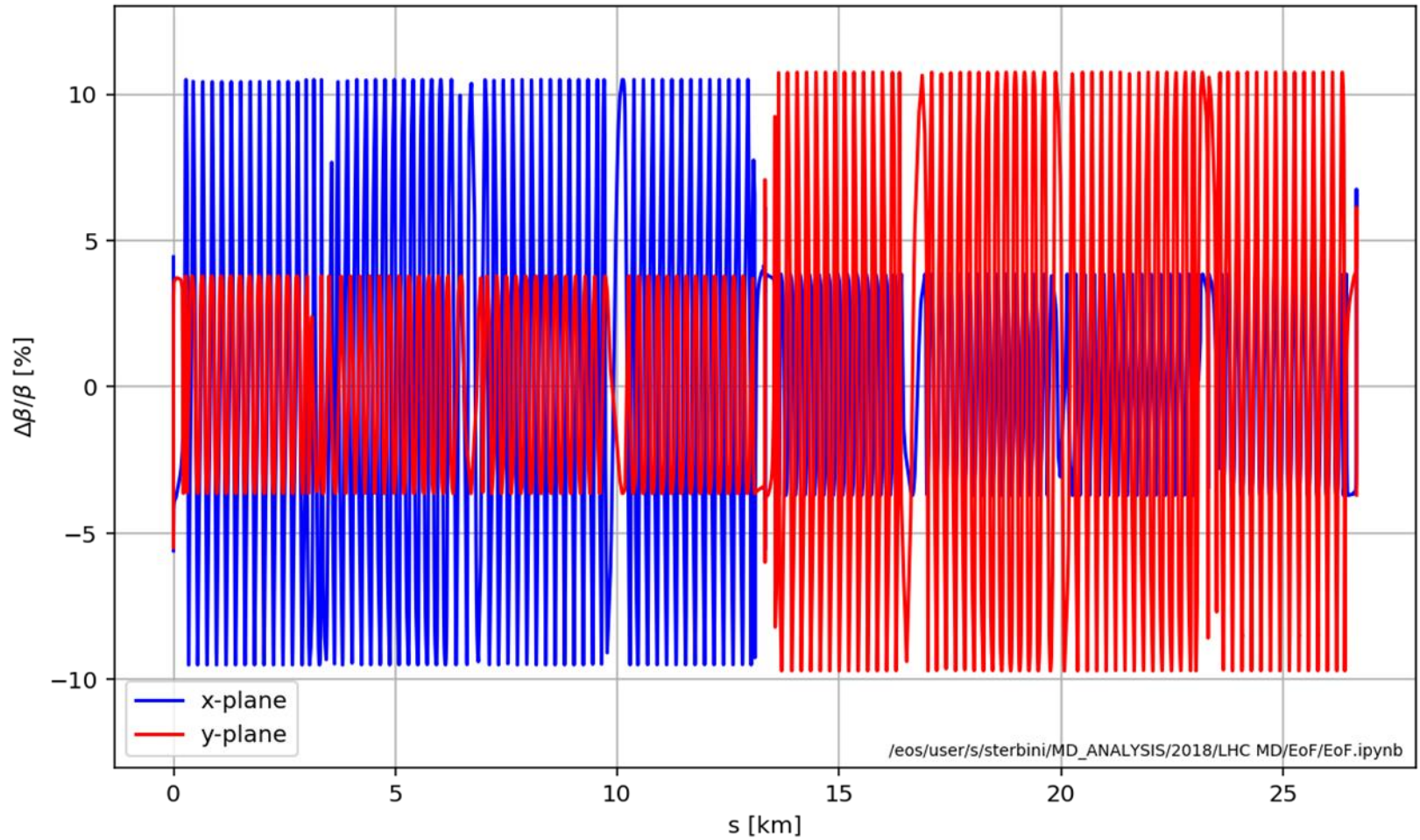
- Insert wire power converter into the matrix of converters for beam dump  
(R. Momo) – to be tested during commissioning
- Finalize tests on interlock delays with FGC2 : During standard commissioning, trigger a fast powering failure → observe the effect on the circulating beam and measure the reaction time of interlocks
- Define required controls changes : Jorg foresees introducing the control of the wire in the LHC sequence LBOC (3 Dec. '19) BUT not possible for all cycle. Needs discussion on operational use cases
  - (Guido at LBOC - 3 Dec. '19), wire switched on at end of levelling (still to be finalised).
- Commissioning procedure to be done, including list of tests after installation, revalidation after failure and replacement of voltage measuring card or power converter, after shut-downs.



***Thank you***



### Optics w/ BBLR vs optics w/o BBLR



# Backup – effective collimator settings

collimator	nominal 25cm	lhcb2_nominal_25c m	lhcb2_nominal_30c m	lhcb2_trip_25c m	lhcb2_trip_30c m	lhcb2_tripr1_25c m	lhcb2_tripr1_30c m	lhcb2_tripr5_25c m	lhcb2_tripr5_30c m	
TCTPH.4R8.B2	15.00	15.00	14.91	14.92	14.52	14.59	14.51	14.58	14.90	14.93
TCTPV.4R8.B2	15.00	15.00	14.82	14.84	14.28	14.36	14.53	14.58	14.61	14.65
TCP.D6R7.B2	5.00	5.00	4.97	4.97	4.98	4.98	4.96	4.96	4.97	4.97
TCP.C6R7.B2	5.00	5.00	5.03	5.04	5.06	5.06	4.91	4.93	5.20	5.17
TCP.B6R7.B2	5.00	5.00	5.01	5.01	5.04	5.03	4.95	4.96	5.09	5.08
TCSG.A6R7.B2	6.50	6.50	6.54	6.53	6.68	6.65	6.58	6.56	6.64	6.61
TCSG.B5R7.B2	6.50	6.50	6.51	6.50	6.66	6.62	6.73	6.68	6.43	6.43
TCSG.A5R7.B2	6.50	6.50	6.52	6.51	6.67	6.63	6.74	6.69	6.44	6.44
TCSG.D4R7.B2	6.50	6.50	6.68	6.65	7.01	6.93	6.88	6.82	6.81	6.77
TCSG.B4R7.B2	6.50	6.50	6.53	6.52	6.69	6.66	6.75	6.71	6.45	6.46
TCSG.A4R7.B2	6.50	6.50	6.48	6.48	6.46	6.47	6.54	6.53	6.41	6.43
TCSG.A4L7.B2	6.50	6.50	6.45	6.46	6.34	6.37	6.42	6.44	6.38	6.40
TCSG.B5L7.B2	6.50	6.50	6.43	6.45	6.19	6.25	6.23	6.28	6.39	6.42
TCSG.D5L7.B2	6.50	6.50	6.44	6.46	6.20	6.25	6.25	6.29	6.39	6.41
TCSG.E5L7.B2	6.50	6.50	6.45	6.46	6.21	6.27	6.25	6.30	6.41	6.43
TCSG.6L7.B2	6.50	6.50	6.52	6.53	6.35	6.38	6.35	6.38	6.52	6.53
TCLA.A6L7.B2	10.00	10.00	9.89	9.90	9.73	9.77	9.77	9.81	9.82	9.85
TCLA.B6L7.B2	10.00	10.00	10.05	10.05	9.78	9.83	9.87	9.91	9.93	9.96
TCLA.C6L7.B2	10.00	10.00	10.14	10.10	10.65	10.52	10.43	10.34	10.35	10.27
TCLA.D6L7.B2	10.00	10.00	10.04	10.04	9.87	9.90	10.13	10.12	9.77	9.81
TCLA.A7L7.B2	10.00	10.00	9.91	9.90	9.88	9.89	10.20	10.15	9.59	9.64
TCDQA.A4L6.B2	7.30	7.30	7.32	7.26	7.36	7.31	7.14	7.12	7.56	7.46
TCDQA.C4L6.B2	7.30	7.30	7.32	7.26	7.36	7.31	7.14	7.12	7.56	7.46
TCDQA.B4L6.B2	7.30	7.30	7.32	7.26	7.36	7.30	7.13	7.12	7.56	7.46
TCSP.A4L6.B2	7.30	7.30	7.31	7.25	7.34	7.29	7.12	7.10	7.55	7.45
TCTPH.4R5.B2	7.80	7.80	7.78	8.52	7.57	8.33	7.65	8.41	7.68	8.43
TCTPV.4R5.B2	7.80	7.80	7.78	8.50	7.91	8.62	7.83	8.55	7.83	8.55
TCP.6R3.B2	15.00	15.00	15.11	15.10	16.02	15.85	15.63	15.53	15.52	15.43
TCSG.5R3.B2	18.00	18.00	18.14	18.13	18.29	18.27	18.29	18.26	18.22	18.20
TCSG.4L3.B2	18.00	18.00	17.93	17.92	19.04	18.84	18.52	18.41	18.43	18.34
TCSG.A5L3.B2	18.00	18.00	17.93	17.91	18.95	18.76	18.59	18.46	18.30	18.22
TCSG.B5L3.B2	18.00	18.00	17.94	17.93	18.81	18.66	18.54	18.42	18.24	18.17
TCLA.A5L3.B2	20.00	20.00	20.19	20.20	20.36	20.33	20.75	20.66	19.78	19.84
TCLA.B5L3.B2	20.00	20.00	19.94	19.94	20.13	20.11	20.12	20.09	20.05	20.02
TCLA.6L3.B2	20.00	20.00	20.28	20.29	19.54	19.68	19.93	19.99	19.96	20.01
TCLA.7L3.B2	20.00	20.00	19.78	19.78	20.05	20.02	19.90	19.89	19.93	19.91
TCTPH.4R2.B2	37.00	37.00	36.86	36.85	39.27	38.95	38.13	37.98	37.94	37.79
TCTPV.4R2.B2	37.00	37.00	36.97	36.98	36.86	36.98	36.12	36.36	37.80	37.67