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Technical specification

Embedded Monitoring and Control Interface

Abstract

This document specifies the features and layout of the new embedded slow control module developed for the HL-LHC experiments. It is based on radiation hard components and primarily meant to serve as a bidirectional interface between experiment front-end electronics and detector control systems (DCS).

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1. Introduction

The importance of the efficient and reliable detector control system (DCS) increases with the complexity of the high energy physics experiments. The High Luminosity upgrade of the LHC puts further radiation tolerance onto the innermost detectors and relevant control systems. To fulfill these requirements a new DCS front-end interface hardware solution based on CERN Radiation Hard Optical Link Project components, the low power Giga Bit Transceiver (lpGBT) and the Versatile Link+ (VL+), is being proposed. This new interface system is targeted for deployment during the Long Shutdown 3 of the LHC. Note that the proposed system is meant to complement the ELMB2 [1] in aspects related to radiation tolerance and appliance.

2. Overview

The new system will consist of two core components: the Embedded Monitoring and Control Interface (EMCI) and the Embedded Monitoring Processor (EMP).
The aim of the EMCI, which is placed in a radiation-hard environment, is to work as an interface for the slow-control signals going in between different Front-Ends (FE) and the DCS system. It is based on the lpGBT, which combines all the signals of the FEs in one bidirectional channel and interfaces with the VTRx+, the optical transceiver, which transmits the data through the high-speed optical link. Both chips were designed at CERN to work in radiation-hard environments.
The connection from the EMCI to the FEs is done using a passive splitter board. This board, plugged into the EMCI by means of an FMC connector, is customized in order to be compatible to the FEs connection interface. Most common versions of the splitter boards are provided, but the user might design his own. Alternatively to interfacing FEs via the splitter board, the EMCI can also be mounted as mezzanine directly onto a carrier with a compatible FMC connector. The power input to the EMCI is provided locally through the FMC connector.

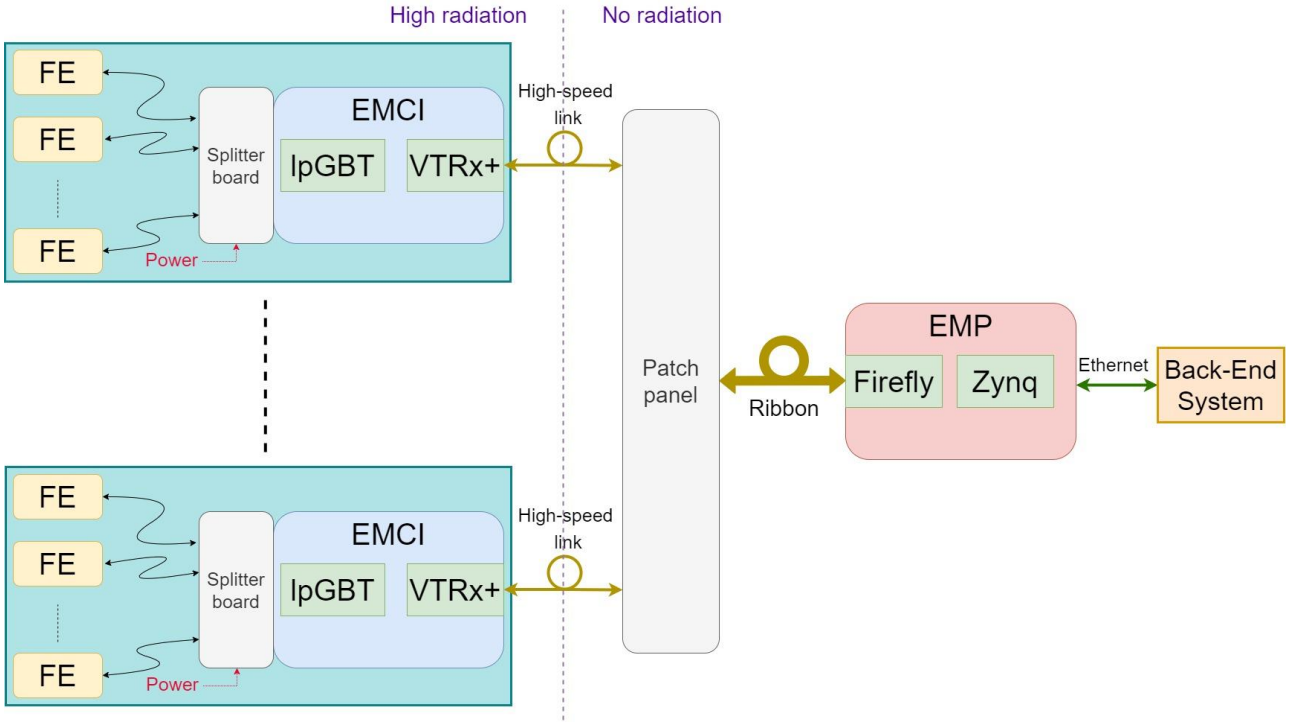

Figure 1: EMCI-EMP block diagram for a typical use case

At the same time, several EMCI VTRx+ are connected through a multichannel optical transceiver mounted on one EMP, which is placed in a radiation soft environment. The EMP, built on COTS components, processes and delivers the data to the counting room by means of an Ethernet connection. Note that the EMP project is still under conceptual design and may evolve in the future.

Given that the lpGBT is the main component of the EMCI, most of the features and descriptions of this document are referred to, and can be extended by the lpGBT manual [2].

3. Functionality

The EMCI offers all features provided by the lpGBT that are listed below:

- eLinks

  The slow-control data to/from FE can be transmitted through electrical connections called eLinks. The EMCI can interface simultaneously up to 28 devices for uplink (RX from the EMCI point of view) transmission and up to 16 devices for the downlink transmission (TX) as well as up to 28 synchronized clock signals, in case the FE requires it. The eLinks use the CERN Low Power Signaling (CLPS) standard, presented in section 4.1.1.1. These communication lines can be DC or AC coupled (see section 4.1.1).

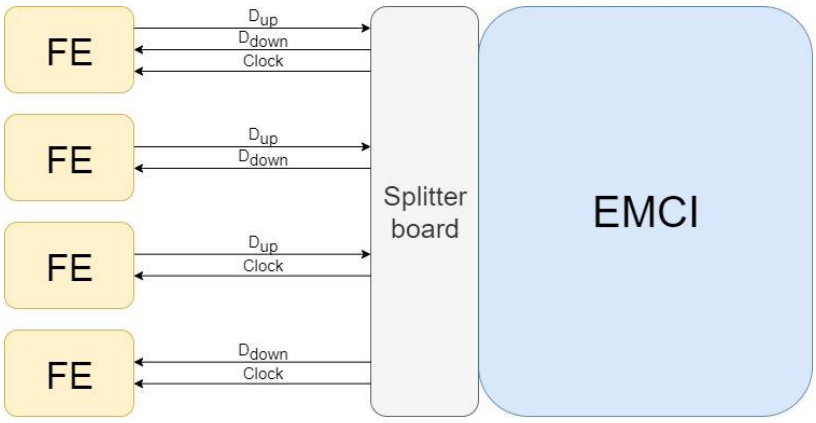

Figure 2: eLink connections to different FEs

The eLinks are divided in groups of 4, each group using the same bandwidth. If the bandwidth is set to minimum (x1), all four eLinks are available. However, if the bandwidth is higher (x2 or x4) less eLinks become available in that group (2 or 1, respectively).

Table 1 and Table 2 show the maximum number of eLinks available (for all the groups) depending on the chosen bandwidth. Additionally, there is available an extra slower eLink which can be used to connect an SCA or another device at 80 Mb/s.

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Table 1: Maximum number of downlinks per bandwidth

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Table 2: Maximum number of uplinks per bandwidth

- Phase programmable clocks

  Apart from the clocks provided with the eLinks, the EMCI provides 4 extra differential clock signals. These clocks are programmable independently in frequency (40, 80, 160, 320, 640 and 1280 MHz) and in phase (in 48.8 ps steps).

- General purpose I/O

  The EMCI has 16 general-purpose I/O pins synchronous with the internal system clock (40 MHz). All pins have built-in pull-up and pull-down circuit, which can be enabled independently.

- I2C interfaces

  The EMCI also has three independent I2C master interfaces (one of which is dedicated to VTRx+ configuration), with the following features:
  - Compliance with I2C standard, including 10-bit addressing
  - Concurrent operation of the three channels
  - Independently programmable data transfer rates: 100 KHz, 200 KHz, 400 KHz, 1 MHz
  - Supports single-byte and multi-byte (<=16) I2C read/write bus operations
  - Support read-modify-write bitwise operations with OR or XOR masks (7-bit addressing)
  - The SCL outputs are configurable as open-drain or full CMOS

  Each of the SCL and SDA pins can have an internal pull-up resistor enabled.
  An additional I2C slave interface is also available for lpGBT configuration (see section 4.1.4).

- Analog peripherals

  The EMCI provides an 8-channel multiplexed 10-bit SAR ADC and a 12-bit R-2R voltage DAC.
  The ADC has 8 input pins, which can be combined for differential measurements as well as be used individually for single-ended measurements. The input dynamic range goes from -1V to 1V and a programmable gain stage (x2, x8, x16 and x32) is used for measuring smaller voltages.
  The ADC is also used for internal measurements of the lpGBT (temperature sensor and power supply voltage).
  The DAC can provide voltages ranging from 0 to +1V.

- High-speed link

  A VTRx+ is plugged into the EMCI for transmitting the data through the fiber optics to the EMP. The system has a downlink bandwidth of 2.56 Gb/s and an uplink bandwidth of 5.12 or 10.24 Gb/s, depending on configuration. The links are equipped with Forward Error Correction (FEC) to detect and correct transmission errors and with scrambling to maintain the DC balance of the transmitted data and to enable reliable Clock and Data Recover (CDR).

4. Implementation

The EMCI core component is the lpGBT, which offers most of the functionality described in section 3. The schematics of the EMCI can be found in the appendix 7.1. A general overview of the EMCI can be seen in Figure 3.

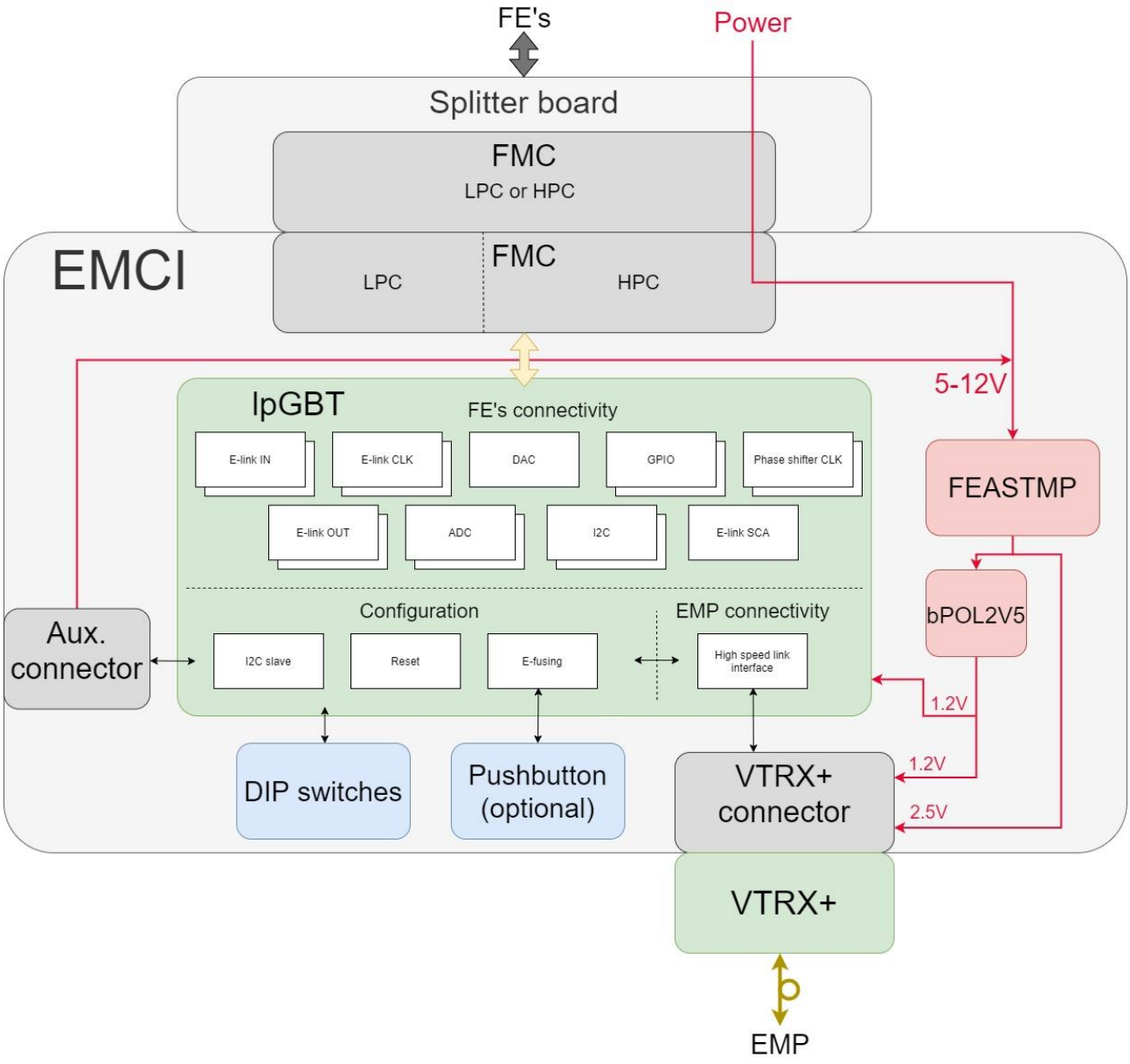

Figure 3: General EMCI block diagram

4.1 Architecture

The schematics of the eLinks and the high-speed interface features are presented below, as well as the power requirements and the configuration of the lpGBT.

4.1.1 eLinks

As explained before, the eLinks supply downlink data or clock or receive uplink data. The transmitters drive 100-ohm differential line without the necessity of any external components to the lpGBT. The receivers can be configured to have an internal 100-ohm termination enabled, as well as the possibility to use an equalizer and common mode bias circuit (see Figure 4).

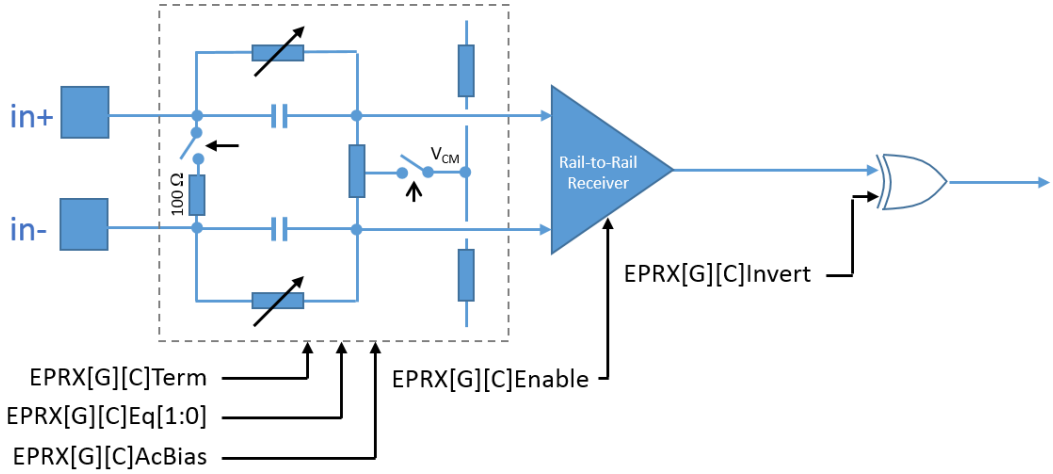

Figure 4: Receiver eLink

In both cases (transmitters and receivers), external capacitors can be added to AC couple the IO lines. Otherwise, the footprint will be populated with a 0-ohm resistor to be DC coupled. Note that this must be decided when assembling the EMCI PCB and, due to the size of these SMD components, cannot be changed afterwards.

4.1.1.1 CERN Low Power Signaling (CLPS)

The eLinks use the adopted CERN standard called CLPS. Its main characteristics are:

- Link types:
  - Point-to-point;
  - Multi-drop transmitter.
- Maximum data rate:
  - 1.28 Gb/s (NRZ signaling).
- Maximum clock frequency:
  - 1.28 GHz.
- Programmable signaling level:
  - 100 mV to 400 mV (single-ended amplitude);
  - 200 mV to 800 mV (differential amplitude).
- Common mode voltage:
  - 600 mV (nominal, for 1.2 V supply voltage).
- Load impedance:
  - 100 Ohm differential.

4.1.2 High-speed link

The high-speed link uses the VTRx+ to transmit all the information from the FEs (eLinks, ADC's, I2C…) to/from the EMP. The downlink (FEs direction) uses a bandwidth of 2.56 Gb/s and the uplink (EMP direction) can be configured to use either 5.12 Gb/s or 10.24 Gb/s.

The main clock used by the lpGBT (40 MHz) is obtained directly from the downlink frames, so there is no need to add external clock source (note that this means that the EMCI cannot be configured to transmit data exclusively in uplink direction).

The high-speed link has Forward Error Correction (FEC) capability to detect and correct transmission errors. It also uses de-scrambling (and scrambling), as well as de-interleaving (and interleaving) techniques to improve Clock and Data Recovery (CDR). For more information about these topics, please see the lpGBT user manual, section 4.

4.1.3 Power

The EMCI is powered through the FMC connector (or through the auxiliary connector when debugging) and needs a voltage input of 5-12V. The consumption depends on the number of eLinks used, as well as the data rate, but some approximations have been made:

- The power consumption of the lpGBT with all eLinks enabled should not exceed 500 mW [3].
- The power consumption of the VTRx+ with all channels enabled should not exceed 254 mW [4].
- The EMCI should not exceed 1W of power, considering the lpGBT, VTRx+, other losses, etc.

The EMCI uses a FEASTMP module [5] to convert the input voltage to 2.5V (used by the VTRx+) and a bPOL2V5 chipset [6] that lowers to 1.2V (used by the lpGBT and the VTRx+). Both devices have been designed at CERN and are radiation hard.

4.1.4 Configuration

In order to operate the EMCI, the lpGBT and the VTRx+ (by means of the lpGBT) must be pre-configured. The lpGBT has an I2C slave interface, which is accessible from the local auxiliary connector (section 4.2.3) that is used for reading and writing all the registers. Moreover, when correctly pre-configured, the lpGBT registers are also accessible via the high-speed link interface, making it possible for the EMP to configure the lpGBT directly.

It is possible to permanently store this configuration by means of e-fusing. This way, the lpGBT can restore the default values in the registers that allow configuration through the high-speed link after power cycling. In order to perform e-fusing operation (which can be executed only once), 2.5V need to be provided to the lpGBT. This may be provided manually, using the pushbutton on the EMCI, or automatically from the local auxiliary connector.

The EMCI also uses several DIP switches to pre-configure the state of the lpGBT:

- MODE: this is used to configure the EMCI as duplex up/downlink or as simplex downlink (simplex uplink is not available), as well as choosing the data rate for the high-speed uplink (5.12 or 10.24 Gb/s) and the FEC encoding (FEC5 or FEC12).
- ADDR: the position of the switches define the I2C address for the lpGBT configuration.
- SC_I2C: this switch selects the interface through which the lpGBT shall be configured (local I2C slave or remote serial high-speed link).

4.2 Interfaces

4.2.1 Front End interface

In order to keep the PCB as simple and small as possible, all the signals going and coming from all the FEs and the power input to the EMCI are routed to a FMC (HPC) connector. Furthermore, given that each EMCI might be connected to a different set of FEs, a customized splitter board is used. This passive board is plugged into the EMCI with the FMC that can be HPC or LPC (having some of the features not available but still with basic functionality provided). To interface with the FEs, the splitter board separates all the signals through the set of pigtails according to the needs of each user (Figure 5).

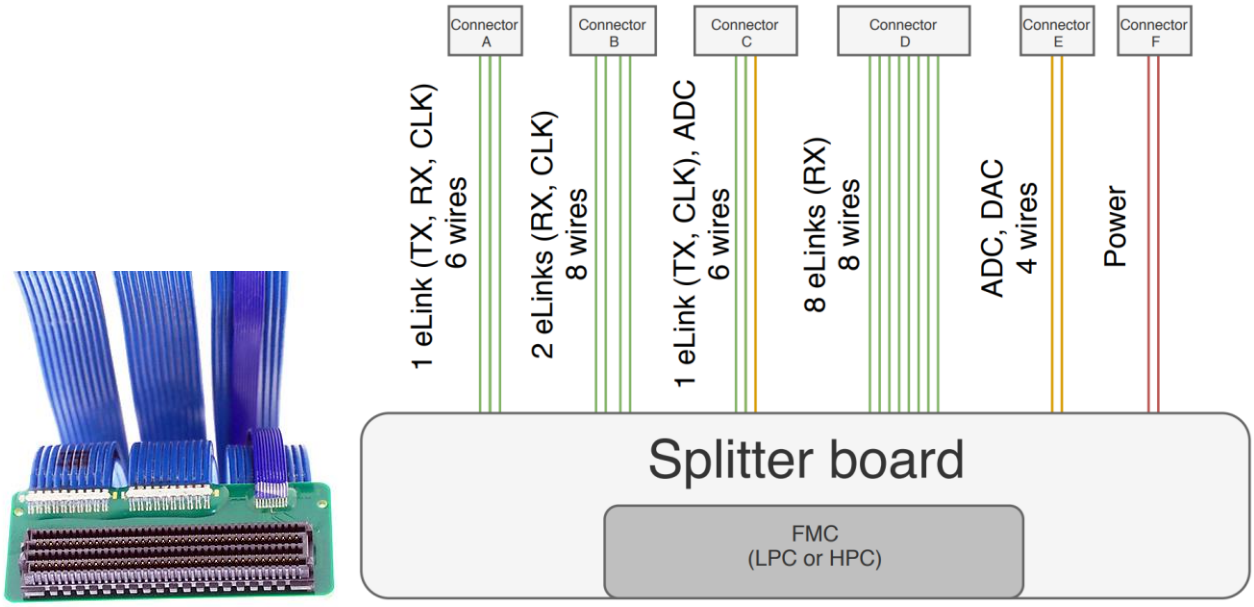

Figure 5: PCB with FMC connector and attached cables (left) and schematic example of a splitter board (right)

Some standard versions of the splitter board are available, but the user may design his own version to cover very specific needs.

The EMCI can be provided with a female FMC connector on the same side as the FEASTMP or with a male FMC connector on the opposite side. Having both connectors at the same time is also possible, but only one should be used at the same time because they share the same signals.
This way it is possible to mount the splitter board as a mezzanine, right over the EMCI, or facing out. The EMCI can also be mounted directly onto a carrier.

The final pinout for the FMC connector is not yet defined and depends on the PCB routing. However, it is expected to be partially compatible with the FMC standard (VITA 57.1). All the power and GND assignments are respected, but in order to fit all the connections, some non-general purpose pins are also used. This way the EMCI is pluggable into another module that follows the standard without damaging any of the devices. The guidelines for the pinout can be found in appendix 7.2.

4.2.2 Back end interface

The interface to the EMP uses the VL+ system [7]. The VTRx+ module is connected to the EMCI (pinout in appendix 7.3) and uses two multimode optic fiber channels (TX and RX) to transmit data between the EMP and the EMCI.

4.2.3 Configuration interface

In order to configure the lpGBT locally, a 14-pin AMP connector (5103308-2) is used (pinout in appendix 7.4). This connector provides the following features:

- I2C slave protocol for writing/reading the lpGBT registers
- Mode set for lpGBT
- E-fusing 2.5V
- FEASTMP enable/disable
- Reset line
- 1.2V output
- 5-12V input for power

5. 3D models

The presented 3D model is a sketch of the EMCI, lacking many small components, and may evolve in the future. The final layout will depend on the appropriate routing following lpGBT guidelines and pinouts with all the components in place.
Approximate dimensions: 90x75mm

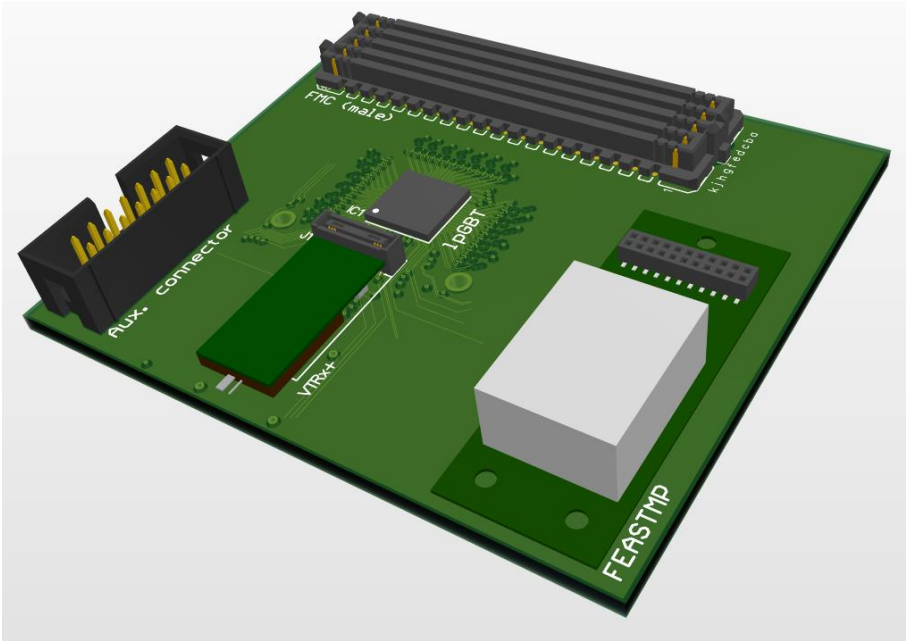

Figure 6: 3D model top side

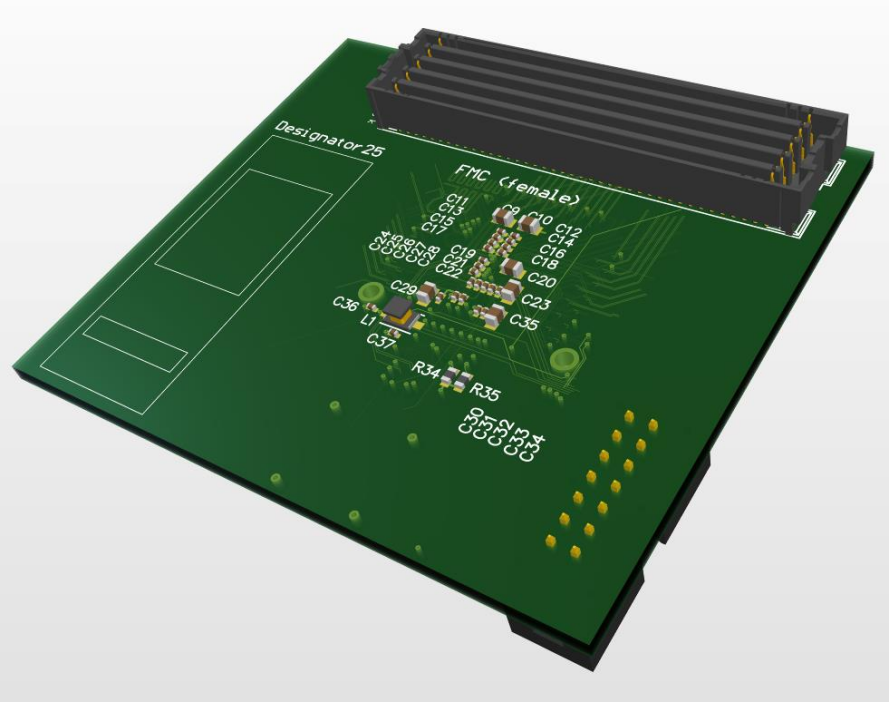

Figure 7: 3D model bottom side

One important factor that will determine the orientation of the FMC connector is the height of the tallest component on the top side (e.g. FEASTMP). In order to place the splitter board as a mezzanine over the FEASTMP, it must be shorter than the two FMC connected, considering also that can dissipate enough heat.

6. References

[1] K. Nicpon et al. The Embedded Local Monitor Board upgrade proposals. https://pos.sissa.it/343/034/pdf

[2] GBT Team. lpGBT manual. https://lpgbt.web.cern.ch/lpgbt/manual/

[3] P. Moreira. "The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC". Topical Workshop on Electronics for Particle Physics, Sept. 2019

[4] J. Troska. Versatile Link+ Transceiver (VTRx+). Technical Specification, part 2.1. https://edms.cern.ch/ui/file/1719329/1/VTRxPlus_spec.pdf

[5] DCDC converters team. FEASTMP Datasheet. http://project-dcdc.web.cern.ch/project-DCDC/public/Documents/FEAST2Mod_Datasheet_gb2016.pdf

[6] DCDC converters team. bPOL2V5_V2.2 Datasheet. http://project-dcdc.web.cern.ch/project-DCDC/public/Documents/bPOL2V5_V2.2%20datasheet%20rev4.pdf

[7] J. Troska, C. Soos, L. Olanterä. The Versatile Link+ Application Note. https://edms.cern.ch/ui/file/2149674/1/VTRxPlusApplicationNote.pdf

7. Appendix

7.1 Schematics

7.2 FMC pin assignments

Final pin assignments depend on PCB routing. The FMC standard is shown in Table 1.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

Table 3: VITA 5.12 standard

User-defined pins:

- LA[00..33]_P/N (LPC) (34 d) – User defined
- HA[00..23]_P/N (HPC) (24 d) – User defined
- HB[00..21]_P/N (HPC) (22 d) – User defined (not debuggable using FPGA eval. board)
- DP[0..9]_M2C_P/N (10 d) – Gigabit transceiver (not debuggable using FPGA eval. board)
- DP[0..9]_C2M_P/N (10 d) – Gigabit transceiver (not debuggable using FPGA eval. board)

Pinout:

- E-links (16+28+28 d):
    - LA[00..24]_P/N (7 OUT, 9 IN, 9 CLK)
    - HA[00..13]_P/N (3 OUT, 6 IN, 6 CLK)
    - HB[00..21]_P/N (6 OUT, 8 IN, 8 CLK)
    - DP0_M2C_P/N and DP0_C2M_P/N (1 IN, 1 CLK)
    - DP[1..9]_M2C_P/N (2 OUT, 6 IN, 6 CLK)

- ADC x8 (8 se, can be used in diff.)
    - LA[25..26]_P/N (4 ch)
    - HA[14..15]_P/N (4 ch)
- GPIO x16 (16 se)
    - LA[27..30]_P/N (8 ch)
    - HA[16..19]_P/N (8 ch)
- E-link for SCA (3 d)
    - HA[20..22]_P/N
- DAC (1 se)
    - LA33_P
- I2C x2 (4 se) (there is extra one for VTRx+)
    - LA[31..32]_P/N
- Phase shifter CLK x4 (4 d)
    - HA23_P/N (1 ch)
    - DP[1..3]_C2M_P/N (3 ch)
- RSTOUTB (1 se)
    - LA33_N

7.3 VTRx+ pin assignments

VTRx+ connector pinout in PCB:

Pin #	Name	Description	Pin #	Name	Description
1	VCCR2V5	2.5V Power supply for TIA	2	n/c	
3	VCCR2V5	2.5V Power supply for TIA	4	RSSI	RSSI current output from TIA, to be pulled up via a resistor to VCCR2V5
5	GND	Ground	6	GND	Ground
7	RXN	Rx $\overline{\text{output}}$	8	SDA	I2C data (to be pulled-up to VCCT1V2)
9	RXP	Rx output	10	SCL	I2C clock (to be terminated to VCCT1V2)
11	GND	Ground	12	GND	Ground
13	TX1N	Tx Ch.1 $\overline{\text{input}}$	14	RSTN	Laser Driver Reset
15	TX1P	Tx Ch.1 input	16	DIS	Laser Driver Disable
17	GND	Ground	18	GND	Ground
19	TX2N	Tx Ch.2 $\overline{\text{input}}$	20	n/c	
21	TX2P	Tx Ch.2 input	22	n/c	
23	GND	Ground	24	GND	Ground
25	TX3N	Tx Ch.3 $\overline{\text{input}}$	26	n/c	
27	TX3P	Tx Ch.3 input	28	n/c	
29	GND	Ground	30	GND	Ground
31	TX4N	Tx Ch.4 $\overline{\text{input}}$	32	TH1	10k Thermistor Terminal 1
33	TX4P	Tx Ch.4 input	34	TH2	10k Thermistor Terminal 2
35	GND	Ground	36	GND	Ground
37	VCCT2V5	2.5V Power supply for Laser Driver	38	VCCT1V2	1.2V Power supply for Laser Driver
39	VCCT2V5	2.5V Power supply for Laser Driver	40	VCCT1V2	1.2V Power supply for Laser Driver

Table 4: VTRx+ connector pinout

7.4 Auxiliary connector pin assignments

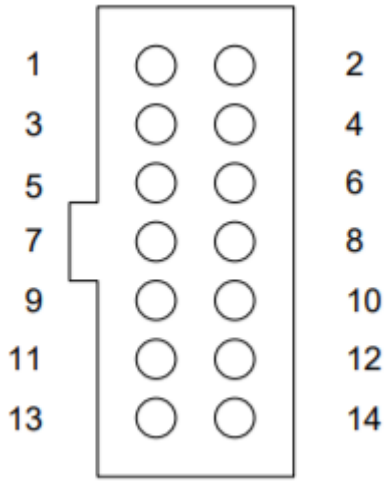

Figure 8: Auxiliary connector schematics

Pin #	Name	Description
1	MODE0	lpGBT mode selection
2	SCL	lpGBT I2C slave communication clock line
3	MODE1	lpGBT mode selection
4	SDA	lpGBT I2C slave communication data line
5	MODE2	lpGBT mode selection
6	GND	Ground
7	DCDC EN	FEASTMP module enable
8	1.2V OUT	1.2V output
9	MODE3	lpGBT mode selection
10	RST	lpGBT reset
11	2.5V IN	lpGBT 2.5V input for e-fusing
12	GND	Ground
13	12V IN	12V input power
14	GND	Ground

Table 5: Auxiliary connector pinout