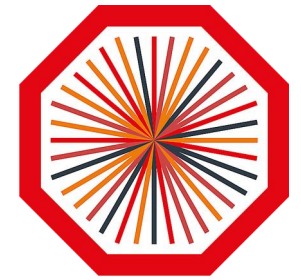


A Large Ion Collider Experiment

# The ITS3 project

[https://alice-collaboration.web.cern.ch/menu\\_proj\\_items/ITS-3](https://alice-collaboration.web.cern.ch/menu_proj_items/ITS-3)



ALICE

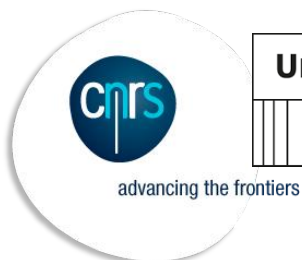
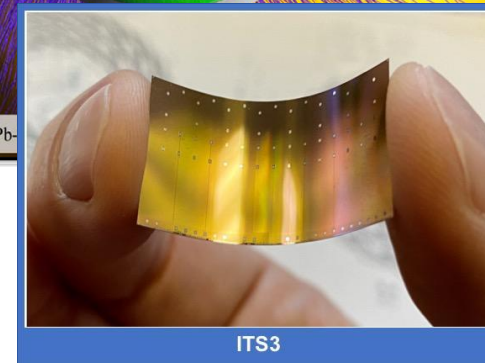
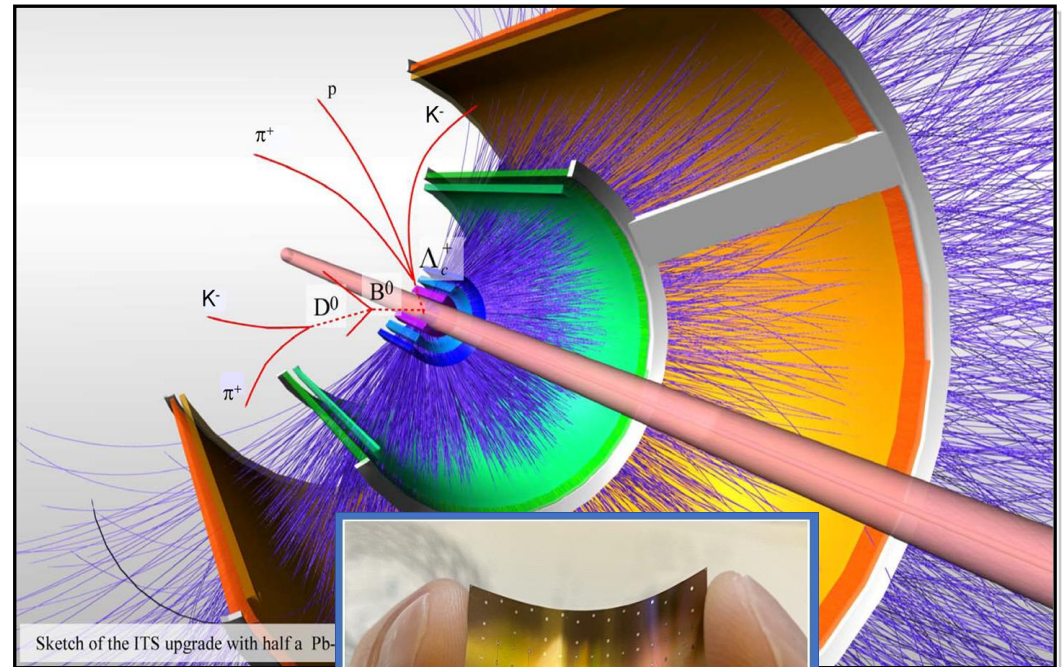
- **Technological feasibility**

- Wafer-scale chips
- Flexible chips

- **Tracking performance**

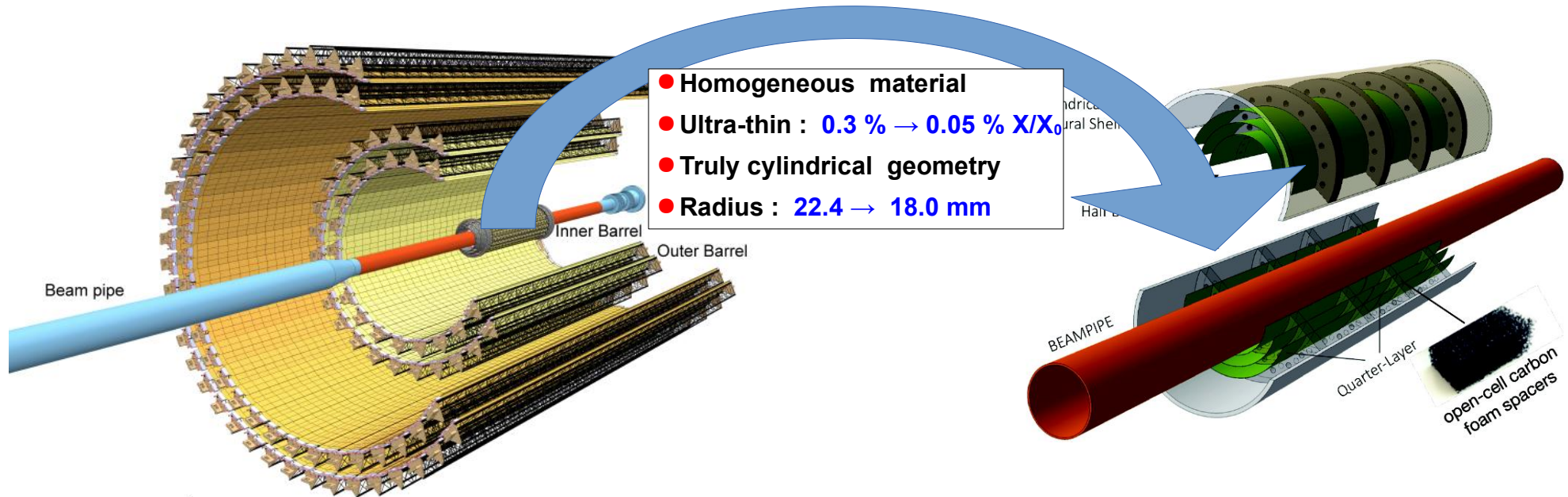
- **Examples of measurements**

- Charmed baryons ( $\Lambda_c$ )
- Thermal di-electrons
- $B_s$ ,  $\Xi_c$ , ...



# From ITS2 to ITS3 ( after LS3, 2027... )

<https://cds.cern.ch/record/2644611>



LARGE HADRON COLLIDER COMMITTEE

CERN/LHCC-2019-010

Minutes of the one-hundredth-and-thirty-ninth meeting held on

LHCC-139

Wednesday and Thursday, 11-12 September 2019

September 2019

- The **LHCC is impressed** by the new concept for the ITS3 with significantly reduced material budget, recognises the physics case presented in the LoI and in the dedicated ITS3 session and appreciates the on-going simulations on various physics channels to further demonstrate the expected gain from better resolution and efficiency at low transverse momentum. The LHCC endorses the plan of ALICE to carry out the necessary R&D studies to demonstrate the technical feasibility of this upgrade project. A TDR to be submitted on a timescale compatible with installation in LS3 will have to include in addition a comprehensive study of its physics gains with respect to the ITS2 detector.

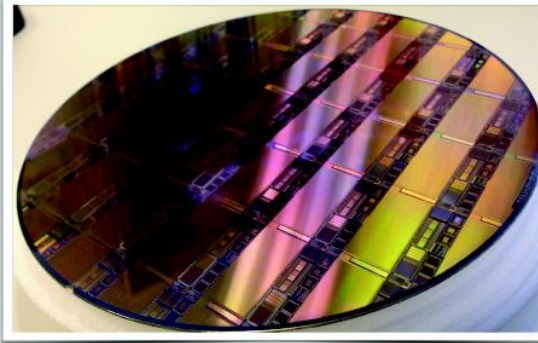


# Wafer-scale chips

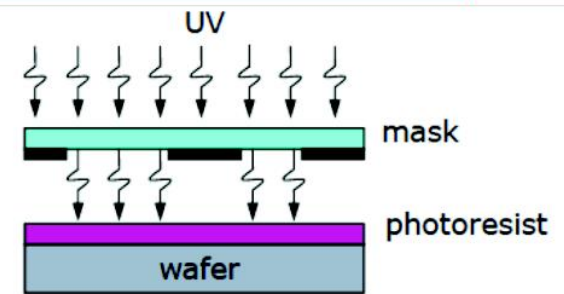
Magnus MAGER (CERN)

- chip size is traditionally limited by CMOS manufacturing (“reticle size”)
- new option: **stitching**, i.e. aligned exposures of given parts of a reticle to produce a larger circuit
- feasible, but needs specific design
- on a with 300 mm wafer (available in 65 nm technology node), a single chip fits a full half-layer

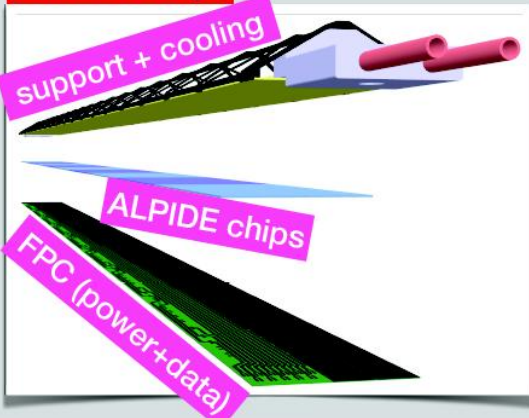
200 mm ALPIDE prototype wafer



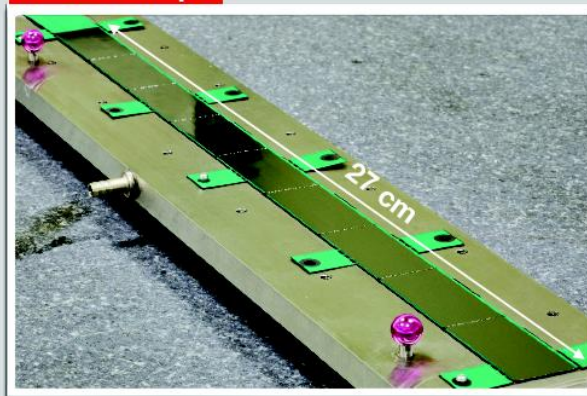
Principle of photolithography



Stave design

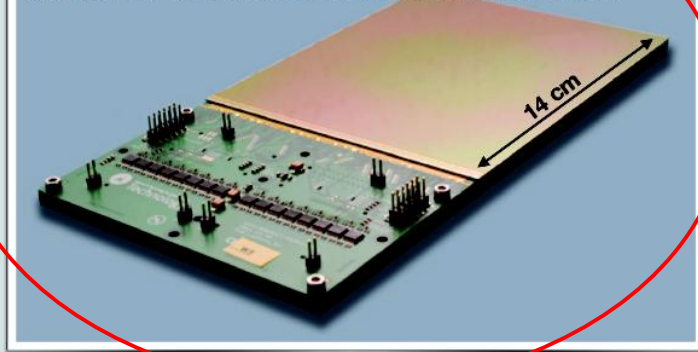


FPC + chips



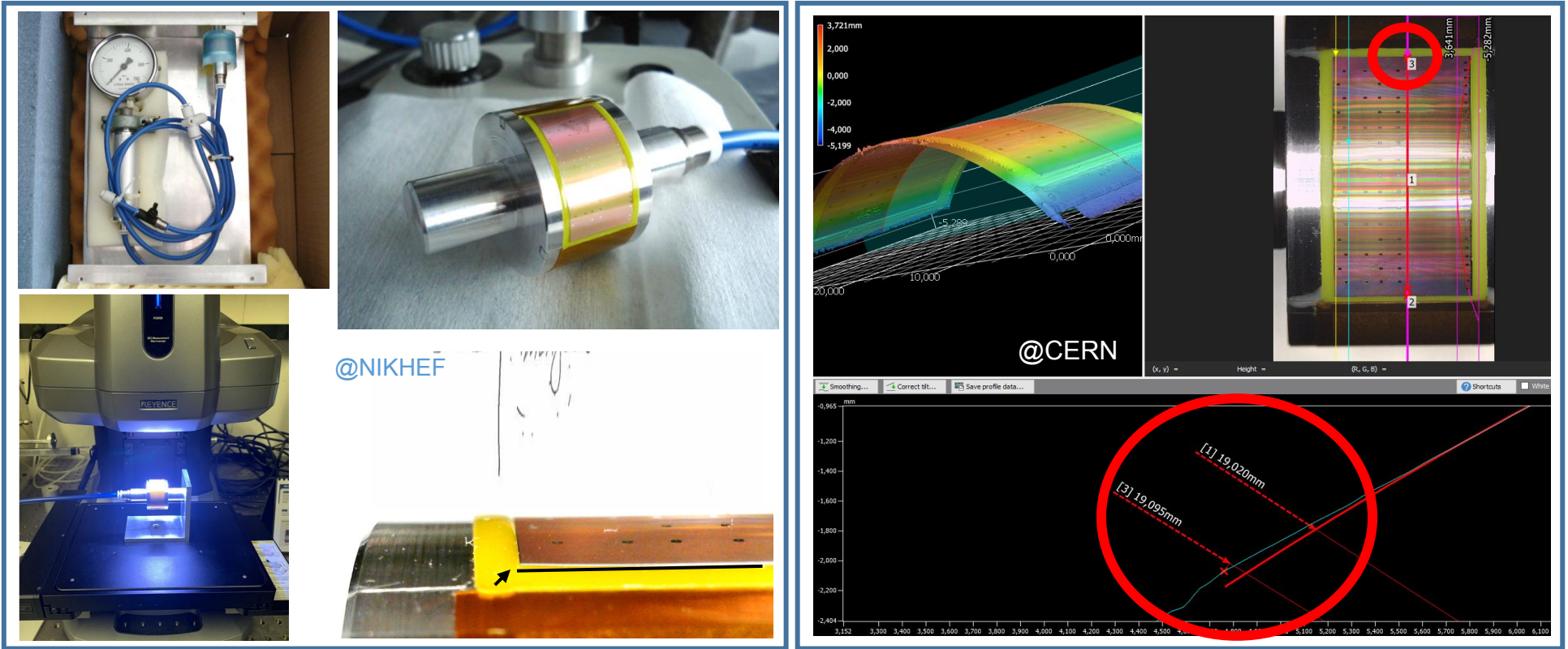
Wafer-scale sensor

Courtesy: R. Turchetta, Rutherford Appleton Laboratory



# Tests with bent ALPIDE chips

Corrado GARGIULO (CERN)



The feasibility of bent MAPS was demonstrated for the first time. In particular, 50  $\mu\text{m}$ -thick ALPIDE chips were measured in the laboratory and in a beam test while being bent to radii of about 22mm. They show no sign of any deterioration in operation. Their charge thresholds remain unaffected by the bending and detection efficiencies are measured to largely exceed 99.9% without any visible systematic degradation across the full chip surface.

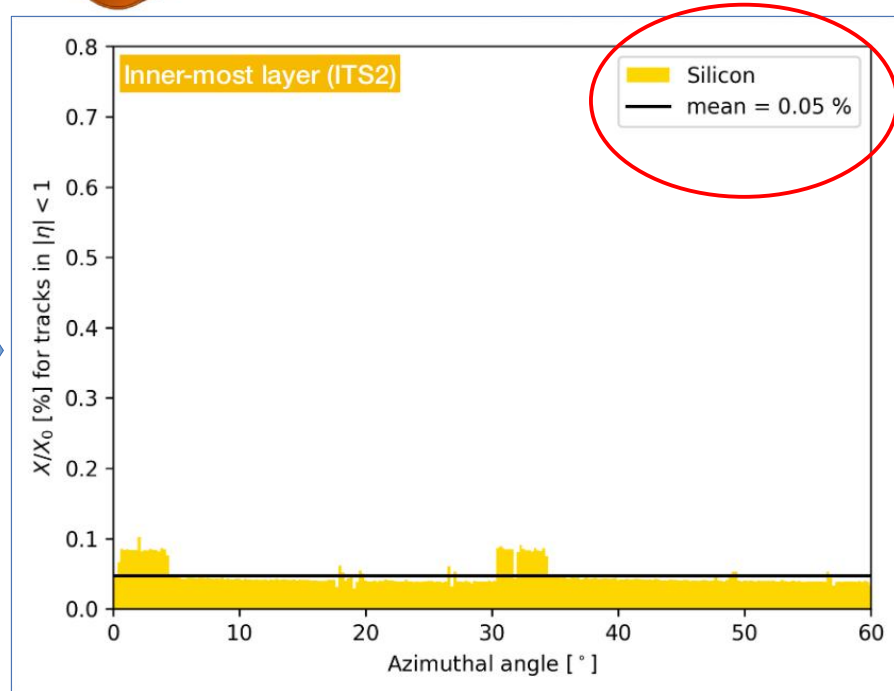
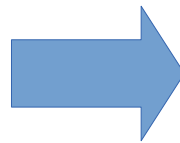
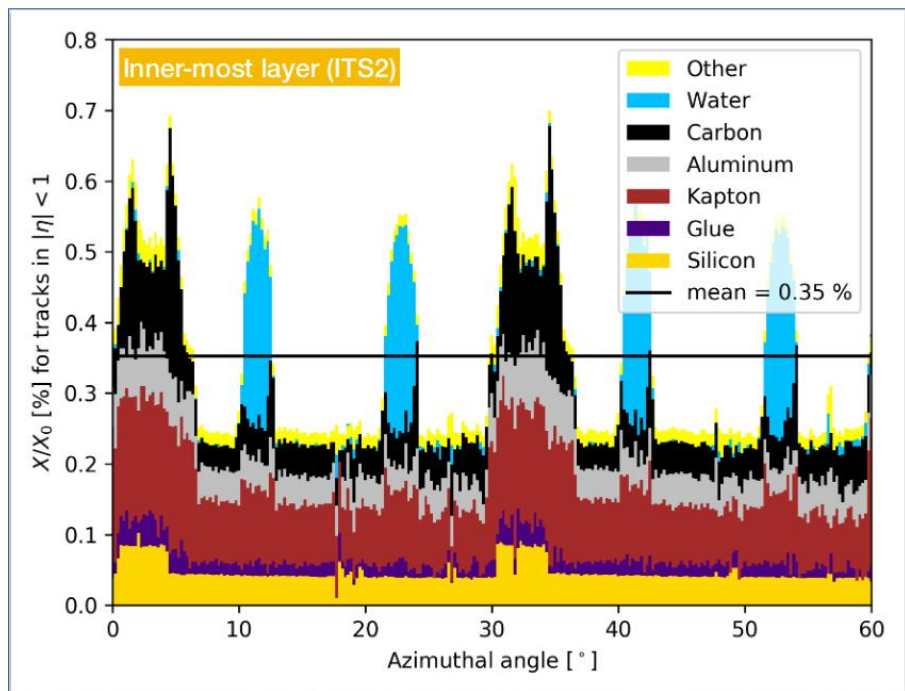
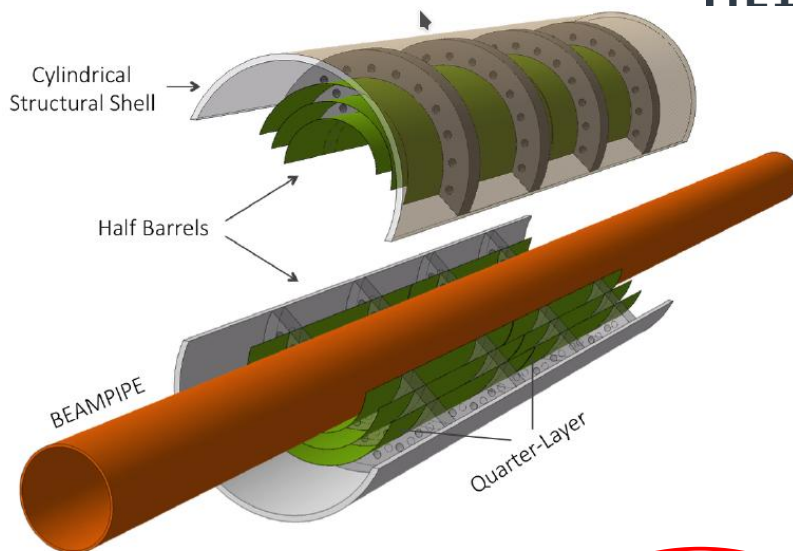
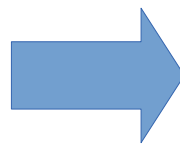
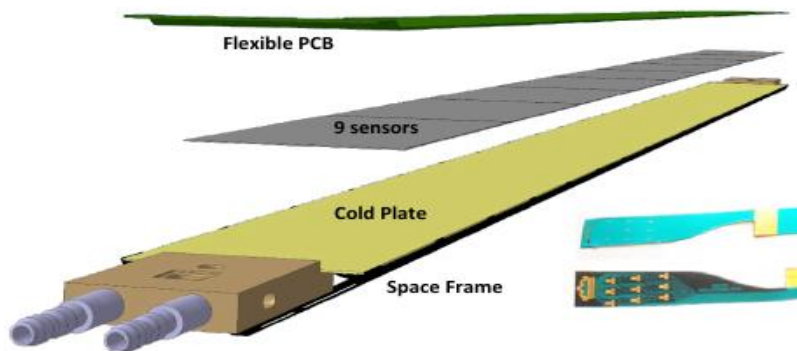
These very encouraging results do not only mark an important milestone in the R&D carried out for the ALICE ITS3, but generally open the way to highly integrated, silicon-only, bent sensor arrangements. A new class of detector designs featuring ideal geometries and yielding unprecedented performance figures is at reach.



arXiv:2105.13000 [physics.ins-det]



# Unprecedentedly low material budget

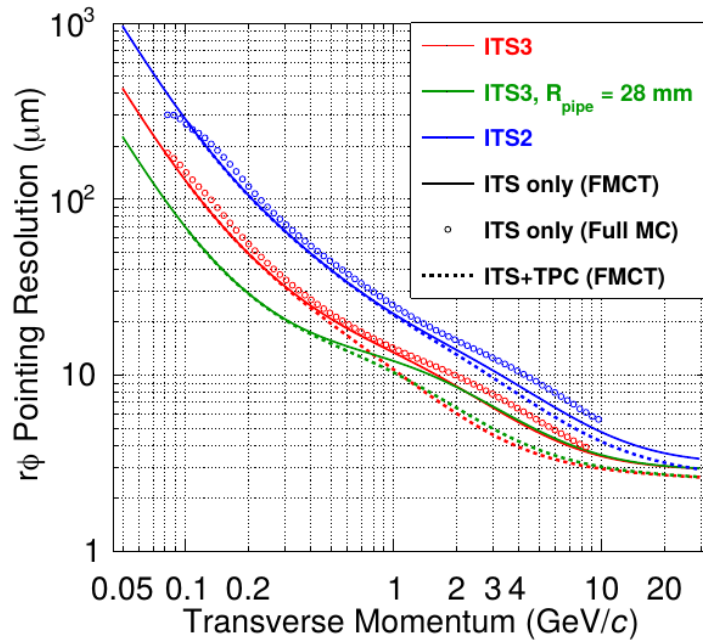


# ITS3 synoptic table

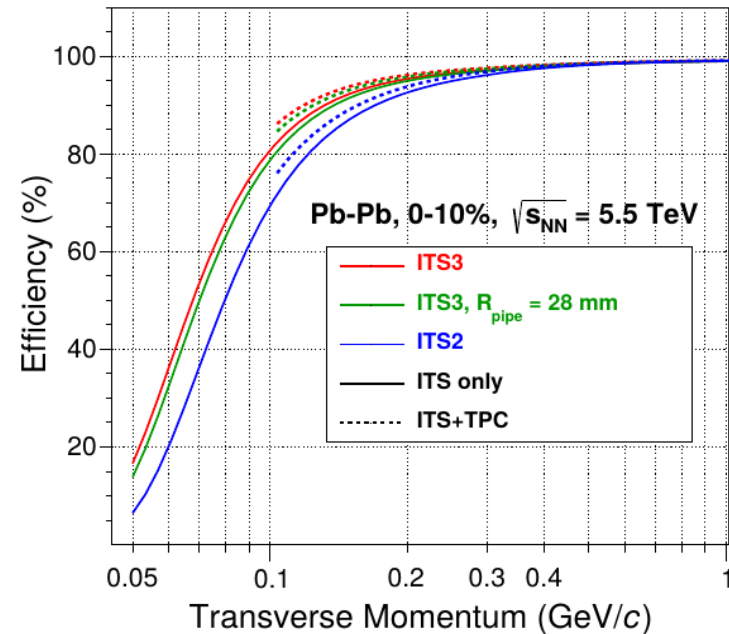
	ITS1 (2 inner)	ITS2 (3 inner)	ITS3 (3 inner)
Beam pipe inner radius/thickness	3.0 cm/0.09 cm	1.82/0.08 cm	1.6/0.05 cm
First-layer radius	3.9 cm	2.3 cm	1.8 cm
X/X° per layer	1.1 %	0.35 %	0.05%
$\eta$   coverage	> 1.4	> 1.2	> 2.0
Sensors on first layer	> 80	108	~4
Pixel size $r_\phi \times z$	$\approx 50 \times 450 \mu\text{m}^2$	$\approx 30 \times 30 \mu\text{m}^2$	$\approx 10 \times 10 \mu\text{m}^2$
Intrinsic resolution $r_\phi$	12 $\mu\text{m}$	5 $\mu\text{m}$	< 5 $\mu\text{m}$
Intrinsic resolution z	100 $\mu\text{m}$	5 $\mu\text{m}$	< 5 $\mu\text{m}$
Readout frequency Pb-Pb	A few kHz ~ 1 ms (SDD)	< 50-100 kHz > 20-10 $\mu\text{s}$	
Cooling needs in the pixel matrix	Liquid cooled	~40 mW/cm <sup>2</sup> Liquid cooled	< 20 mW/cm <sup>2</sup> Air-flow cooled

# Tracking performance of the ITS3

*EoI ITS3, ALICE-PUBLIC-2018-013*



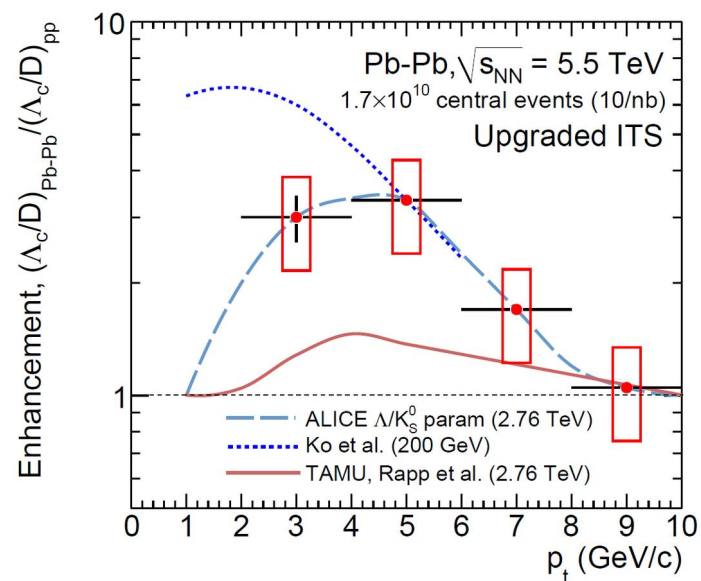
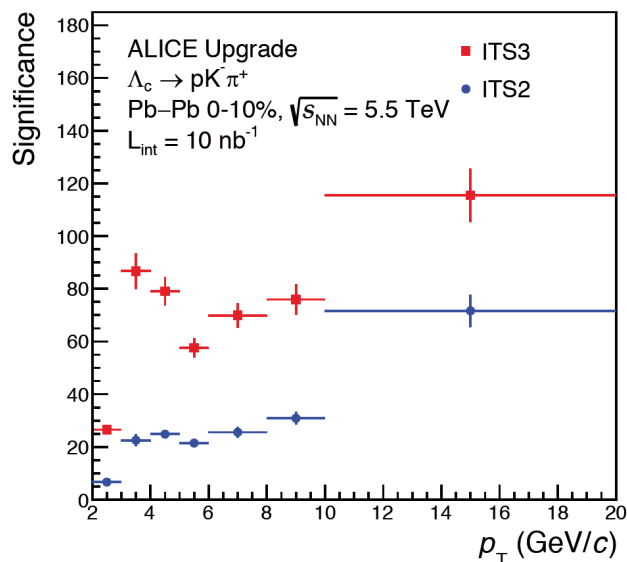
DCA resolution 2x better at all momenta



Tracking efficiency is 2x better at  $p_T \sim 60 \text{ MeV}/c$

# Charmed baryons ( $\Lambda_c$ )

EoI ITS3, ALICE-PUBLIC-2018-013



DCA resolution becomes better than the  $\tau$  of  $\Lambda_c$  !

$\Lambda_c$	Significance	S/B
ITS3 / ITS2	4	10

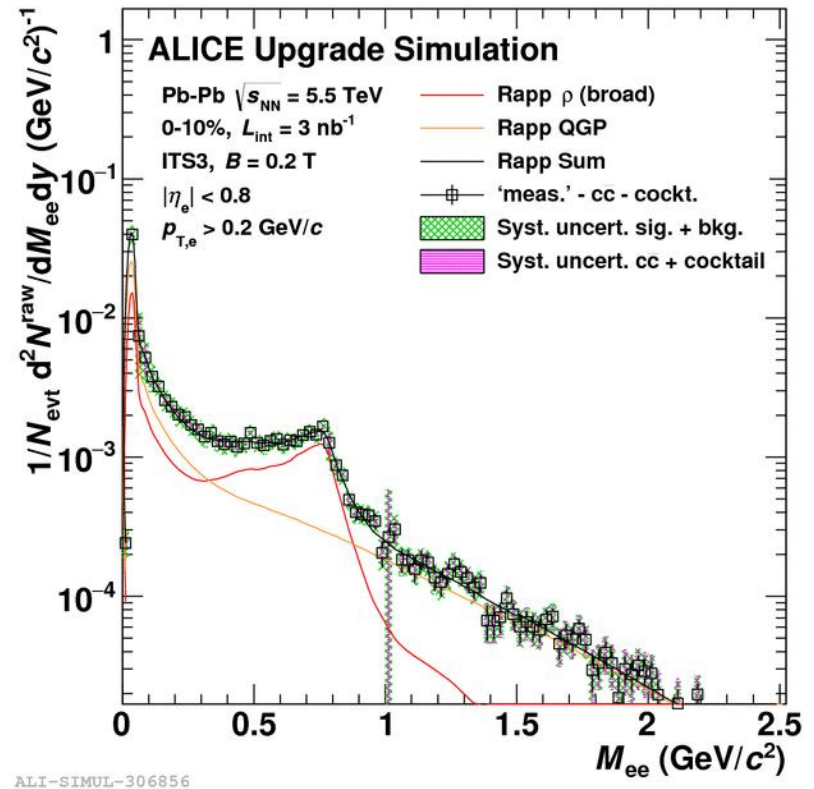
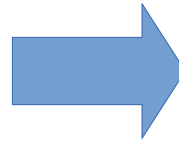
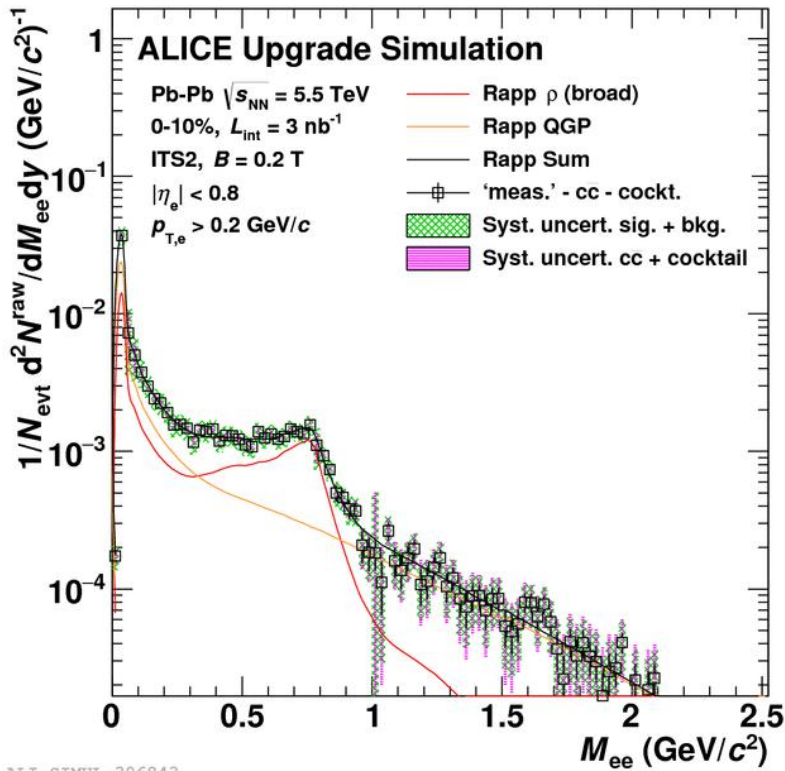


# Thermal di-electrons

EoI ITS3, ALICE-PUBLIC-2018-013

ITS2

ITS3

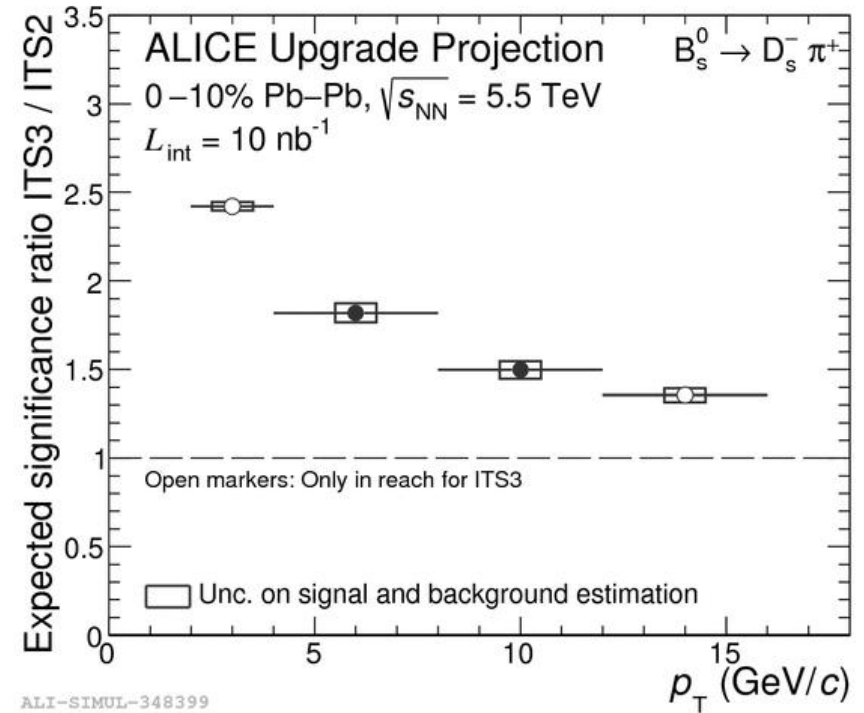
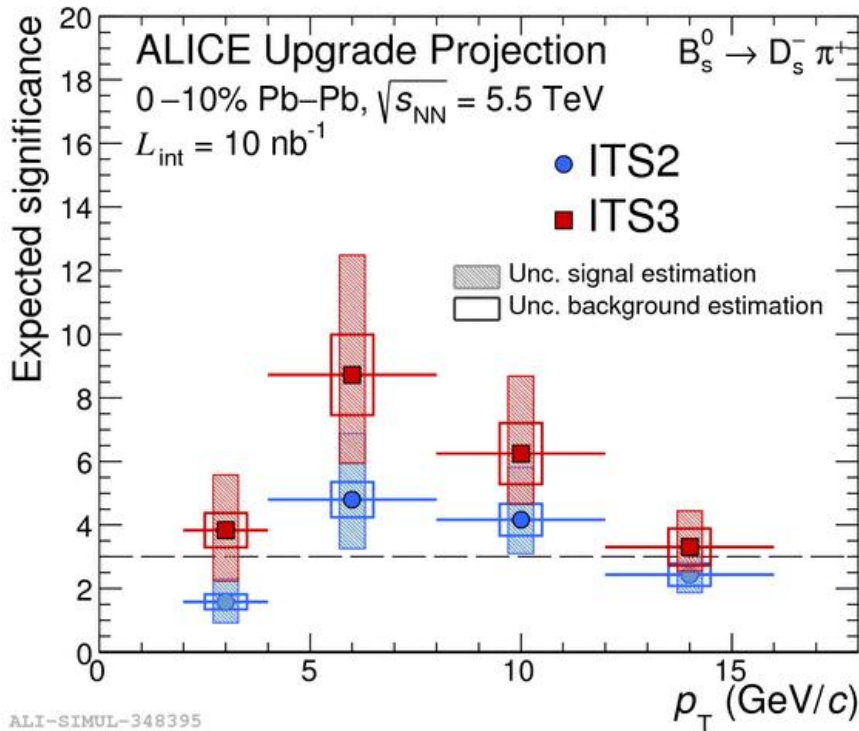


1. Much less  $\gamma$ -conversions
2. Less background from charm

T (QGP)	Stat. error	Syst. (bkg)	Syst. (charm)
ITS3 / ITS2	1/1.3	1/2	1/2

# Full topological reco of $B_s$

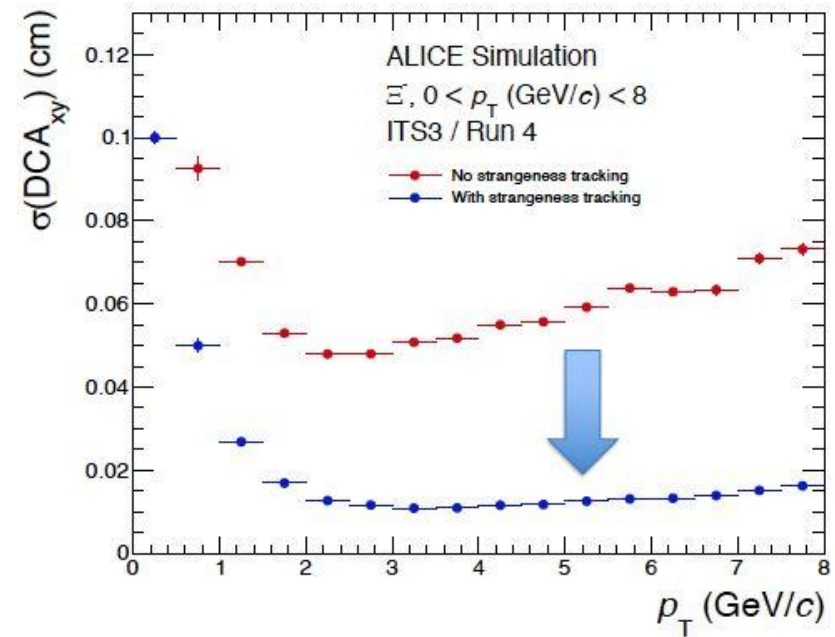
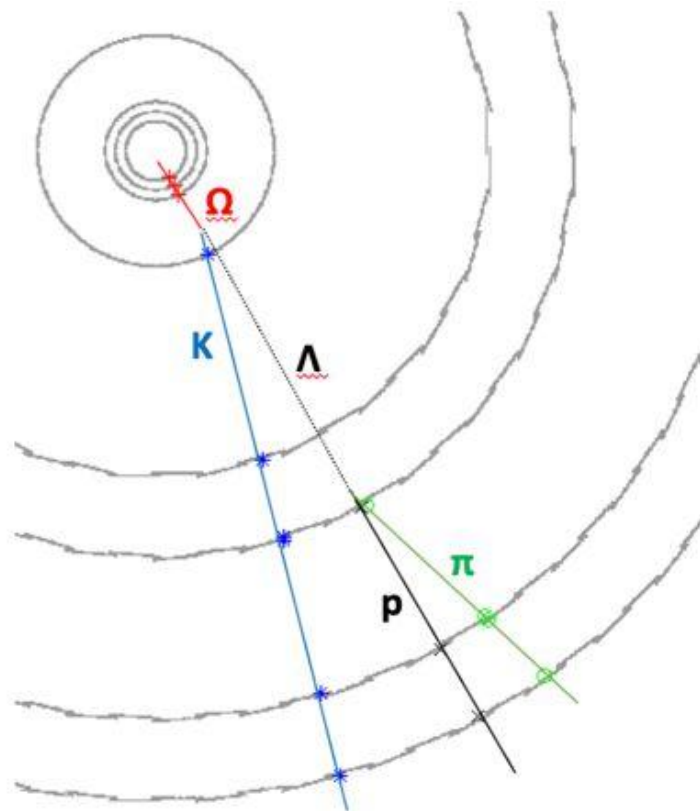
Luuk VERMUNT (Utrecht)



**Twice larger significance ! Twice larger momentum range !**

# “Strangeness tracker”

David CHINELLATO (Campinas), Alexander KALWEIT (CERN)



With the ITS3, the DCA resolution for  $\Xi$  becomes comparable with the  $c\tau$  for  $\Xi_c$  ( $\sim 130 \mu\text{m}$ )!



# Summary

- A technological feasibility of a super-light tracker (0.05% X0) thanks to
  - ◆ Wafer-scale sensors
  - ◆ Thinned down to a few 10  $\mu\text{m}$
  - ◆ ( 18 mm from the beam. Cylindrical geometry... )
  
- Opens a possibility of several measurements involving
  - ◆ Charmed baryons
  - ◆ Low-mass di-electrons
  - ◆ Multi-flavour particles via decays to strange baryons
  - ◆ Full topological reconstruction of Bs
  - ◆ c-deuteron, ...
  
- France has all needed expertise.
  - ◆ For example in Strasbourg:
    - Silicon hardware : C4Pi ( <http://www.iphc.cnrs.fr/-Plateforme-C4Pi-.html#nb1> )
    - Reconstruction and physics analysis software for strange, charm and beauty particles
  - ◆ ...
  
- A step on the way towards a full-silicon ALICE3

# ITS3: a cost estimate...

LHCC 04.06.2019 , ALICE LS3 upgrade proposal, Magnus Mager

R&D 2020-2023	Cost breakdown		
→ Wafer thinning+bending			
→ 2019: contact to industry			
→ 2019-2020: first prototypes with ALPIDE chips and wafers			
→ later: continue with specific prototypes			
→ Stitched sensor development			
→ 2019-2020: technology test structures			
→ 2020-2022: prototyping chips			
→ 2022-2023: full-scale prototype + final chip			
Technical Design Report 2022			
Construction 2024-2025			
	NB: ~40% is R&D		

Item	R&D (kCHF)	Construction (kCHF)	Total Cost (kCHF)
Total	2000	3300	5300
Beampipe	600	900	1500
Pixel CMOS Sensors	700	700	1400
Sensor test	100	150	250
Thinning & dicing	200	300	500
Hybrid printed circuit	100	100	200
Mechanics	150	350	500
Assembly & test	50	200	250
Installation tooling	0	200	200
Air cooling	100	150	250
Services	0	100	100
Patch panels	0	150	150



# LHC schedule ...

