Preliminary Results of Spatial Resolution Performances of Capacitive Sharing Large Pad Readout in Test Beam

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Outline

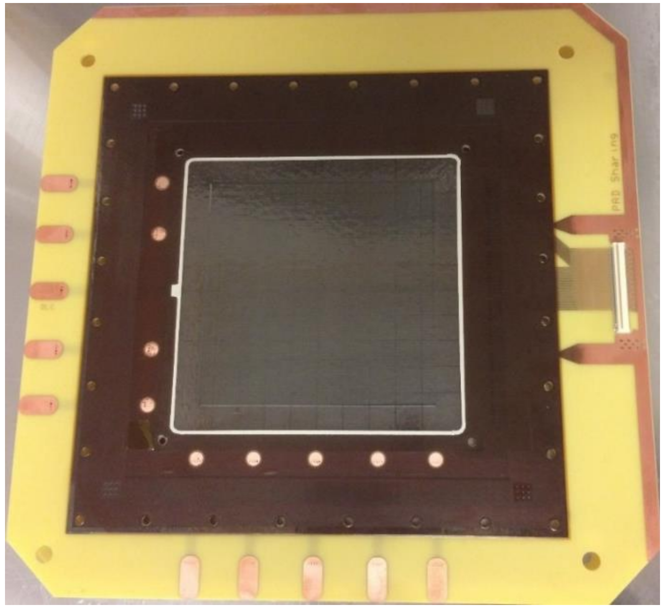
- Principe of Capacitive-Sharing Large-Pads Readout PCB
- Potential Applications for EIC MPGD-based Tracking & PID Detector Options
- First Prototype & Preliminary Test Beam Results
- Further R&D on Large-Pads Capacitive Readout

Principe of Large Pads with Capacitive Sharing readout PCB

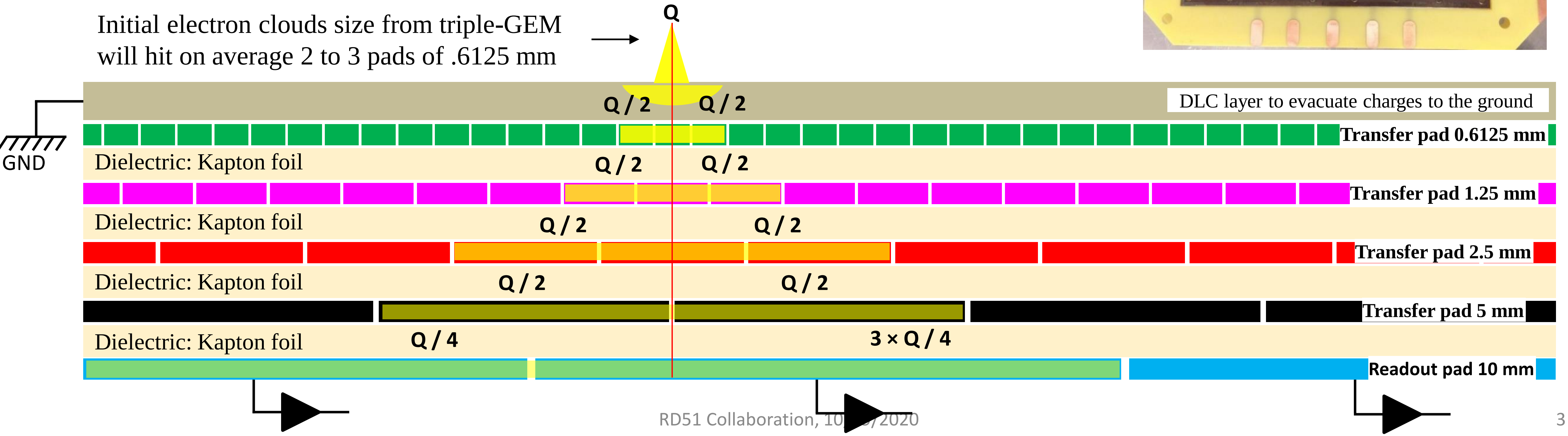
Principle of capacitive-sharing large-pad Readout

- Vertical stack of pads layers ⇨ Transfer of initial charge from MPGD by **capacitive coupling**
- Space arrangement of the pads and doubling pad size from one layer to the one below allow:
  - ⇨ Preservation of the spatial resolution (Goal ⇨100 μm for 1 cm^2 pad readout)
  - ⇨ significant reduction of number of electronic channels to be read out
- Low cost and flexible readout technology
  - ⇨ Suitable to a variety of applications related to EIC detector R&D programs

large-pad readout prototype @ UVa



Initial electron clouds size from triple-GEM will hit on average 2 to 3 pads of .6125 mm

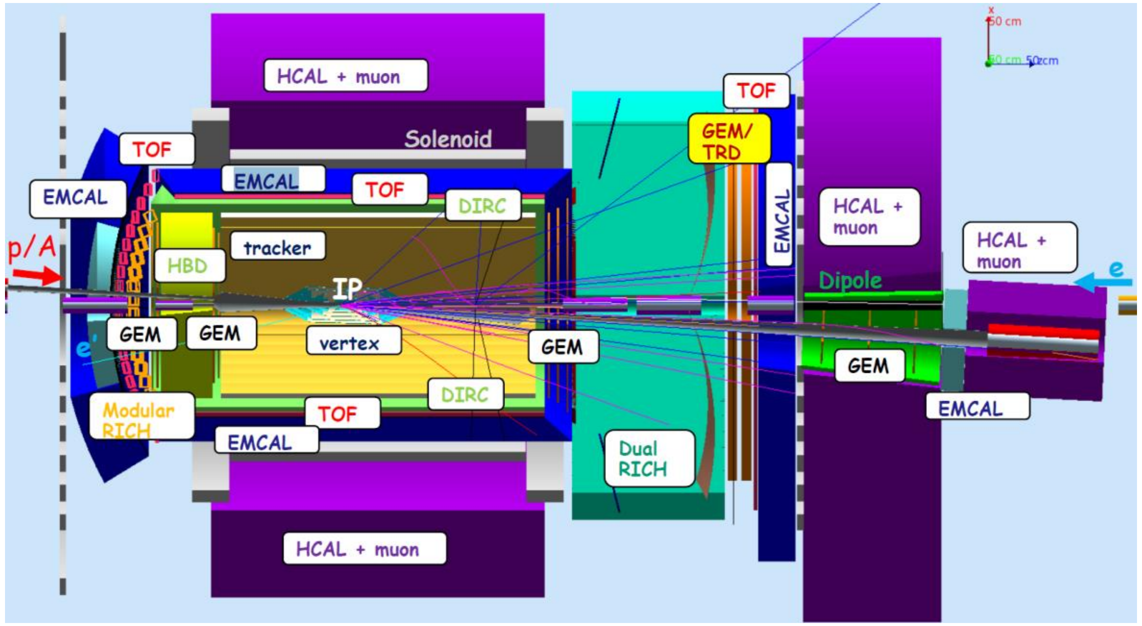


Potential Applications for EIC MPGD-based Tracking & PID Detector Options

Several MPGD technologies under consideration for EIC tracking and PID

- **Tracking detectors options with MPGDs**
  - ⇨ TPC for central tracking with GEM or hybrid MPGDs readout planes
  - ⇨ Multilayer Cylindrical MPGDs for the EIC barrel tracker
  - ⇨ Planar MPGD disc layers in both electron and hadron end caps
- **PID options with MPGDs**
  - ⇨ Hybrid THGEMs & Micromegas for high momentum RICH in hadron end cap
  - ⇨ Short length GEM-RICH for high momentum RICH in hadron end cap
  - ⇨ GEM-TRD (Transition Radiation Detector) ⇨ both end caps

EIC Detector Concept (JLEIC) Design



Why is large pads with capacitive sharing readout is an option for all MPGD technologies and applications cited above:

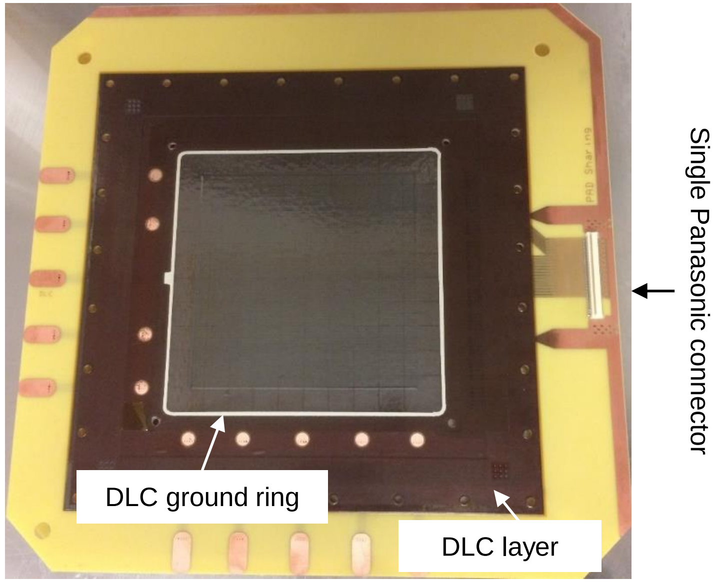
- Relatively low particle flux rate expected at the EIC tracking detectors in all eta regions (compared to LHC or fixed target experiment at JLab)
  - ⇨ Don't have to worry about pile-up and multiple hit events for trackers
- Flexibility of the readout concept: One can design the large-pad readout PCB parameters to address specific detector technology and application
  - ⇨ i.e. pad size for the top and / or bottom pad layers, numbers of layers, pad geometry and thickness … can be detector specific
- The large pads with capacitive sharing readout technique is pretty straight forward: don't anticipate an extensive R&D program to fully validate the concept
  - ⇨ Cost effective solution with low production risk

GEM prototype with Capacitive Sharing 1 cm × 1 cm Pad Readout

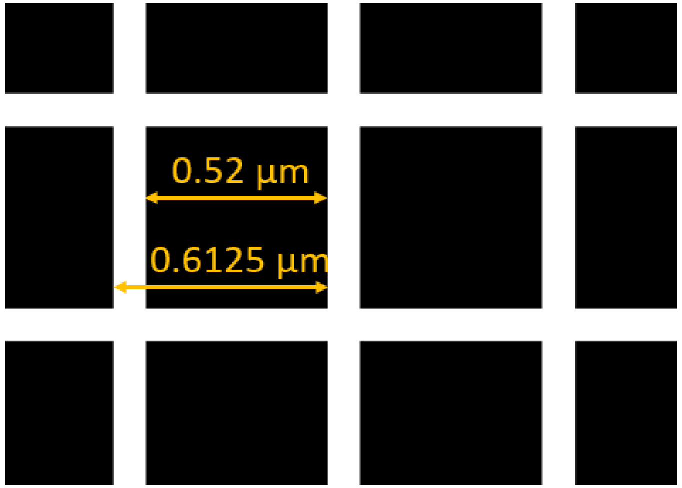
5-layers capacitive-sharing pad readout prototype:

- **Top pad layer** (define basic resolution performances):
  - Pitch: 0.6125 mm × 0.6125 mm (**0.1 mm inter-pad)**
  - Pad size: 0.52 mm × 0.52 mm
- **Bottom pad layer** (readout pad):
  - Pitch: 10 mm × 10 mm (**0.1 mm inter-pad)**
  - Pad size: 9.9 mm × 9.9 mm
- DLC layer with surface resistivity 10 - 20 MΩ
- 100 readout Pads

Bottom Layer: 1 cm × 1 cm pads

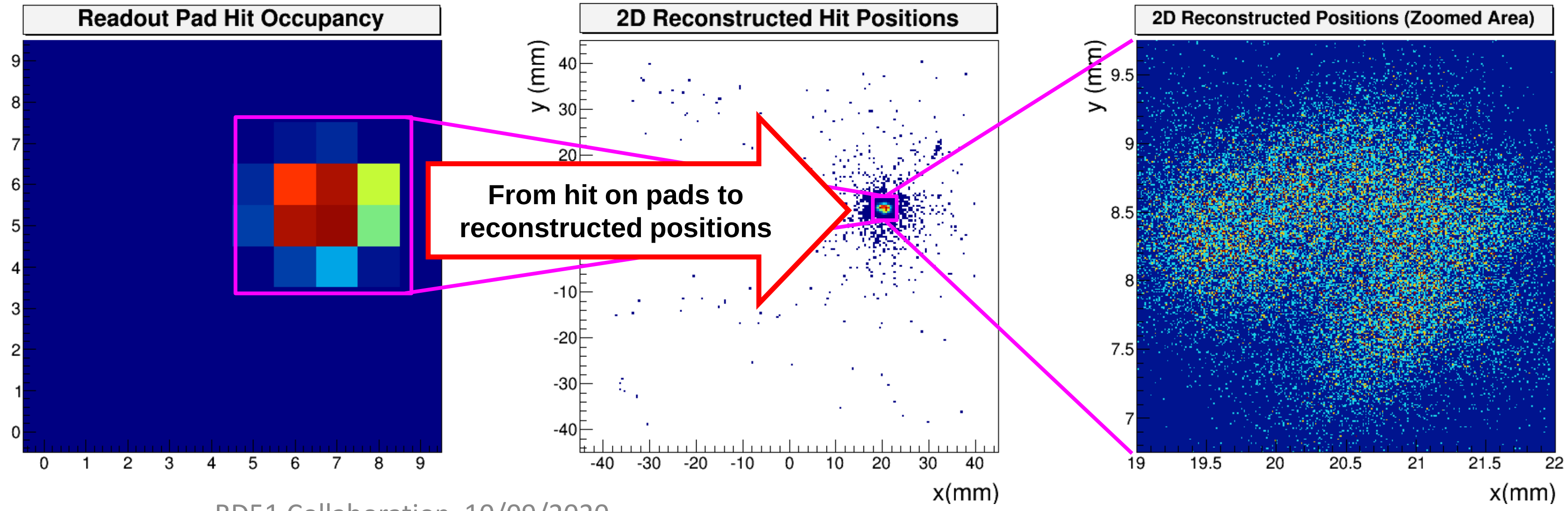


Top Layer : Pad pitch = 0.6125 μm × 1 0.6125 μm



GEM prototype with capacitive-sharing pad in x-ray

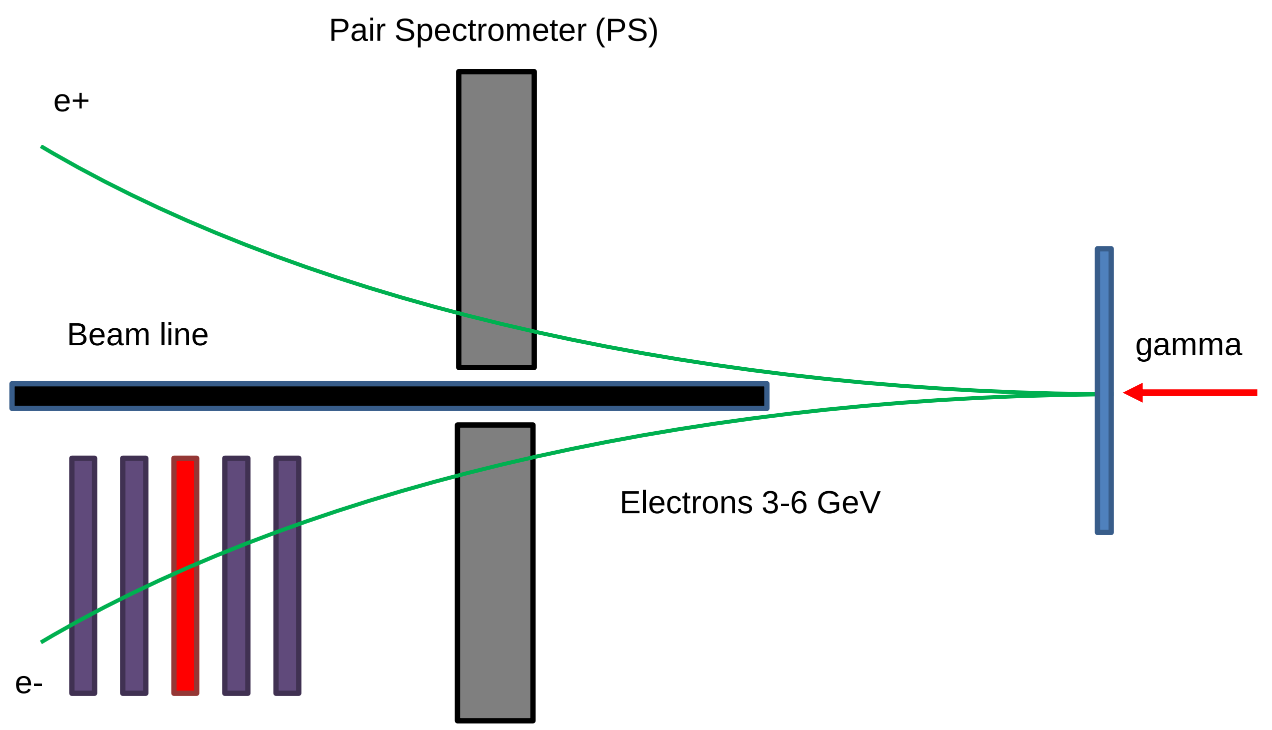
Pad Occupancy & 2D hit reconstruction with x-ray



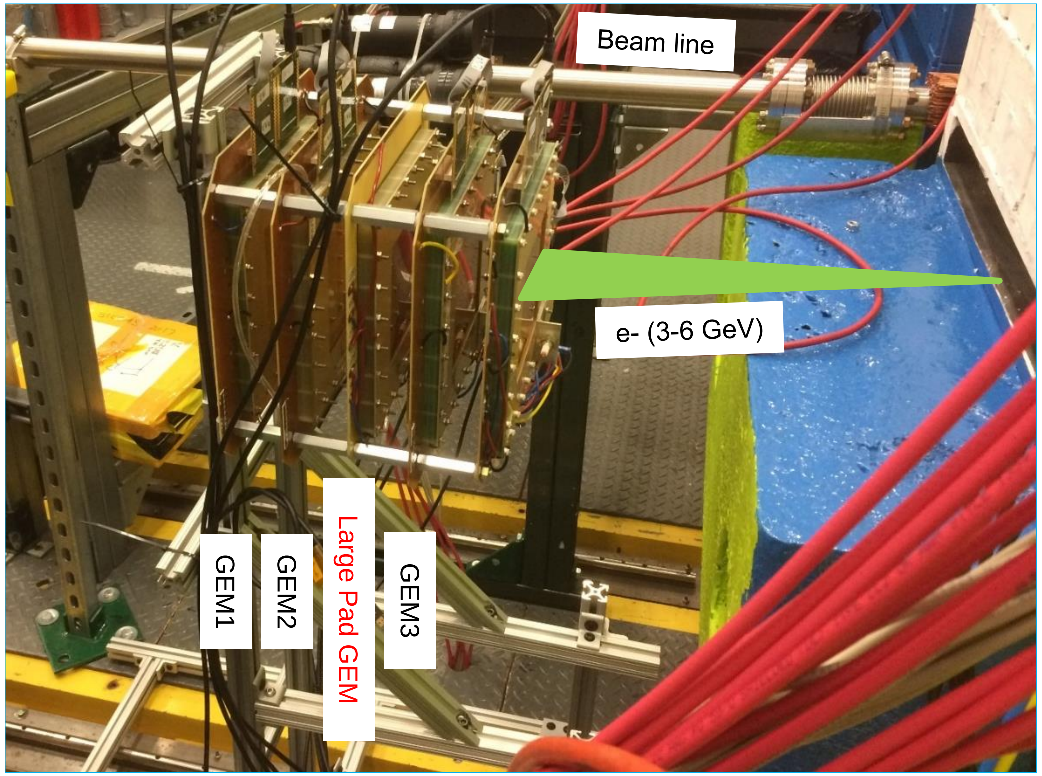
Test Beam in Hall D @ JLab

Parasitic setup in the electron arm of Hall D Pair Spectrometer (PS) @ JLab.

- ❑ Clean electron beam (3 to 6 GeV), incoming angle up to 8 degree
- ❑ Large Pad GEM + 3 small X-Y CERN standard triple-GEM for tracking
- ❑ APV25-SRS readout (DATE + AmoreSRS), trigger rate limited to 400Hz
- ❑ Large volume of data for HV scan and for spatial resolution - Mid-September 2020



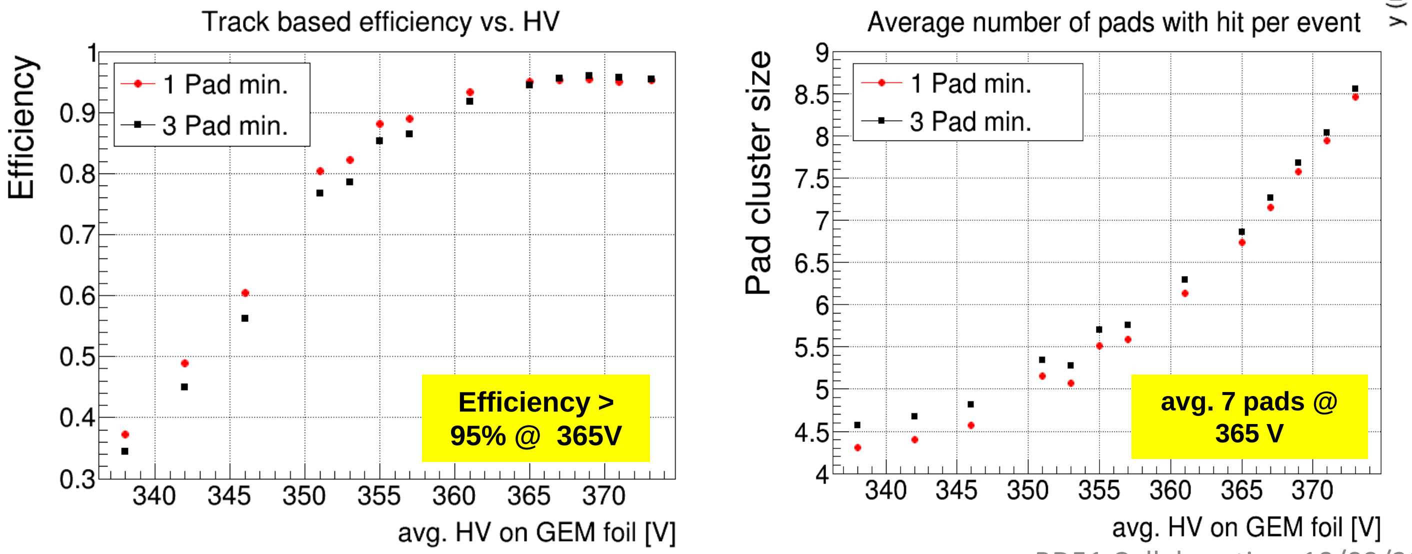
Large Pad GEM Telescope



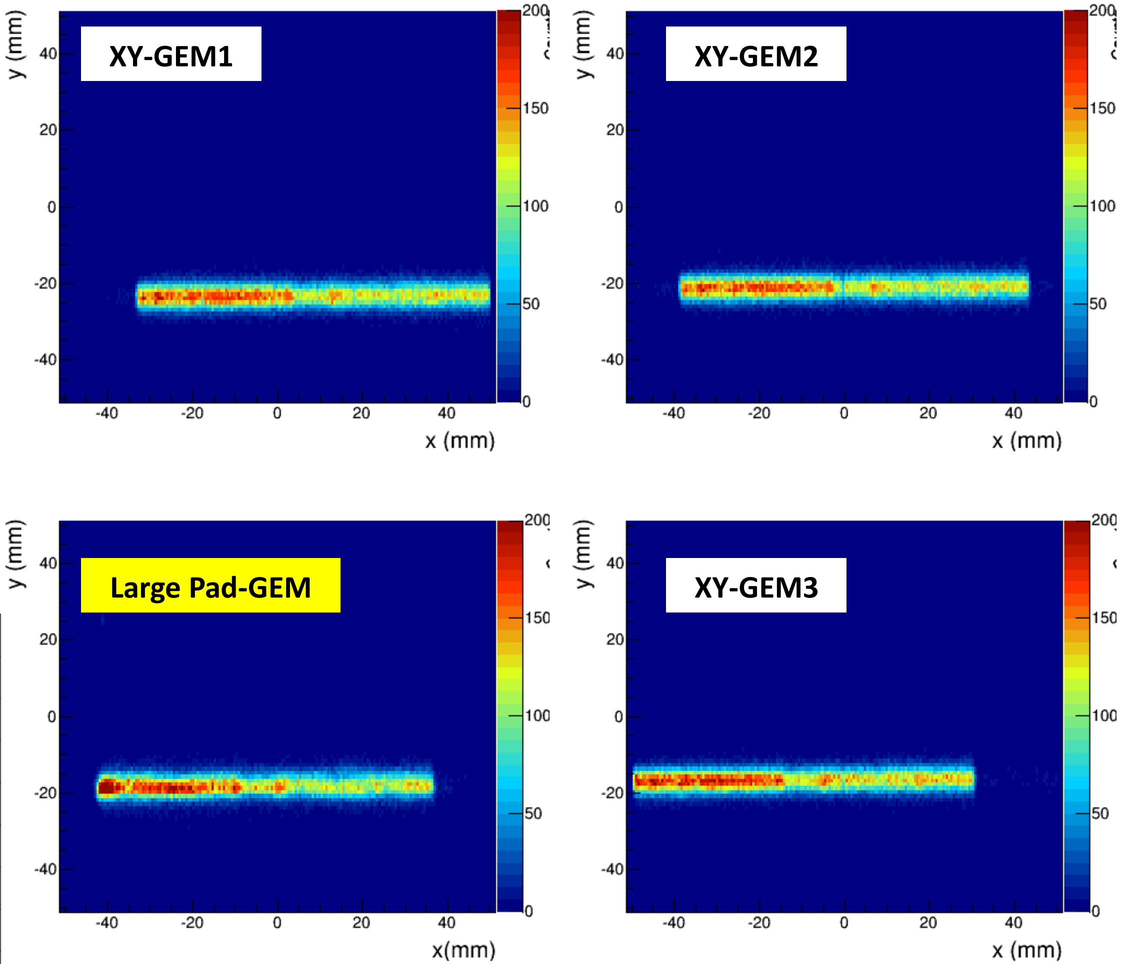
Preliminary Results with JLab Test Beam Data

Large Pad GEM detector performances:

- HV scan from with 340 V to 375V to GEM foils
  - 372V is the average voltage on GEM foil for a COMPASS GEM @ 4100 V
  - Track based efficiency using 2 XY trackers as reference
- Full efficiency above 365V
  - **1 Pad min.:** all pads above 2σ pedestal cut considered in analysis
  - **3 Pad min.:** We only consider event with at least 3 pads above 2σ pedestal cut
    - At full efficiency, at least 3 pads record hit above pedestal for all events
- Average number of pads above 2σ pedestal cut
  - > 7 pads on average with hit at a GEM voltage > 365V



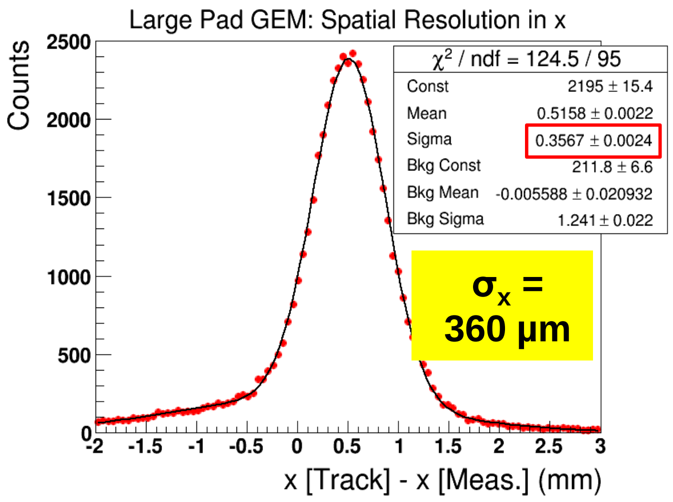
2D hit map of the reconstructed electron beam profile

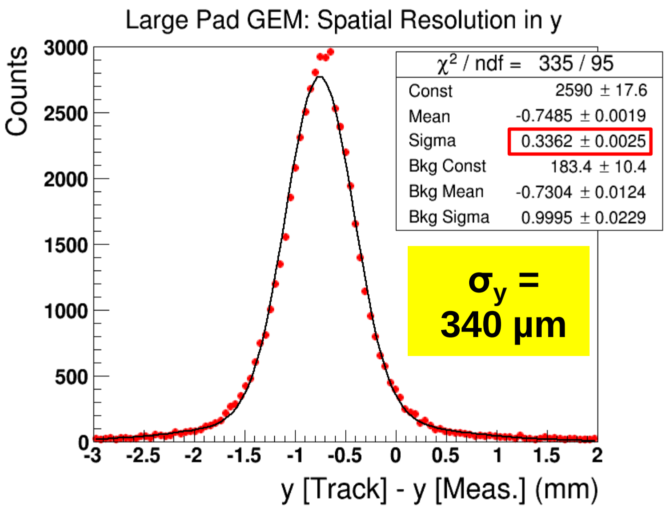


Preliminary Results with JLab Test Beam Data

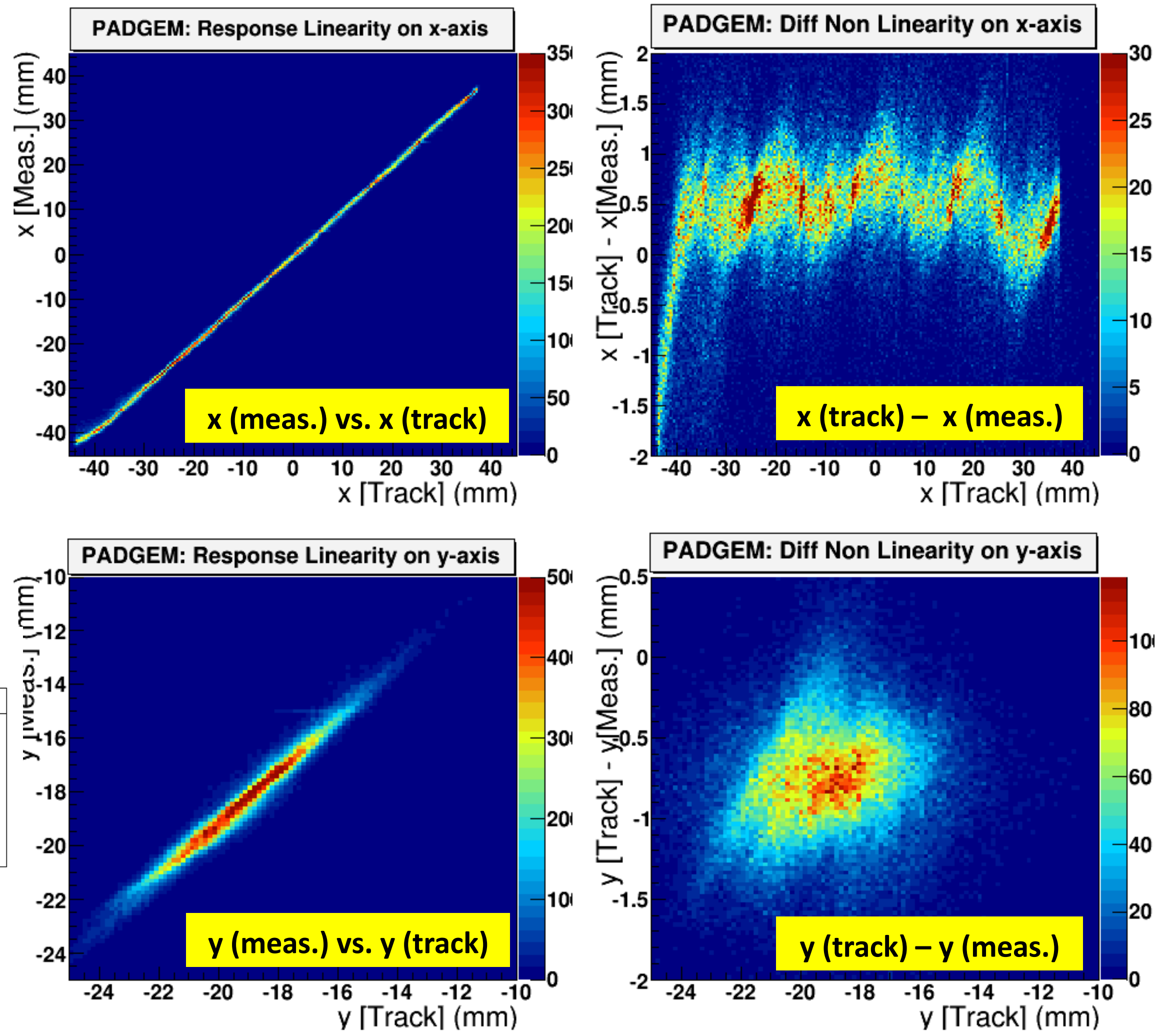
Spatial resolution studies:

- Very preliminary analysis:
  - Track was based on straight line from only 2 XY trackers (GEM1 & GEM3
  - No alignment and offset correction performed yet
- Good response linearity of the chamber
  - Strong correlation between expected and measured positions
  - Non linearity pattern (DNL): could be parametrized as correction to the position
- Extracted resolution from residual width **~ 350 um** in both x and y direction
  - This is before any correction from alignment and track fit error
- Analysis is still on going and we expect some improvement of resolution performances
  - First results are very encouraging and provide clear direction on where the improvement is going to come from





Pad GEM: Response linearity



How to achieve the goal of 100 μm resolution with 1 cm × 1cm pad R/O?

4 areas where we see room for improvement of the spatial resolution performance

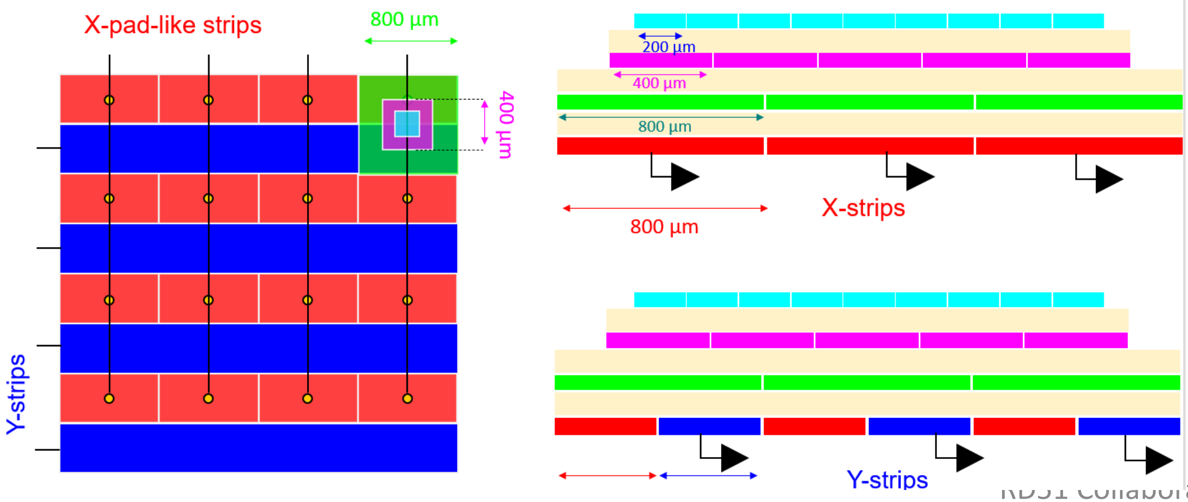
1. **Minimize the inter-pad gap between pads**
   - This is even more crucial for first pad layers where the pad size is small
   - In our prototype the ratio pad size / pitch for the first pad layer is 17% ⇨ meaning 17 % of charges are not collected but most importantly, this affect the charge sharing between adjacent pads
   - When this propagate through 5 layers, the charge sharing distortion becomes significant
   - We plan to study the effect of inter pad gap on the resolution with a prototype with 4 different gap from 100 um to 40 um
2. **Optimization of the min pad size:**
   - With this concept of capacitive charge sharing, the parameters of the top pad layers are crucial for the resolution performances of the R/O
   - We plan to study the impact of different top layer pad size on the spatial resolution
3. **Minimization of the noise:**
   - Large pads = large capacitance noise to input of the FE pre amplifier. There are ideas to minimize the pad size of the readout layer while maintaining large pitch i.e. low channel count
   - Also one need to optimize the traces to minimize their contribution to cross talk and noise
   - We plan to study the impact of different top layer pad size on the spatial resolution
4. **Offline correction for the non linearity response**
   - This is the next step of our analysis we expect big improvement (with maybe a factor 2) with the current not optimized prototype

Extend the capacitive-sharing concept to 2D (and 4D XY-UV) R/O

Capacitive sharing with strip R/O

- ❑ **More interesting approach for large area detector**
  - ❑ even less channel count and less pad layers to achieve high spatial resolution
  - ❑ Pad size of top layer to be adjusted to the type of MPGD amplification i.e. smaller pad (e.g.200 µm) for uRWELL/micromegas, larger pad for GEM (e.g 400 µm)
  - ❑ Strip / pad-like strip R/O to ensure equal sharing and very good X/Y charge correlation
- ❑ **Idea to expand this idea to a XY-UV readout boad**
  - ❑ Concept explored by D. Majka @ Yale U. with an XYU R/O to help solve **multiple hit ambigiuty**
  - ❑ They reach 100 um resolution with 800µm pitch
  - ❑ With capacitive charge sharing, pitch can be increased by 2 or 4, with 4 coordinate capabilities XY-UV capability
  - ❑ This is also a solution for lare area detector where multiple hit ambiguity is a concern

Capacitive-Sharing Large-Strip Readout: Low channel count X-Y strip readout



High Performances 3D - coordinates strips Readout:
D. Majka, Yale U.

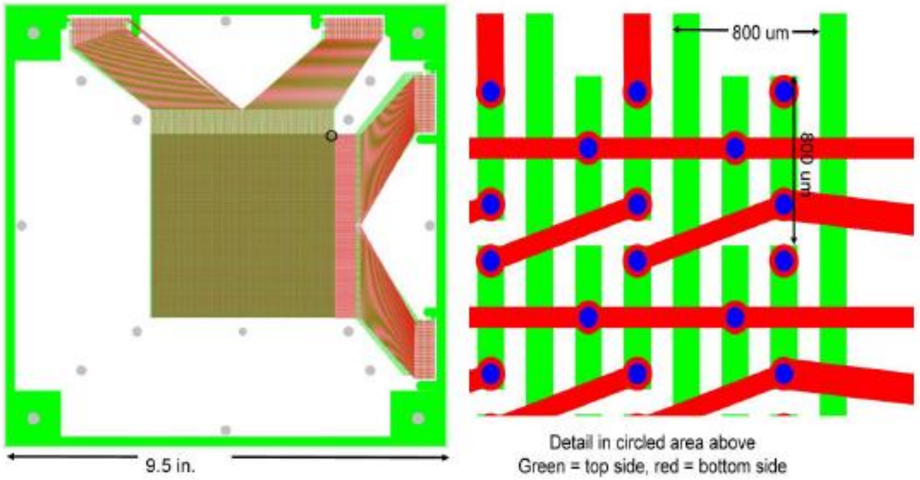
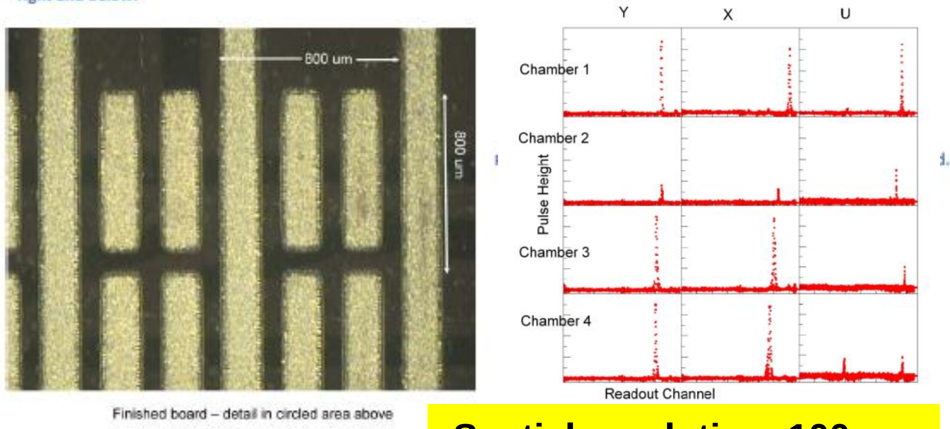


Figure 23: Layout of prototype 800 µm pitch 3 coordinate readout board. Detail for circled area at upper right is shown at right and below.



Spatial resolution: 100 µm

https://wiki.bnl.gov/conferences/images/7/76/RD6-December-2013_Dehmelt-Hemmick.pdf

Summary & To Do Next

Preliminary results on spatial resolution performance of 1 cm x 1cm pad readout with capacitive sharing very encouraging

- Reach 350 µm resolution with he first prototype before tracking error and offset and DNL corrections
- There is plenty room for improvement being implemented in the next generation of prototypes: Goal is to achieve a spatial resolution of 100 µm

Some challenges specific to the capacitive charge sharing concept

- Minimizing the material thickness of such RO: Adding these layers considerably increases the thickness of the detector
    - Exploring the idea with Chromium pads to considerably reduce the overall thickness.
- Need to minimizing the capacitance noise of the large size pads: In first order, spatial resolution not limited by the readout layer pad size
    - However large pad ⇨ large capacitance noise that will degrades signal to noise and therefore the spatial resolution performance

The concept of capacitive charge sharing can be applied to a variety of readout pattern for MPGDs

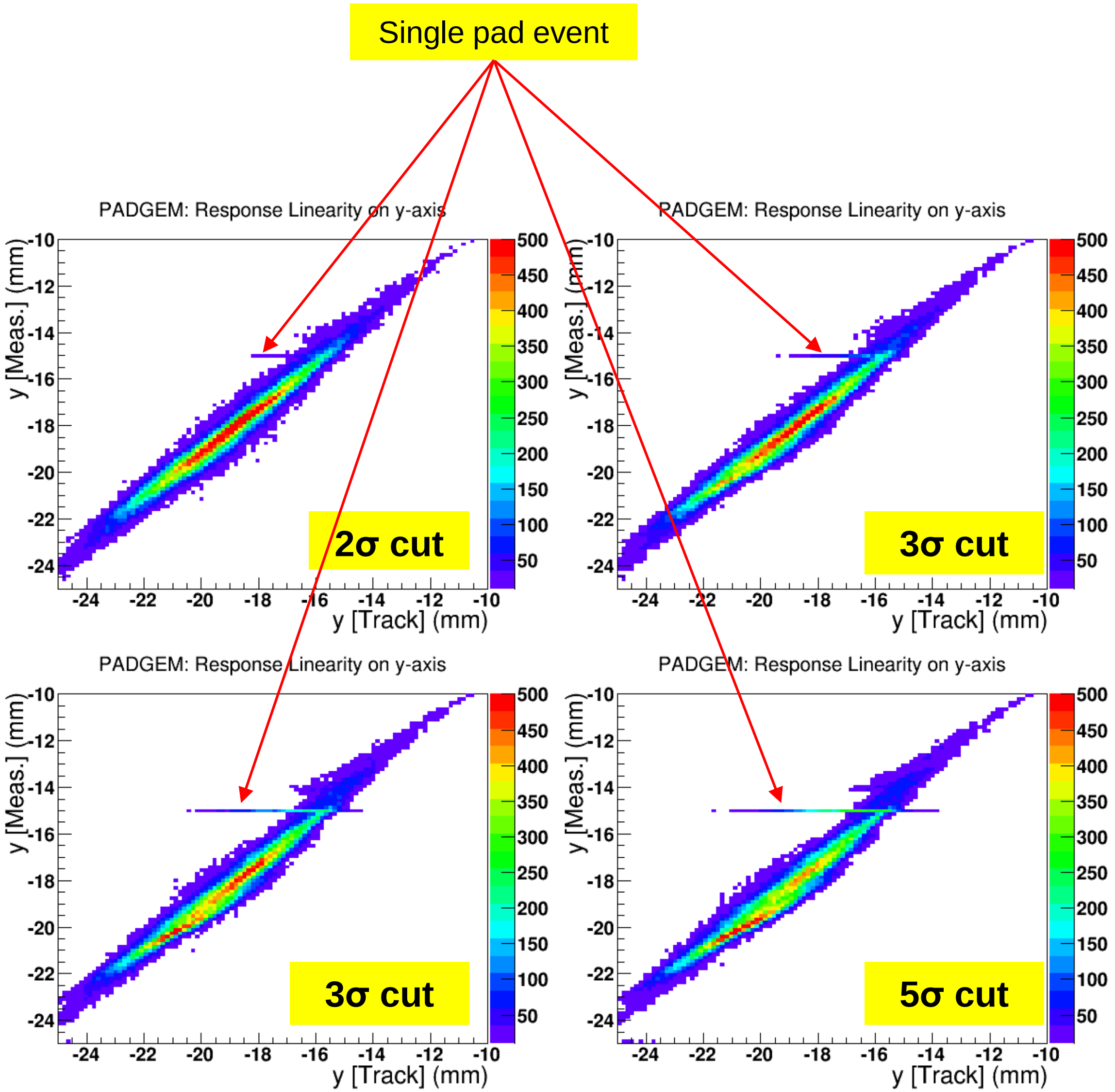
- This can be applied to 2D (and 4-coordinates) strip readout for large areas detector, XY-UV strips readout can help with multiple hit ambiguity
- This concept is flexible enough to be used for pad R/O for small chambers,

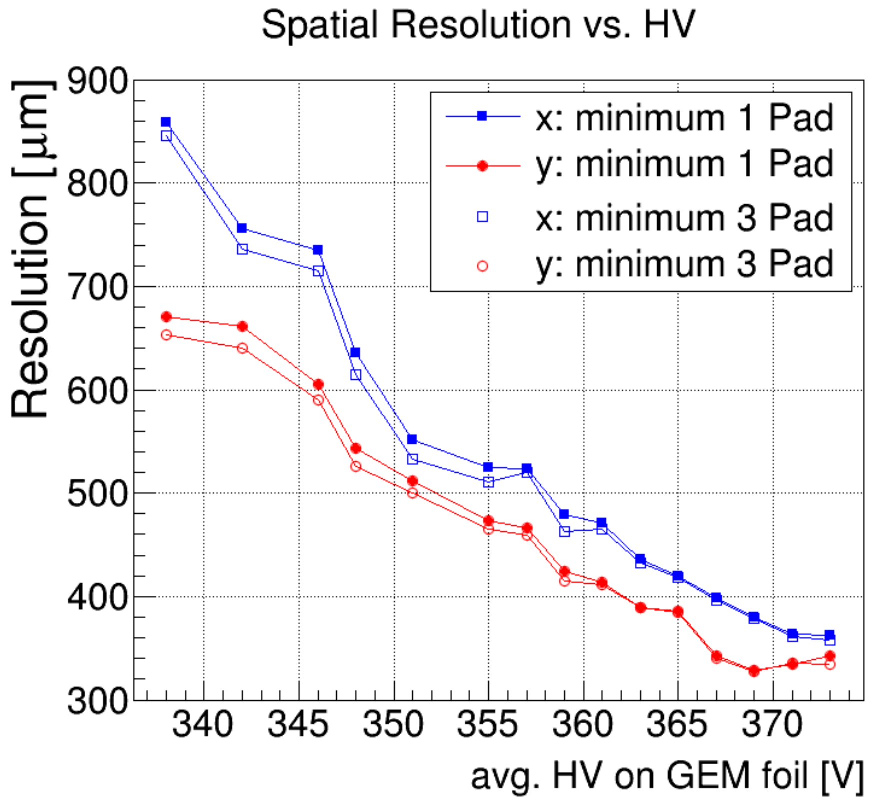
Some obvious applications in our field of Tracking detector R&D

- Applying the same idea charge sharing through capacitive coupling to other type of readout geometry
- This concept will work perfectly well in moderate rate environment like for EIC tracking system

BACKUP

Preliminary Results with JLab Test Beam Data





Preliminary Results with JLab Test Beam Data

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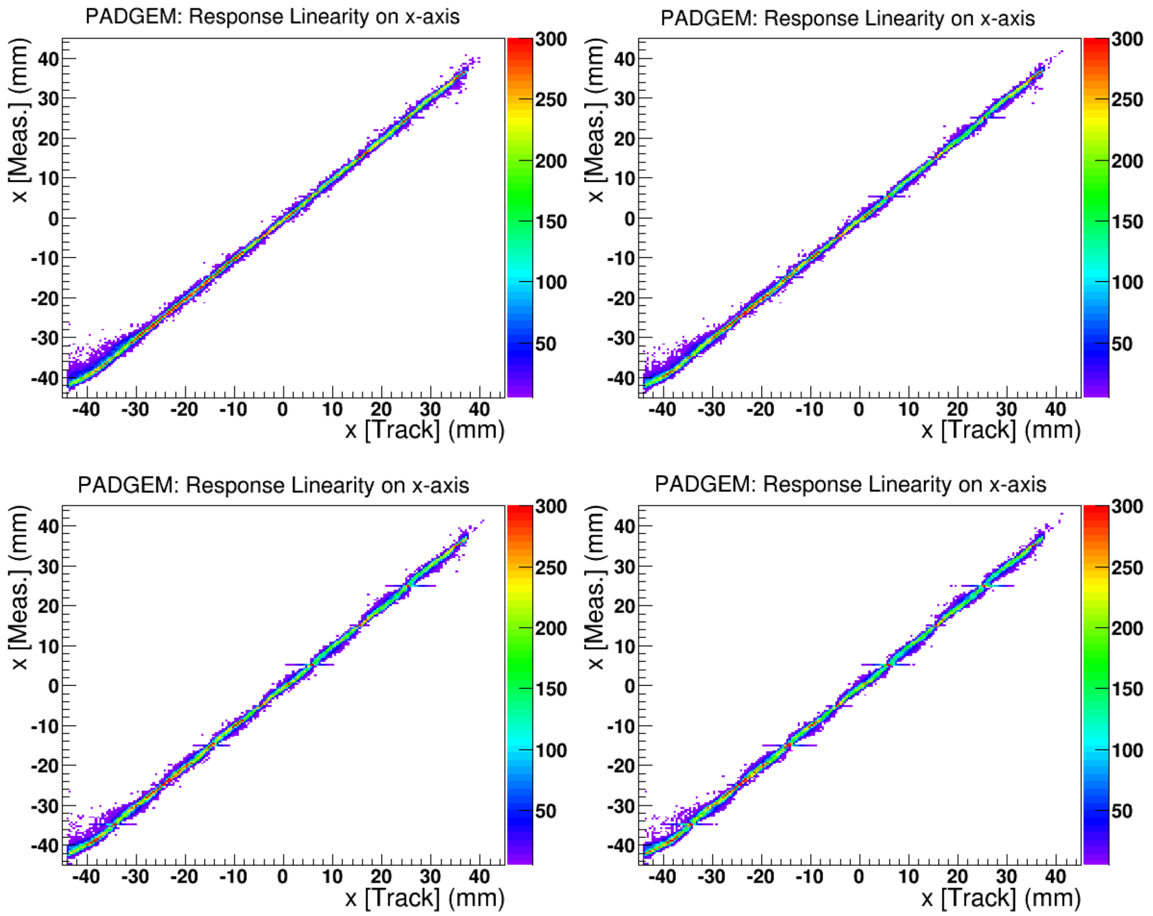
- ❑ APV25-SRS readout (DATE + AmoreSRS), trigger rate limited to 400Hz
- ❑ Large volume of data for HV scan and for spatial resolution studies

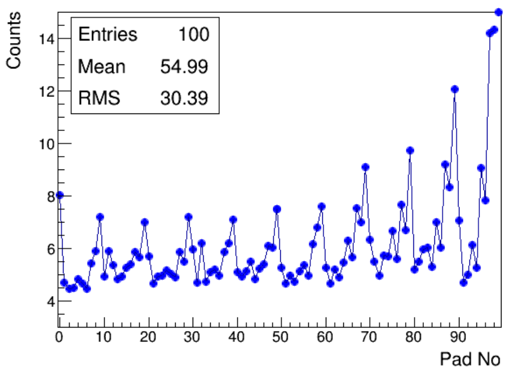


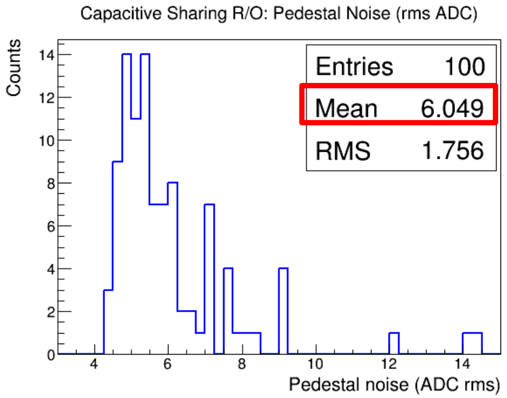
First Prototype Tested at UVa & Preliminary Results

Impact of the pad size on the pedestal noise

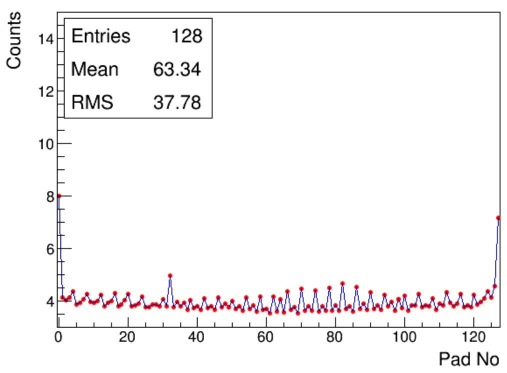
- We compare noise ofAPV2 connected to the pad board with typical noise performance of COMPASS 400 µm X-Y strips
- Bottom strip of COMPASS readout is 340 µm wide so the strip area is 0.34 cm^2 so the area of the pad is 3 times bigger
- But the average noise of the capacitive-sharing large-pad is just 1.5 times higher

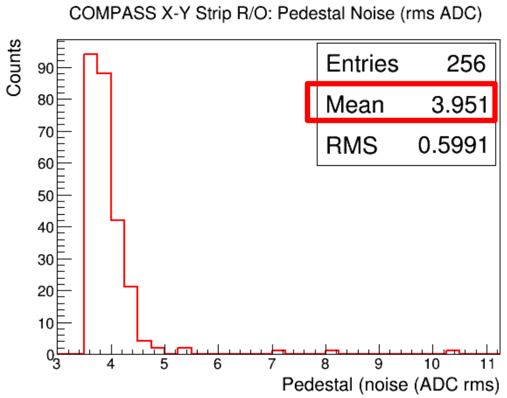
1 cm^2 pad readout

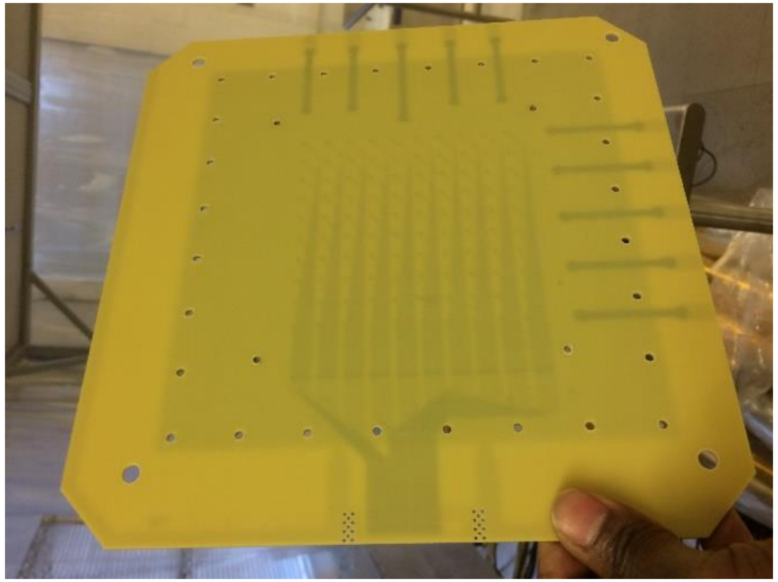




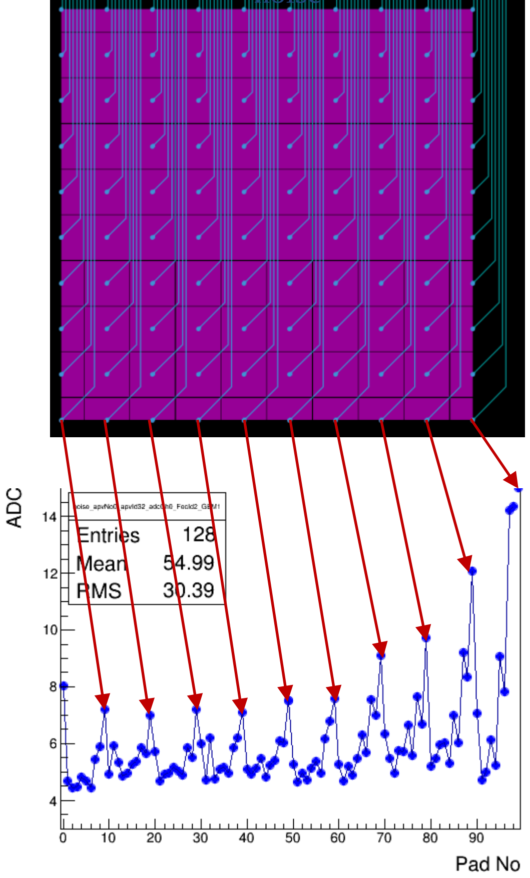
0.34 cm^2 COMPASS strip







Contribution of the traces to the noise



- The traces connecting the pad to the FE boards has a significant contribution to the noise
  - ⇨ Clear correlation between the pic and the length of the traces
- For this prototype, the traces are 200 µm wide
- Obvious improvement for next prototype: reduce the width to 50 µm
- Reduce the length as much as possible and keep a relative equal length between traces

Principe of Large Pads with Capacitive Sharing readout PCB

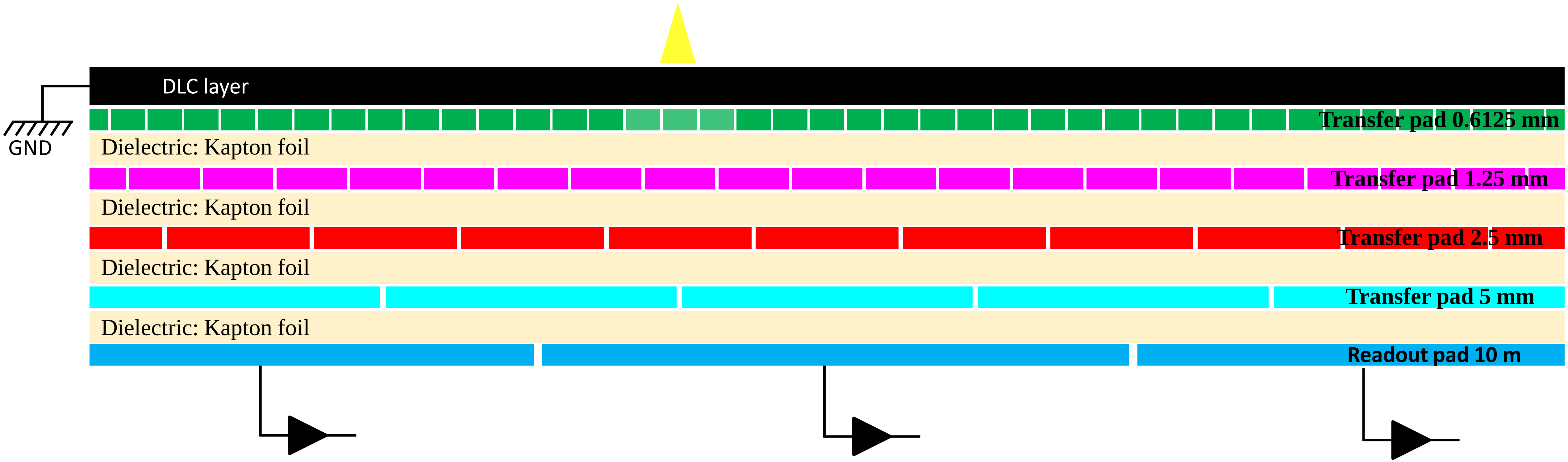
- The PCB is a vertical stack 50 µm Kapton foils with 5 µm (or less) Cu pads on top ⇨ The pad size doubles from a layer to the one underneath
- pad of layer[i] is arranged so that its center is either aligned with the center of a pad or to the boundary between 2 adjacent pads of layer[i+1].
- This pad arrangement ensured that the charges collected on 2 adjacent pads on layer[i] are always transferred to 2 adjacent pads of layer[i+1]

  ⇨ **Regardless of the pad size, at least 2 pads will always share the charges from charge cloud from the upper layer**
- The charges are transferred from one layer to the layer underneath through capacitive coupling
- The pads of the bottom layer (readout layer), are the only one connected to FE readout cards to rea he signal out
- All other layers with floating pads are transfer layers that only participates in charge spreading through the capacitive coupling
- Spatial resolution is de facto imposed in first order by the pad size of the top layer, no matter the pad size of the bottom layer (readout layer)
- The number of FE readout channels is imposed by the pad size of the bottom layer, no matter the required spatial resolution

  ⇨ **High spatial resolution achievable with reduced number of readout channels ⇨** 10 cm × 10 cm triple-GEM with 1 cm × 1 cm pad readout requires only 100 pads instead of 512 strips with the COMPASS readout to achieve similar spatial resolution performance level

  ⇨ **High flexibility** with his type of readout ⇨spatial resolution does not depend on the readout pad size
- DLC on top of the first pad layer is mostly to evacuated the charges from the amplification but also contribute to the initial charge spread

Principe of Large Pads with Capacitive Sharing readout PCB



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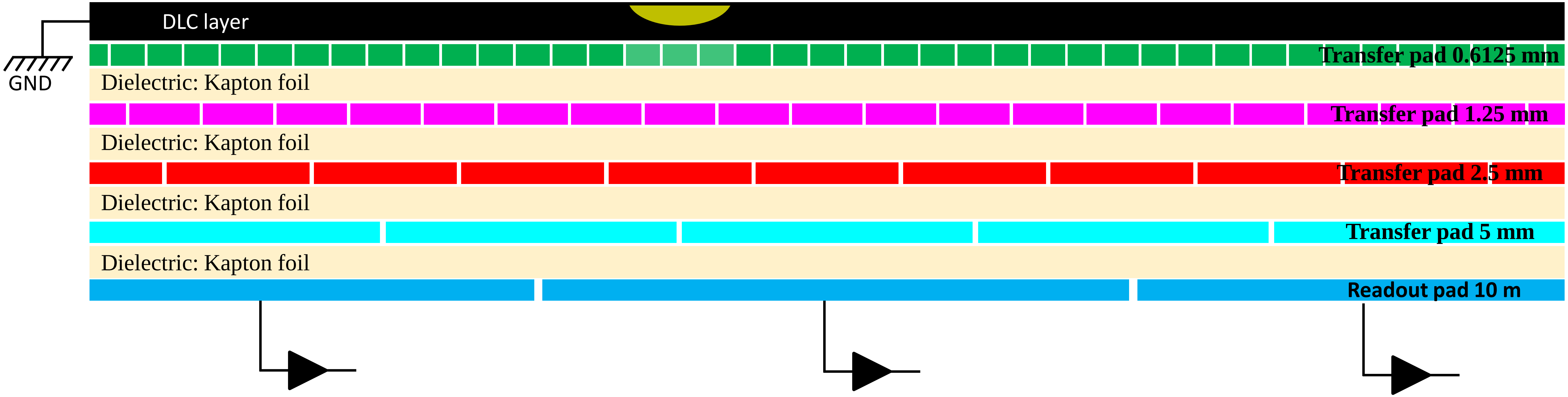

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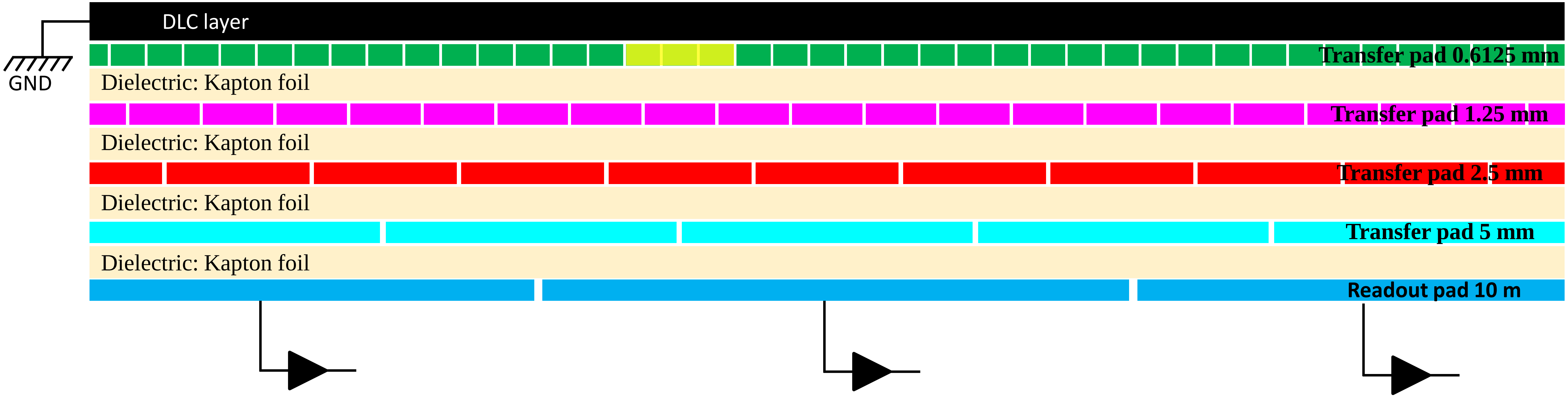

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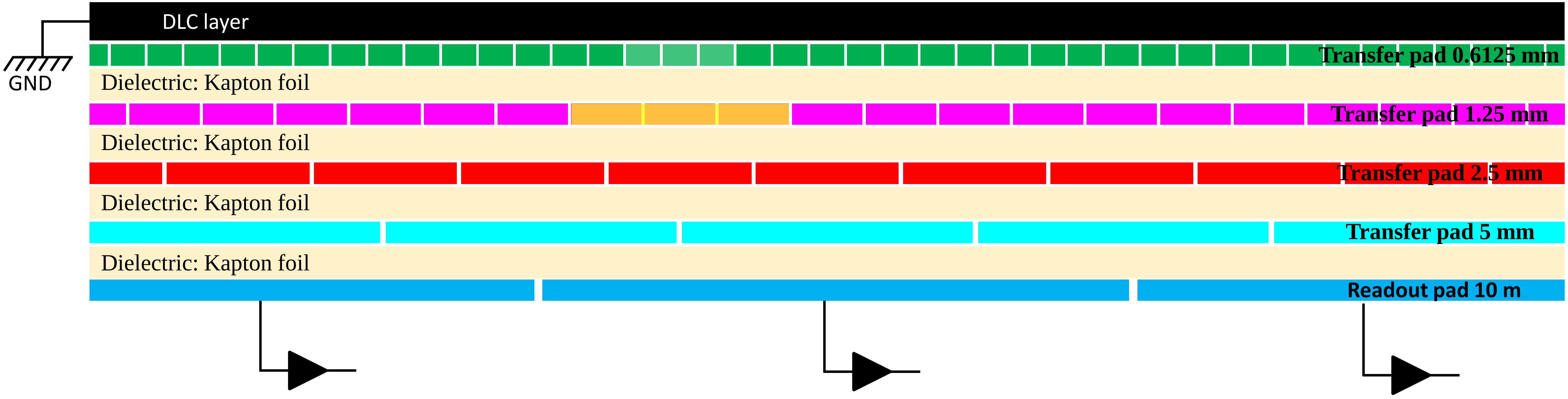

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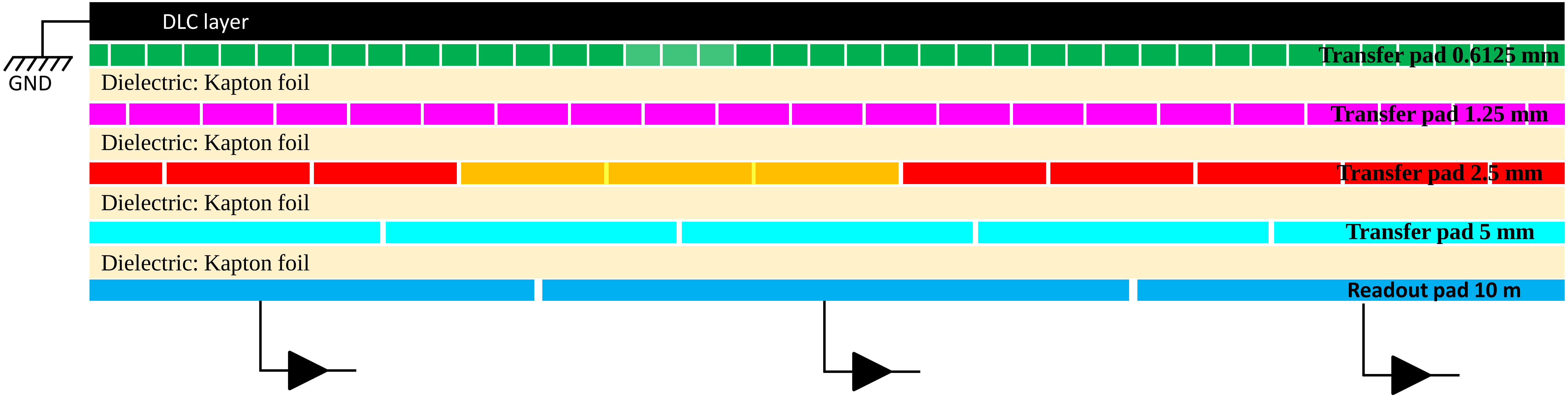

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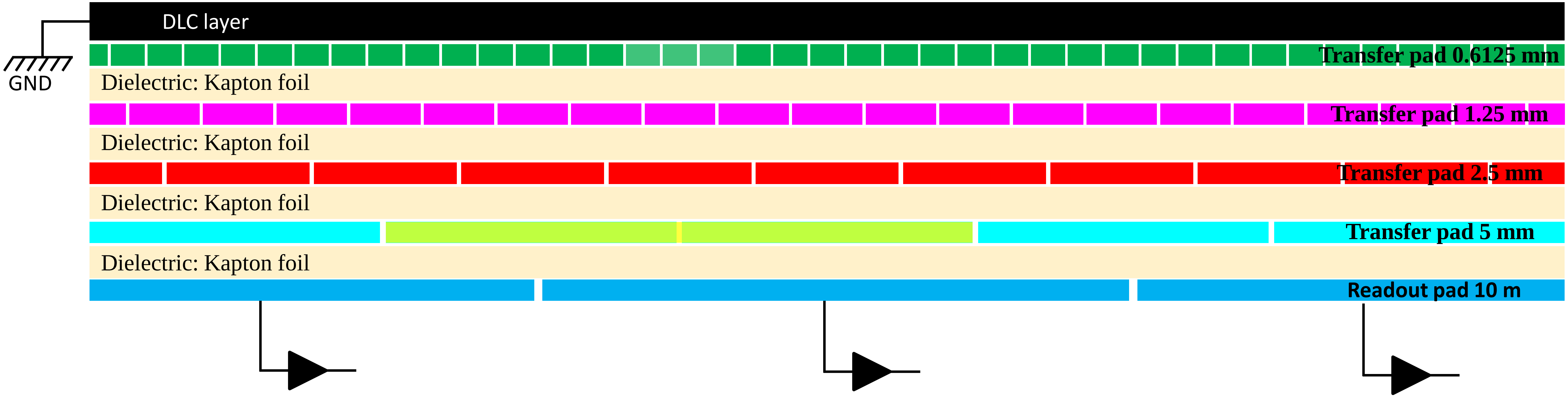

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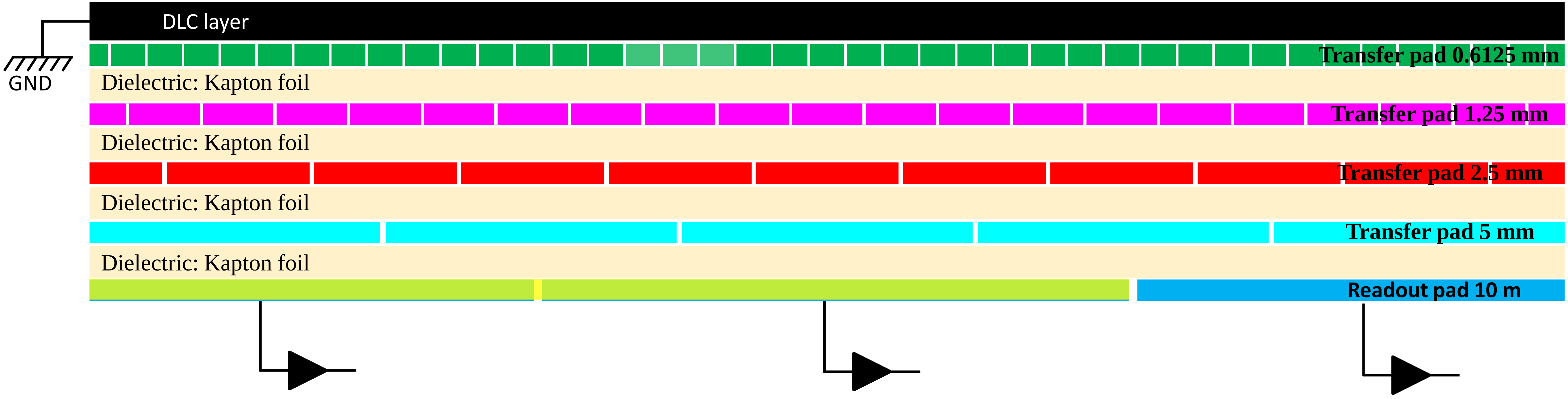
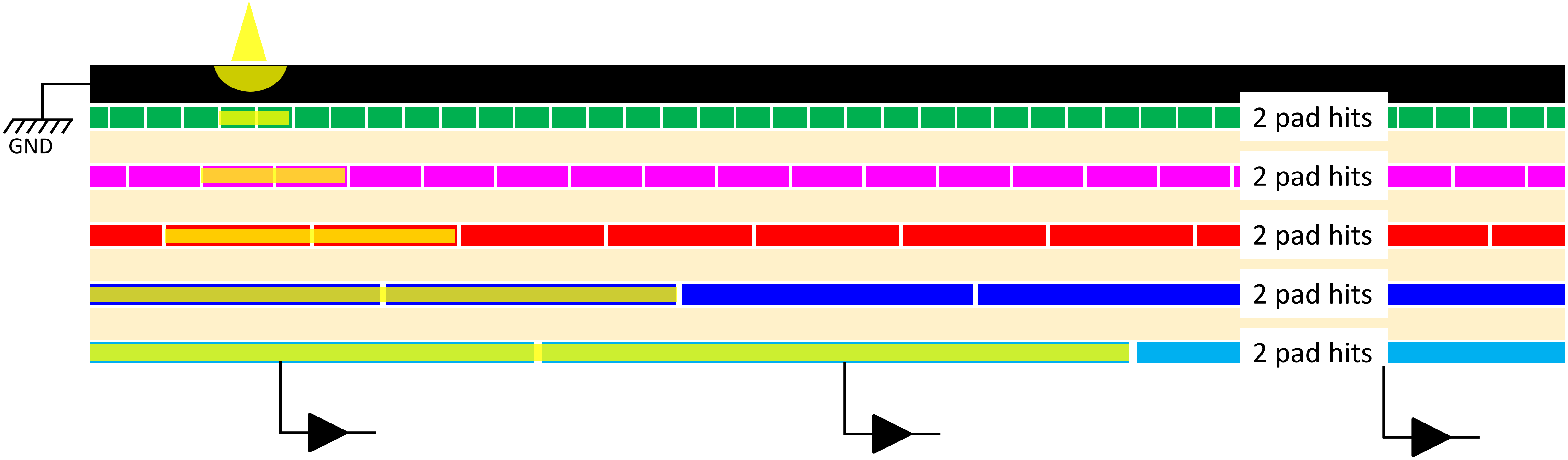


Principe of large pads readout with high spatial resolution capabilities

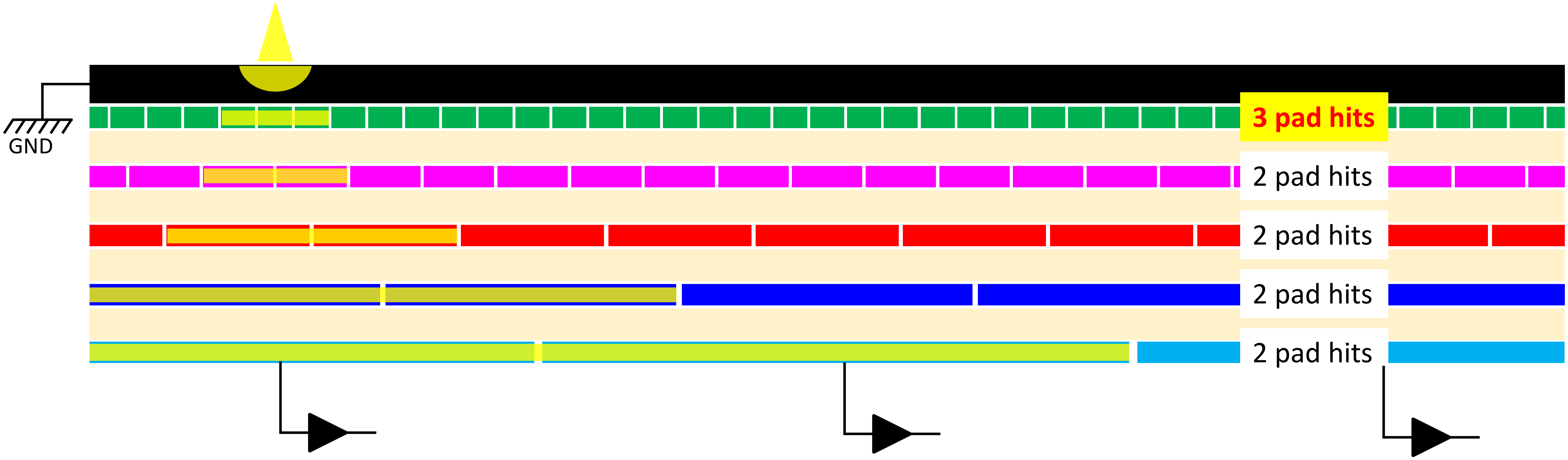


Spatial resolution performances basically depends on how many pads from top layers have hits

- Typically, charges from a standard (3-2-2-2-) triple-GEM will hit on average 3 COMPASS X-Y (400 µm pitch) strips,
- So with DLC layer contribution, top layer pad size of 0.6125 µm will always have at least two pads with hit on average in each direction
  - ⇨ Meaning at least 4 pads (x and y direction) on average with hit on top layers ⇨ so expect an average number of pad on the readout layer > 4

Illustration here in one direction only

Principe of large pads readout with high spatial resolution capabilities



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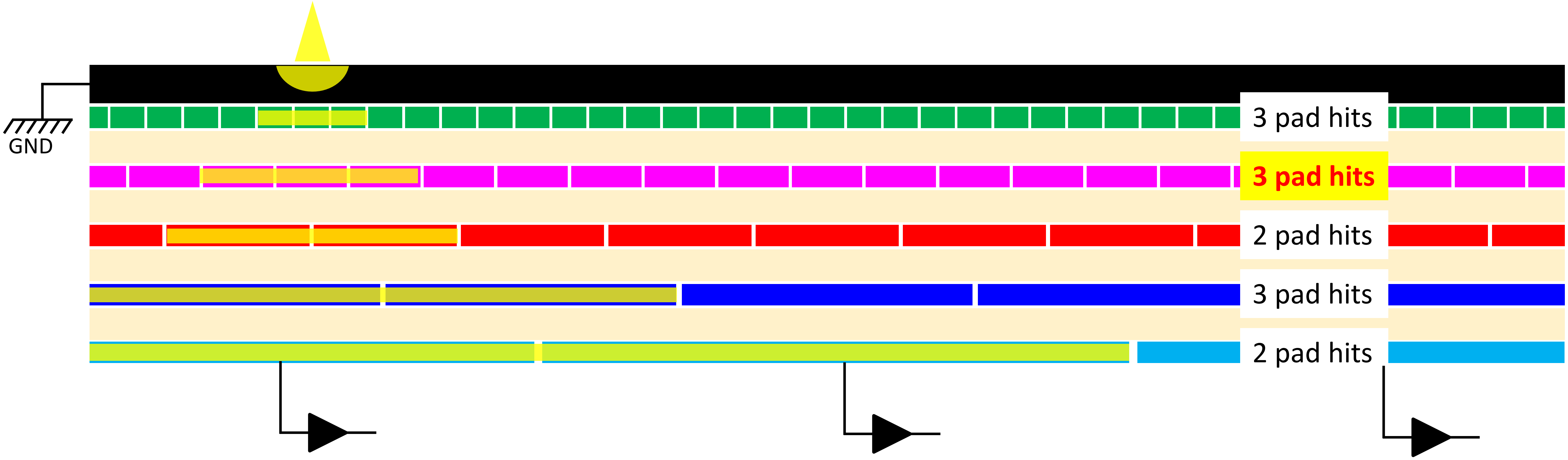

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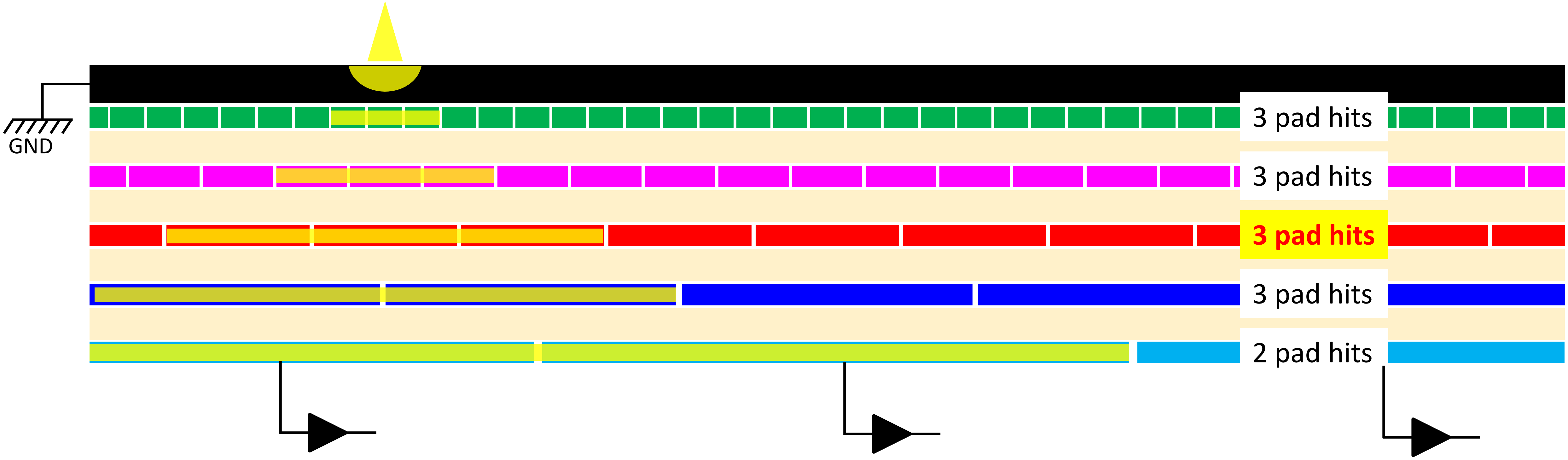

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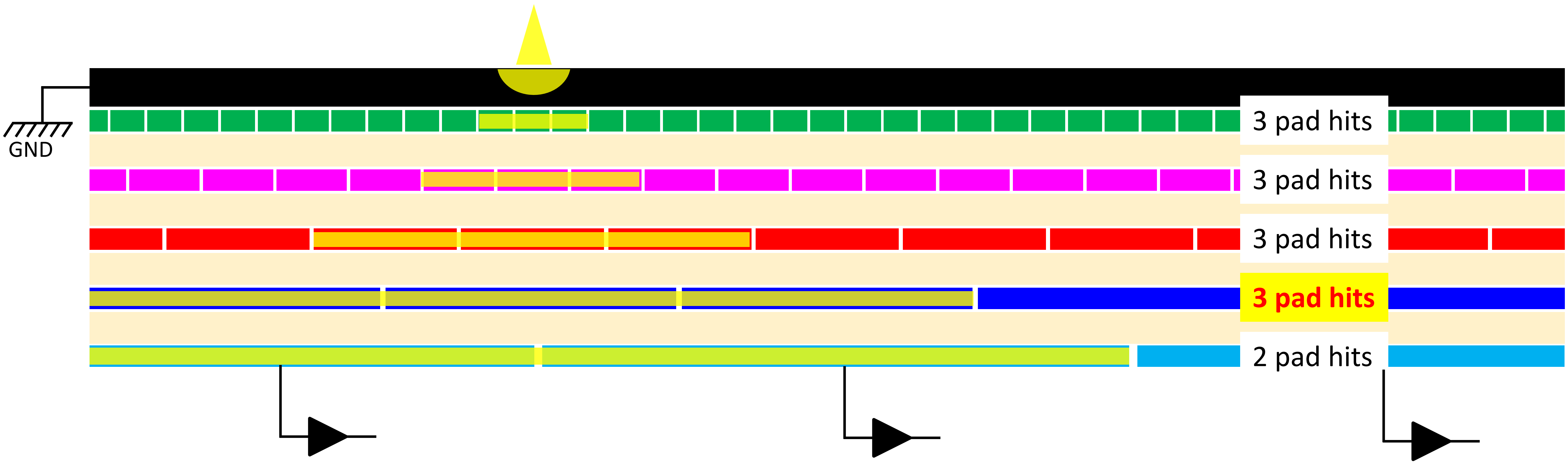

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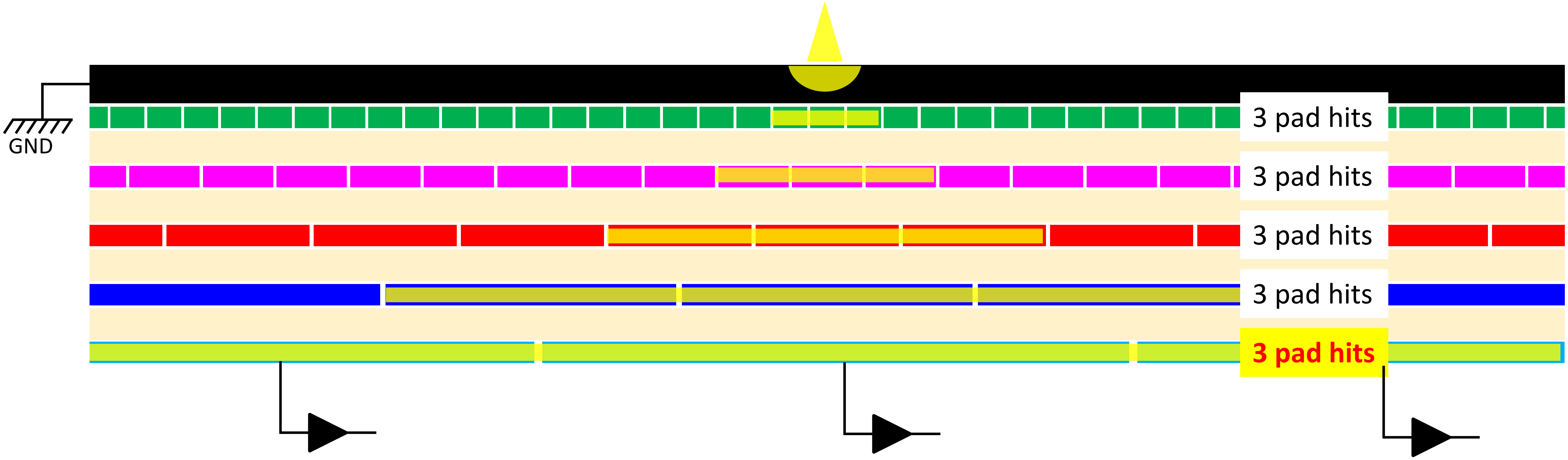

Spatial resolution performances basically depends on how many pads from top layers have hits

- Typically, charges from a standard (3-2-2-2-) triple-GEM will hit on average 3 COMPASS X-Y (400 µm pitch) strips,
- So with DLC layer contribution, top layer pad size of 0.6125 µm will always have at least two pads with hit on average in each direction
  - ⇨ Meaning at least 4 pads (x and y direction) on average with hit on top layers ⇨ so expect an average number of pad on the readout layer > 4

Illustration here in one direction only