SAMPA SRS Integration Status Report

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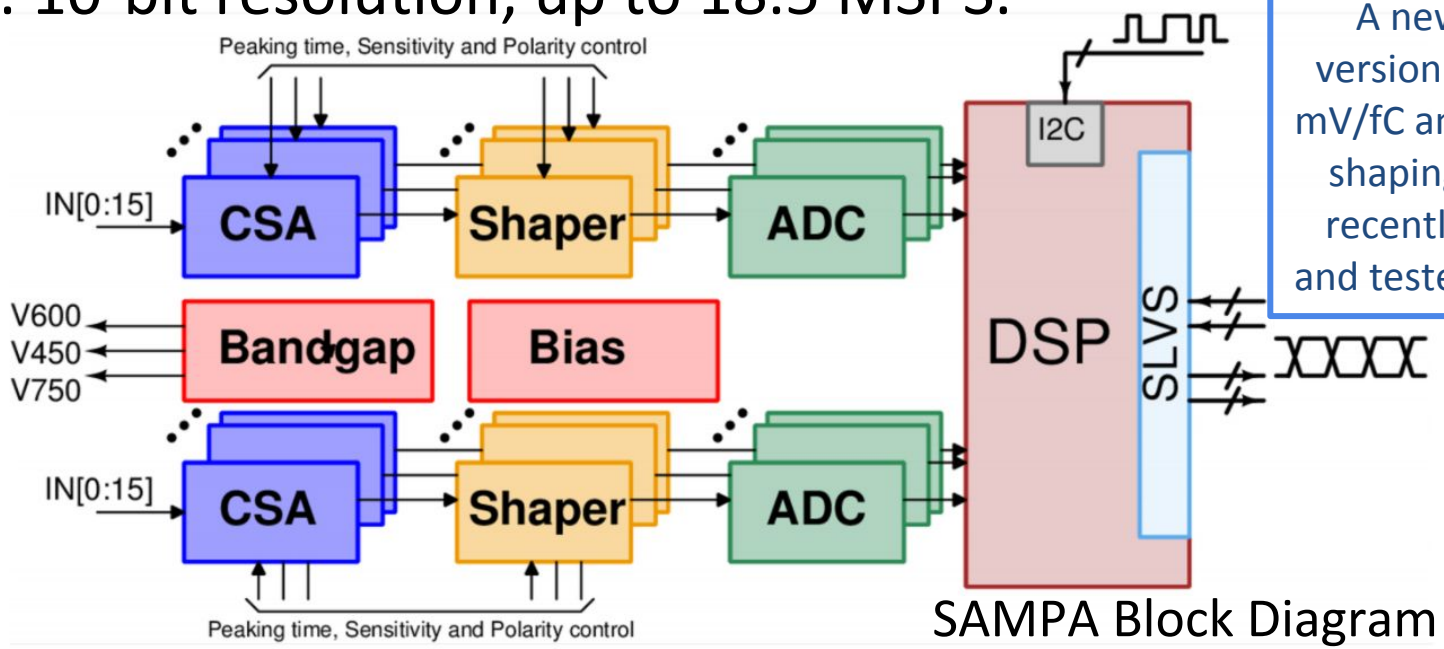
SAMPA Overview

- TSMC CMOS 130nm, 1.25V technology.
- 32 Channels, Front-end + ADC + DSP.
- Positive and negative polarities with 2 analog front-end modes:
  - 20 or 30 mV/fC with 160 ns shaping time.(Sensor Cap: 12 - 25 pF)
  - 4 mV/fC with 300 ns shaping time. (Sensor Cap: 40 - 80 pF)
- ADC: 10-bit resolution, up to 18.5 MSPS.

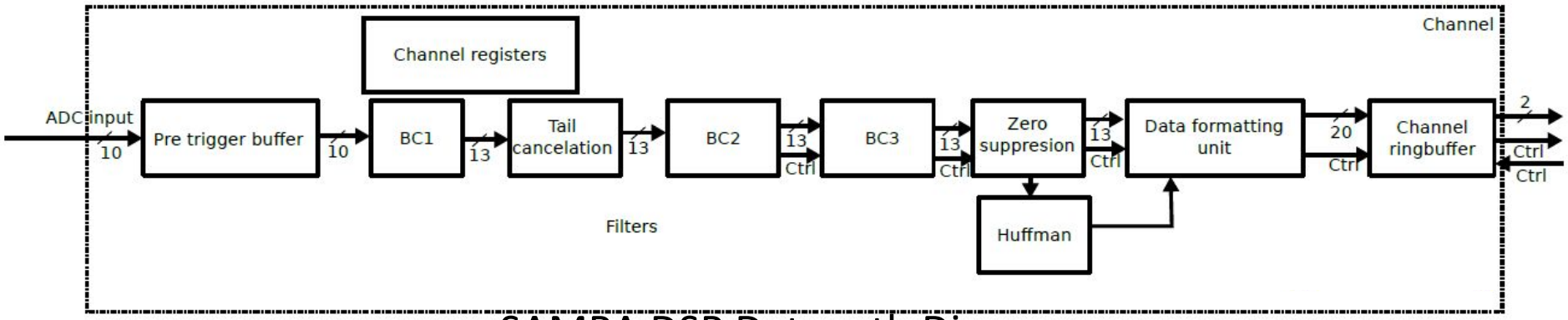


SAMPA Block Diagram

A new SAMPA version with 20/30 mV/fC and 160/80 ns shaping time was recently designed and tested on silicon.

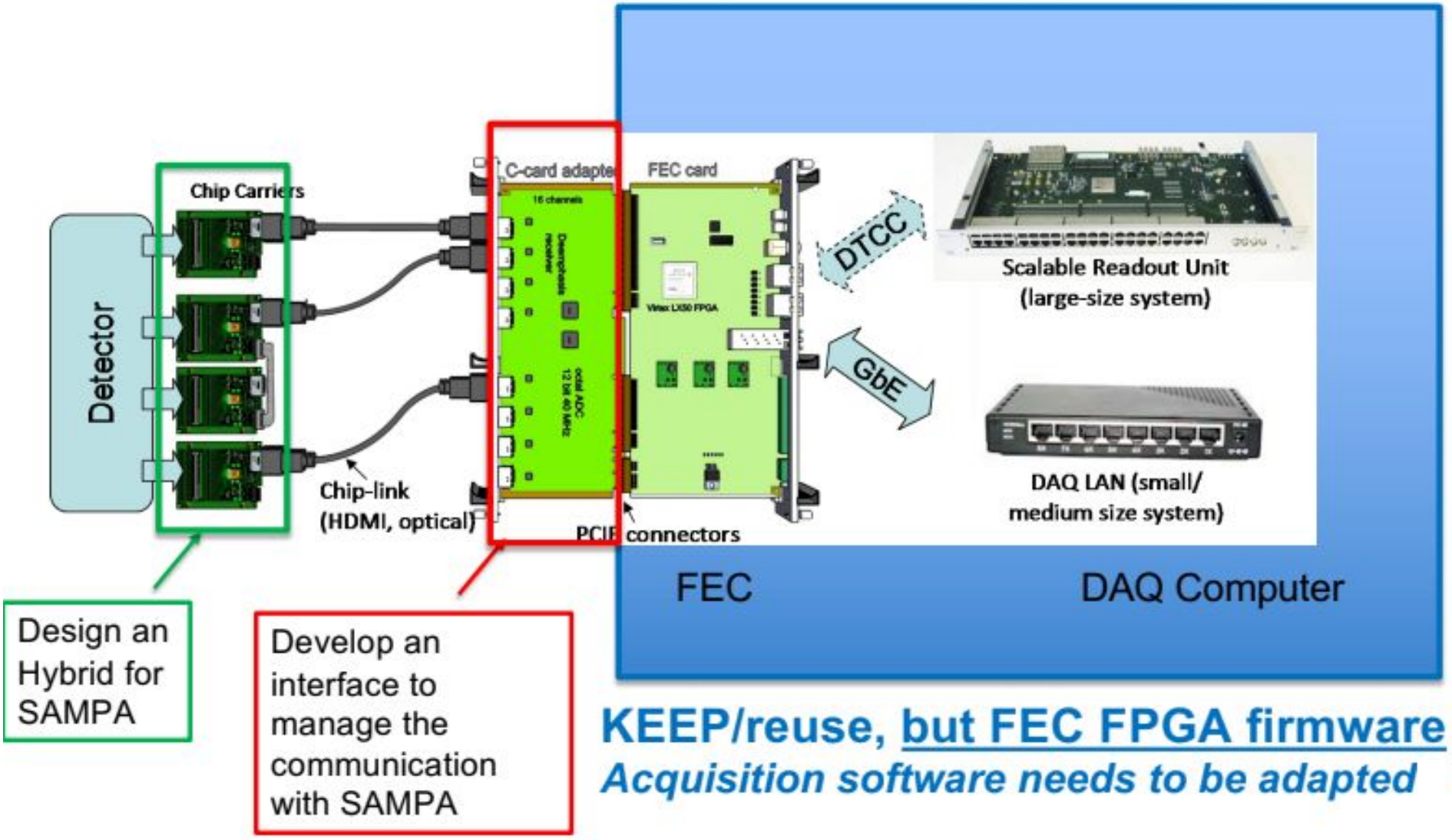
SAMPA Overview

- DSP functionalities:
  - I2C Configurable.
  - Pedestal Memory.
  - Pre-trigger buffer.
  - Baseline correction.
  - Tail cancelation.
  - Zero-suppression.
  - Huffman compression.
  - Individual operations per channel.
- Triggered or continuous acquisition modes.
- Data transmission: up to 11 e-links @ 320 Mbps, SLVS.



SAMPA DSP Datapath Diagram

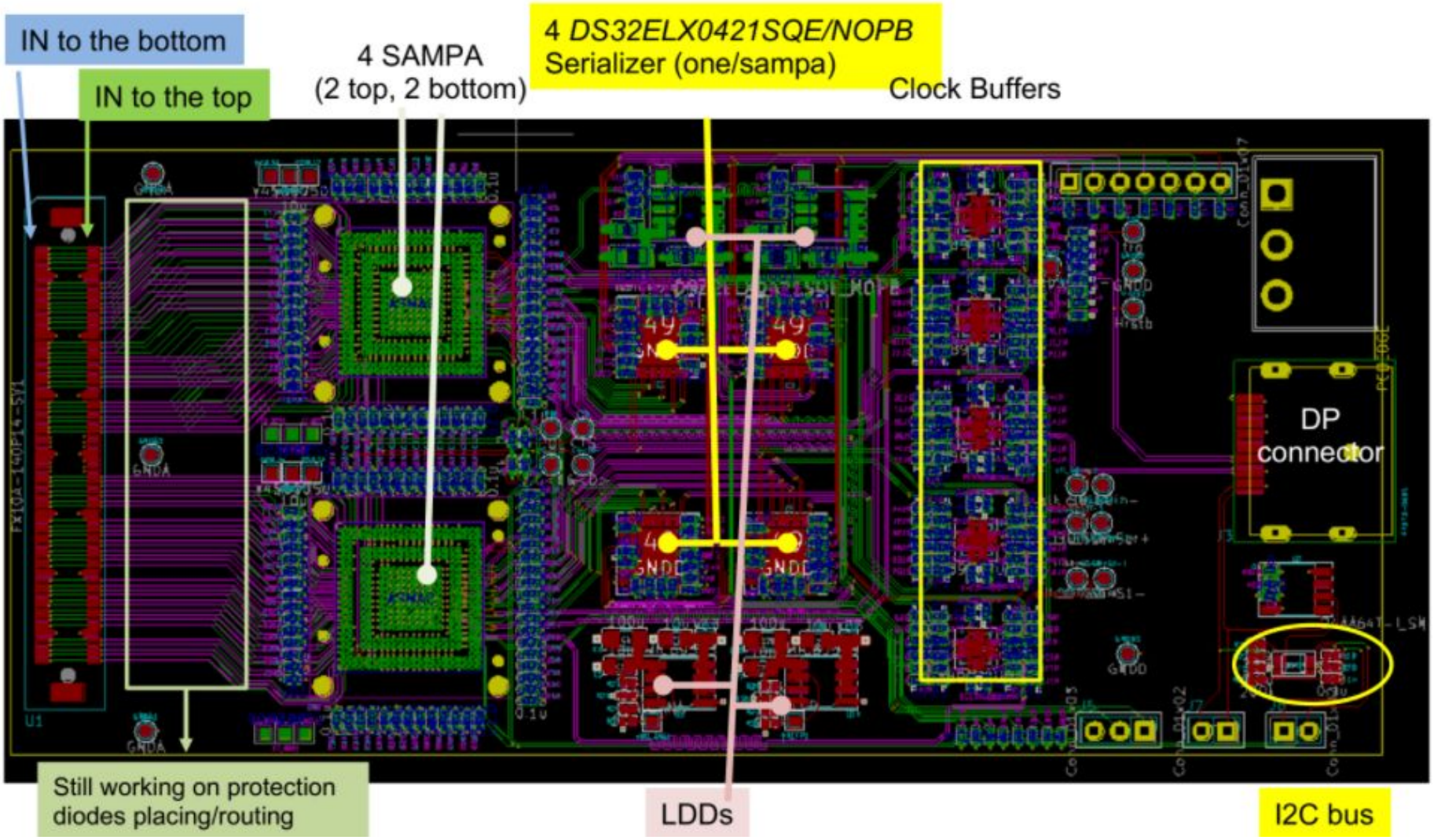
SRS and how to fit SAMPA in



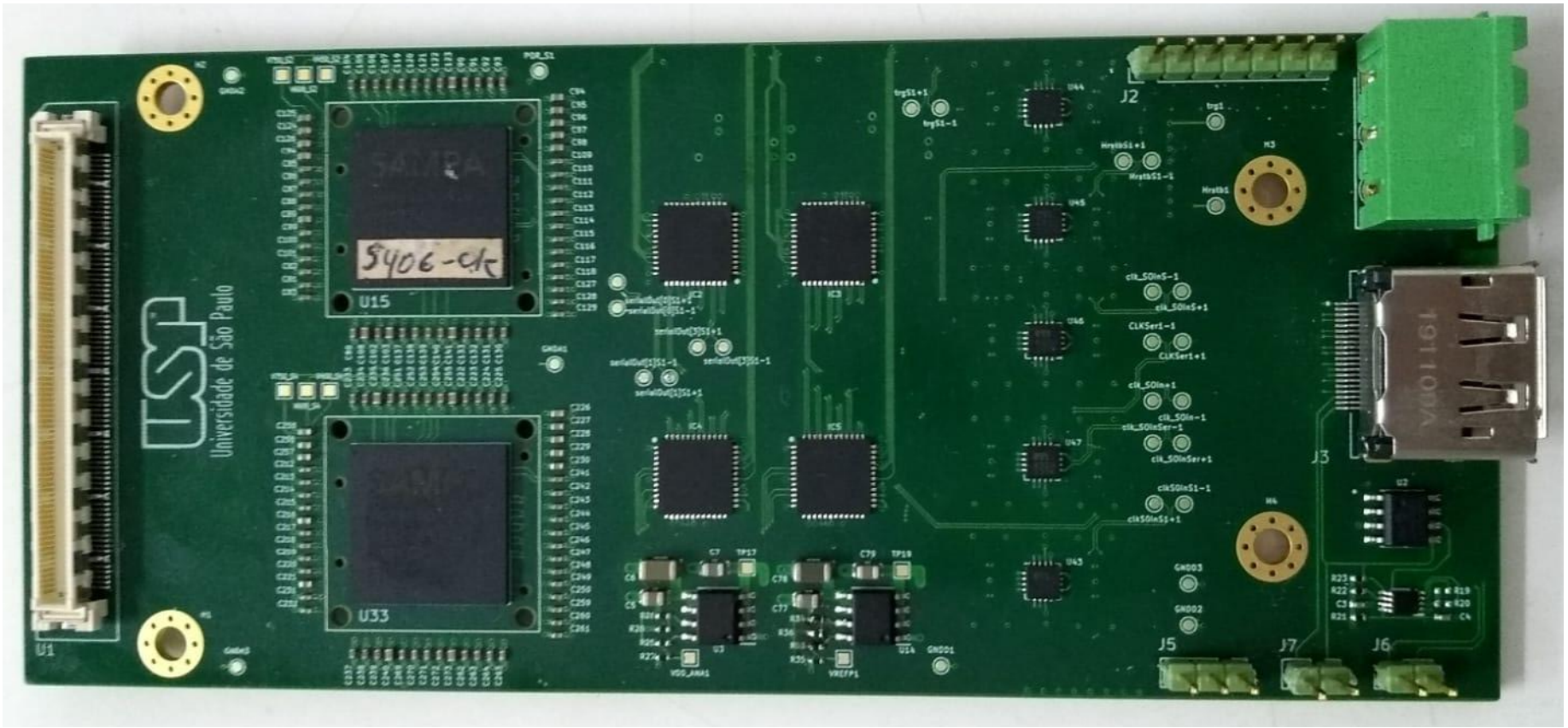
The Prototype

- Hybrid Board
  - Needs to read 128 channels (Each SAMPA reads 32).
  - As close as possible to the final board.
  - But still a prototype version (testpoints + fail-safe).
  - How to send data from SAMPA to SRS?
    - SAMPA chip in default mode (Plug and Play)
      - 4 eLinks each -> 4 SAMPAs = 16 eLinks.
    - Serializer - DS32EL0421 - 4 eLinks to 1 High Speed Link.
  - HDMI vs DisplayPort (4 vs 5 Differential Pairs)
    - 4 High Speed Links (1.2 Gbps) + 1 Clock (300 MHz).
- Adapter Board
  - As simple as possible, interface SRS (FECv6) and Hybrid.
    - Deserializers + DisplayPort Connector.

Prototype Hybrid Board

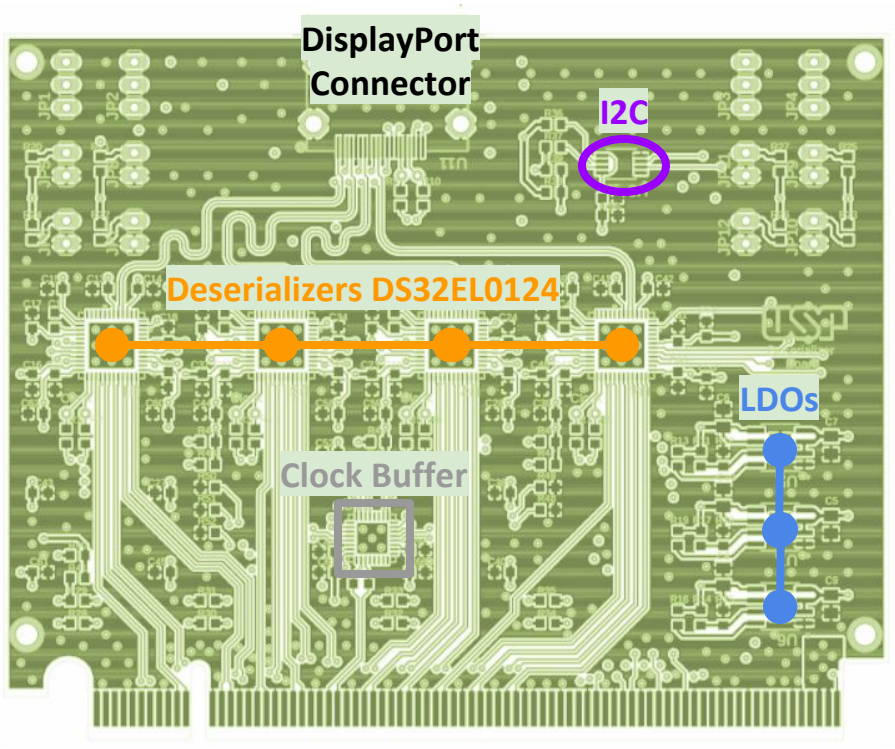


Prototype Hybrid Board



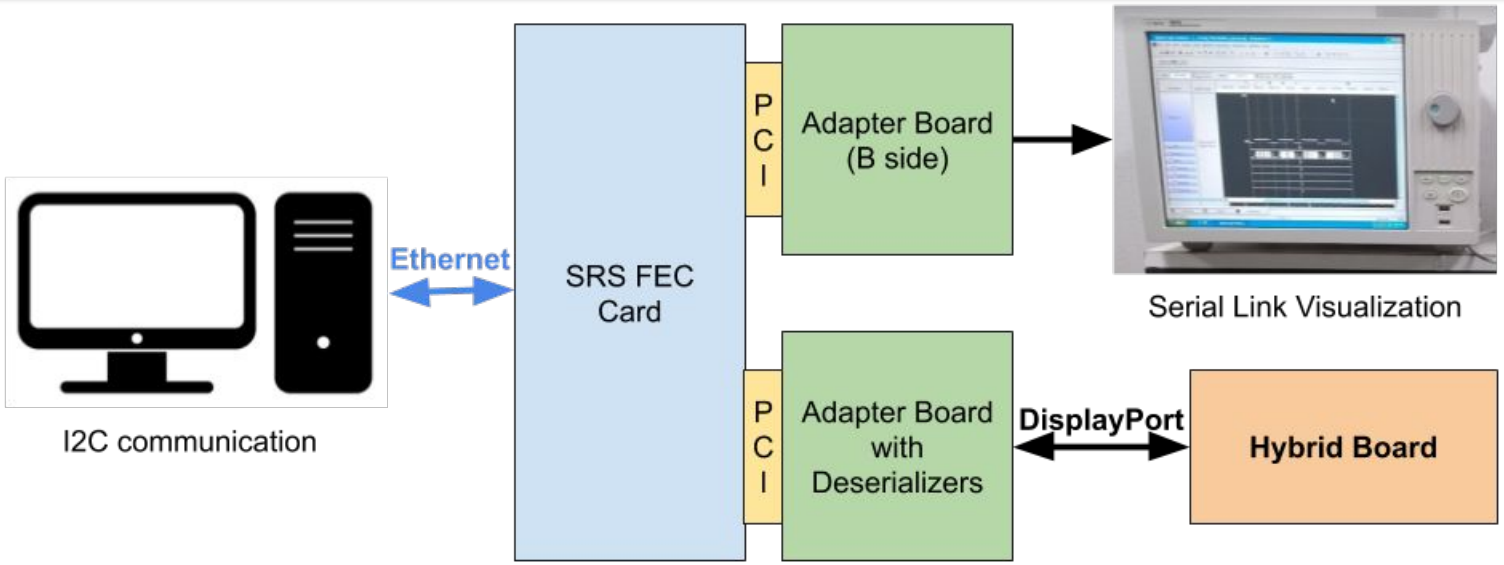
- DisplayPort connector - 5 DIFF lanes + 4 SE lanes.
- Serializer: DS32EL0421 - Translates 4 SAMPAs e-links to 1.
- I2C communication for configuration (SRS Slow Control).

Prototype Interface board



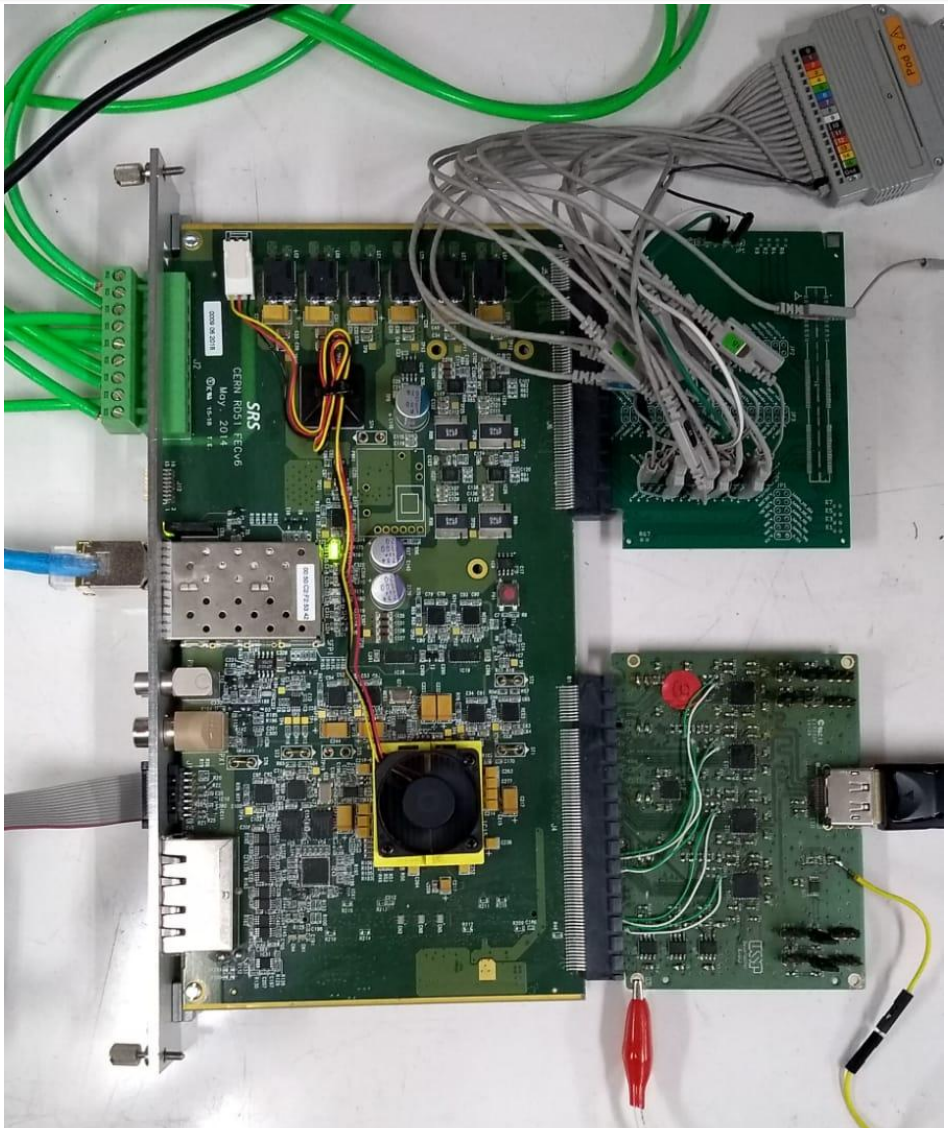
- DisplayPort Connector - 4 data links + 1 CLK + RST + TRG + I2C .
- Deserializer : DS32EL0124 - Recover the 4 SAMPA e-links.
- Only 1 Hybrid for now (16 ADIFFs for SAMPA serial Links + 1 Clock + 4 recovered clocks) at PCI connector.

Testbench



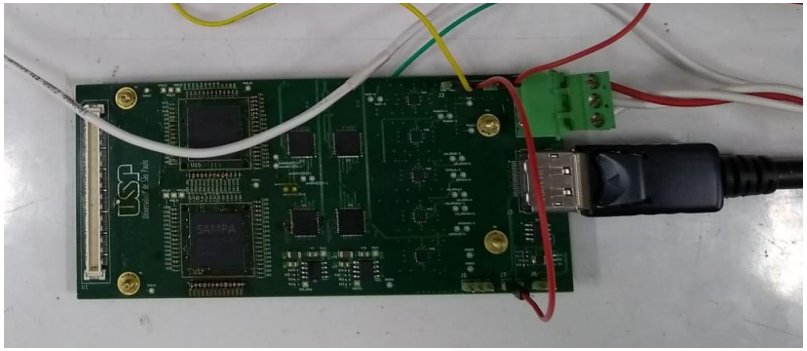
- SRS FEC Card - Decoder of data and manager of interfaces.
  - A side - Adapter board for Hybrid.
  - B side - “Breadboard” for firmware debug (Logic Analyser).
- Ethernet for SRS slow control and data reception.
- Logic Analyser to help with our debug.
- FPGA is responsible for Decoding SAMPA signals and manage the different interfaces (Ethernet, I2C, Clock, Trigger, Reset).

Testbench



Some adaptations:

- Recovered clocks in AIOs rerouted.
- External auxiliary power supply for lower power dissipation on Hybrid.
- I2C SCL rerouting on DisplayPort connector.



Results (Slow Control)

```
PS C:\Arquivos de Programas\PacketSender> .\packetsender -b 6007 -w 500 -u 10.0.0.2 6024
"80 00 00 00 FF FF FF FF BB AA FF FF 00 00 00 00 F6 F8 00 00"
UDP (6007)://10.0.0.2:6024 80 00 00 00 FF FF FF FF BB AA FF FF 00 00 00 00 F6 F8 00 00

From: ::ffff:10.0.0.2, Port:6024
Response Time:08:59:43.579
Response HEX:00 00 00 00 FF FF FF FF BB AA FF FF 00 00 00 00 00 00 00 01 00 00 00 0C
Response ASCII:\00\00\00\00\ff\ff\ff\ff\bb\aa\ff\ff\00\00\00\00\00\00\00\01\00\00\00\0c
```

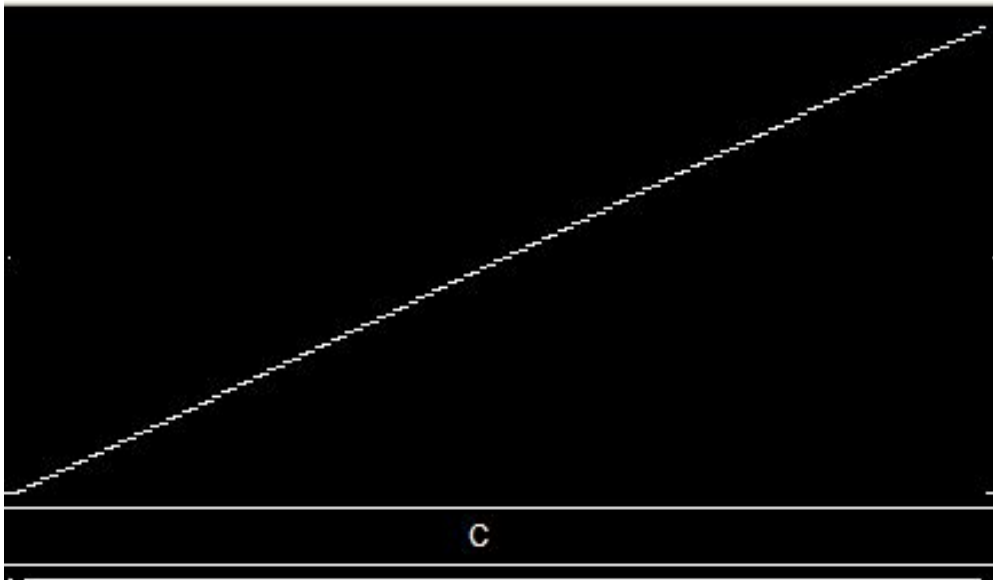
SRS Slow Control Protocol UDP Datagram sent

SAMPA read register through I2C

Use I2C through SRS slow control protocol for configuration & status update:

- SAMPA.
- Serializer.
- Deserializer.

Results (Serial data links)

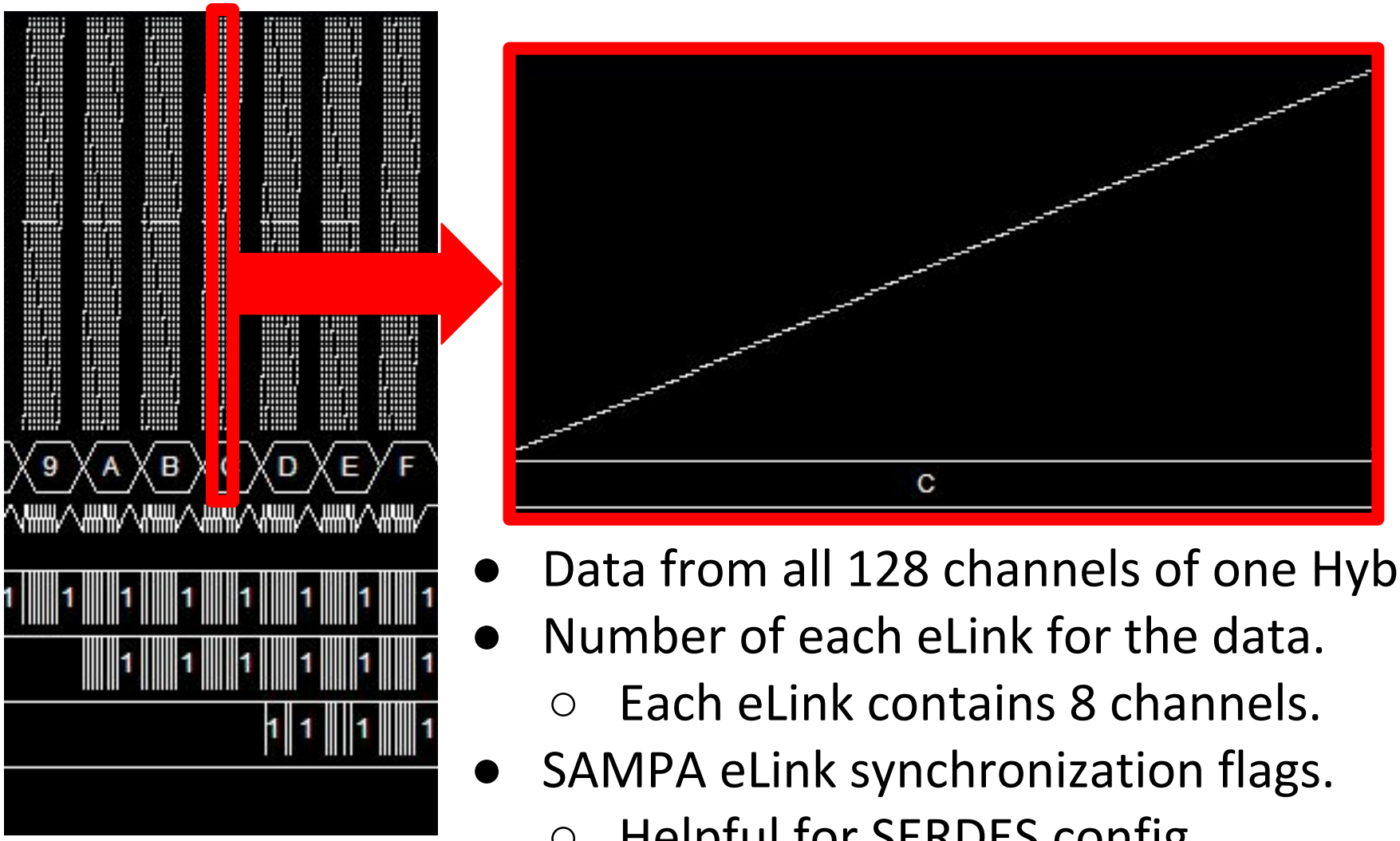


Data visualization for each channel on Logic Analyzer

1. Load SAMPA memory with one ramp for each channel (SRS Slow Control).
2. SAMPA Data >> SERDES >> SRS FEC.
3. Data visualization with Logic Analyzer System after decoding on FEC.

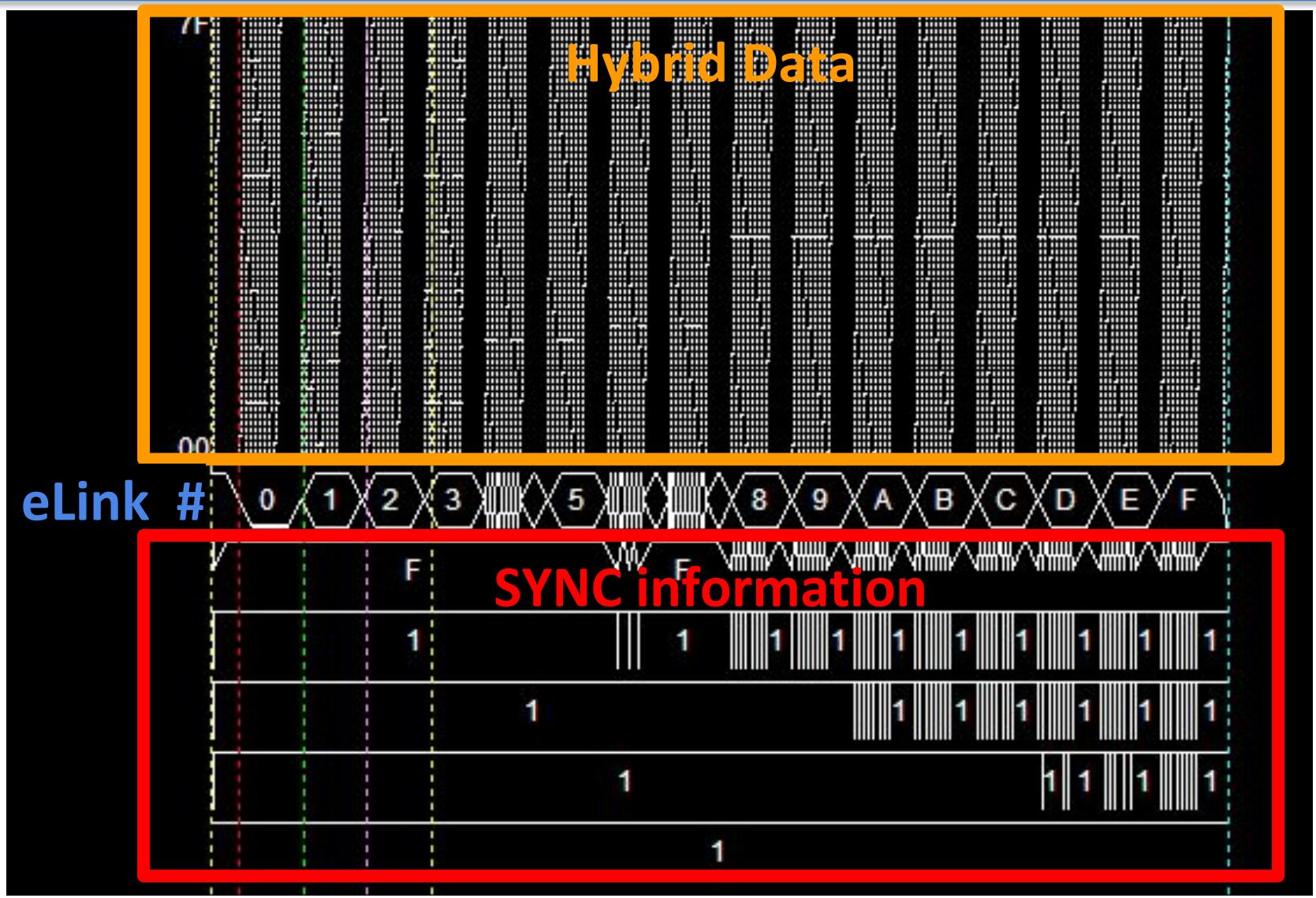
Logic Analyzer System

Results (Serial data links)



- Data from all 128 channels of one Hybrid.
- Number of each eLink for the data.
  - Each eLink contains 8 channels.
- SAMPA eLink synchronization flags.
  - Helpful for SERDES config.

Results (Serial data links)



Next Steps

- Test the Hybrid boards with input signals at HRS.
- Evolve prototype boards to beta version of one Hybrid per SRS FEC Board.
- Plans for the future: Four Hybrids in one FEC Board.

Currently in development:

- Send SAMPA data through Ethernet.

Under investigation:

- Automatic SAMPA Serial Links Synchronization.
- How to deal with the maximum data throughput:
  - 300 Mbps x4 (eLinks) x4 (SAMPAs)
    => 4.8 Gbps per Hybrid. (x4)

Conclusions

- A prototype (close to final) Hybrid Card with four SAMPAs was designed, fabricated and tested.
- Control of Hybrid Card is performed through SRS Slow Control Protocol (minor adjustments - I2C restart).
- SRS FEC Card generates SAMPA control signals (CLKs, TRG, RST).
- SERDES pair is able to handle SAMPA packets.
- SRS FEC Card is capable of reading and decoding four SAMPAs simultaneously (expected to be independent of trigger rate).

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