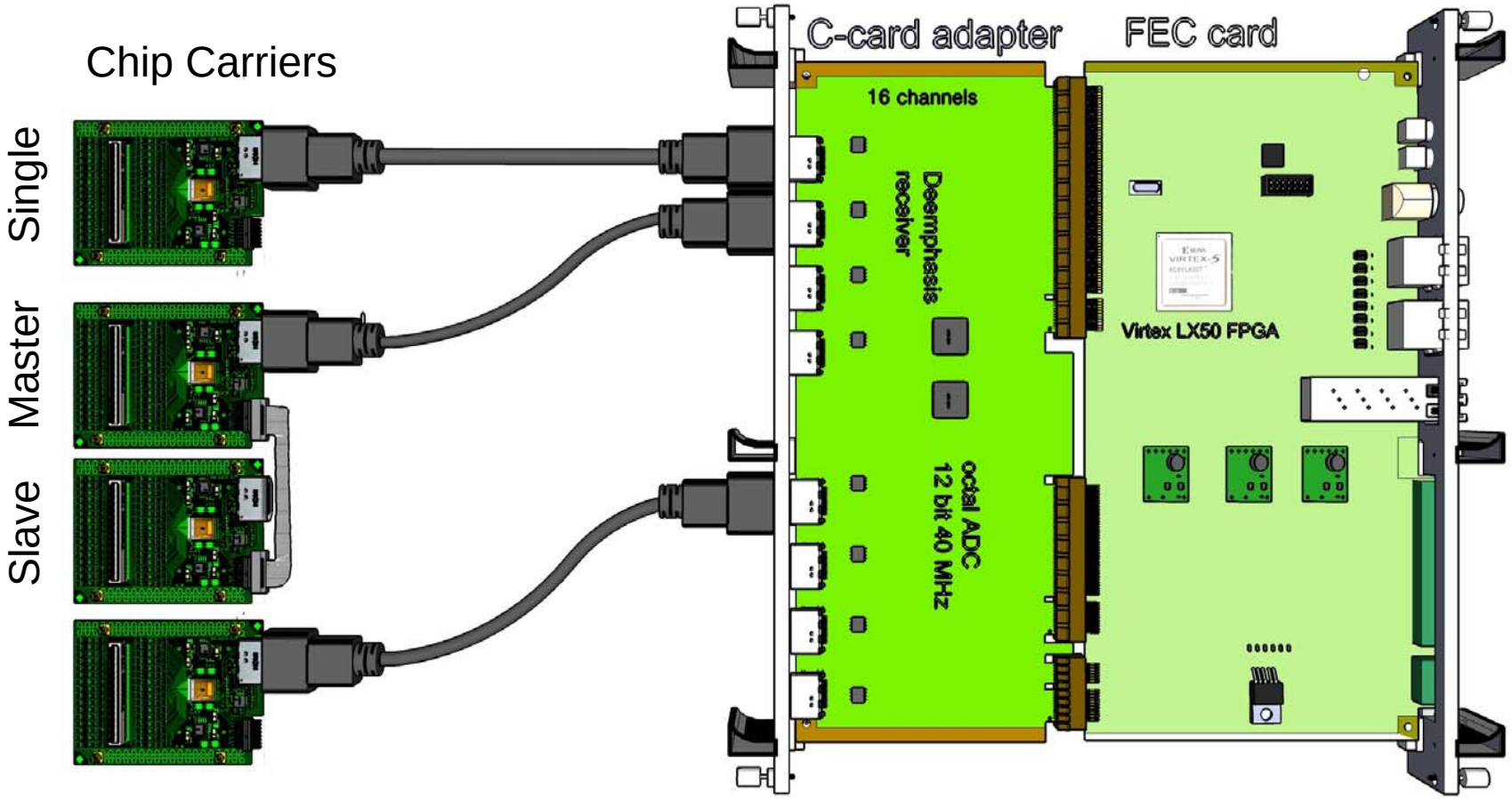
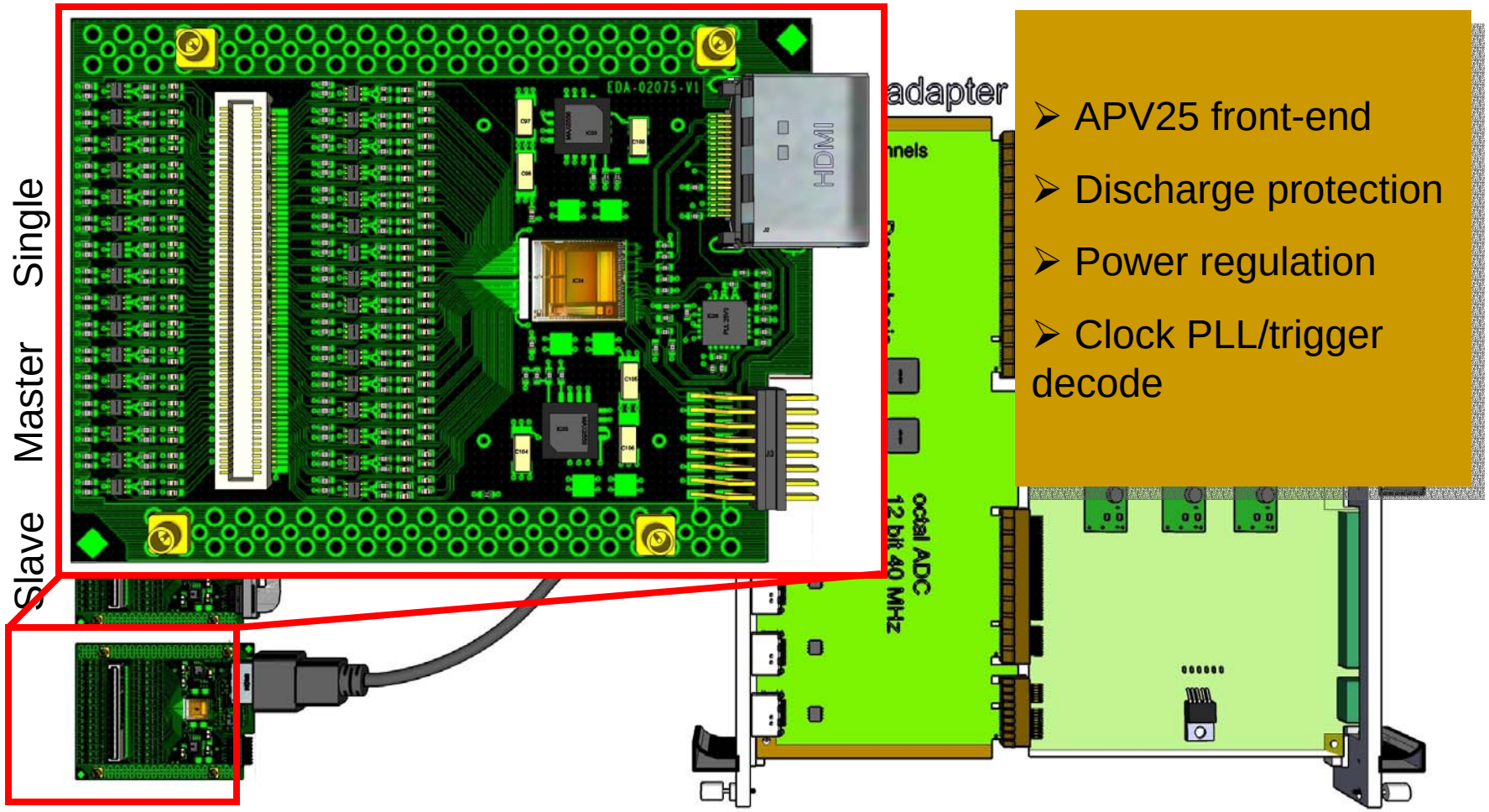
Status of the APV Hybrid and Digitizer card

Sorin Martoiu, CERN PH/DT

SRS APV DAQ

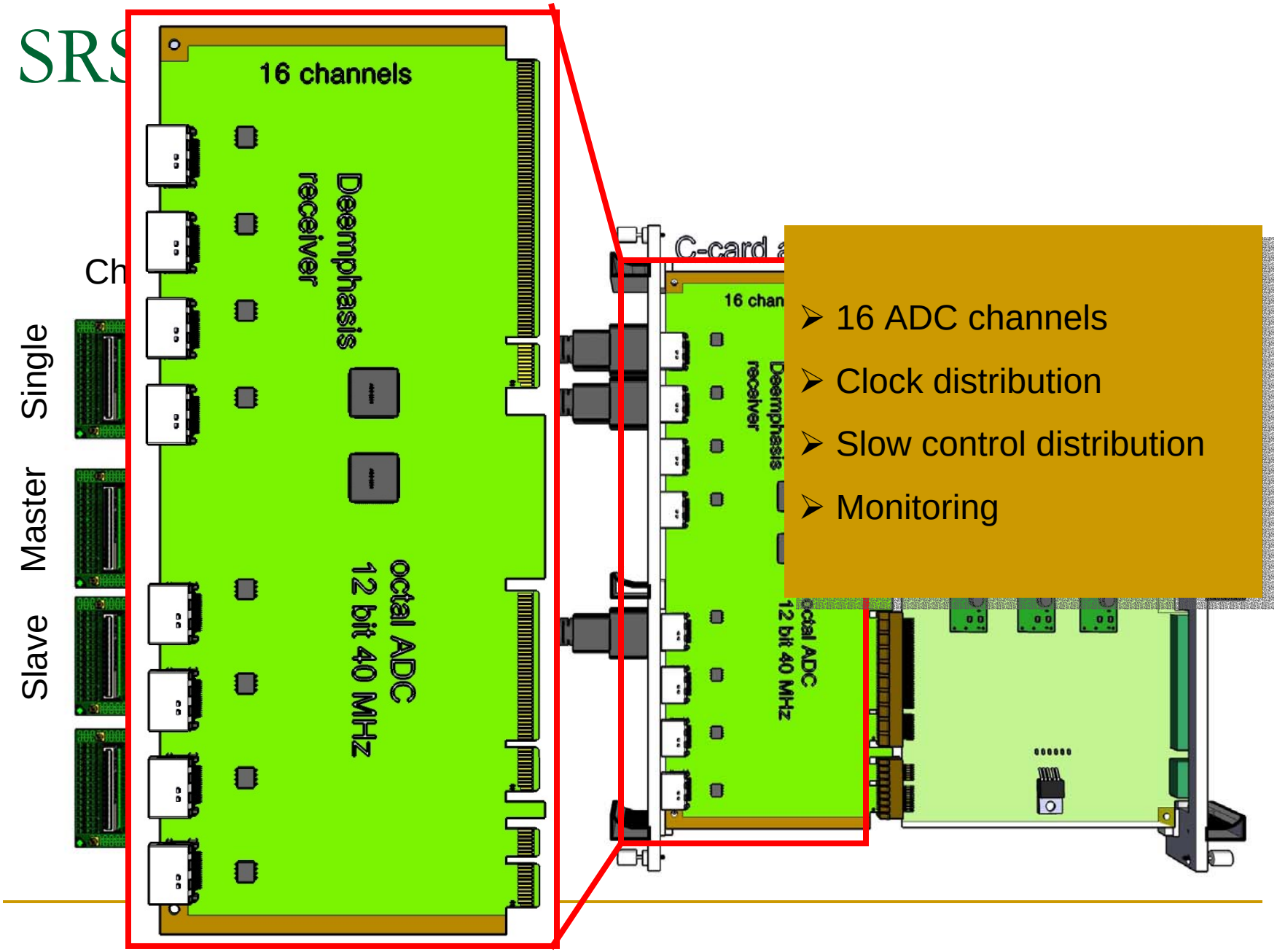

Chip Carriers
Single
Master
Slave
C-card adapter
16 channels
Deemphasis receiver
octal ADC 12 bit 40 MHz
FEC card
Virtex LX50 FPGA

SRS APV DAQ



- APV25 front-end
- Discharge protection
- Power regulation
- Clock PLL/trigger decode

SRS

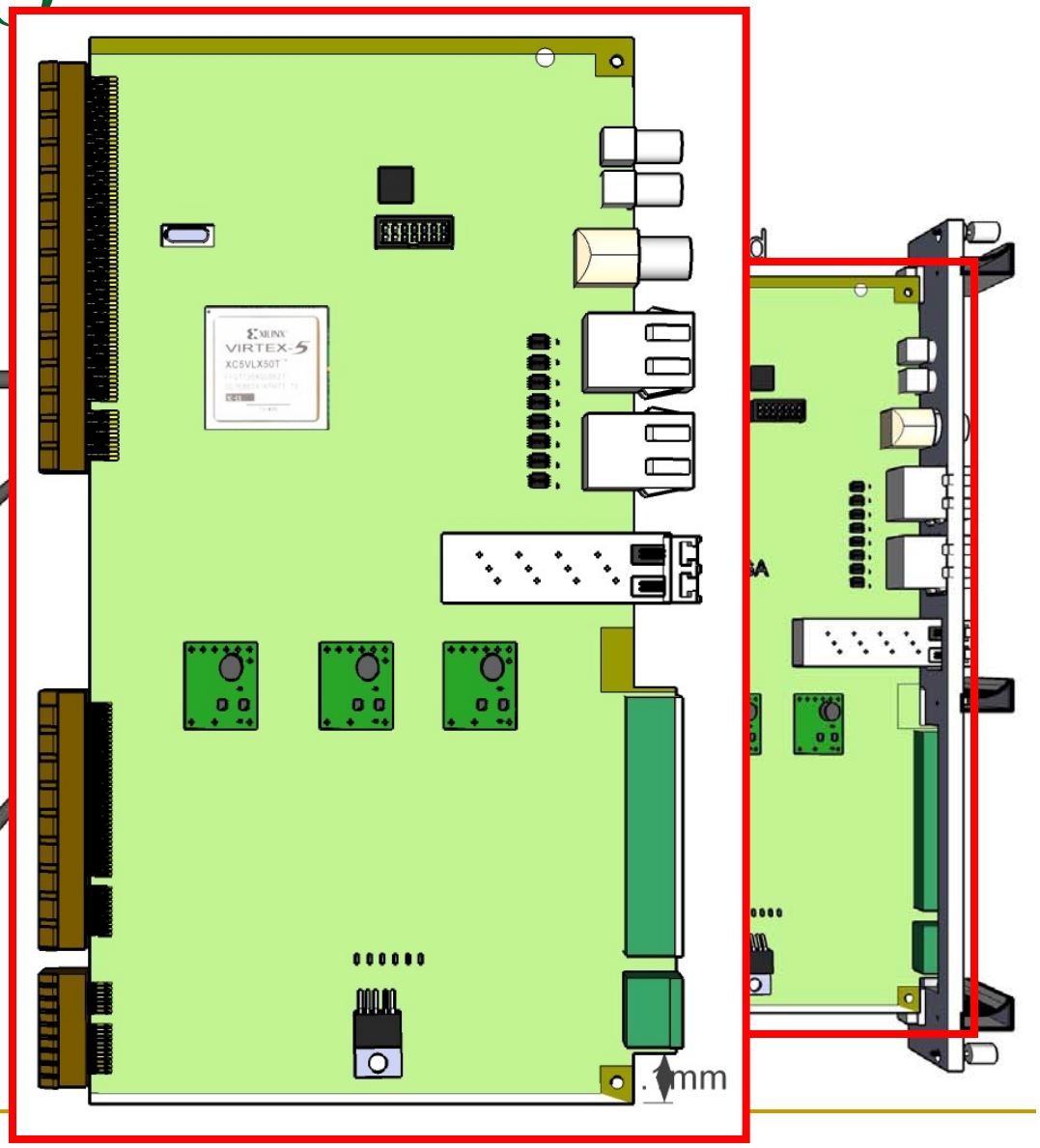


- 16 ADC channels
- Clock distribution
- Slow control distribution
- Monitoring

SRS APV DAQ

- Virtex5 LX50
- 2GB RAM (optional)

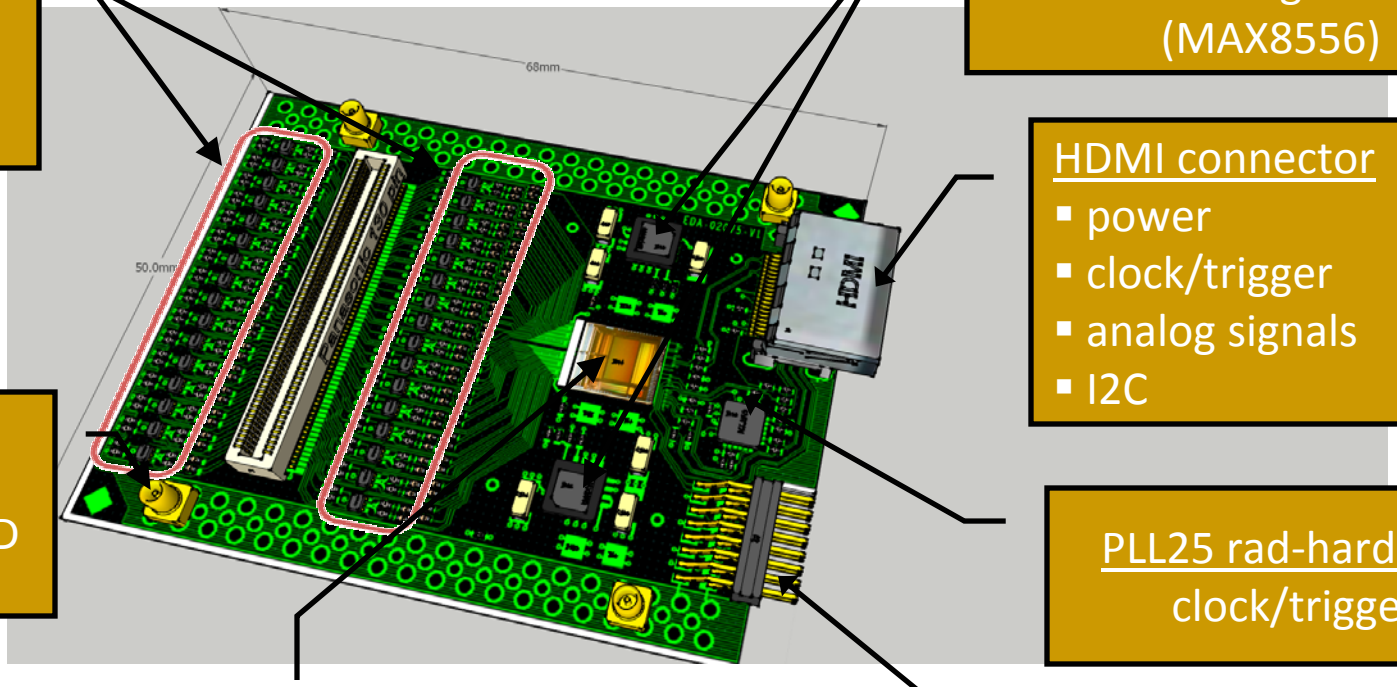
- Data acquisition
- Slow Control
- Event builder, feature extraction, etc.
- Gb Ethernet/DTC interface



APV Hybrid Overview

Discharge protection (NUP4114)

Power regulators (MAX8556)



HDMI connector
- power
- clock/trigger
- analog signals
- I2C

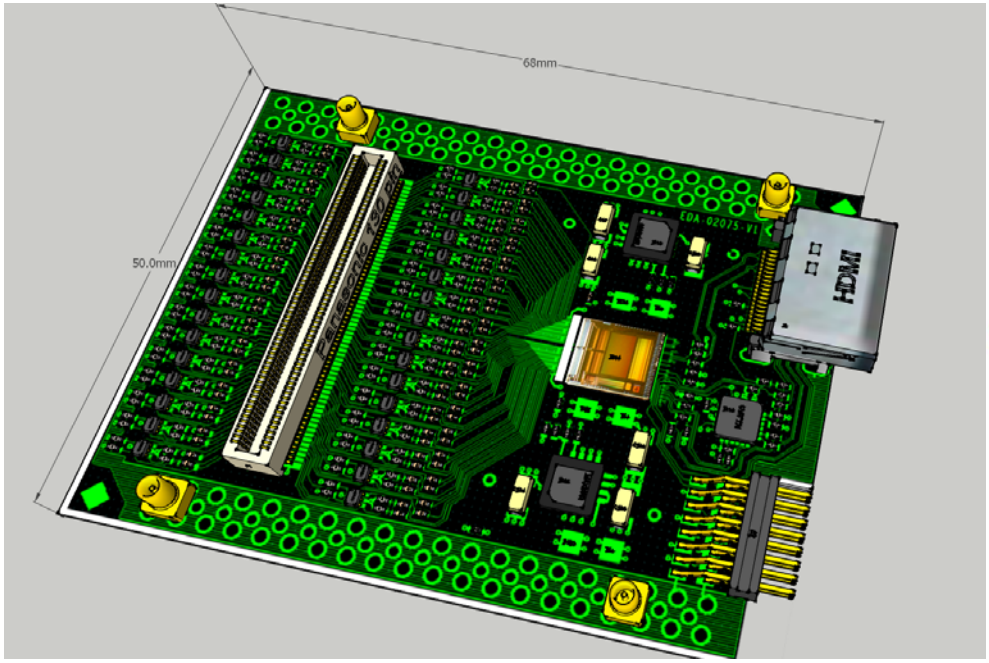
Coax Connectors
- <2mohm GND
- mechanical

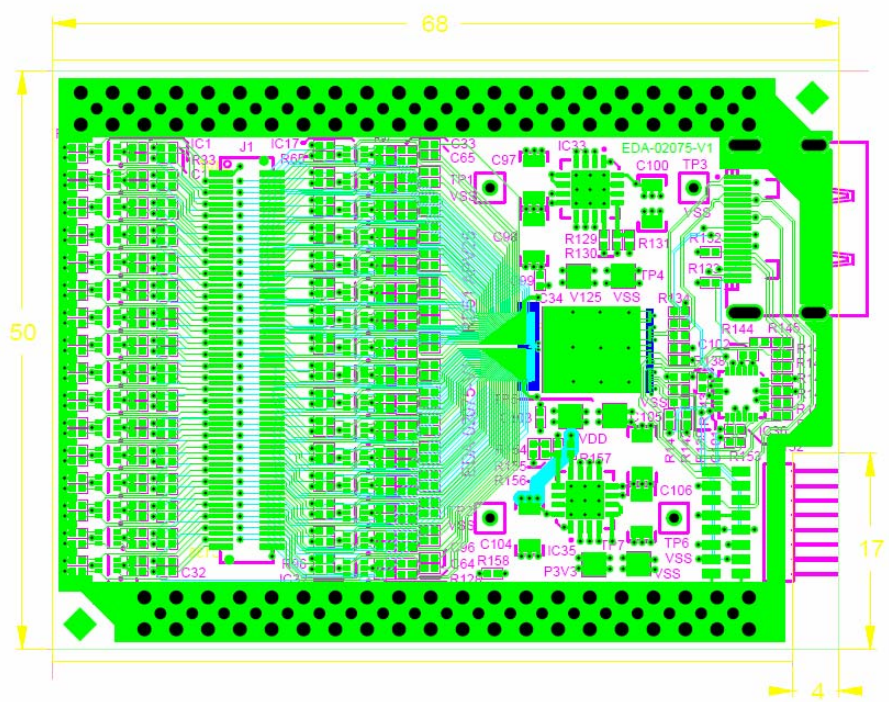
PLL25 rad-hard chip
clock/trigger

APV25 chip
- 128 channels
- 192-deep analog sampling memory

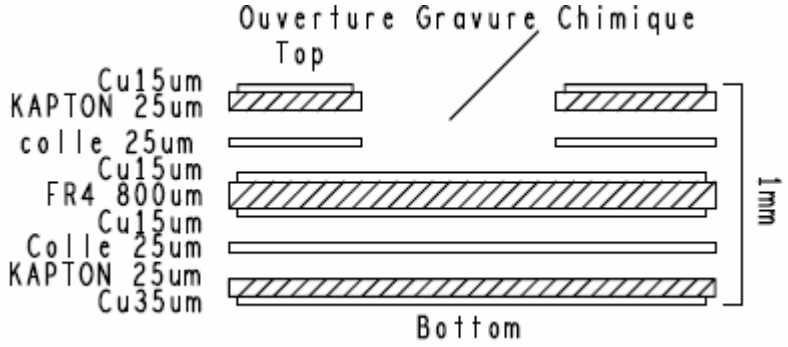
Extension connector for a second APV25 Hybrid

APV Hybrid Overview

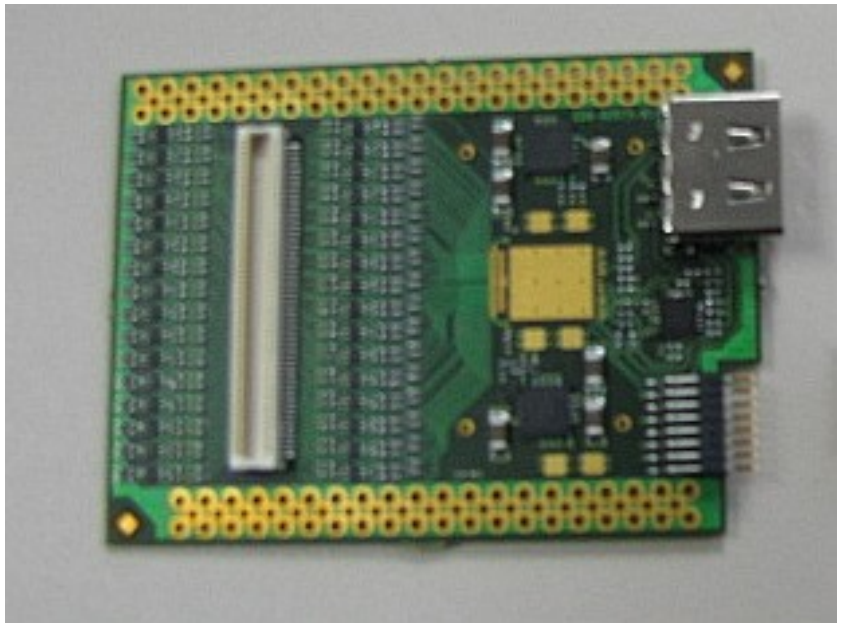


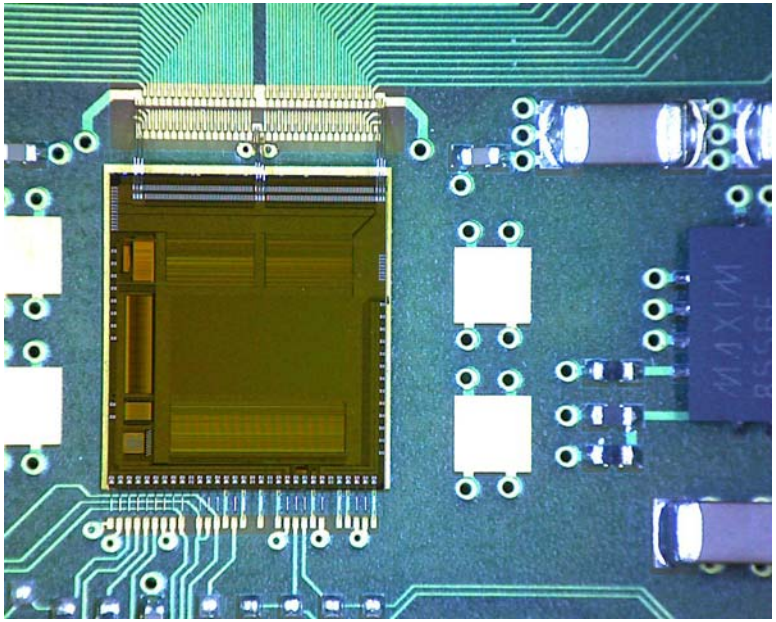


- 50mm x 68mm form factor
- 4 layers PCB/capton
- 1 mm thickness



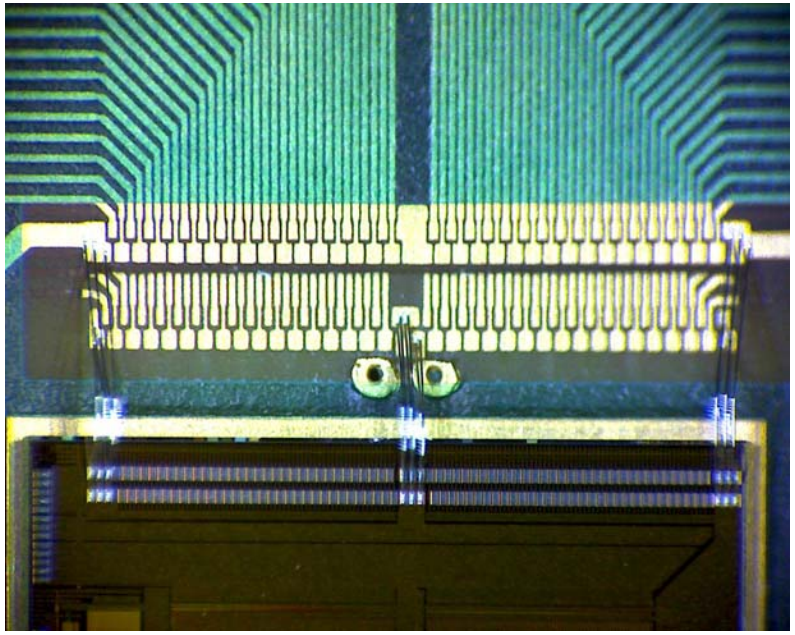
APV Hybrid Status (I)

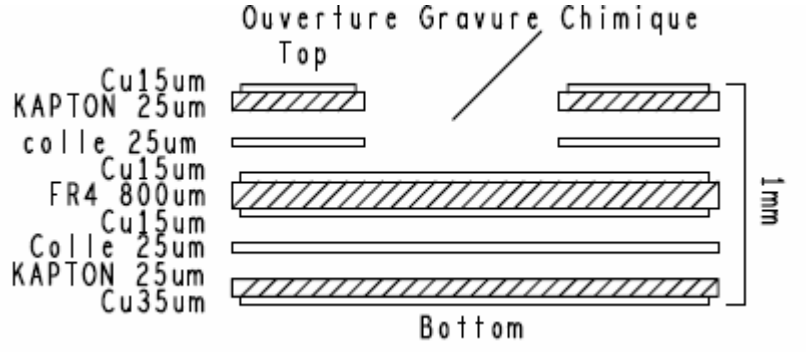




- First prototypes arrived
- Some delay due to some metallurgy problem
- Bonding works fine
- Tests under way

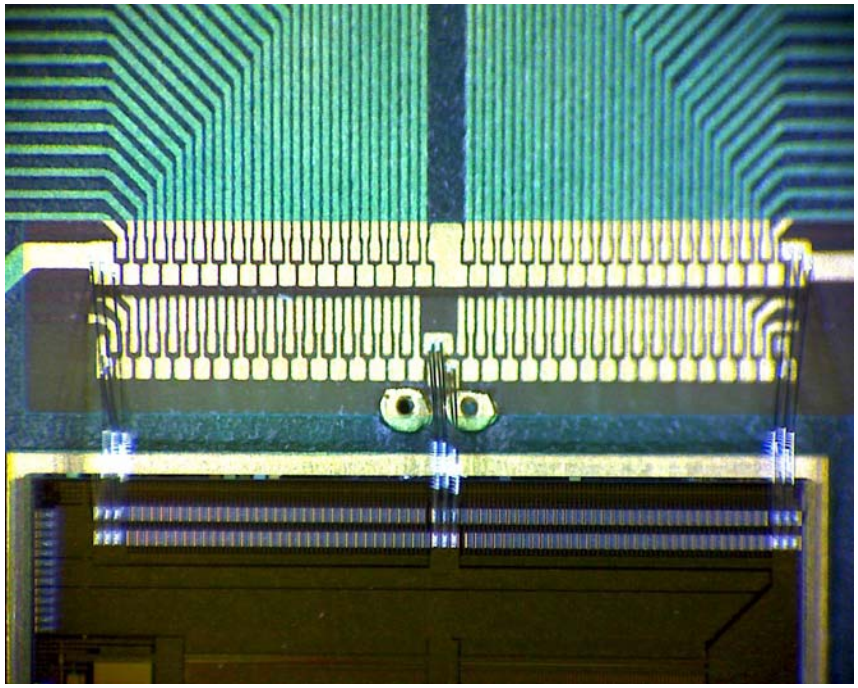
APV Hybrid Status (II)





- Bonding pads are distributed on two overlapping layers
- Lower pads are accessed through a cut in the upper layer

APV Hybrid - Future

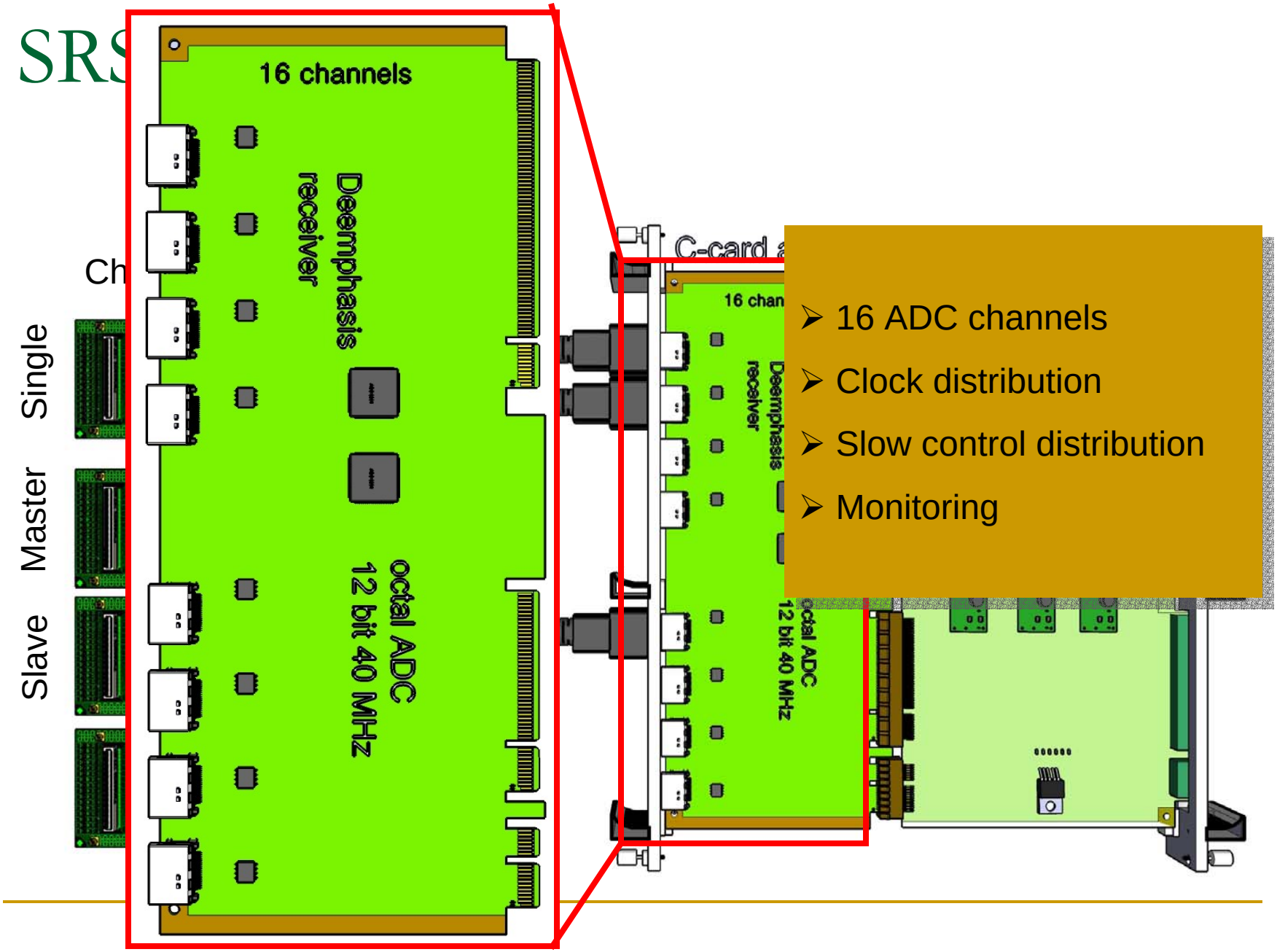


- The two vias in the bonding region will be eliminated to improve manufacturability
- Some common-mode stability issues addressed in the same time

APV Hybrid – Mini Connector

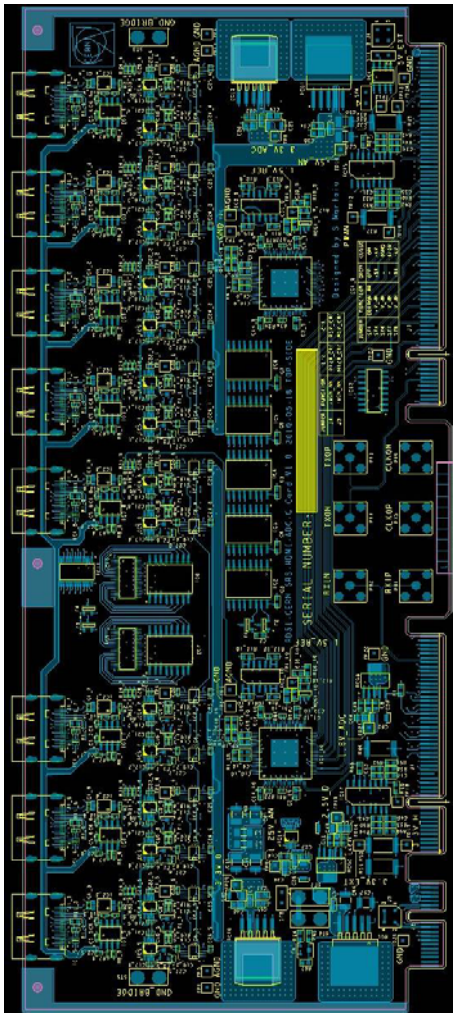
- Standard HDMI connector replaced by the mini version
  - Smaller footprint
  - Lower mechanical stress
  - More clearance for bonding

SRS



- 16 ADC channels
- Clock distribution
- Slow control distribution
- Monitoring

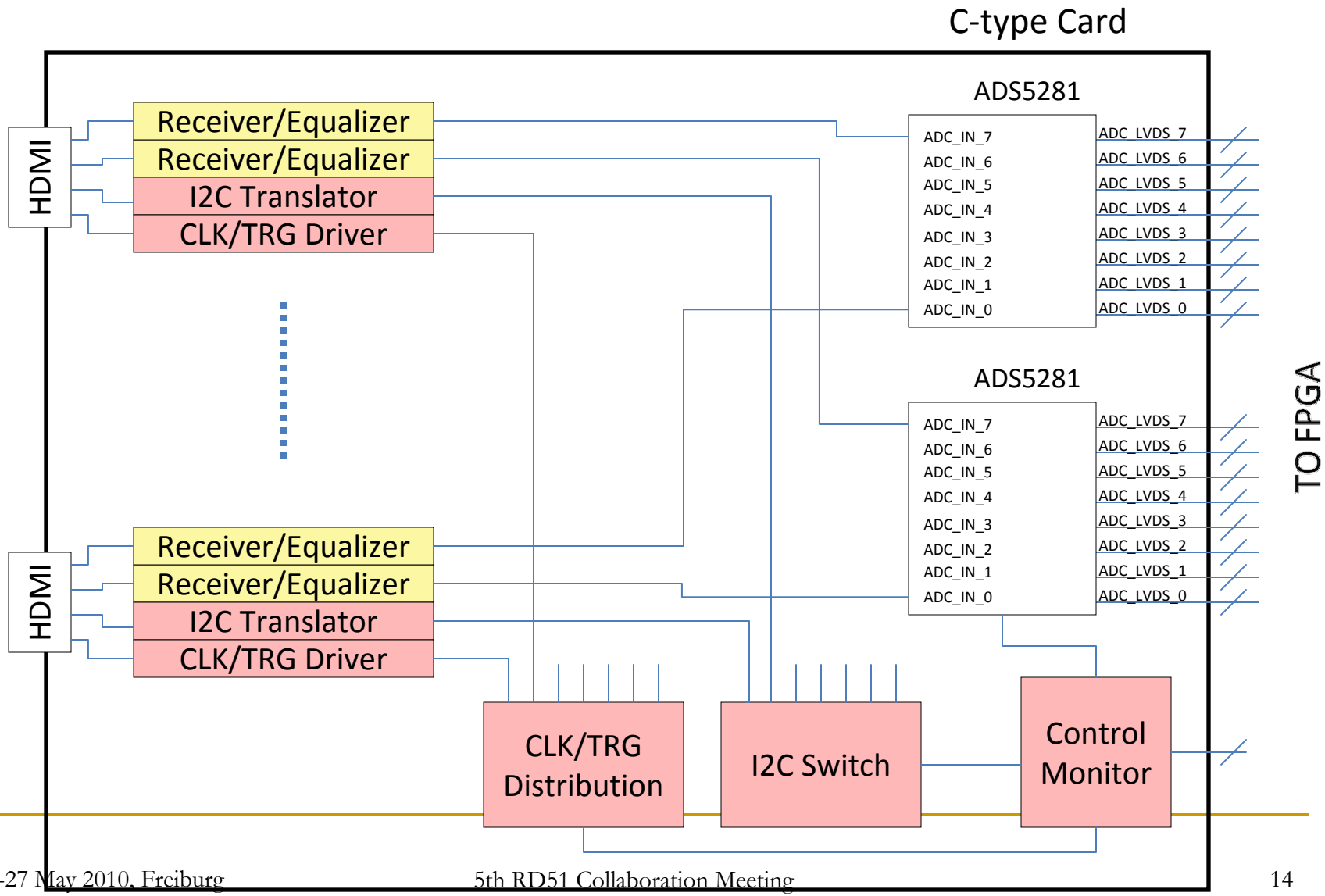
ADC C-Card Overview



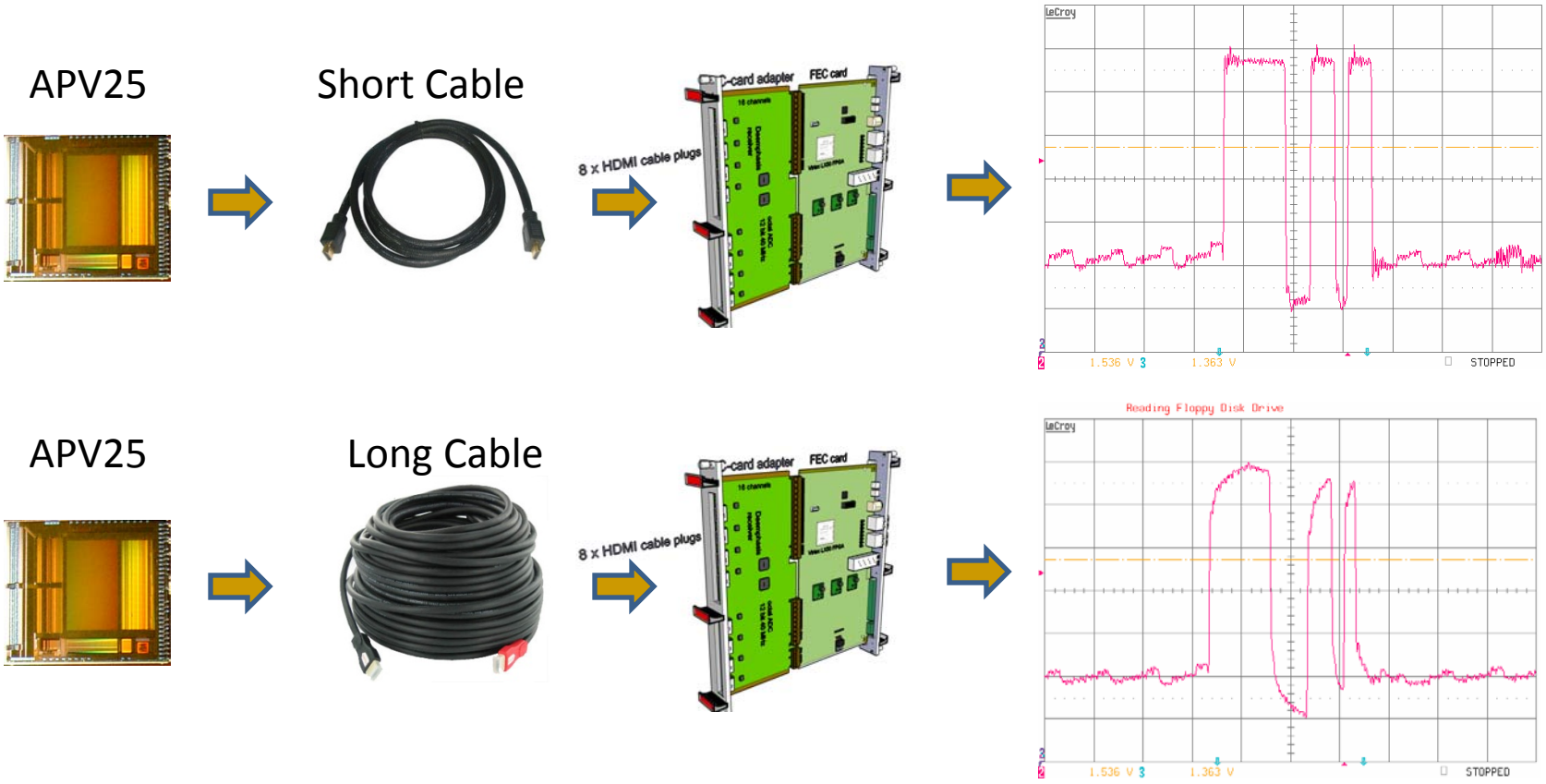
- 2 Octal ADCs with LVDS serial outputs (TI-ADS5281)
  - 16 Analog Inputs
  - 40MHz sampling
- Support for
  - 8 MASTER hybrids
  - 16 MASTER/SLAVE hybrids
- Power distribution
- Power/Temp monitoring

- Forward compatibility for future hybrids (Beetle,…)

Simplified Block Diagram

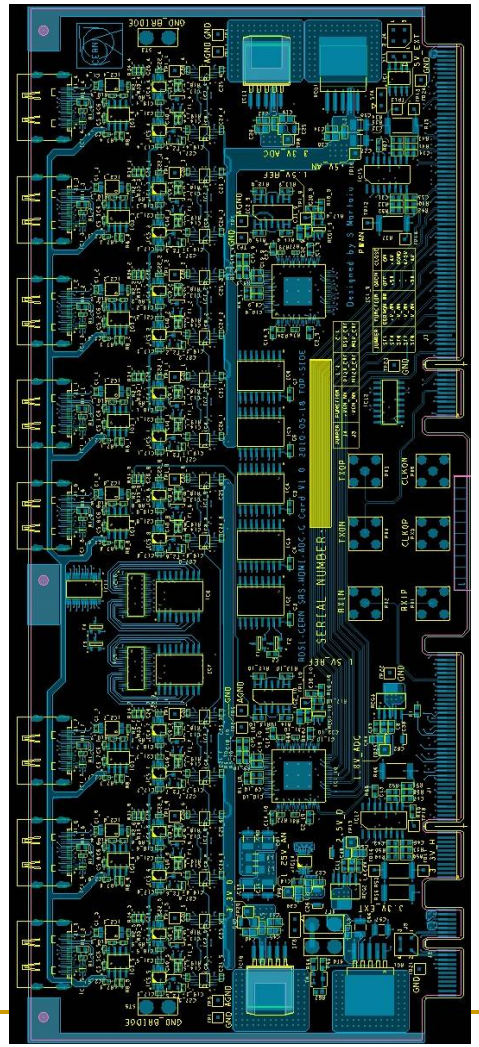


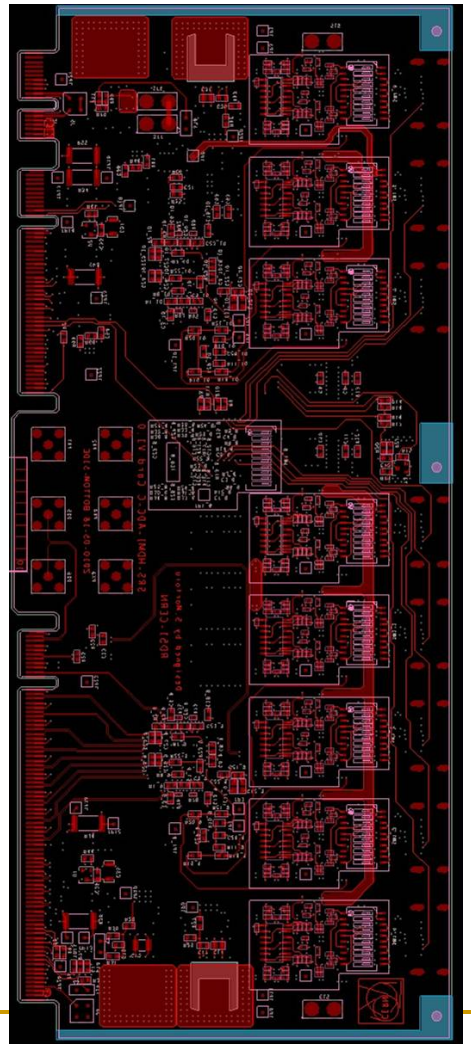
Input Equalization



- 4 equalization steps to accommodate cables up to 30 meters

ADC C-Card Status





- PCB design finalized
- 10 layers
- 1.6mm thickness
- controlled impedance
- ~ 1000 components

- Prototype production will start shortly

Conclusions

- First APV25 chip carriers were produced
- First results are very promising. Some results will be presented in next presentation
- PCB design of first digitizer C-Card finalized
- First prototypes foreseen in 4-5 weeks time