Ethernet-driven control and data acquisition scheme for the Timepix-based TPC readout

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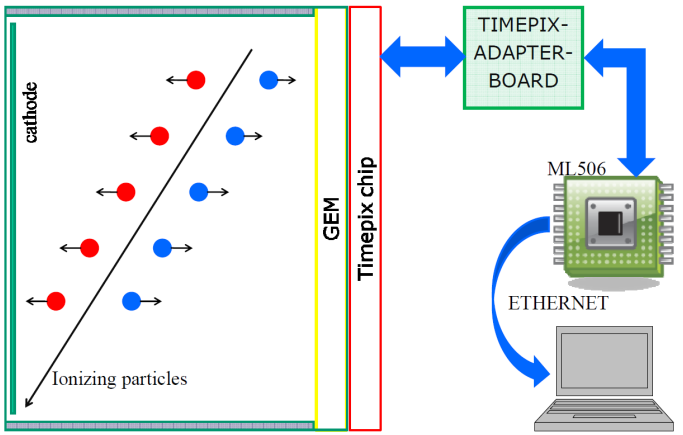
Overview

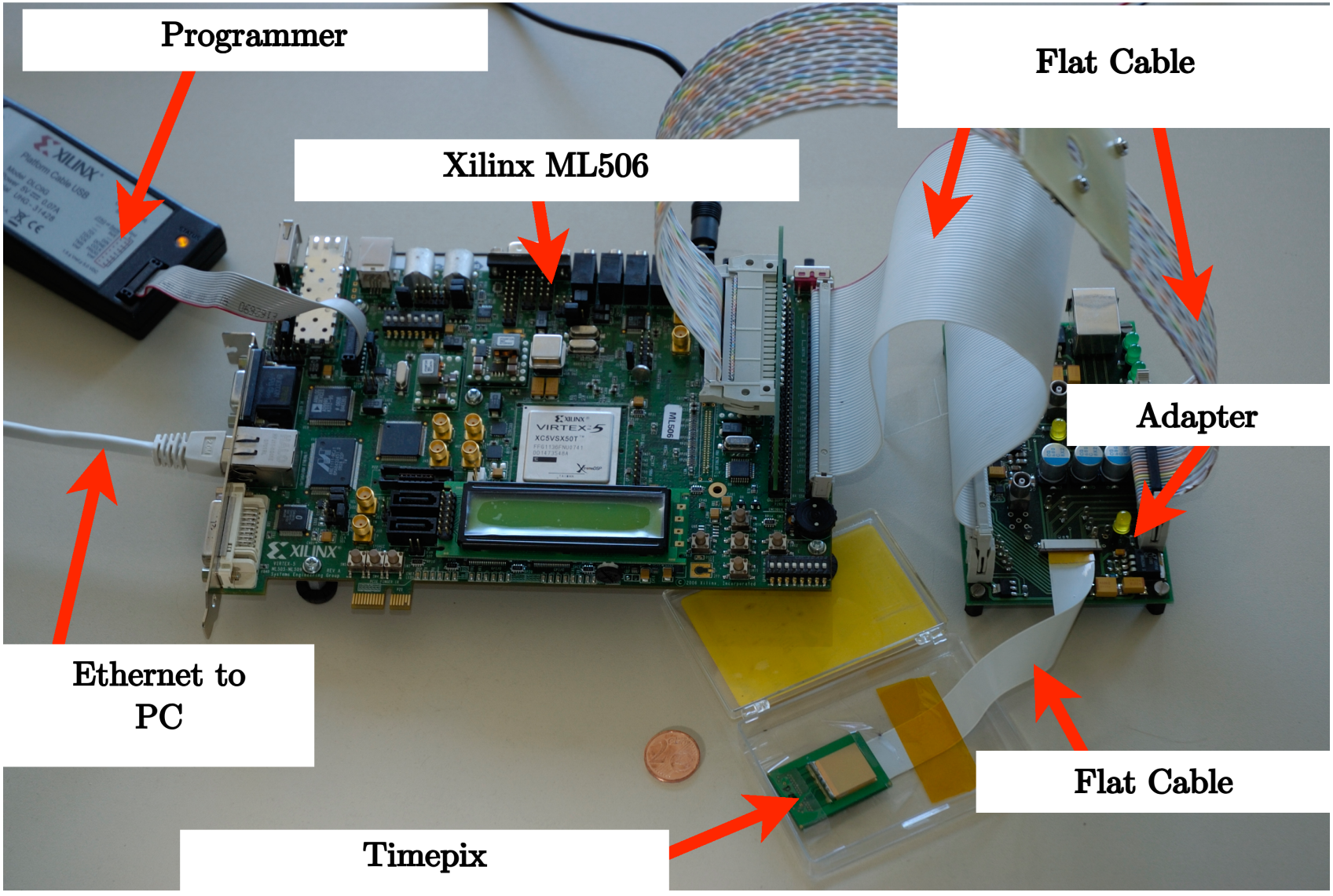
TPC Readout

TPC to be read out by one or several pixel sensors

- Timepix chip bonded on a FR4 carrier
  - TDC
    - Time Over Threshold
    - Common stop
  - Serialiser (LVDS link)
- Adapter board
  - Trigger, test pulse, voltage monitor
- Xilinx ML506 evaluation board
  - FPGA Virtex-5 (XC5VSX50-TFFG1136)
    - Deserialiser
    - Ethernet / IP packet engine (UDP)
  - Ethernet link to computer

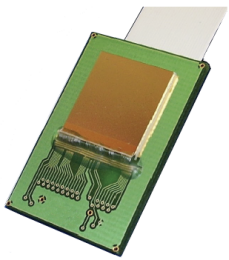


Lab test setup

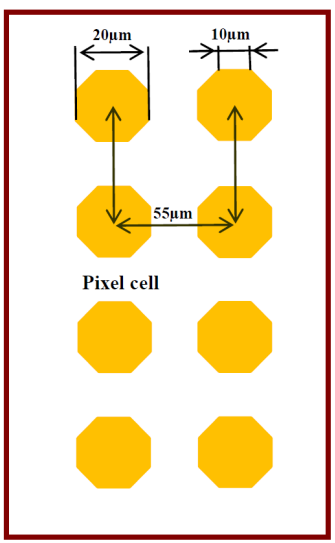


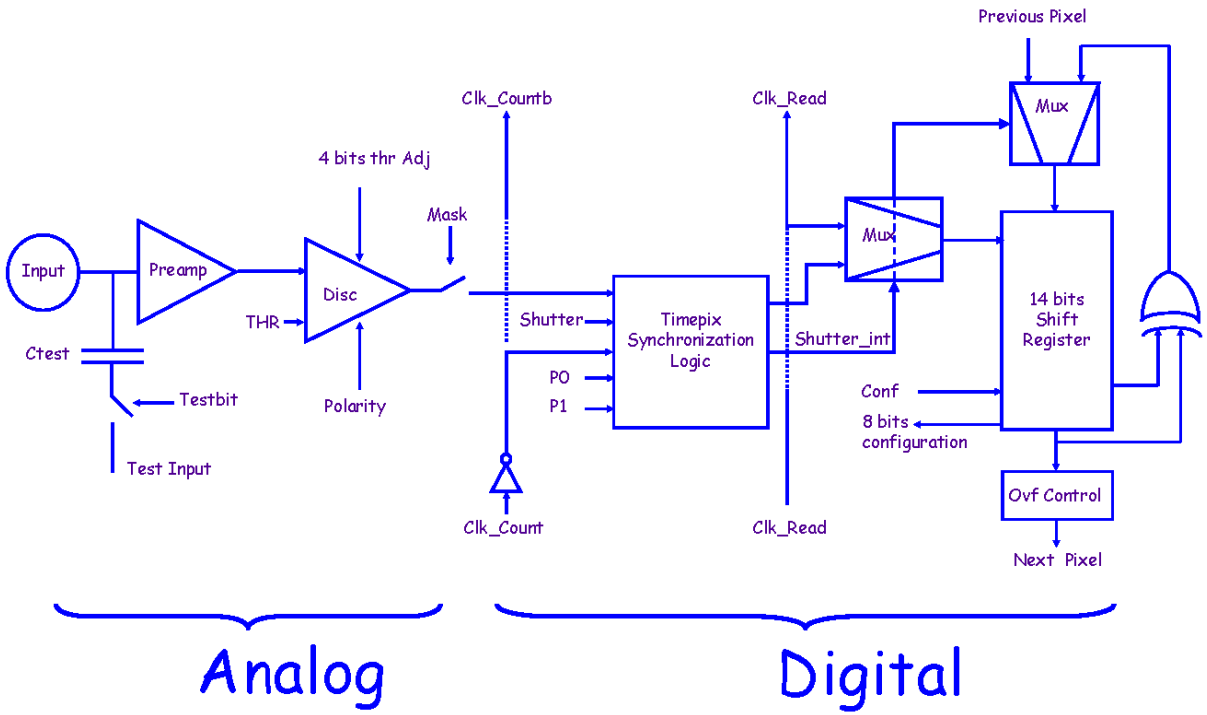
Timepix

- $256 \cdot 256$ channel matrix
- $55\mu m \cdot 55\mu m$ pitch
- Analogue input stage with per-pixel threshold adjust
- Digital TDC with 14-bit LFSR counters (max. 100MHz)
- Several conversion modes incl. TOT and common stop
- No zero suppression
- Serialisation of matrix data (1Mbit) into LVDS output
- Auxiliary controls:
  - Test pulse in
  - Diagnostics: analogue monitor for internal current sources (DAC_OUT)

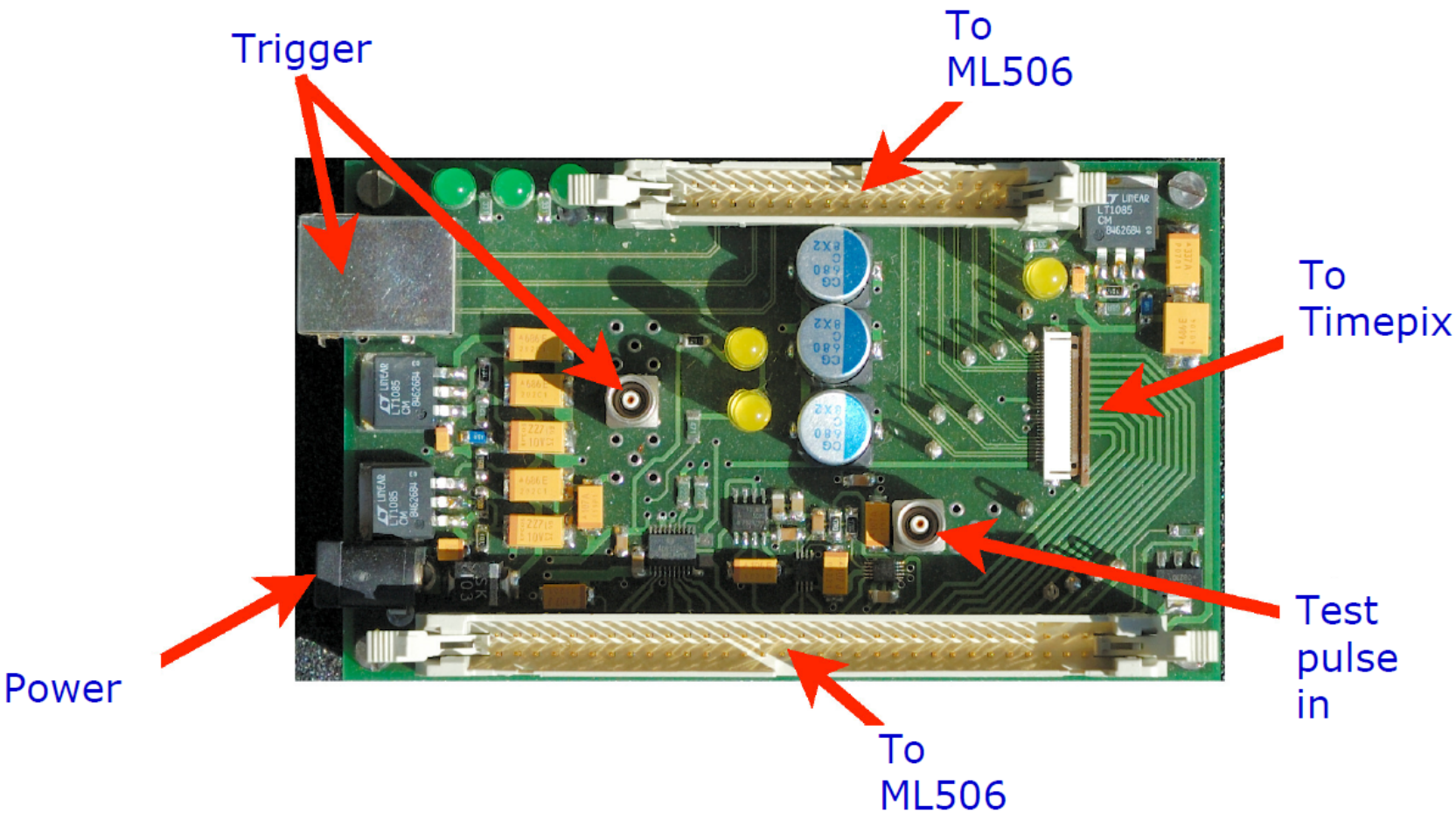


Timepix


20µm
10µm
55µm
Pixel cell


Previous Pixel
Clk_Countb
Clk_Read
4 bits thr Adj
Mask
Mux
Input
Preamp
Disc
Mux
14 bits
Shift
Register
THR
Shutter
Timepix
Synchronization
Logic
Shutter_int
Ctest
PO
P1
Conf
8 bits
configuration
Testbit
Polarity
Test Input
Ovf Control
Clk_Count
Clk_Read
Next Pixel
Analog
Digital

Adapter board



FPGA

FPGA module : Xilinx ML506 - Virtex-5 based

- On-chip Ethernet MAC and On-board Gigabit Ethernet phy chip (1000BASE-T)
  - No embedded CPU
- Firmware
  - VHDL description
  - Common clock for digitisation and data transfer, crystal based
  - SerDes interface to the Timepix bit-serial port
  - Timepix matrix data not buffered on FPGA, data kept on Timepix while awaiting packet transmission
  - Shutter operated under software control or in response to a trigger (TLU) with programmable delay and width
- Nonvolatile configuration storage via SystemACE (CompactFlash card)

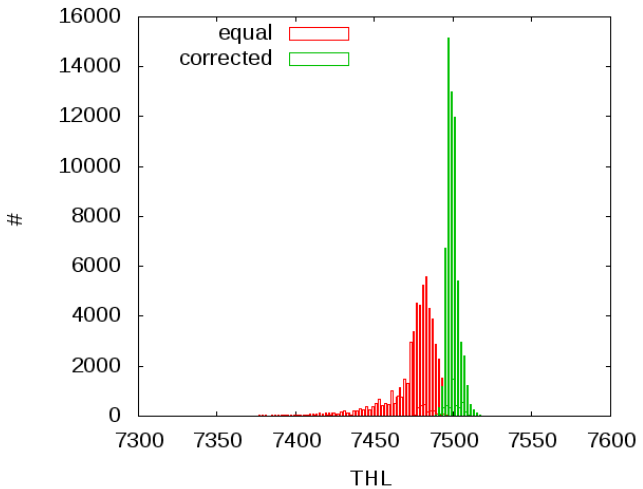
PC software

- C++ with Qt
- Command line interface, GUI currently in development
- Data pulled by computer (handshake)
- Minimalist network protocol stack
  - ⟨ethernet⟩⟨IP⟩⟨UDP⟩⟨control⟩⟨data⟩
  - No management protocols (ARP etc.)
- Functionality:
  - Basic operations: reset, setup (current sources, measure mode), operate shutter, readout, enable test pulse, choose trigger
  - Displaying the recorded data
  - Start a run : initialise matrix and read it out upon reception of a trigger, linearise data, write to file
    - Multithreading: Run control not disturbed by user-interface
  - Calibration: Threshold adjustment

Controlling: Threshold Adjustment

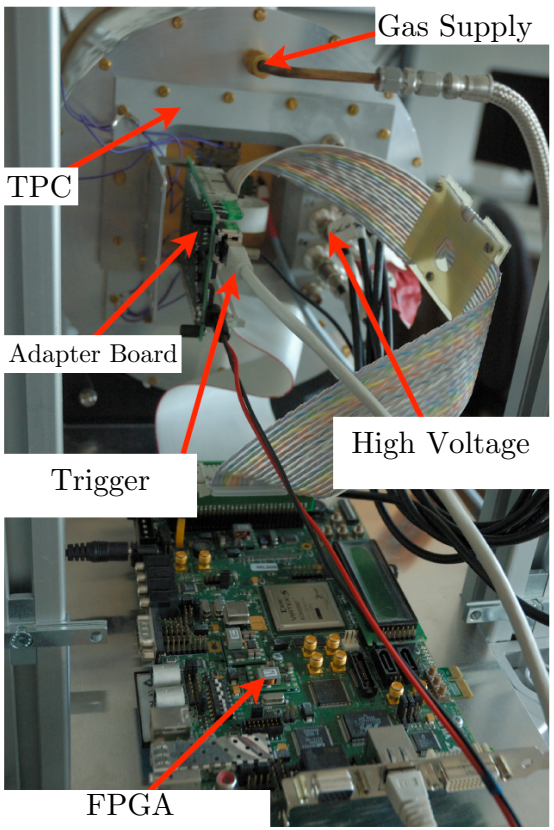
Intercalibrate all pixels so as to achieve a uniform noise level across the whole of the chip

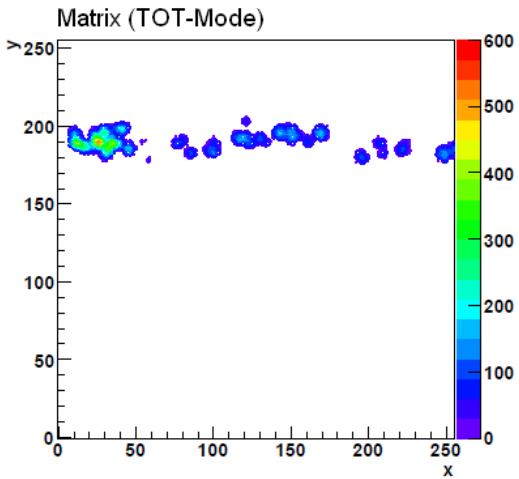
- Measure noise in TOT mode for a fixed period of time at a central correction level by varying the global threshold
- Find the minimal gain of the per-pixel correction: Increase the gain until extreme corrections are above/below the noise level
- Calculate the optimum per-pixel correction values out of the deviation of the pixel to the average

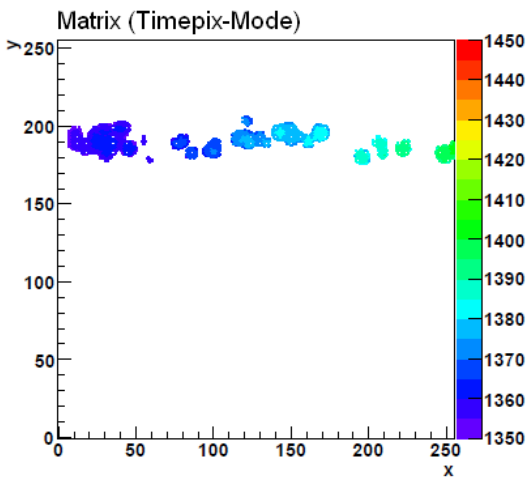


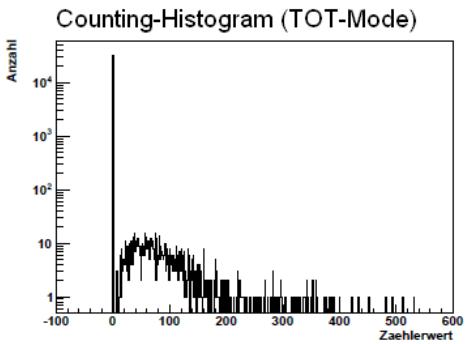
In the field...

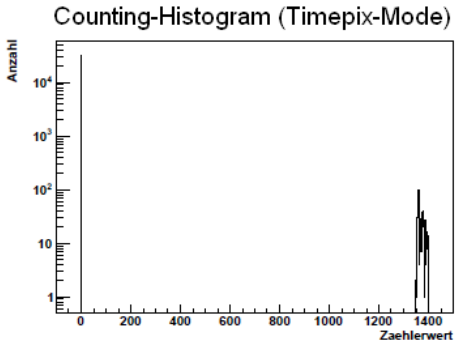
First *real* measurements at the TPC in Bonn (22.-24. July 2009)











Event rates up to 23Hz @ 40MHz system clock and 33Hz @ 100MHz
$\Rightarrow$ Improvement to the existing readout-system (MUROS2), but lower than expected

Acquisition rate

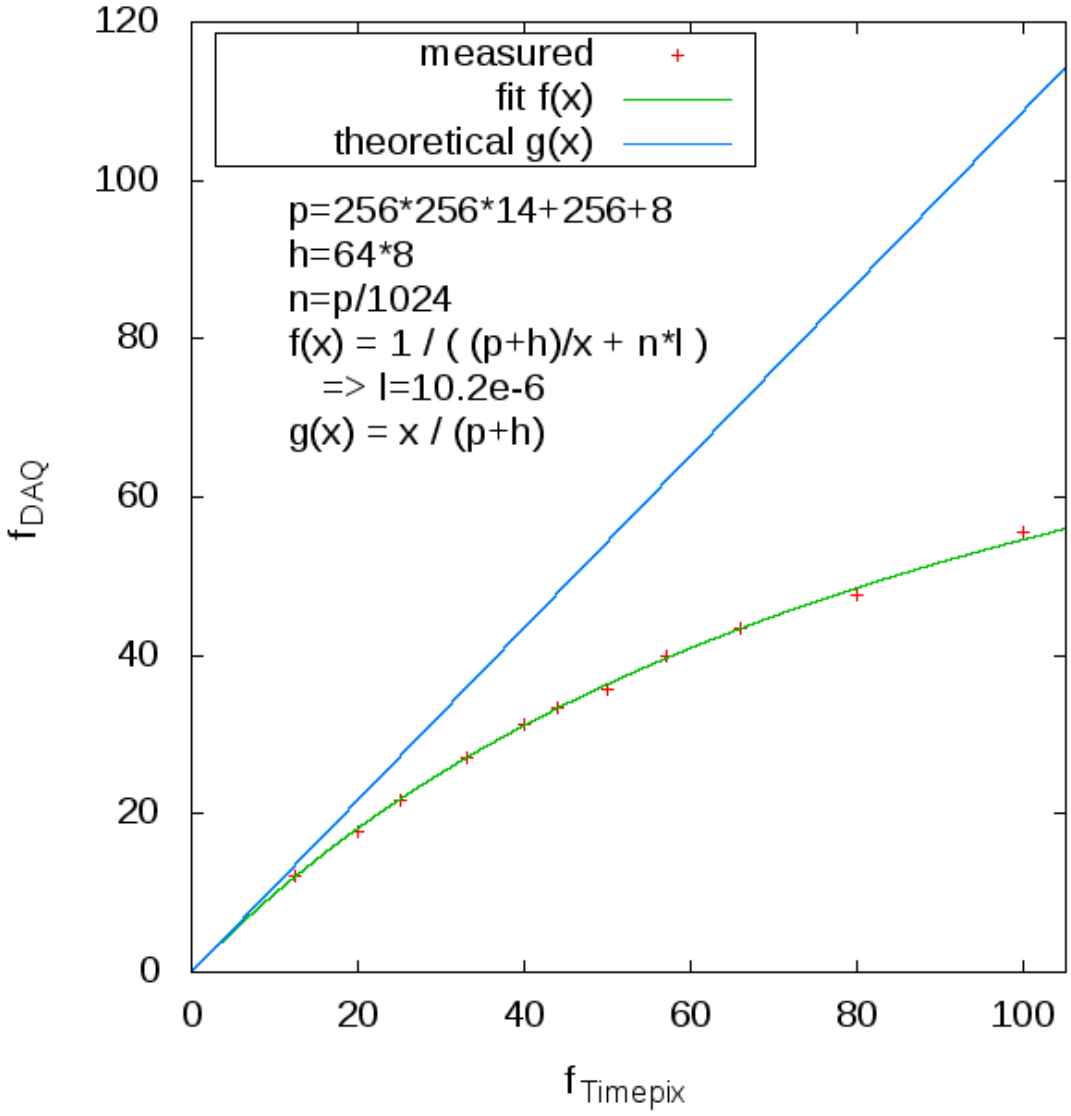
Readout only: $f_{DAQ} \approx 55{,}5\text{Hz}$ @ 100MHz

Raw data: $256 \cdot 256 \cdot 14$ bit $\approx$ 1Mbit $\Rightarrow$ Readout rate of bare Timepix would be (100Mbit/s) / 1Mbit = 100Hz.

- Data is pipelined through the FPGA without noticeable latency, the packet overhead is low
- FPGA currently polled by PC, i.e. handshake for each packet transmitted
  $\Rightarrow$ Bottleneck probably due to latency in Linux IP stack

$$\Rightarrow f_{\text{DAQ}} = \left(n \cdot \left(\frac{\text{payload} + \text{header}}{f_{\text{timepix}}} + \text{latency} \right) \right)^{-1}$$

f_{timepix}: operating frequency (variable 12.5 - 100 MHz)
n: number of packets


measured
fit f(x)
theoretical g(x)
p=256*256*14+256+8
h=64*8
n=p/1024
f(x) = 1 / ((p+h)/x + n*l)
=> l=10.2e-6
g(x) = x / (p+h)
f DAQ
f Timepix
0
20
40
60
80
100
120

Summary / Outlook

- A readout system for a TPC, with Timepix-based digitisation, has been implemented on a Xilinx ML506 development board (Virtex-5)
- Providing possibility of calibration
- System successfully operated in the electronics lab and on a TPC
- Readout rate currently up to 33 events per second
- Plans:
  - Improving the acquisition rate by decreasing the latency of the data transmission to PC (no handshake)
  - Re-target to Virtex-6
  - Increase channel count
  - Consider zero-suppression on the FPGA
  - ...