Spark effects on integrated circuits

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Outline

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Introduction

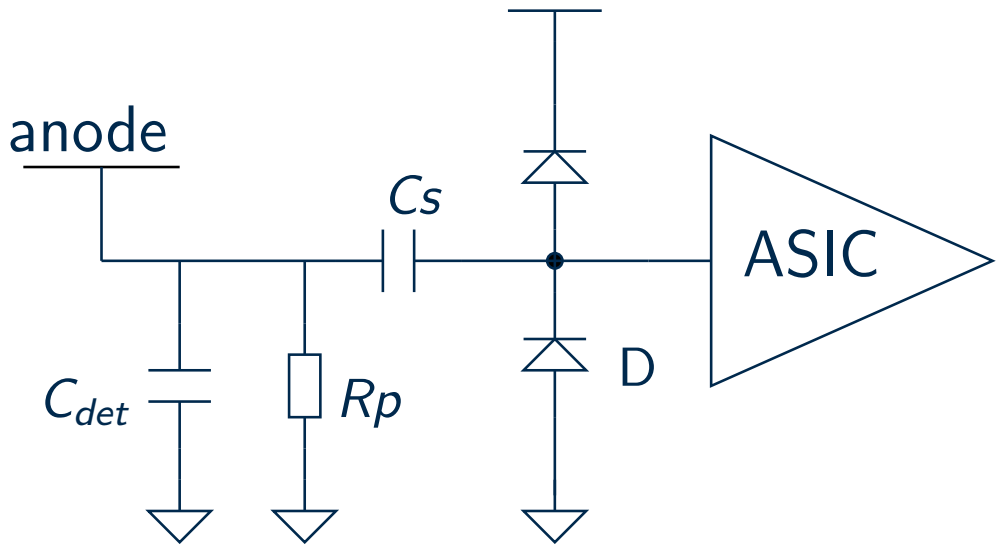
We use bulk MicroMegas of various size in testbeam with the following configuration:

- 6 cm×16 cm and 12 cm×32 cm with Gassiplex baord from SACLAY → no problem noticed;
- 8 cm×8 cm with Dirac 1 chip → no problem noticed;
- 8 cm×32 cm with Hardroc 1 chip → several dead chips, but seems from packaging issue;
- 8 cm×8 cm with Dirac 2 chip → all analog channels burns-out, digital still OK;
- 32 cm×48 cm with Hardroc 2 chip → 2 kinds of problems, analog or digital;

All channels of all detectors use the same protection network.

Present protection network

Schematic, from SACLAY Gassiplex board:



D: BAV99W or BAV99S

C: Yageo ref. CA0612JRNPO9BN471 (0612, ±5%, NPO, 50 V, 471 pF, 4 GΩ)

Rp: Yageo ref. YC164-FR-071ML (±1%, 100 V, 1 MΩ)

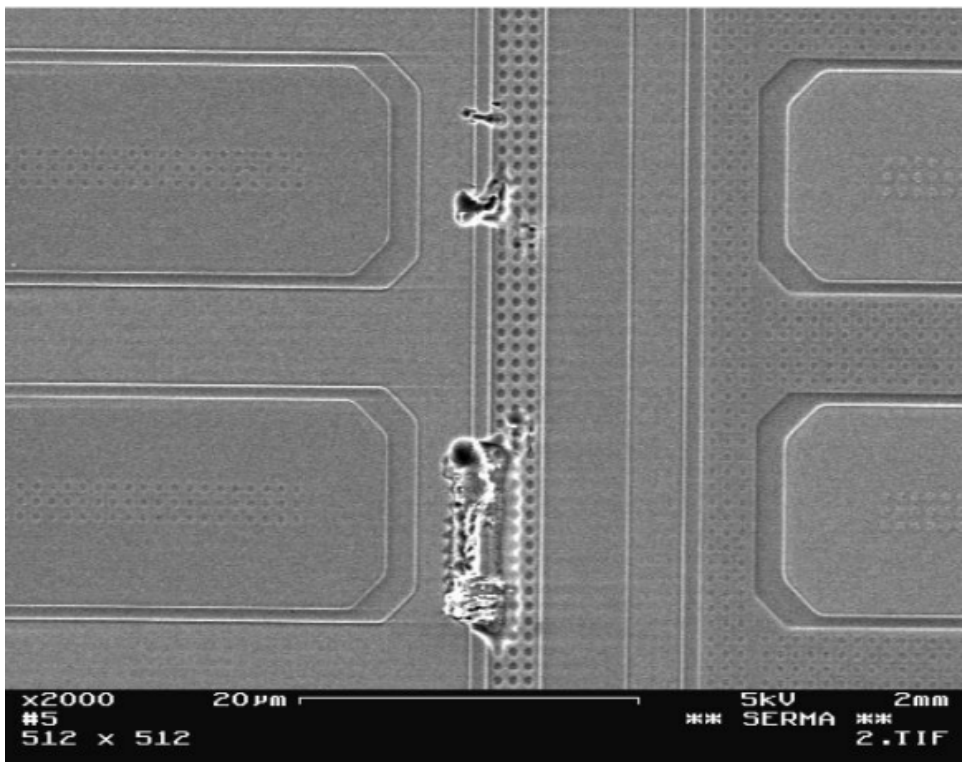
C_{det}: 80 pF (pad/mesh + pad/power planes, measured)

Outline

Encountered problems

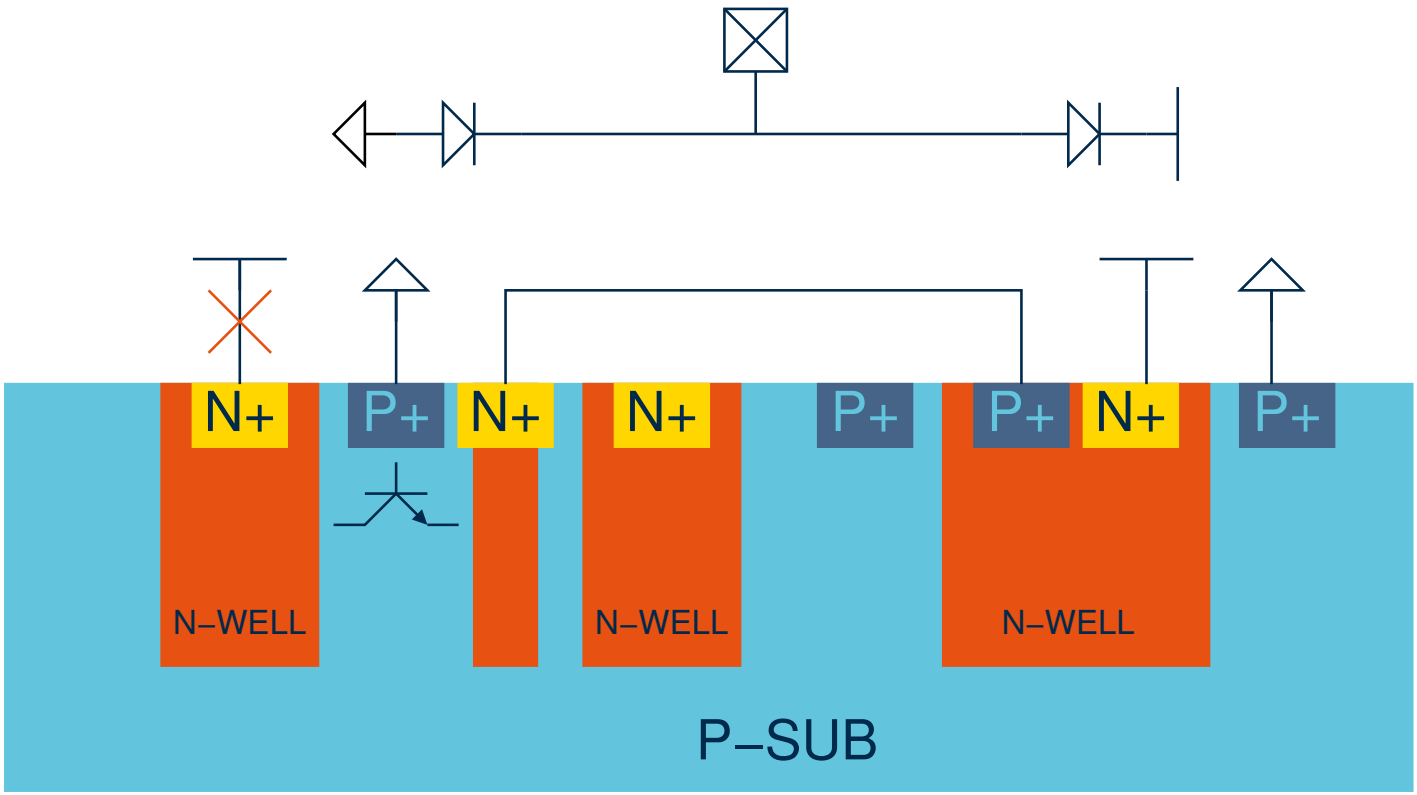
Two kinds of uncorellated problems:

- All analog front-end input have clamped to vdd (discussed here);
- All digital part died (still under investigation).



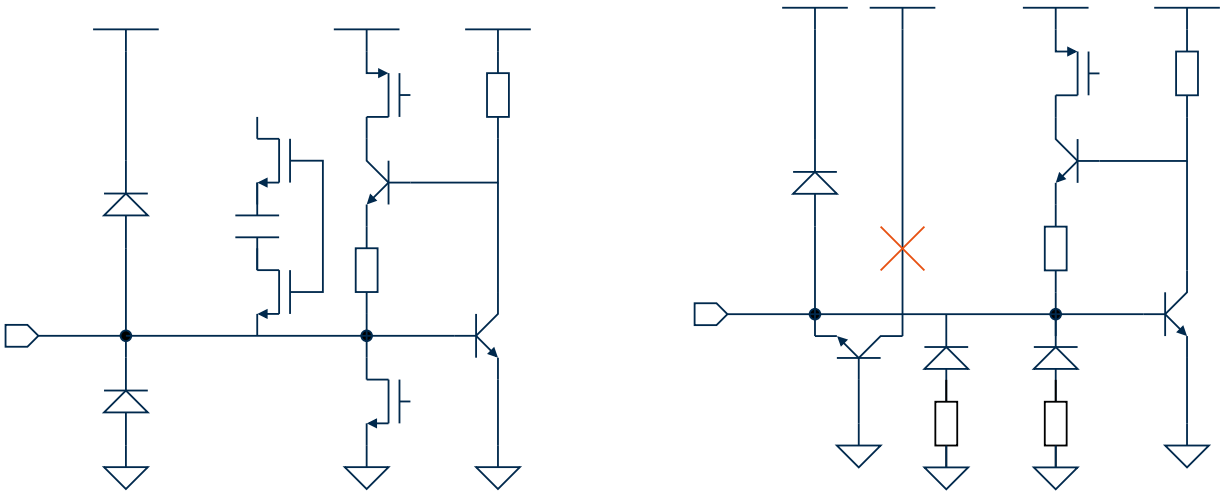
Si cut

The guardring of the subdiode forms a parasitic NPN bipolar transistor. This transistor enter in conduction with a gain proportional to the distance between guardring one negative input pulse. The drawn current destroy the contact, not designed to whistand high current.



Equivalent schematic

Left: input stage schematic
Right: equivalent schematic from Si point of view



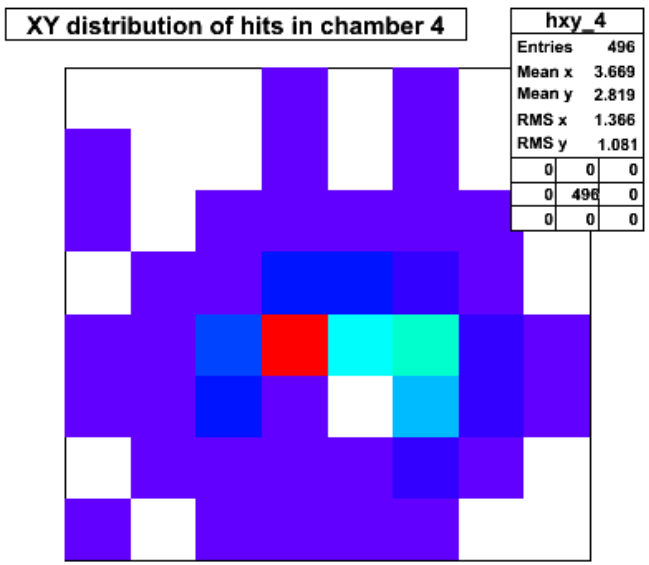
Solutions:

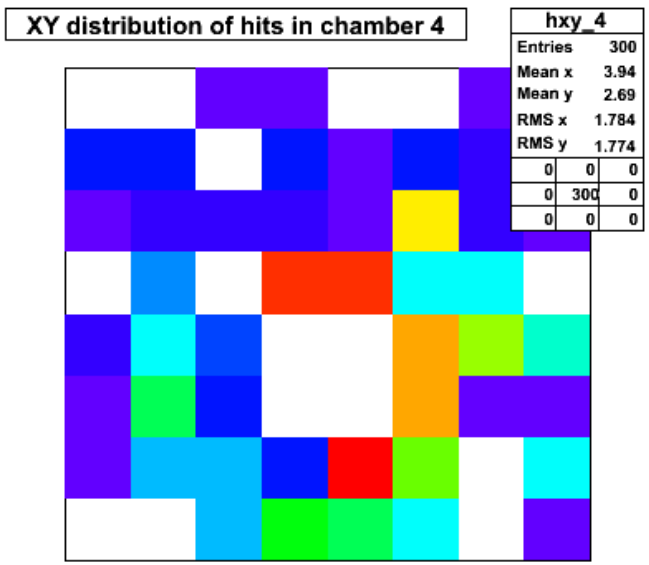
- Increase the distance between guardring and N+ diffusion (10 µm instead of 5 µm);
- Remove the guardring;
- Connect the guardring to vdd (no risk of latchup in this structure);
- Completely redesign the diode.

Outline

Encountered problems

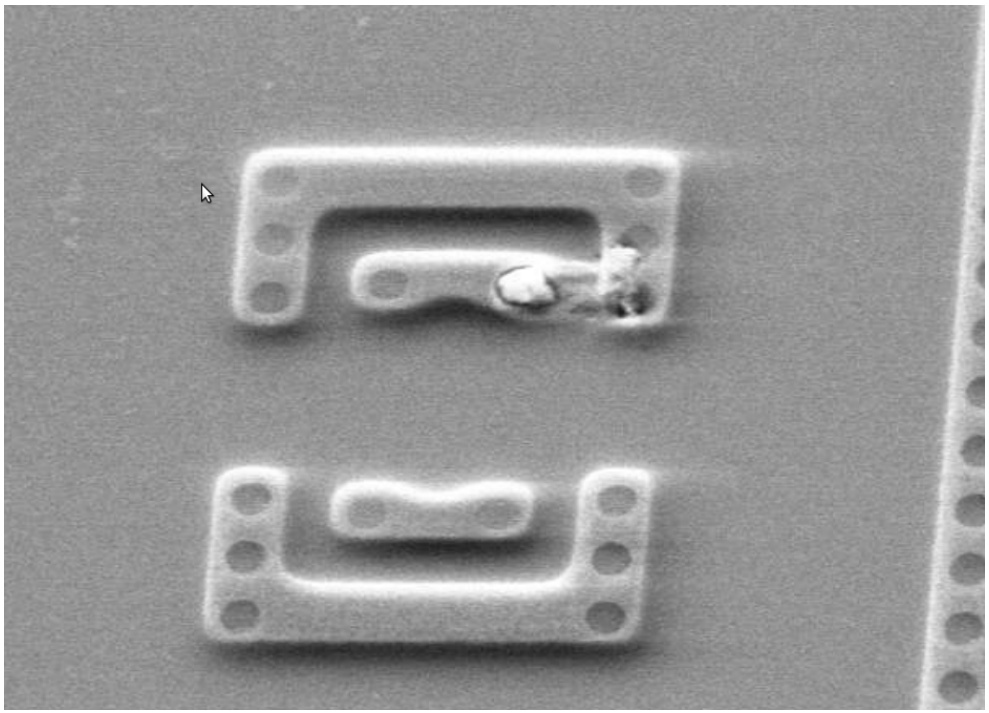
Operating condition: same I/O pad as Hardroc, but mesh is smaller. All channels in beam died slowly, but digital readout is still operational.

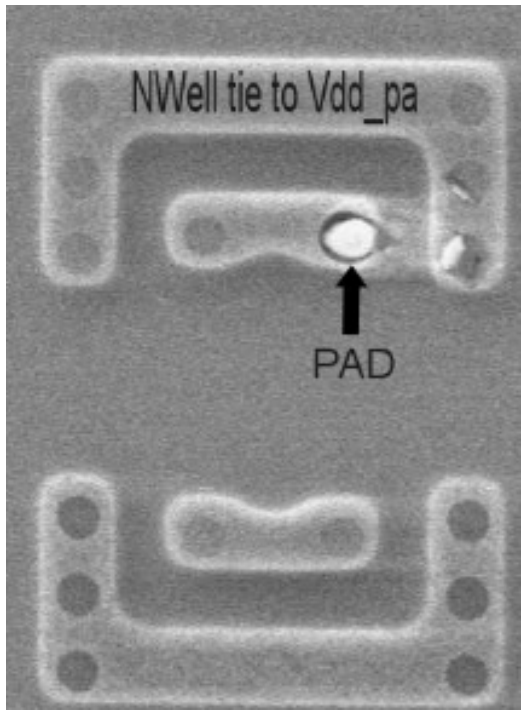




What happened?

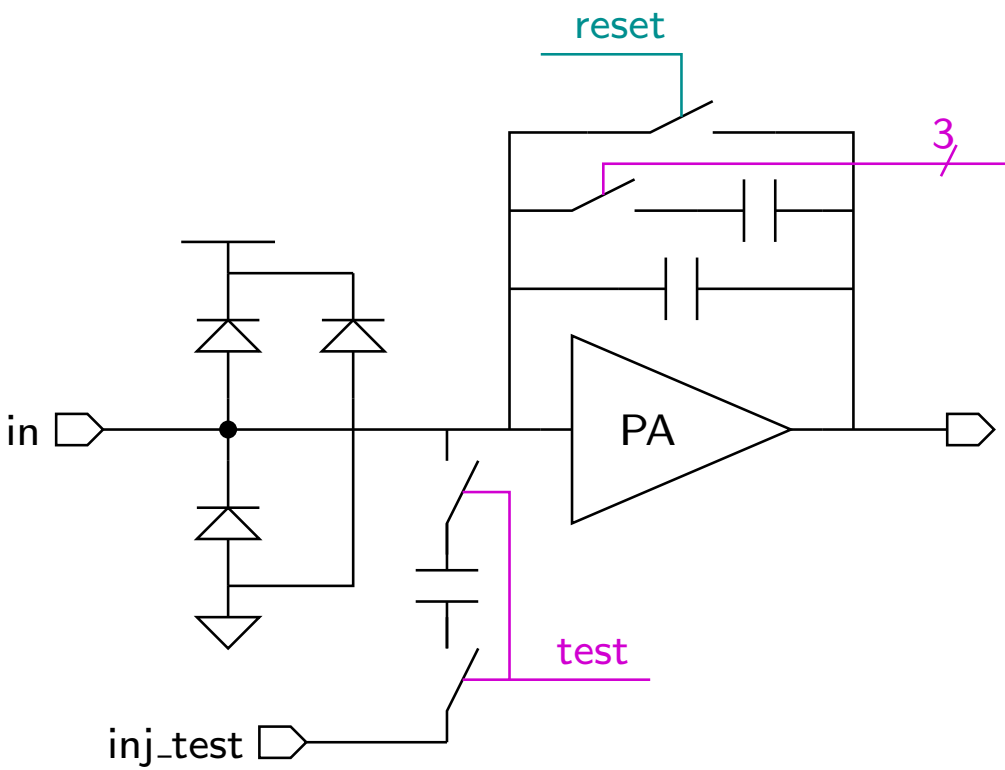
A contact between input and NWell in short circuit! No defect in IO clamping diodes.

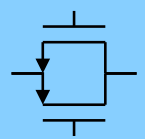




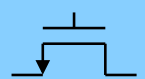
Schematic

The damaged structure is the reset switch of the charge preamplifier.





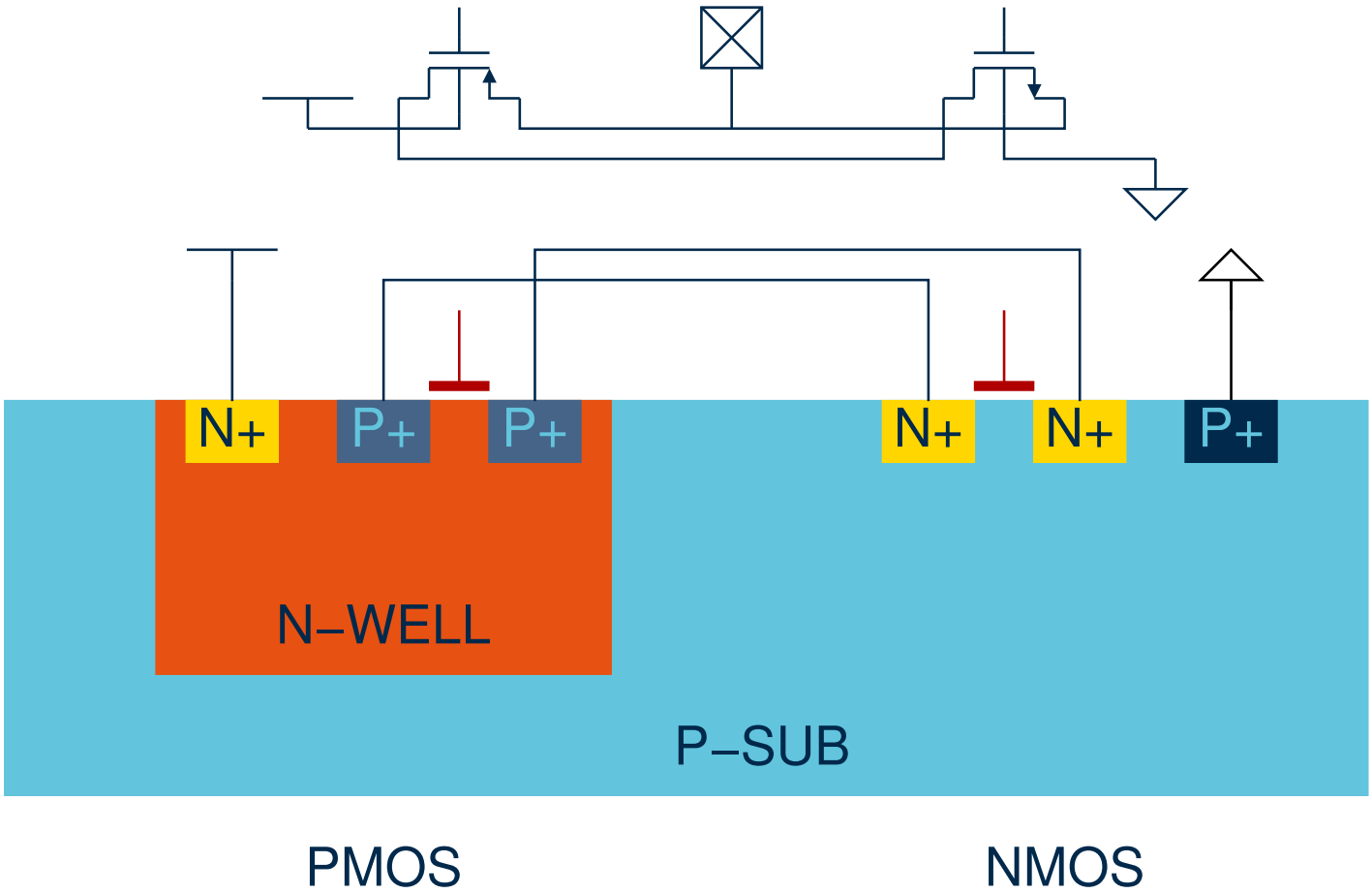
reset switch
is made of
complementary MOS



static switches
are made of
N-type MOS only

Si cut

The CMOS complementary swwitch:



Failure analysis

Analysis:

- Direct junction polarisation due to positive sparks;
- Reverse voltage of junction (9 V) has been reached due to poor NPN parsitic transistor.

Solution:

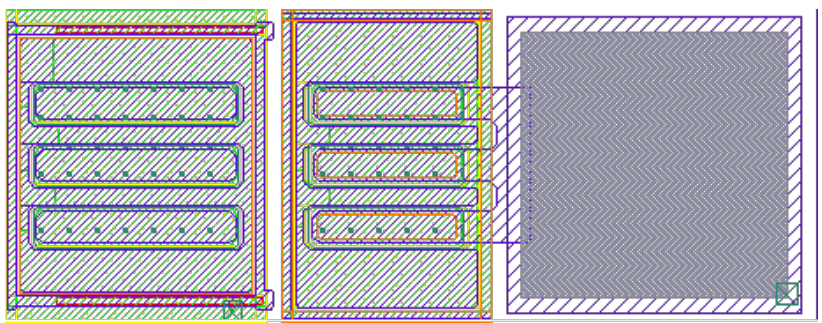
- Increase the distance for the guardring of the transistor;
- Add a serial resistors for guardring polarisation;
- Improve clamping diode.

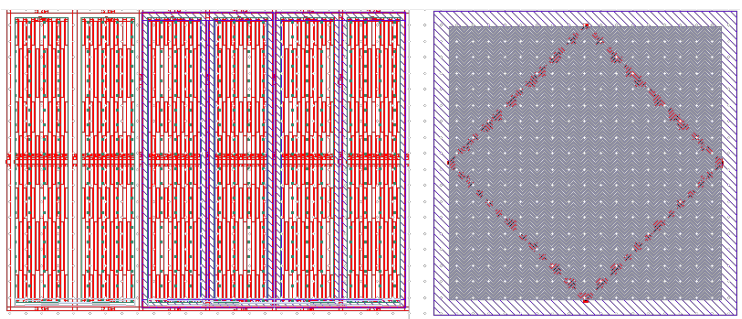
Outline

Basic design rules

To avoid the weakness of AMS analog I/O pads from library, a custom pad with clamping diode is currently designed for our next generation of readout chip (MICROROC, in coll. with LAL).

- Remove all active devices from input path, especially PMOS;
- Increase NWell to NWell distance above DRC ($\times 2$ or $\times 3$);
- Use minimum distance between N+ and P+ for clamping diode;
- Minimize access resistance of power supply, ground, I/O.





Conclusion

We have understand most ASIC existing weaknesses.
A new ASIC will be submitted with the new diode design in june, in 0.35 µm AMS CMOS.
Another specific chip with several clamping diodes designs will be submitted in september.