Status of the "Scalable Readout System" S. R. S.

for the RD51 collaboration
and LHC detector upgrade

Collaboration meeting Freiburg Mai 24-27, 2010

RD51, Working Group 5
=>Electronics and Readout systems for RD51

http://rd51-public.web.cern.ch/RD51-Public/Activities/WG5.html

Convenors:

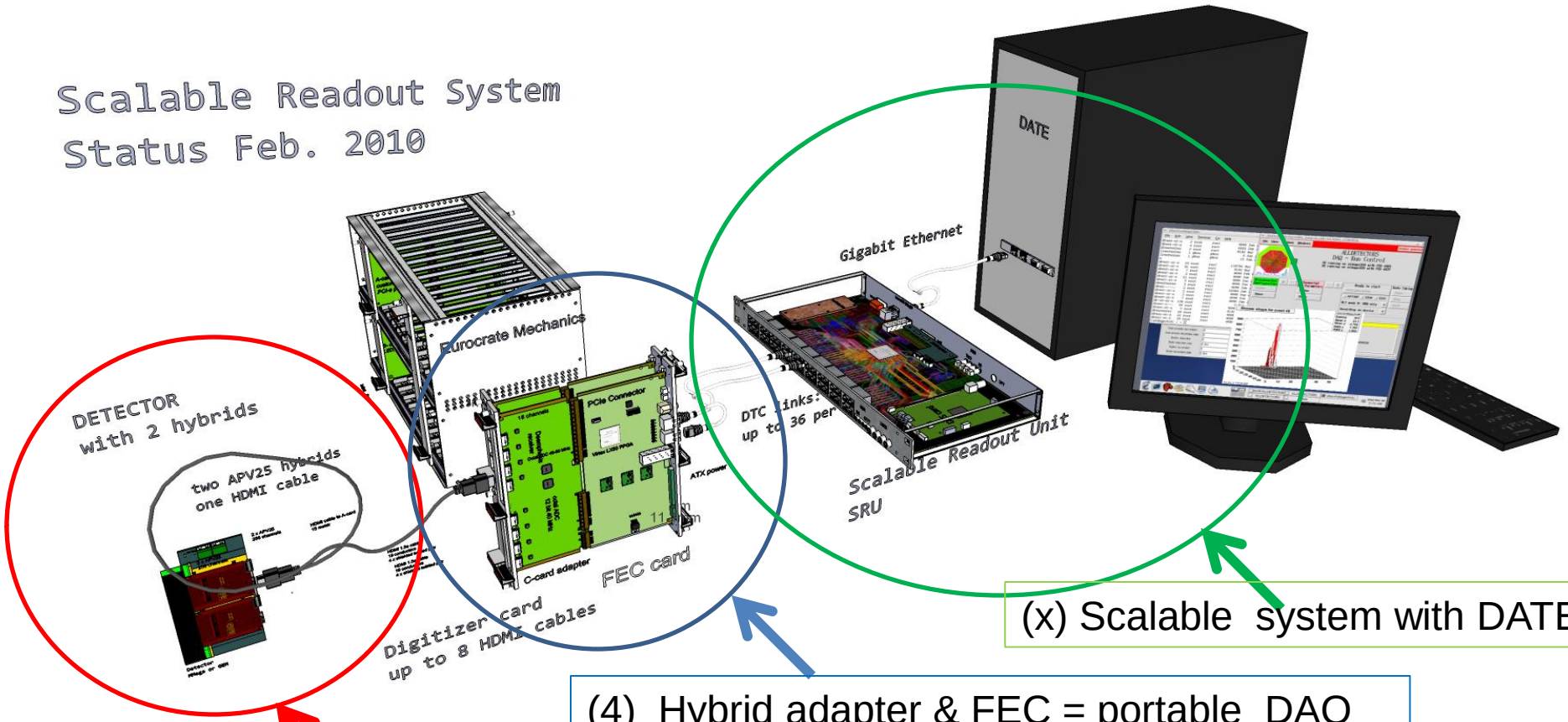
Hans Muller, Jochen Kaminski

1. Definition of front end electronics requirements for MPGDs
2. Development of general purpose pixel chip for active anode readout
3. Development of large area detectors with pixel readout
4. Development of portable multichannel data acquisition systems for detector studies;
5. Discharge protection strategies.

This talk:

1 -4-5: development of a portable and scalable multichannel data acquisition system, named Scalable Readout System (SRS) with discharge-protected chip-carriers (hybrids) . Scalability is an additional feature

physical overview SRS of RD51



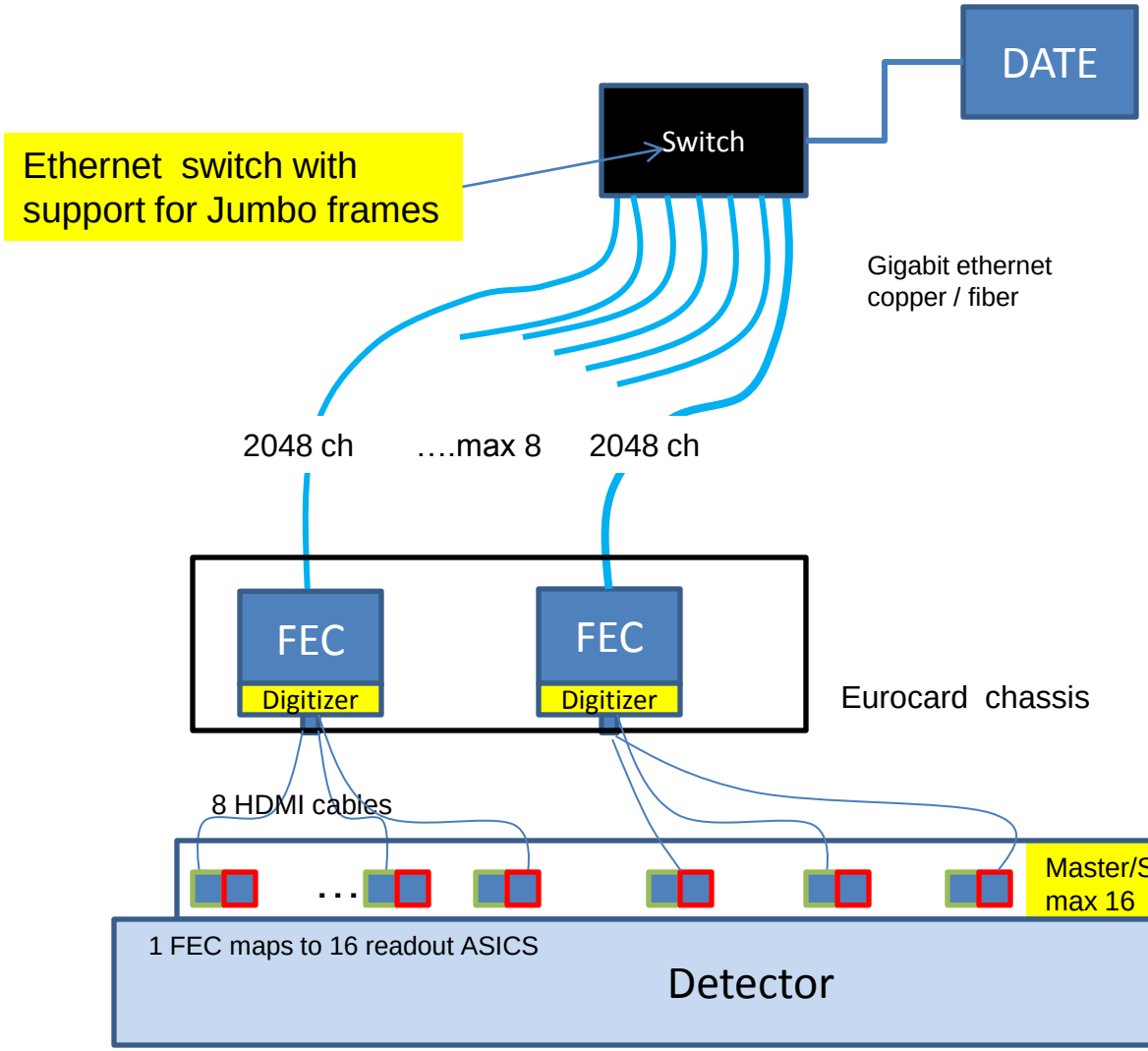
(x) Scalable system with DATE

(4) Hybrid adapter & FEC = portable DAQ

(1-5)Hybrids: user –specific front end electronics with discharge protection

Small systems*

Scale up to 16 k Channels, no SRU needed, Gigabit switch connects up to 8 FEC cards in a Eurocrate



Recommended Server PC for DATE:

CPU a 8 core

processor : 0 1 2 3 4 5 6 7
vendor_id : GenuineIntel
cpu family : 6
model : 23
model name : Intel(R) Xeon(R) CPU E5405 @ 2.00GHz
stepping : 10
cpu MHz : 2000.038
cache size : 6144 KB
physical id : 0
cpu cores : 4

bogomips : 4003.34
clflush size : 64

HDD 160 GB

3 slot PCI-X
3 slot PCIe

RAM 4 GB

Mother board
http://www.supermicro.com/products/motherboard/Xeon1333/5000P/X7DBE.cfm

* 1 Eurocrate chassis:
assume 8 FEC cards
connected via 1 octal switch to DATE
Each FEE serves 16 chips of 128 ch
=> 163854 channels

Frontend electronics

for 6Ux 220 mm Euro-Chassis

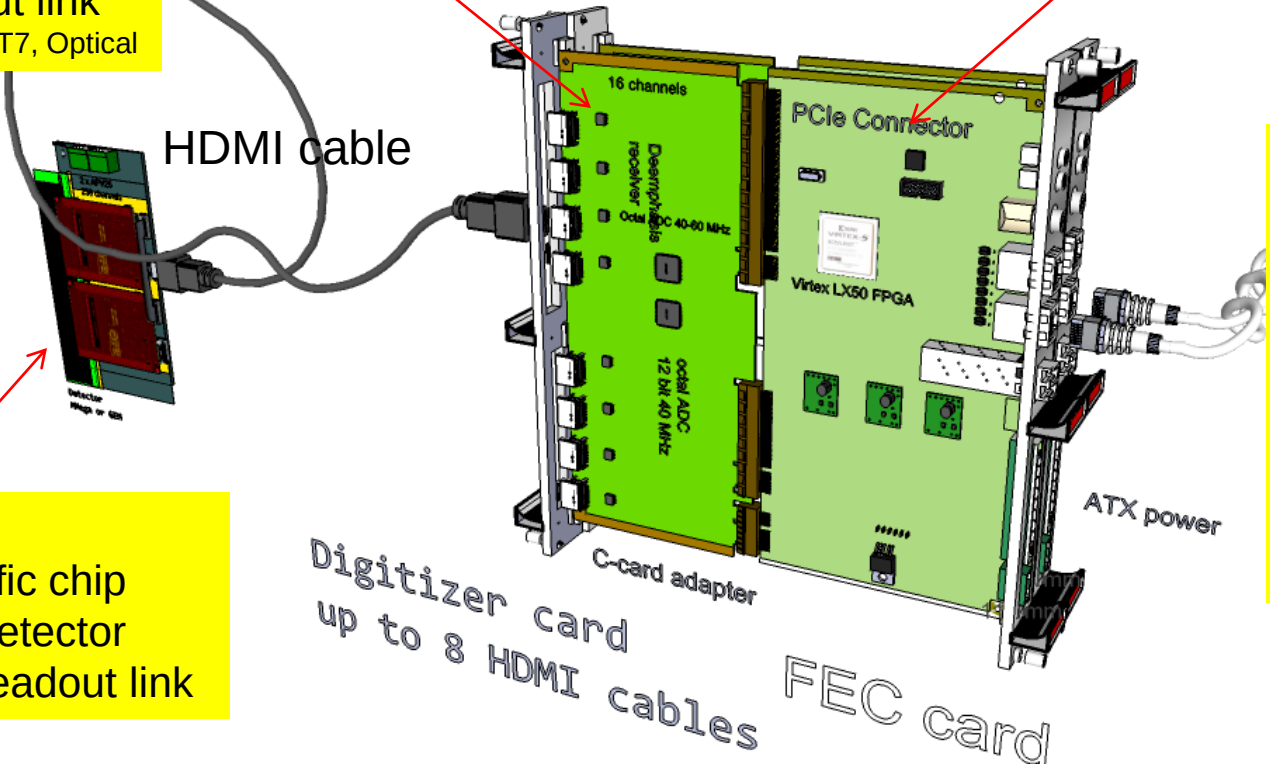
Adapter Card (C format shown)
Matches with chip carrier type
->analogue chips: digitizer card
->digital chips: event buffer card
->photodetectors: amplifiers/shaper/ADC

Programmable Frontend Card (FEC)
-Xilinx-V5 based with interface to Adapter Card –
-Gigabit Ethernet and DTC link

Chip-readout link
(HDMI, RJ45/CAT7, Optical

HDMI cable

chip carrier
on detector



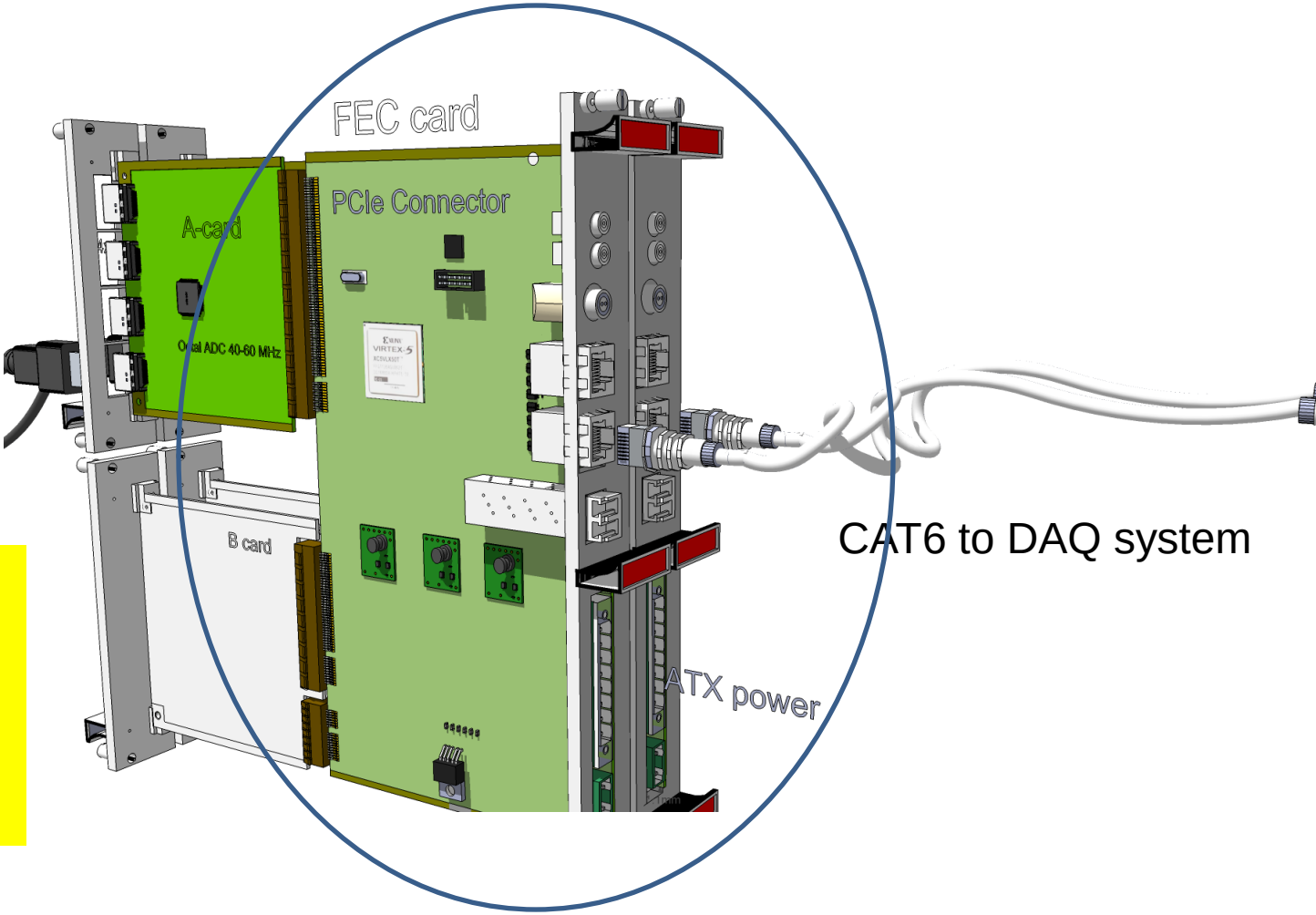
Chip carrier:
-detector specific chip
-plugs on the detector
-interfaces to readout link

either
DTC link
- Data
-Trigger
-Control
-➔ SRU

or
ETHERNET
➔ DAQ computer

FEC card for SRS

designed by U.P.V. Valencia



other A,B or C cards are under design:

CDTC16 LVDS Rx/Tx Buffer for Si-PMs (NEXT collab.)

Digitizer Card for BNL chip (Atlas MMega)

FEC Card production and test in Valencia

- 6 PCBs arrived on 22nd April (manufactured in Lab-Circuits, Barcelona)
- 3 FECs mounted by Uvax-Concepts, Valencia. Received on 13th May
- Electrical and functional tests to be carried out during May/June
- After tests are successful we'll produce a second batch (June/July?)

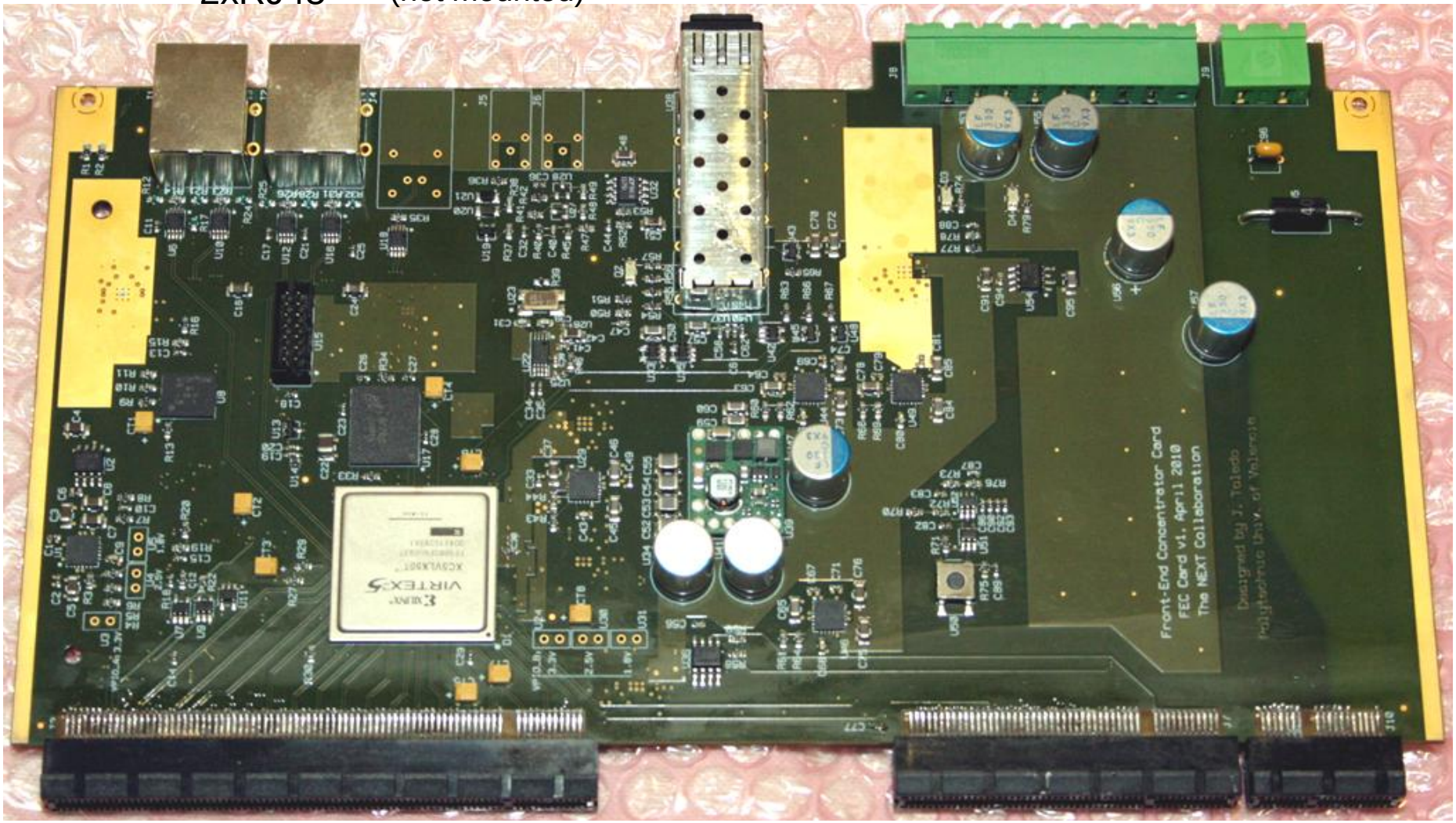
2xRJ45

LEMO I/O
(not mounted)

SFP socket

Power conn.

Bias conn.



A-Card connector

B-Card connectors

FEC firmware

- Manpower in Valencia: 2 engineers + 1 student
- SRU interface provided by Wuhan University
- GbE code exists and has been tested
- Common firmware modules to be written before summer:
  - DDR2 interface (student)
  - FPGA System Monitor (student)
  - I2C interface (engineer 1, work in progress)
  - Main Control (engineer 2)
- Application-specific modules to be written:
  - All A-Card, B-Card and C-Card interfaces (?)
  - First code to be written in Valencia: APV25/Beetle ADC C-Card (engineer 2, work is advanced)
- Basic FEC test firmware in May

Costing FEC card

So far No cost figures received

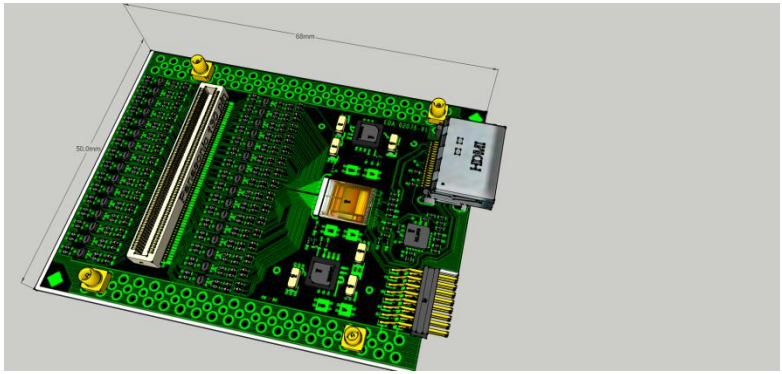
Ad interim: assume 1000 Eu
2048 channels

Estimated cost: (0.448 Eu/ch)

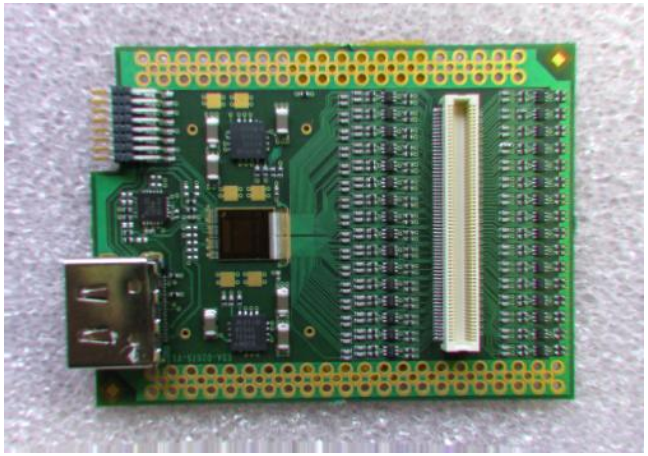
APV-25 hybrid

(see talk S. Martoiu)

Design Started Jan. 2010
Layout and Proto production
by CERN DEM



Bonded Hybrid April 2010



First hybrid, APV25 with HDMI interface

Next hybrid: Beetle? V-FAT, N-Xyter?
RD51 community to decide

<u>Mai 2010: under discussion:</u>
Industrial R&D collaboration with Spanish Industry (CRISA) on design of future hybrids

APV chip bonding

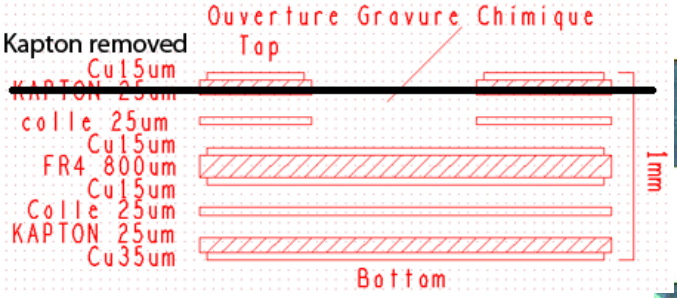
no chip carrier

SIGNAL bonding

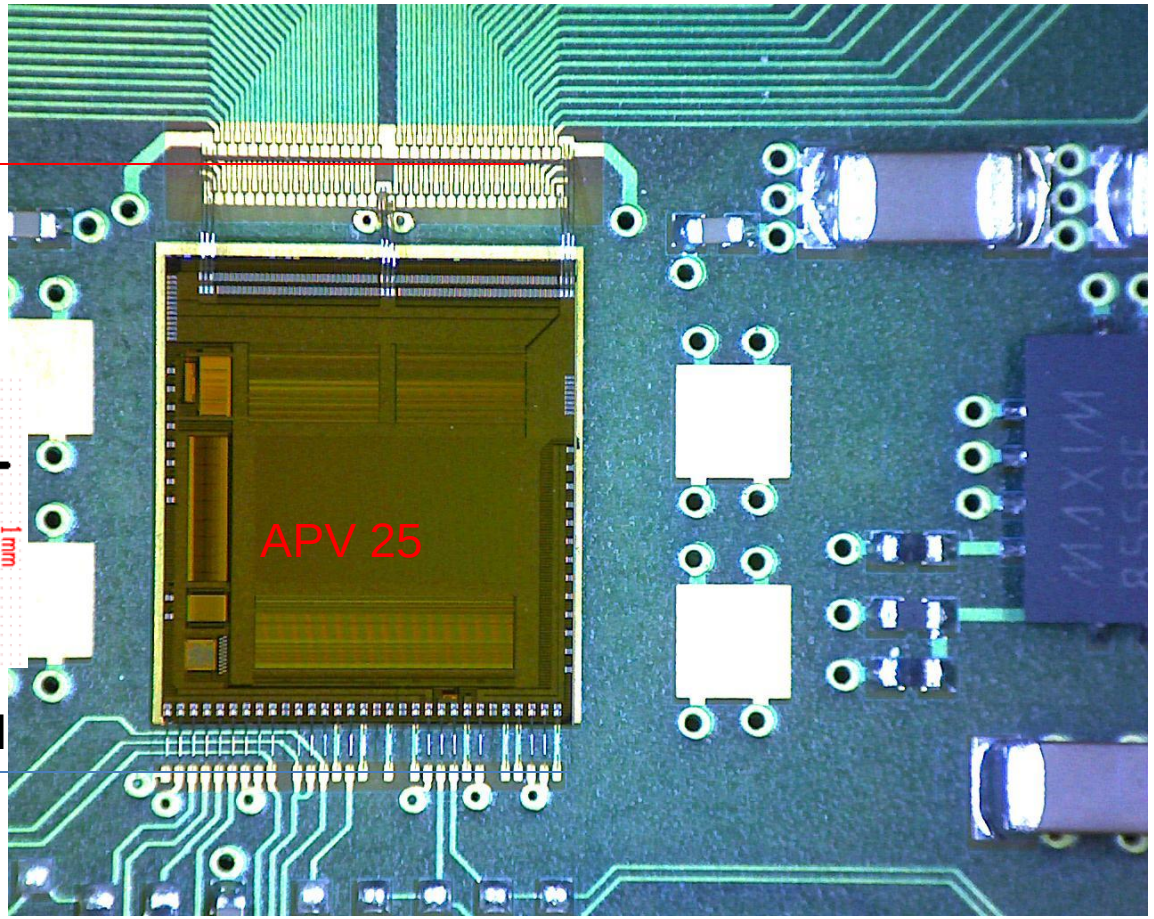
64 pads from surface

64 pads from below
+ power / GND

Stackup:

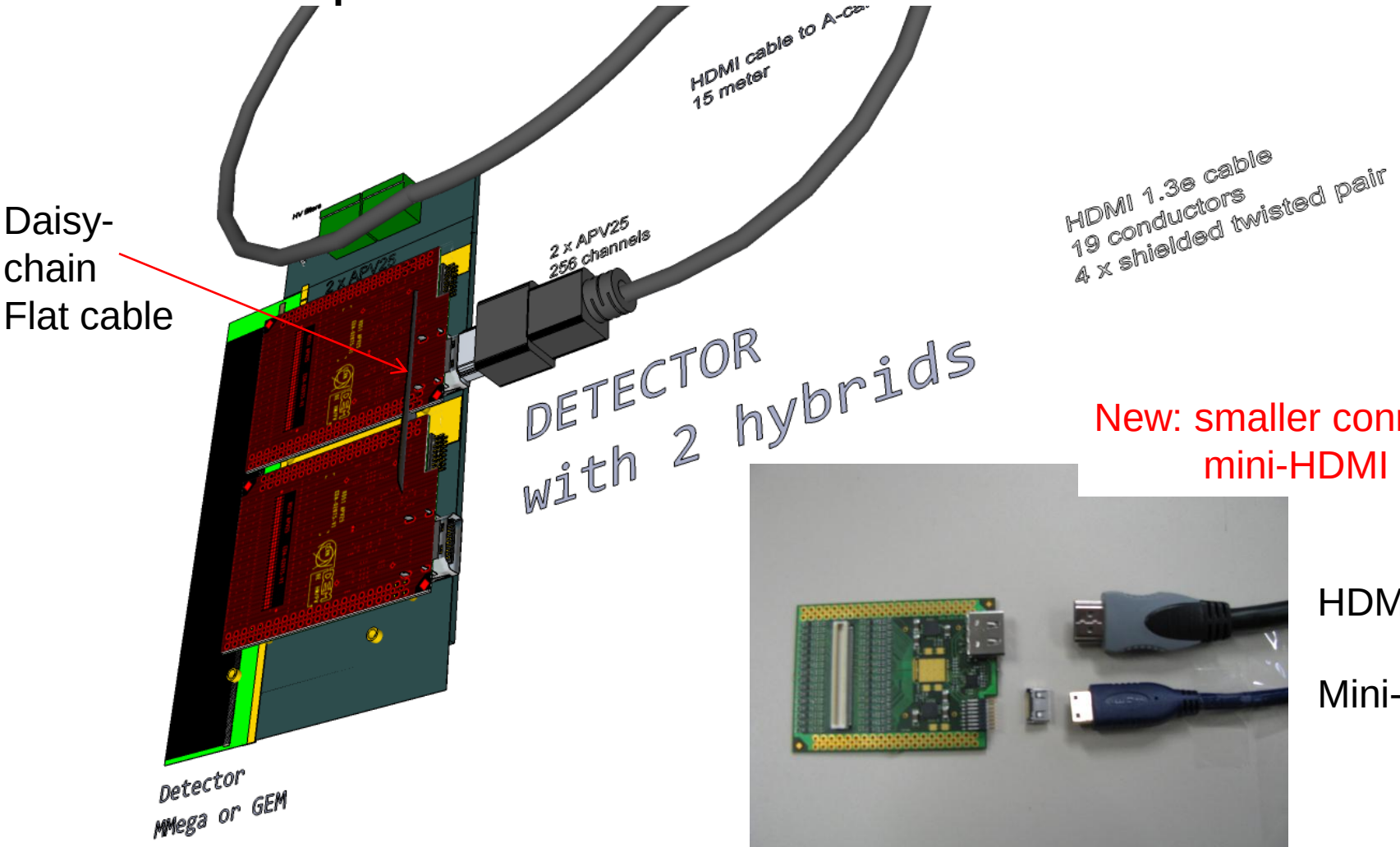


28 pads R/O & control



Chip carriers

up to 30 m remote from FEC crate



New: smaller connector mini-HDMI

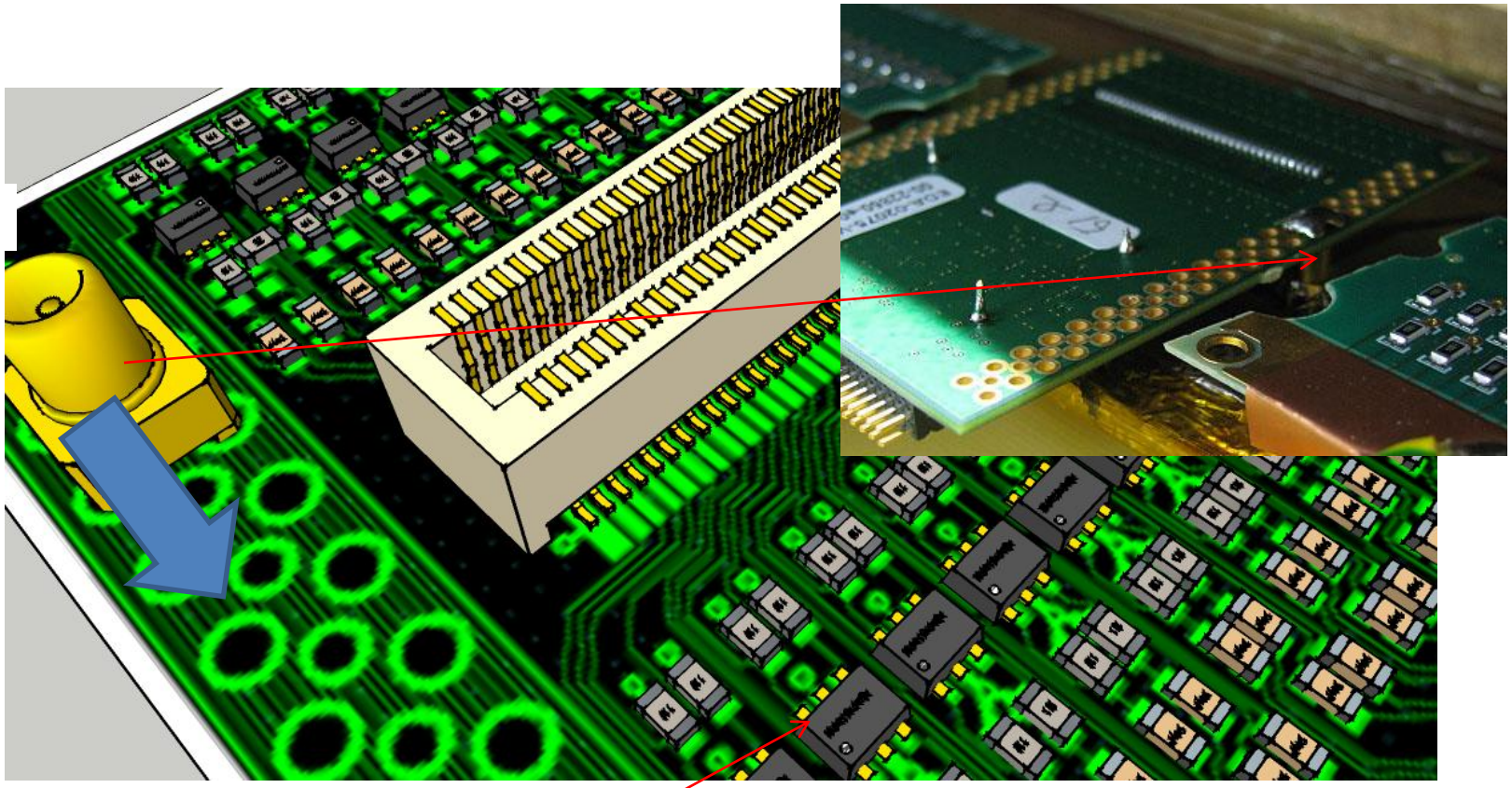
HDMI

Mini-HDMI

Connectivity, GND, AC-DC-coupling

Click&GND

MMCX can be placed every 2.5 mm

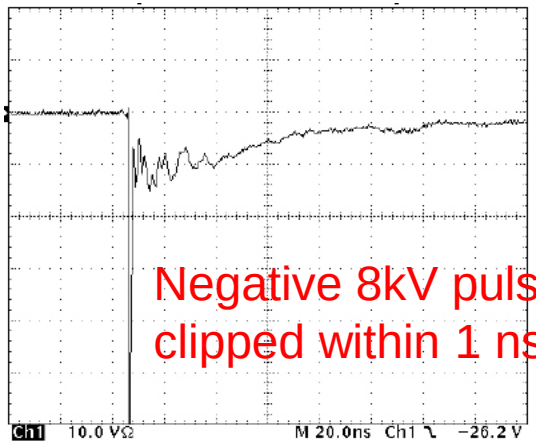


Quad ESD diode arrays , 10 A , 1 pF 0402 resistors & capacitors

For DC coupling place 0-OHM resistors instead of capacitors

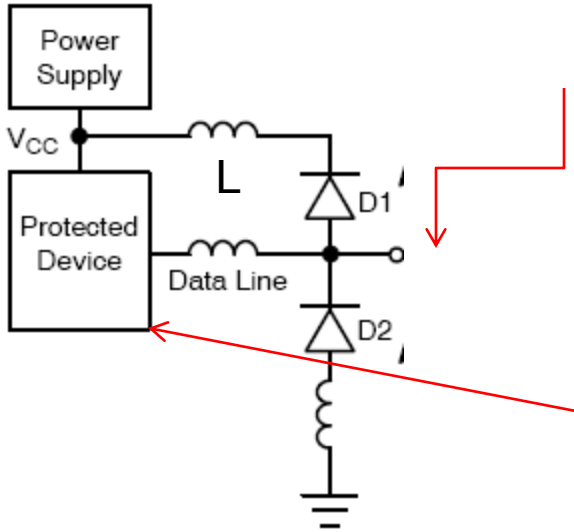
Sparc protection on hybrid

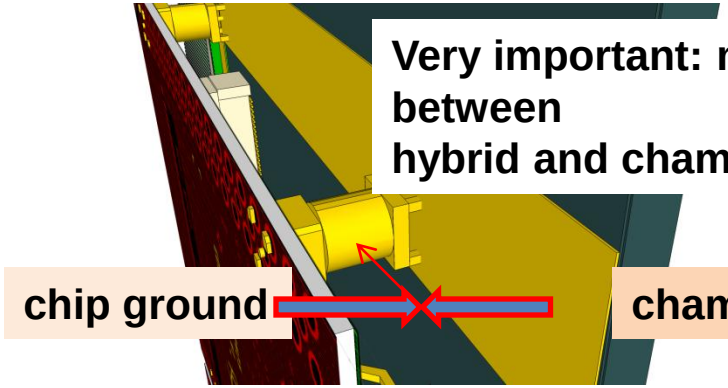
NUP4114UPXV6 quad ESD diodes: < 1 pF



IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8





Very important: minimize L between hybrid and chamber: MMCX plugs

Negative clipped: $V_n = -V_f - L \times dI_{esd}/dt$

Positive clipped: $V_p = V_{cc} + V_f + L \times dI_{esd}/dt$

Cost Issues APV hybrid

Assume production of 200+ hybrids

- development and Prototyping DEM 7000 Eu

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cost per hybrid

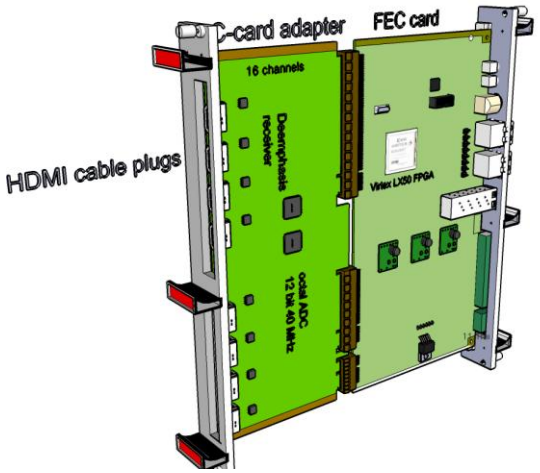
• Components	55	Eu
• PCB industrial production (+200)	10	Eu
• APV 25-S1 chip (128 ch)	20	Eu
• PCB mounting (estimated !)	15	Eu
• Bonding and Potting	5	Eu
• Participation in development cost (200+)	35	Eu

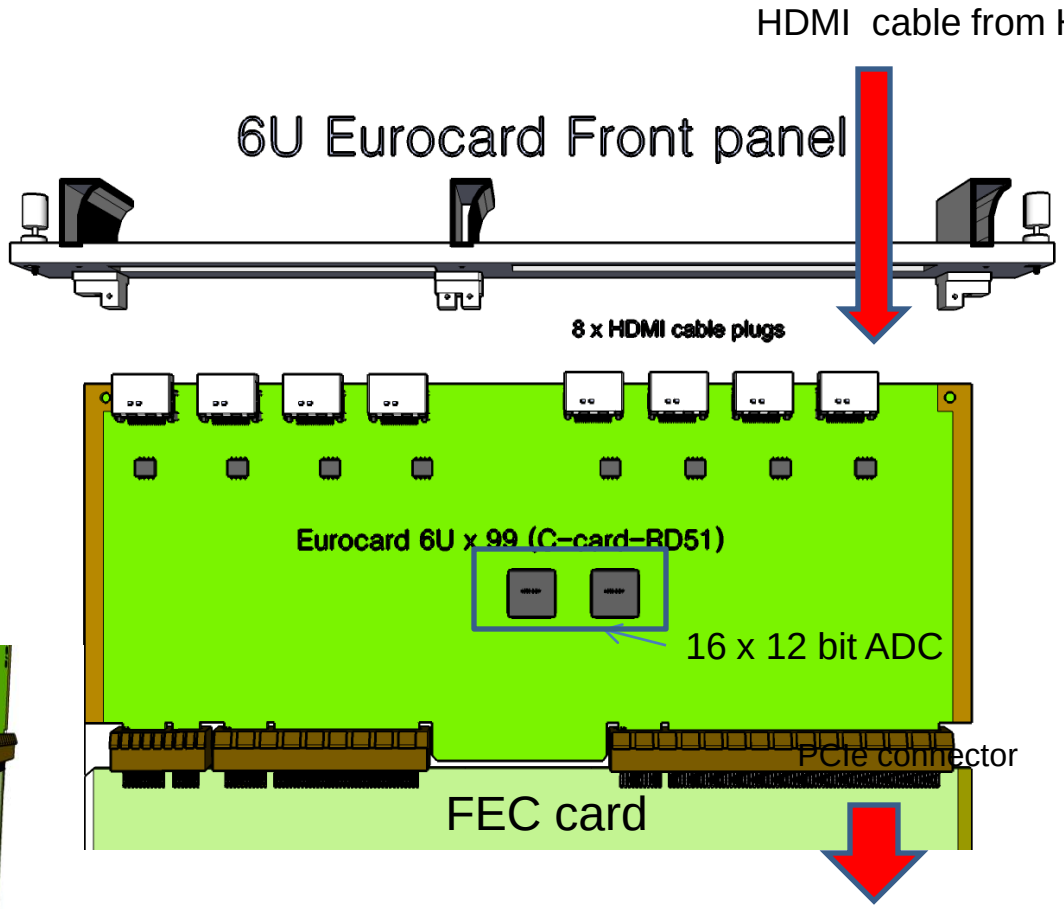
total 140 Eu
+ testing & yield 10 Eu

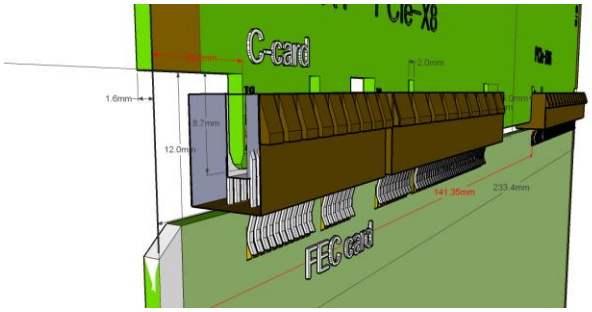
Estimated cost: 150 Eu/hybrid (1.17 Eu/ch)

Octal ADC card with HDMI interface

(see talk S.Martoiu)





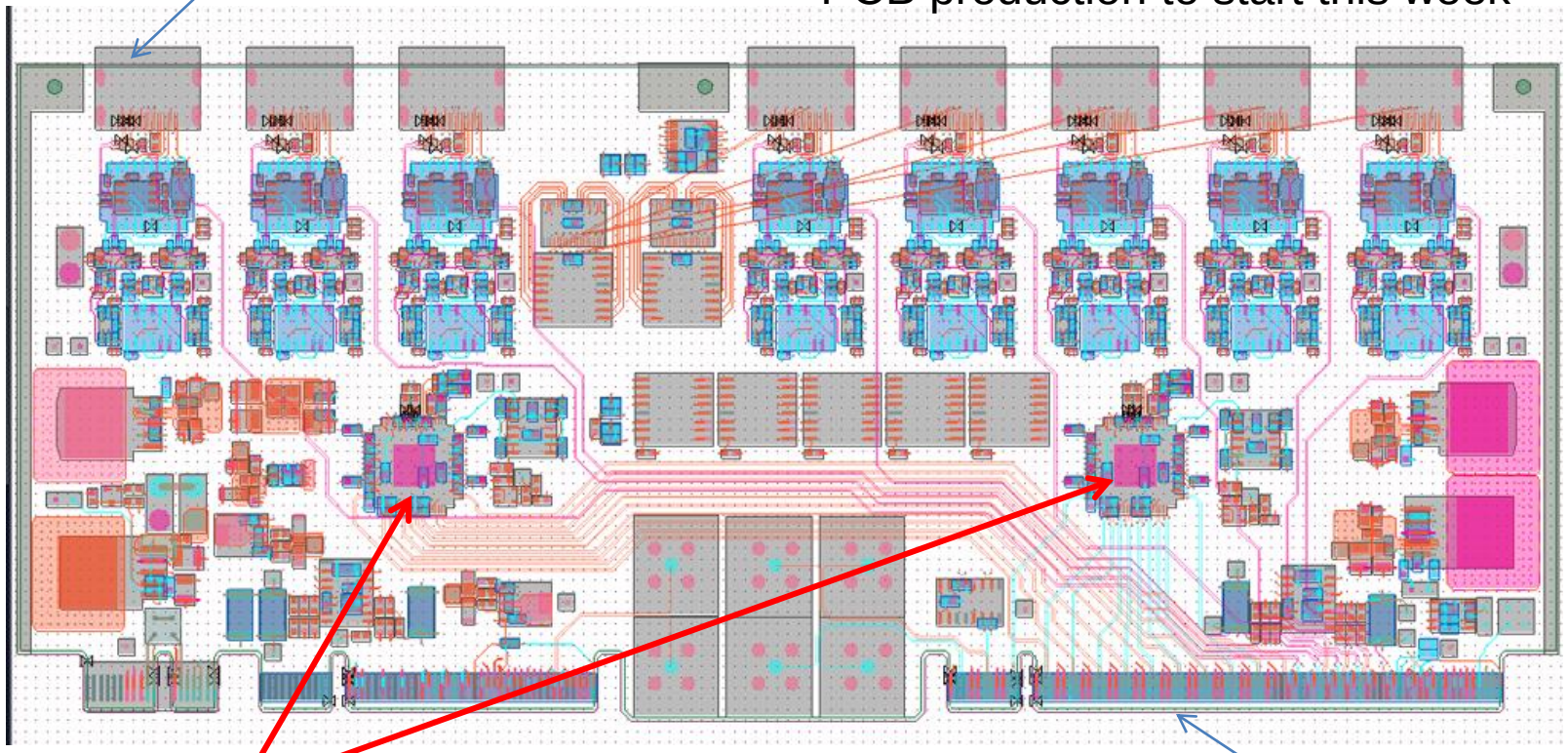


Digitizer for analogue hybrids

C-card layout

8 x HDMI connector

10 layer card 1.6 mm , Eurocard format
PCB production to start this week



ADC chips (12 bit@ 40 MHz)

PCI connector interface to FEC

Cost Issues Digitizer card

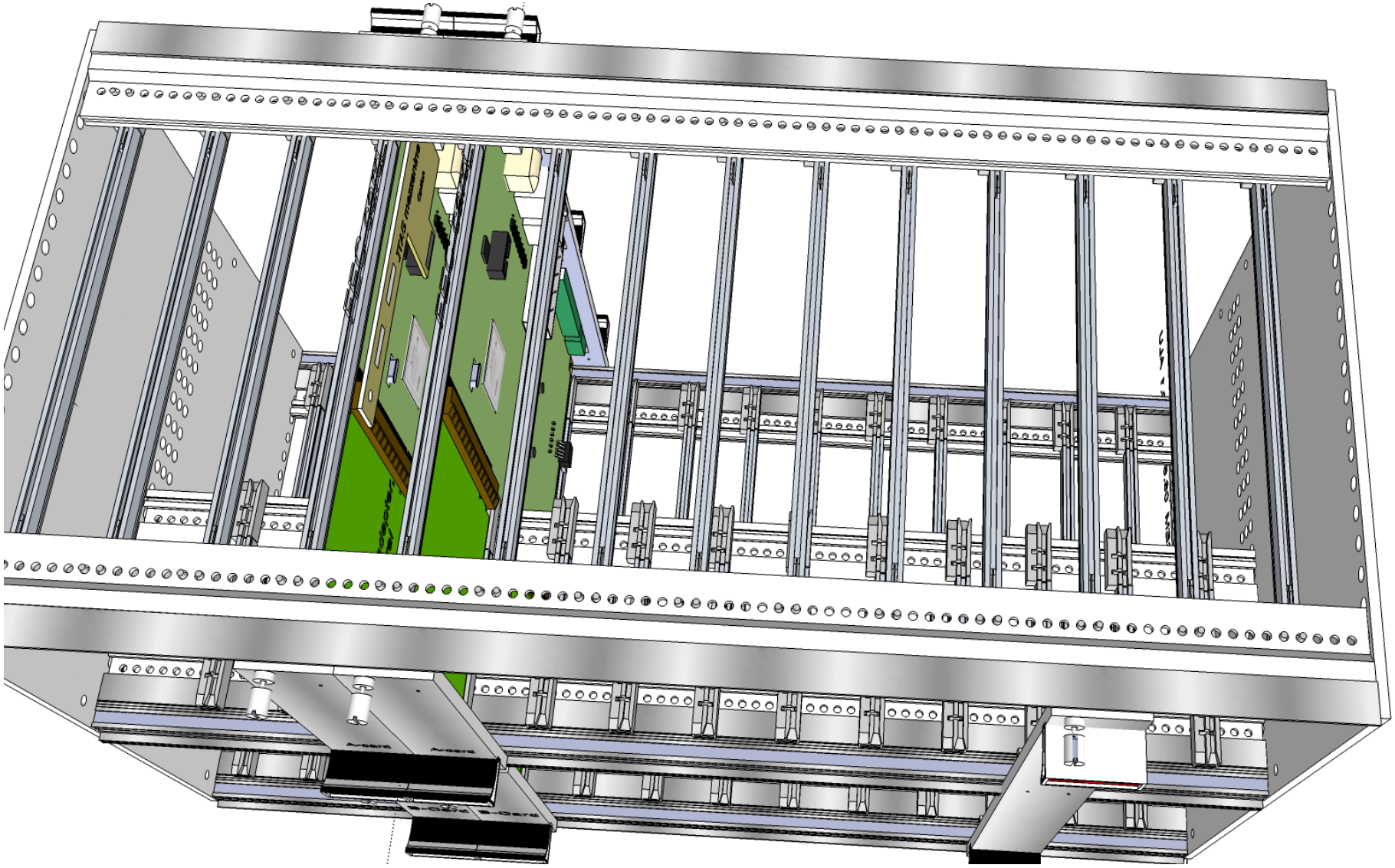
• Commercial Allegro design Intrasys Inc.	2900	Eu
• Commercial PCB production (ELTOS) 12 PCB@2500 Eu	208	Eu
• (alternatively " " " 40 PCB@3560 Eu	89	Eu)
• Component mounting TESLA estimated 40+	50	Eu
Total 40+	~210 Eu	

Components

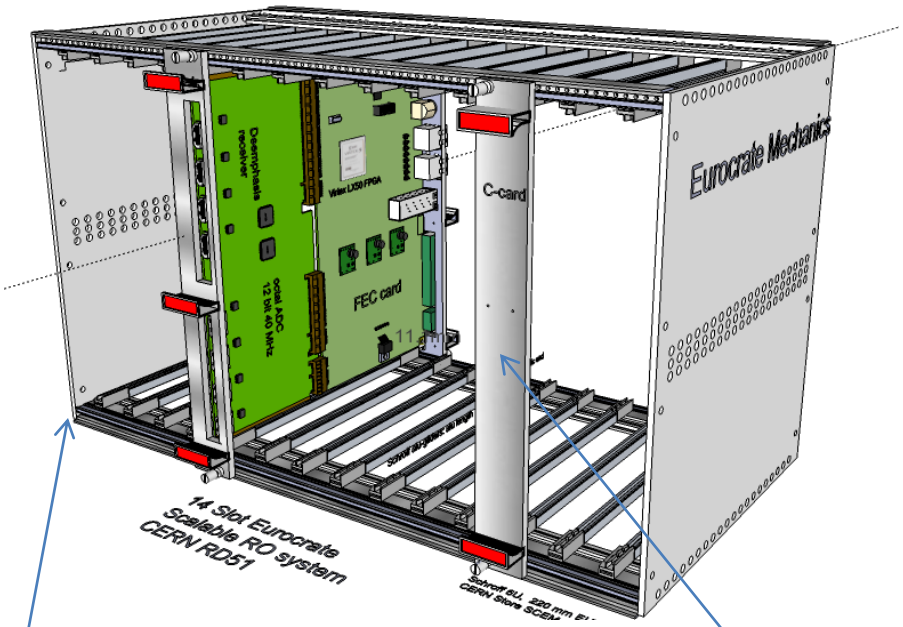
• ADCs (16 x 12bit@50 MHz)	100	Eu
• Components (OpAmps etc estimated	100	Eu
• Eurocard front panel	25	Eu
• Testing	25	Eu
Total estimated 40+	250	

Estimated cost: 460 Eu/ADC card max 2048 channels (0.22 Eu/ch)*

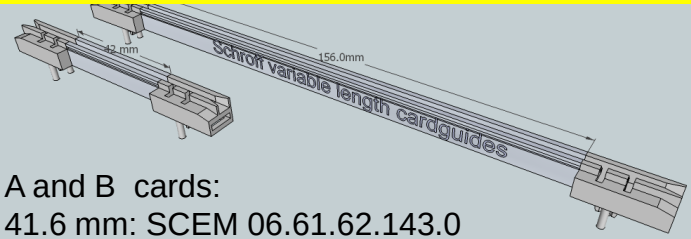
Eurocrate for SRS



Chassis and mechanical

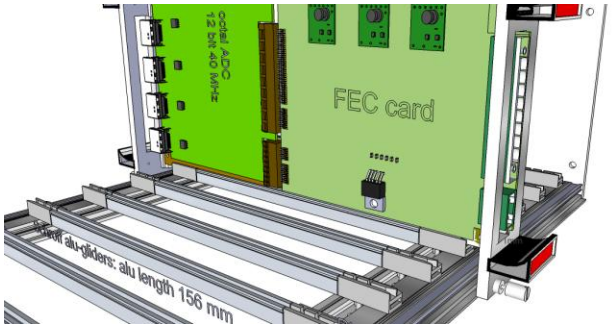


Card guides for SRS now in CERN store:



A and B cards:
41.6 mm: SCEM 06.61.62.143.0

C-cards only:
155.6 mm: SCEM 06.61.62.143.1



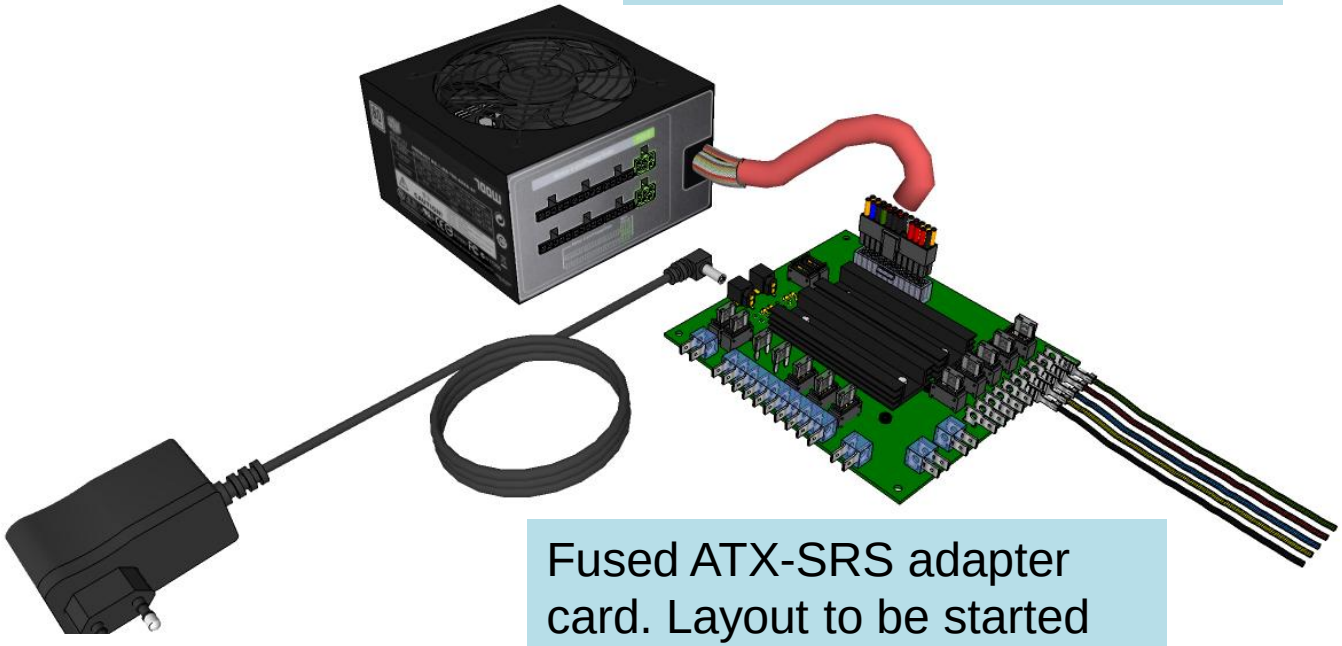
Chassis: 6U x 220 mm, Schroff
WWW.Schroff.BIZ -> Europack
CERN SCEM 06.61.61.045.7

C-cards and FEC cards:
Front panel set 6U-6TE with fixations:
CERN SCEM 06.61.63.156.3

A-cards and B-cards
Front panel set 3U-6TE with fixations:
CERN SCEM 06.61.63.056.6

ATX power for SRS

ATX power supply min.500W



24-pin ATX12V 2.x power supply connector
(20-pin omits the last 4: 11, 12, 23 and 24)

Color	Signal	Pin	Pin	Signal	Color
Orange	+3.3 V	1	13	+3.3 V	Orange
				+3.3 V sense	Brown
Orange	+3.3 V	2	14	−12 V	Blue
Black	Ground	3	15	Ground	Black
Red	+5 V	4	16	Power on	Green
Black	Ground	5	17	Ground	Black
Red	+5 V	6	18	Ground	Black
Black	Ground	7	19	Ground	Black
Grey	Power good	8	20	No connection	
Purple	+5 V standby	9	21	+5 V	Red
Yellow	+12 V	10	22	+5 V	Red
Yellow	+12 V	11	23	+5 V	Red
Orange	+3.3 V	12	24	Ground	Black

The three shaded pins (8, 13, and 16) are data signals, not power.

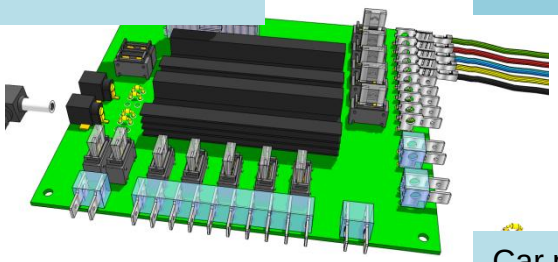
Pin 20 used to provide −5VDC (white wire) in ATX and ATX12V versions 1.2 and earlier. Version 1.2 allowed the omission of this pin, and versions 1.3 and beyond prohibited this pin.

The right-hand pins are numbered 10 through 20 in the 20-pin version.

Fused ATX-SRS adapter card. Layout to be started early June

cable bundle to SRS system

Standard Power packs for User-defined Voltages



Car plugs and fuses

Very prelim! SRS costings

small SRS system without DAQ computer

Estimated cost SRS based on 200 hybrid / 40 ADC card cost

APV hybrid ~	1.17 Eu/ch	min 150 Eu
ADC card ~	0.22 Eu/ch	min 460 Eu
FEC card ~	0.448 Eu/ch	min 1000 Eu
HDMI cables ~	0.12 Eu/ch	min 30 Eu
ATX power ~	0.1 Eu/ch	min 200 Eu
Crate ~	0.1 Eu/ch	min 200 Eu

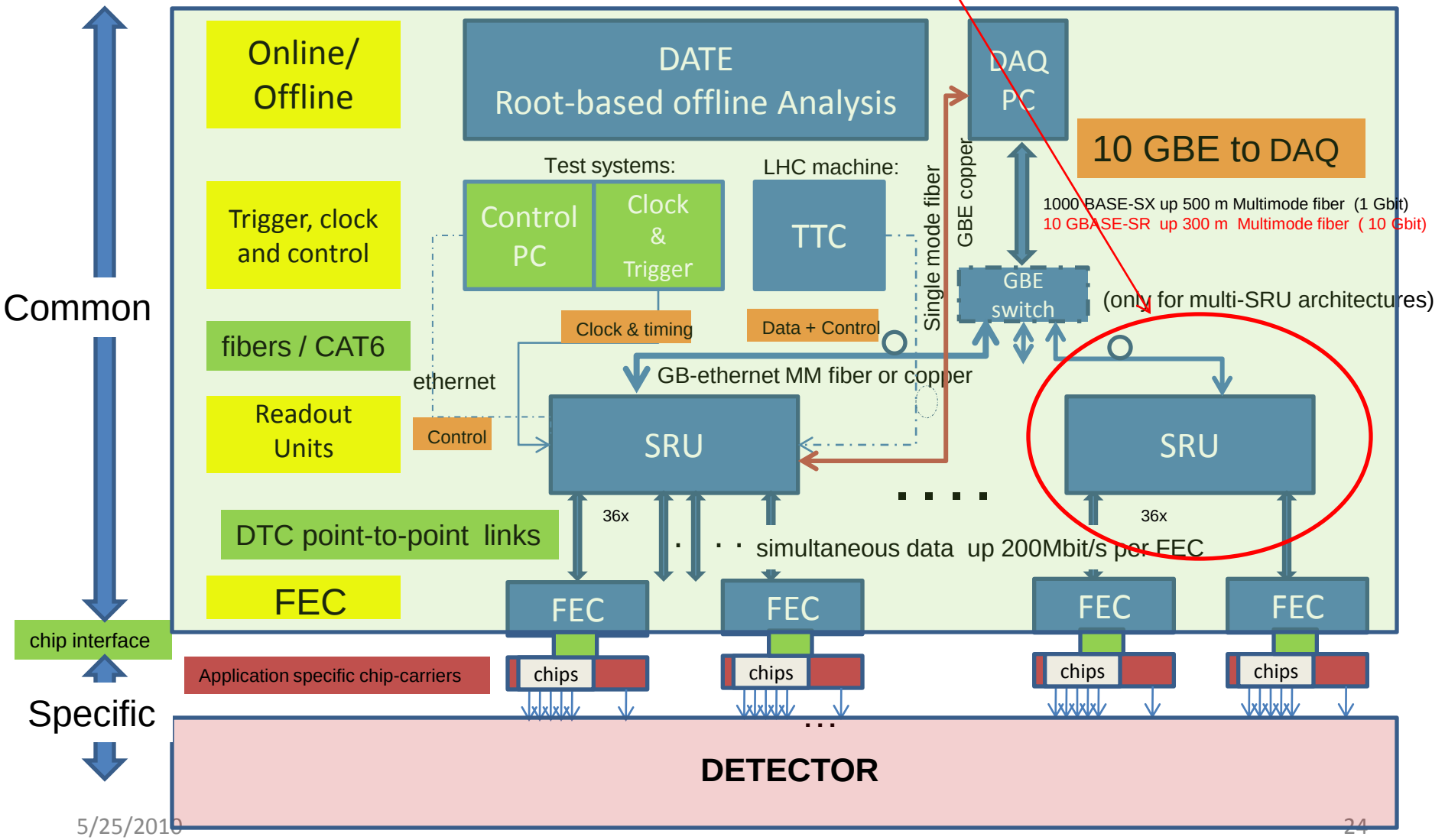
Total SRS small system **2.158 Eu / ch**

system with 2048 channels: 4420 Eu*
system with 128 channels: 2040 Eu*

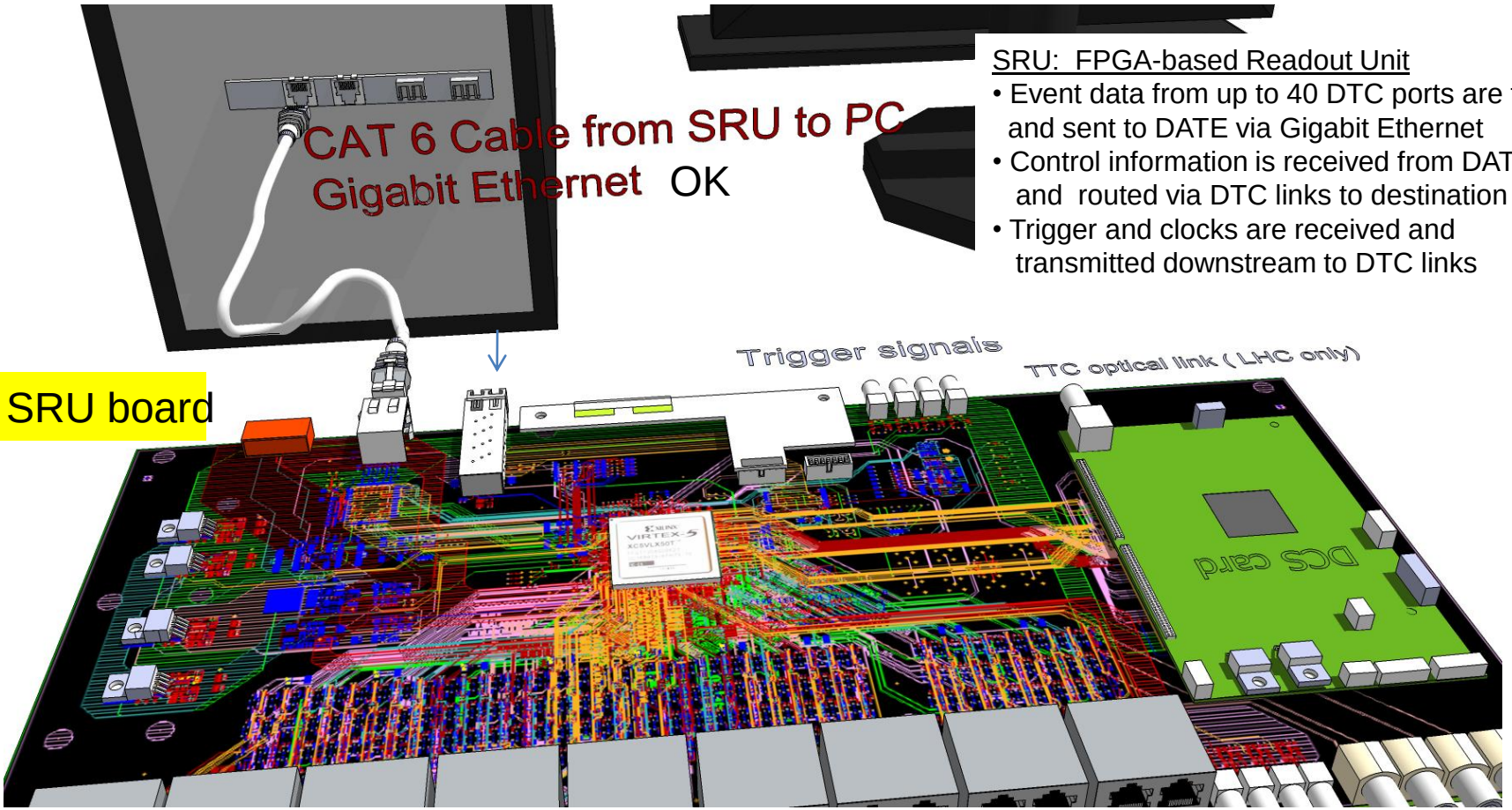
* add cost for server PC

Scalable architecture > 16 k channels

➔ requires SRU



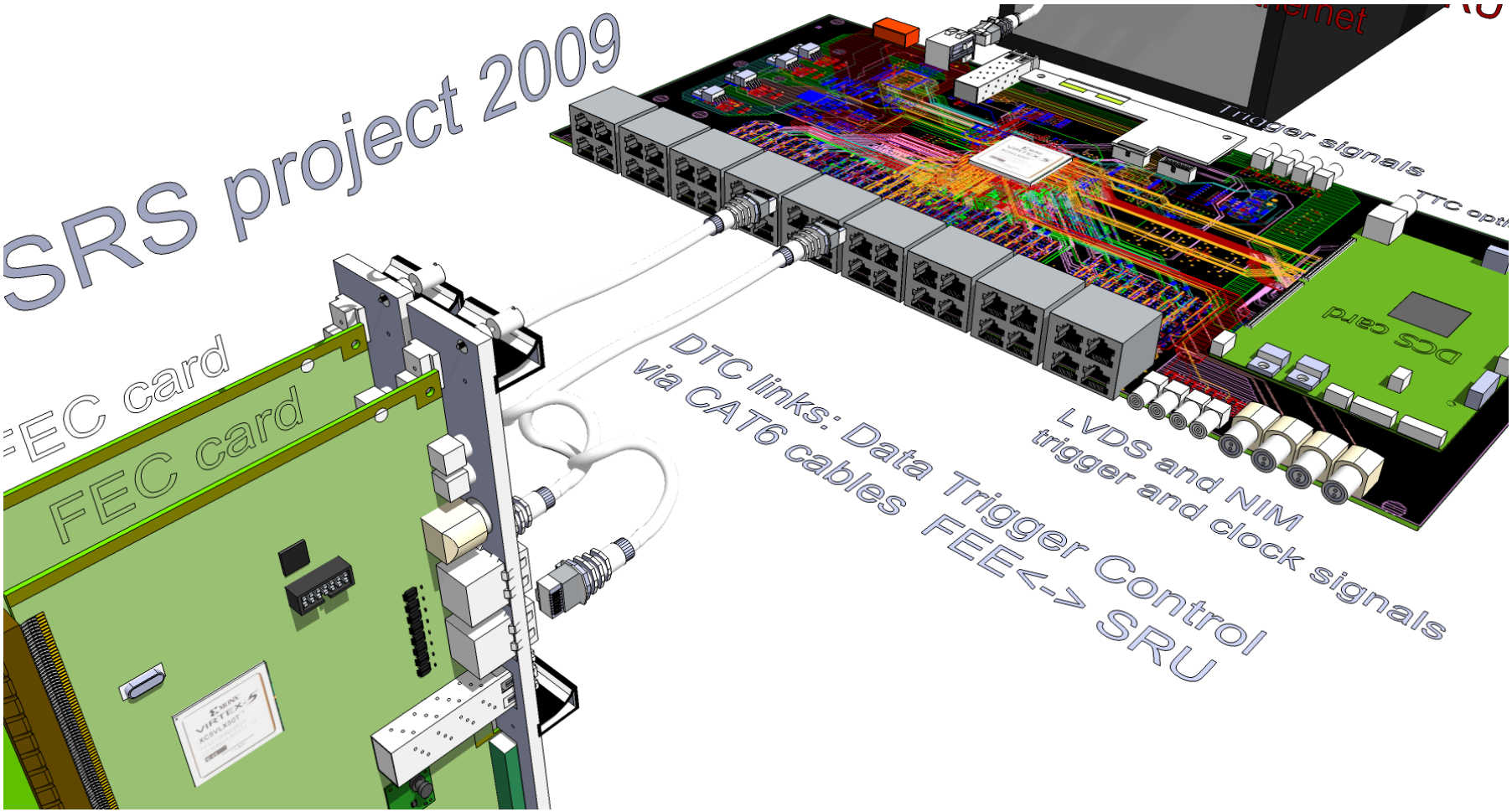
Gigabit Ethernet to DATE Computer



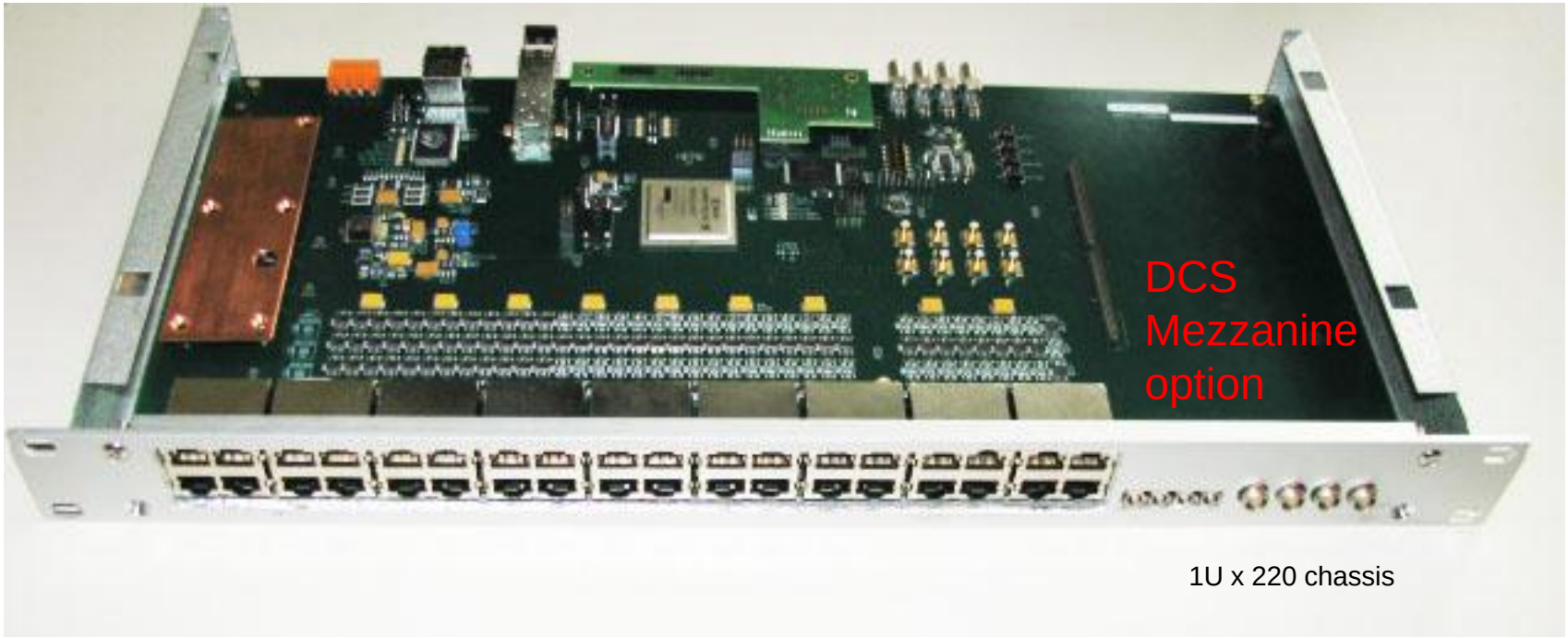
SRU: FPGA-based Readout Unit

- Event data from up to 40 DTC ports are formatted and sent to DATE via Gigabit Ethernet
- Control information is received from DATE / DCS and routed via DTC links to destination
- Trigger and clocks are received and transmitted downstream to DTC links

DTC links between 1 SRU and 40 x FEC's



First SRU Prototype* March 2010



March 2010: 4 prototypes produced, fully debugged, 1 installed in LHC area as LED Monitoring Control Unit of EMCal/ALICE. 1 board in Wuhan for DTC link work, 1 Board at CERN for GBE development, 1 spare

*prototype version: Virtex-5

Revised SRU features

ongoing design/production project with CCNU Wuhan

- fix some some bugs of the prototype (+ add one LDO)
- upgrade to Virtex-6 (X6LVX130..240T) FPGA for 6.5 Gigabit Ethernet capability
- 2 x SFP+ (fiber) for dual data streams
- 1 x 1000-Base-T (copper) for control
- upgrade from 36 to 40 DTC links
- add FPGA-external memory (2 Gbyte , 800 MHz, 16 bit I/O, DDR-2,)
- place TTCrx and optical receiver on SRU board (DCS card becomes “very optional”)
- dual Flash boot: a.) default config.1 on RESET from NIM or TTC
  b.) config. 2 on control command via Ethernet
  c.) remote program of config.2 via Ethernet
- replace LVDS-100 transceivers by LVDS101 with integrated termination
- use better power connector
- add Banana plugs for Chassis GND and for ATX Power Sense
- add SEU protection of Virtex-6 (using partial reconfiguration logic)

New schematics : Wuhan
Availability: planned for September 2010

SRU costing

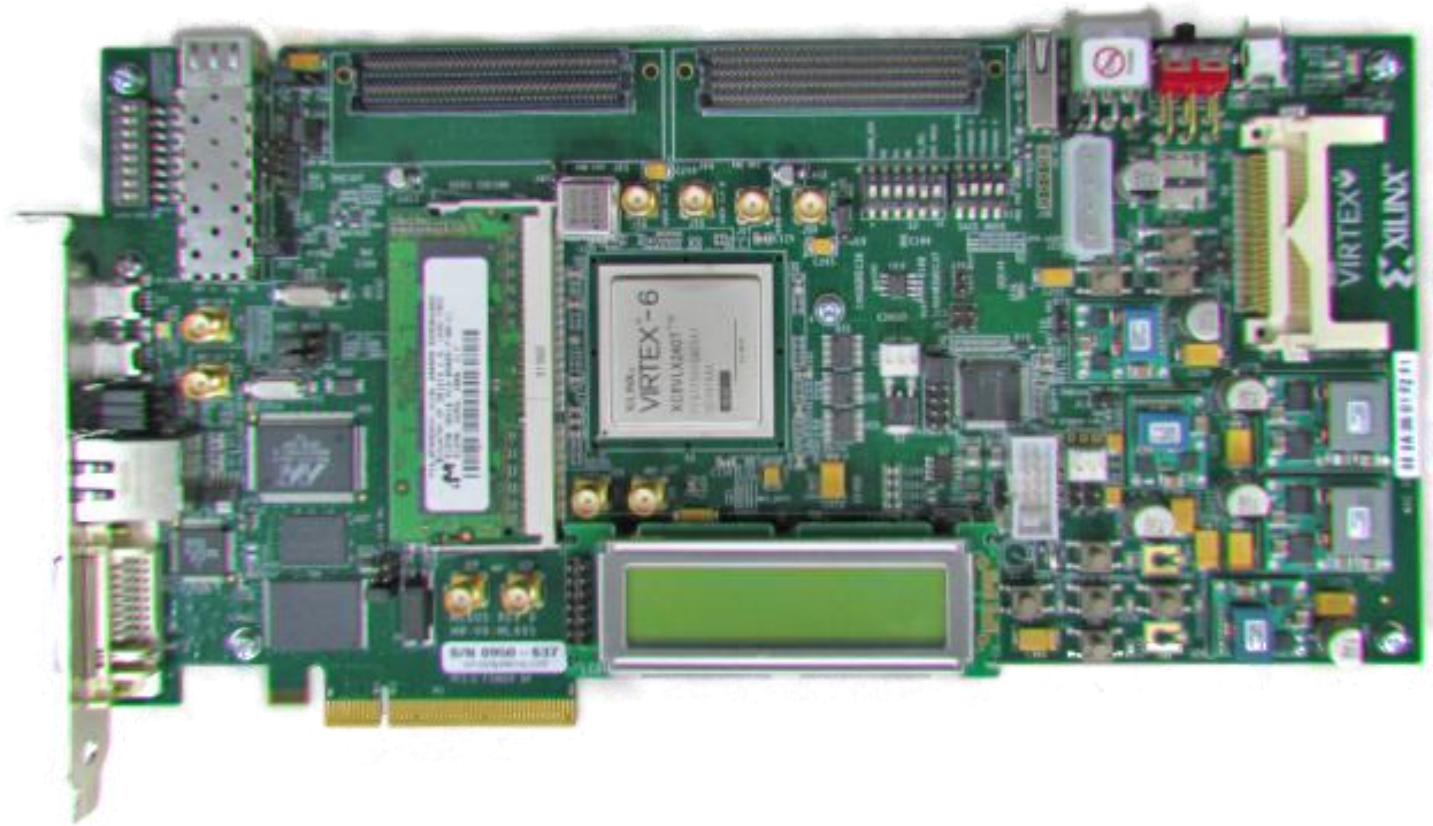
To be defined, estimate min. 2500 Eu

1 SRU can handle 40 x 2048 channels

➔ add 0.03 Eu/channel

Virtex-6

ad-interim development platform for SRU
in use



Gigabit Ethernet tests - DATE

CERN DAQ team , Filippo Costa

TEST #1

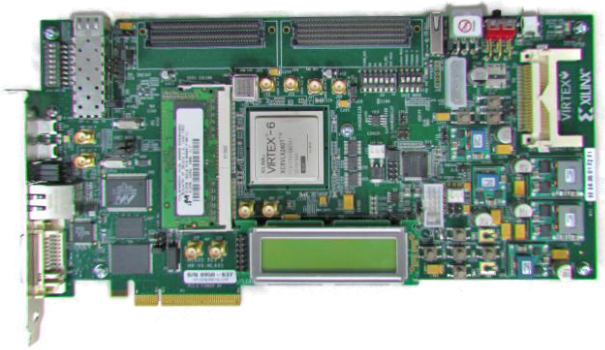
2 asynch DATA sources : 1 HW + 1 SW

DATE Gb ethernet readout

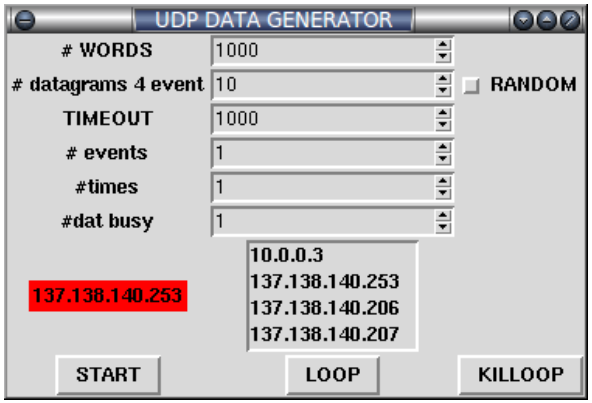
1 Gb/s

1 Gb/s

HW (Virtex 6 dev. board)



SW



Ev size : **~500KB**
Readout rate : **~300Hz**
Throughput : **~144 MB/s**

Data transport via UDP to DAQ/DATE

UPD for the transport of event data from the SRU buffer to the DATE buffer

There is no higher layer, i.e. Bit-errors will be unrecoverable: events with bit errors are to be flagged and/or discarded

The UDP transport is " transparent" for the Eventbuilding that starts at the SRU's DTC input buffer level (subevents_> event)

The standard max. MTU payload is 1.6 kbyte, but by using Jumbo packets, up to 9 kB of event data can be transmitted per packet.
9kB Jumbo frames are preferred as for higher throughput.
Events bigger than MTB =1.6 / 9kB generate ethernet fragmentation with increased error rates. (Try to stay below fragmentation level).

Events much smaller than 1.6 kByte suffer from bandwidth penalties due to increasing ratio overhead/payload. Use Multi-event packing (MEP) for very small events (like LHCb). For normal events, MEP=1

TEST #2
2 asynch DATA sources : 1 HW + 1 SW
1 network switch in the middle

HW (Virtex 6 dev. board)

DATE Gb ethernet readout

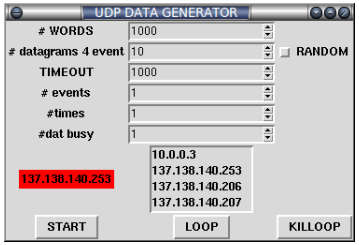
1 Gb/s

Network switch

1 Gb/s

1 Gb/s

SW



Ev size : **~900KB**
Readout rate : **~110Hz**
Throughput : **~110 MB/s**

Summary Gigabit Ethernet ->DATE tests

- The system has succesfully used **JUMBO** frames of **9KB** during the data acquisition.

- **DATE** checked the synchronization of the different data sources and the quality of data, after several milions of events received no errors have been detected.

- All these tests have been succesfully reproduced **changing randomly** the event size.

- The throughput of the acquisition was always near the maximum reachable using **1Gb/s** speed link.

- **DATE** configured the board automatically, using slow control instructions, at each **START OF RUN**.

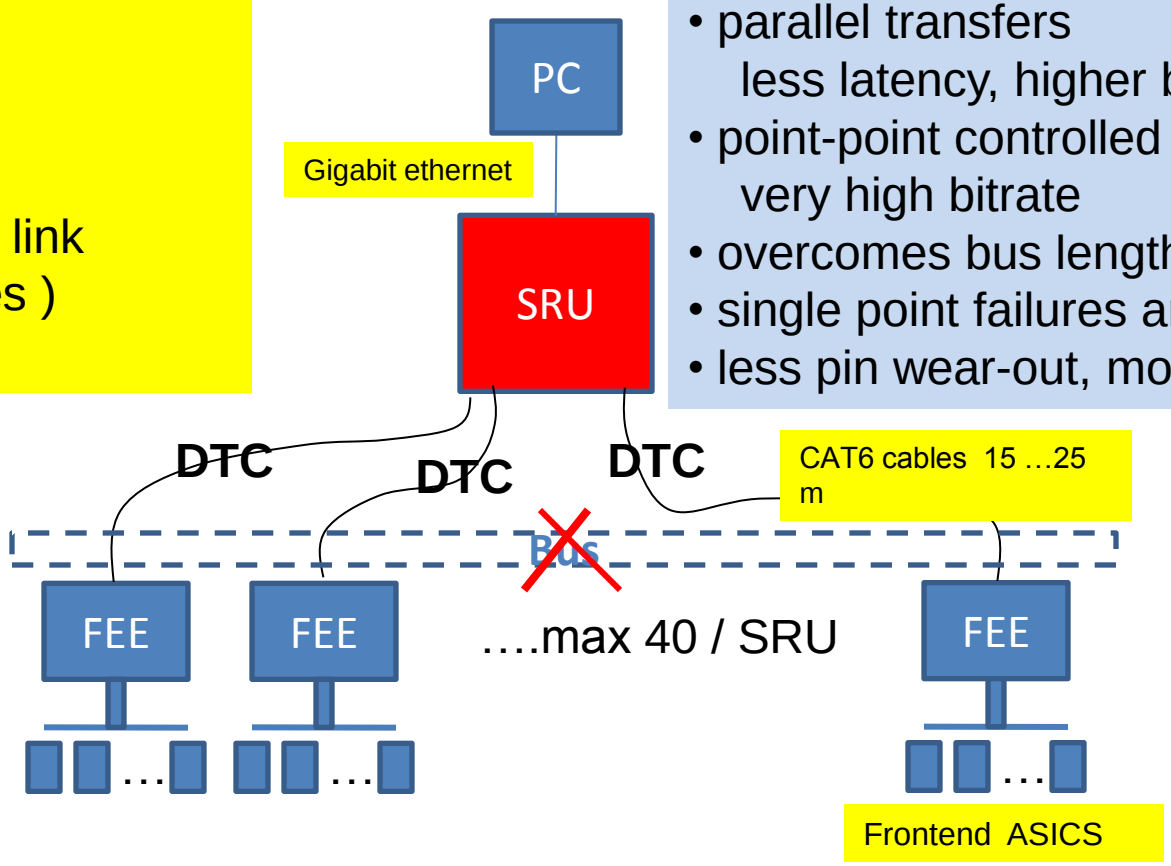
Next step: 10 GbE
Example: 10 GbE NIC's* for servers from HP

The NC522SFP is an eight lane (x8) PCI Express (PCIe) 10 Gigabit network solution offering the highest bandwidth available in a ProLiant Ethernet adapter. This dual port PCI Express Gen 2 adapter supports SFP+ (Small Form-factor Pluggable) connectors, requiring either Direct Attach Cable (DAC) for copper environments, or fiber transceivers supporting SR, LR, or LRM optics plus fiber cables for fiber optic environments.
Fiber optic modules and cables available from HP allow the NC522SFP to connect to SR, LR, and LRM environments

*cost ~ 600 Fs

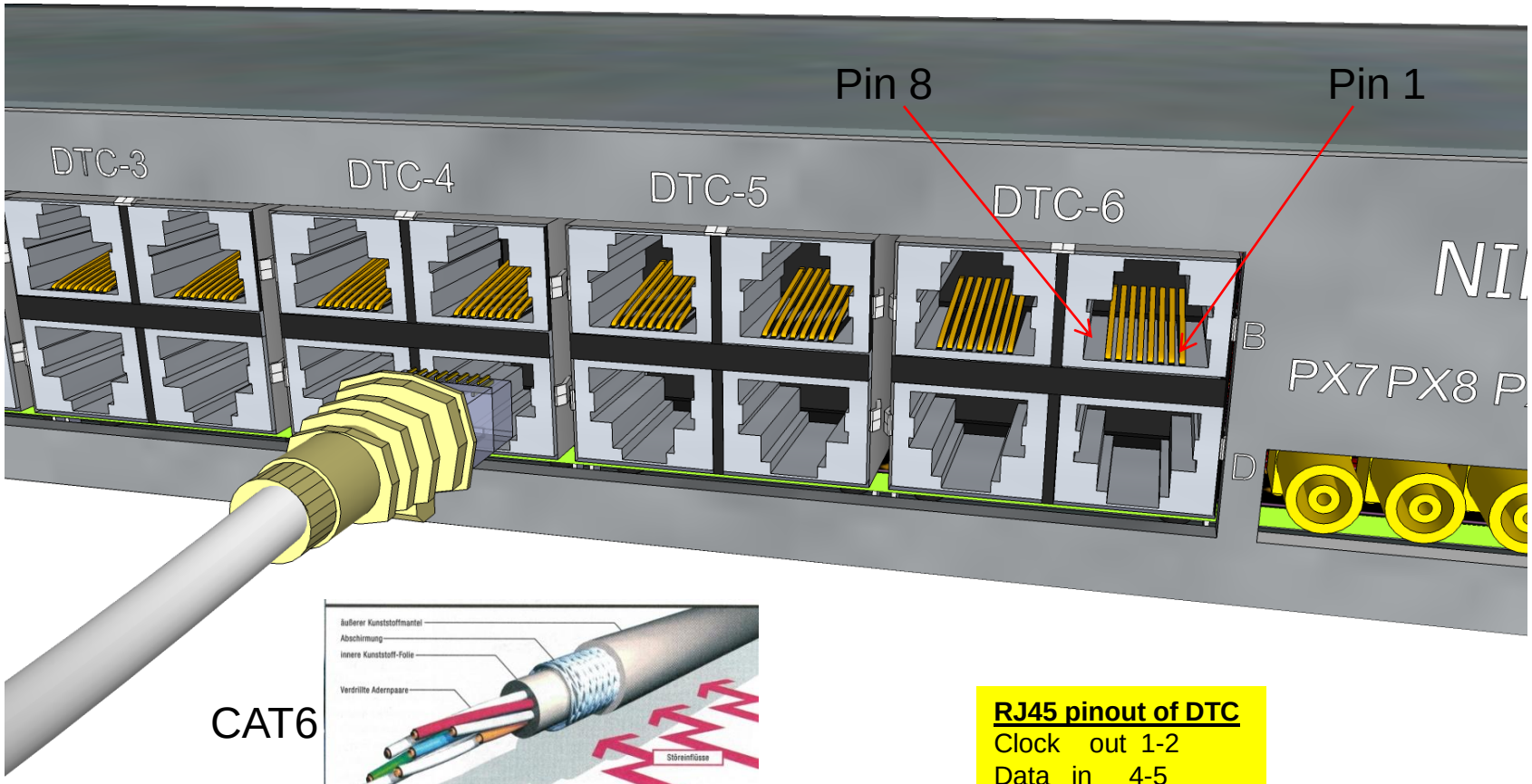
DTC links
(buses are obsolete)

DTC link
Data
Trigger
Control
via the same link
(CAT6 cables)



- parallel transfers
  less latency, higher bandwidth
- point-point controlled impedance
  very high bitrate
- overcomes bus length limit to SRU
- single point failures are not fatal
- less pin wear-out, more cost effective

DTC link pinout: 2-in, 2-out



CAT6

4 x twisted pairs
CAT6 shielded cable

RJ45 pinout of DTC
Clock out 1-2
Data in 4-5
Trigger out 3-6
Return in 7-8

Don't use unshielded UTP cables

DTC link protocol

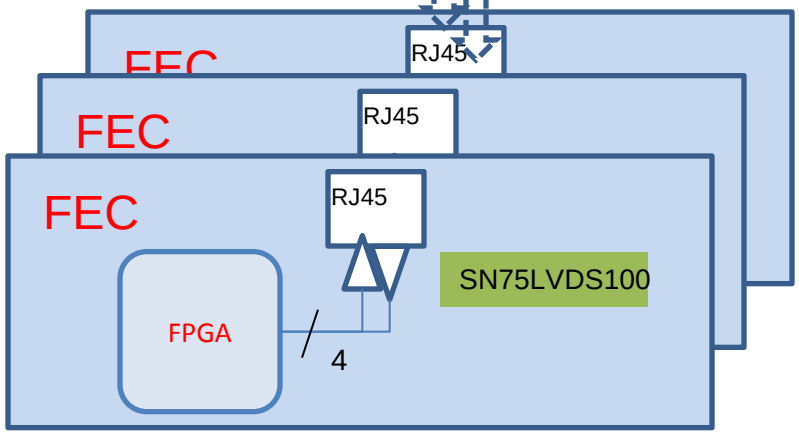
➔ revised DTC protocol by Fan Zhang , CCNU Wuhan:

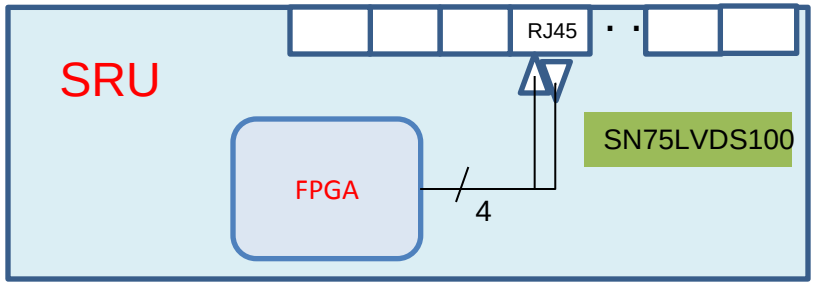
Constant SRU clock. Coded trigger and Control for dynamic actions.
Assume SRU clock 240 MHz: Input stream from 40 FEC's @ 240 Mbit/s ~ 10 Gbit/s

Clock ← **DTC_CLK clock to FEC** pin 1-2
Data → **DTC_DATA data from FEC** pin 4-5
Select ← **DTC_TRIG coded trigger to FEC** pin 3-6
Return → **DTC_RETURN status or local trigger** pin 7-8

buffered , terminated LVDS signalling over 15-25 m CAT6

40 x





- **DTC_DATA = Serial data or ACK to SRU**
- **DTC_TRIG = Serial data or ACK to FEE**
- **DTC_RETURN = Coded status to SRU (Ready or Error ~)**

- **Note: for disabling a defective FEC card (bad FPGA) we need a unique code : stop CLK at high level, clock trigger line.**

- **Mode detection : detect DTC_TRIG pulse**
- **If (Widths of DTC_TRIG pulse, number of T_{DTC_CLK})**
  - **2 : Level-0 trigger**
  - **4 : Level-1 trigger**
  - **6 : Level-2 trigger = Readout command**
  - **8 : Control operation**
  - **>=9 : Error**

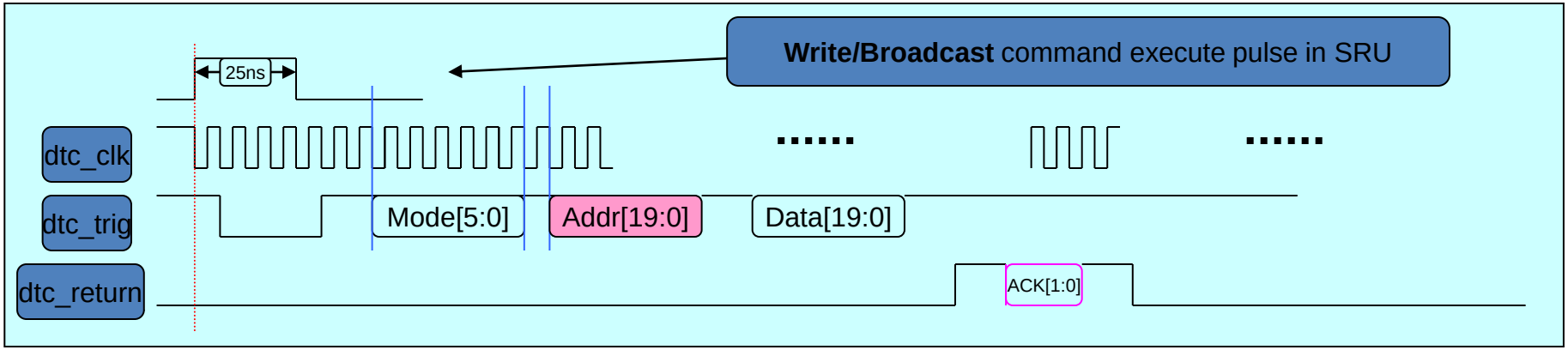
DTC link protocol

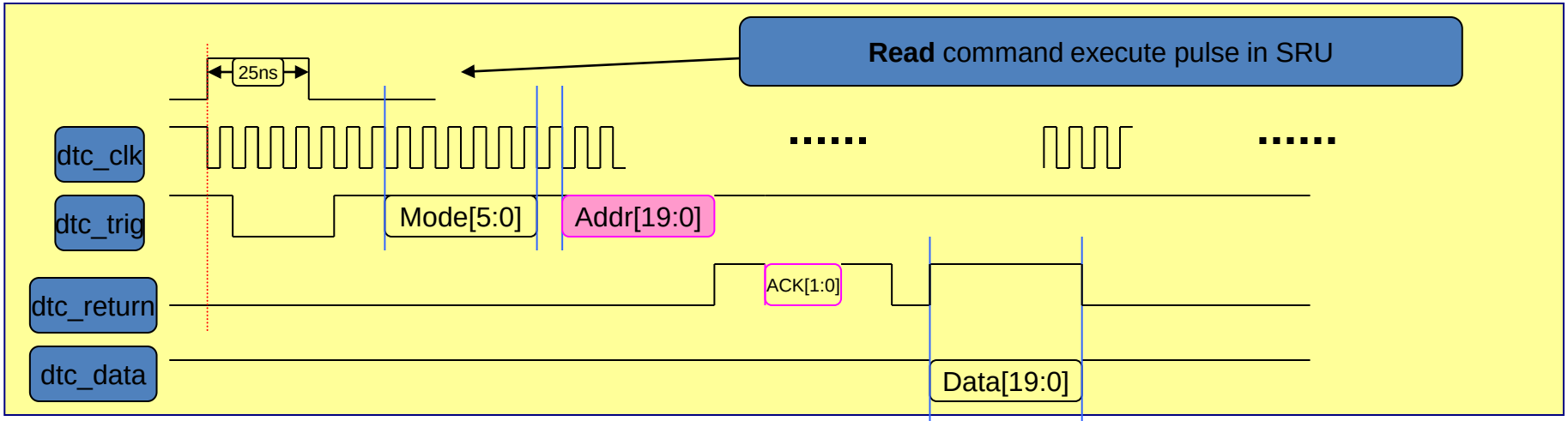
(CCNU Wuhan, Fan Zhang)

- Trigger Mode 2: L0 trigger distribution
- Trigger Mode 4: L1 trigger distribution
- Trigger Mode 8: L2 trigger accept
- Data Mode: Block event readout
- Command Mode: Write/Broadcast/Read command
- Check codes and error reporting

Example: DTC Command Mode

Write/Broadcast/Read command





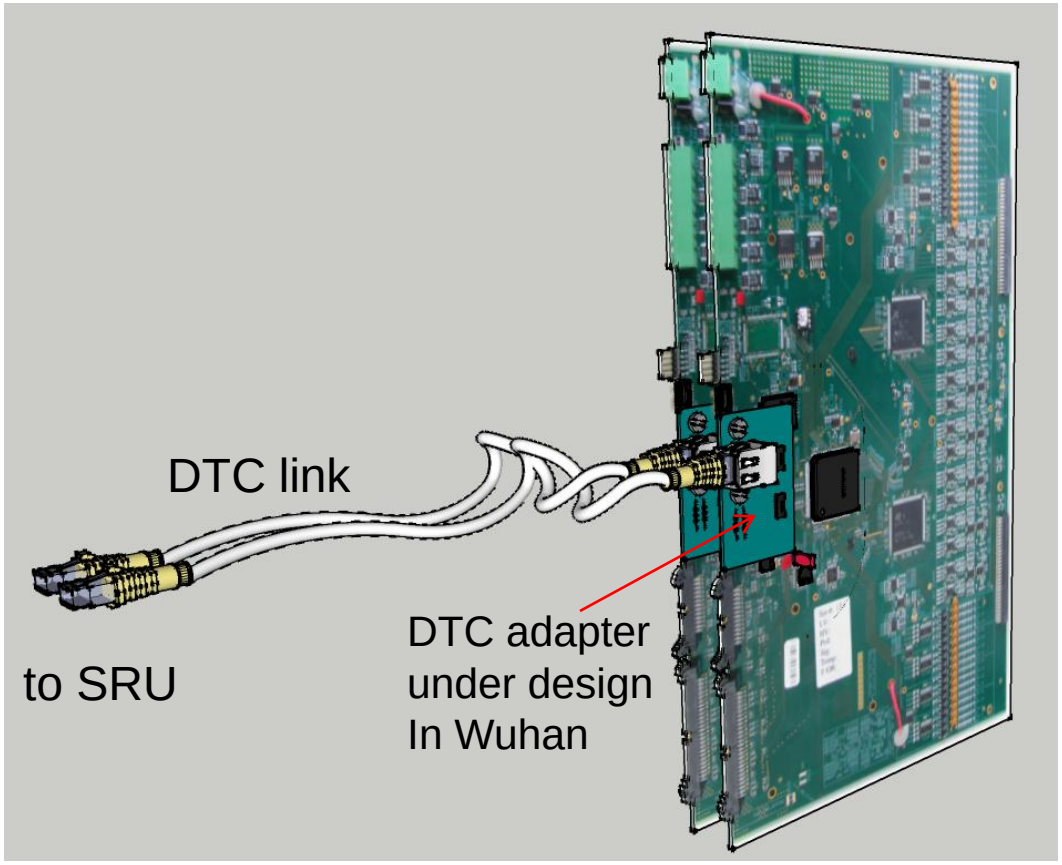
A timeout counter is started when SRU waiting for ACK from FEE card.

Mode[5:0] = {L1,L2,CMD,/L1,/L2,/CMD}

Addr[19:0] = {Reserved[1:0], RW, BC_AL, Broadcast, /RW, /BC_AL, /Broadcast, reg[11:0] }

LHC application of SRS

Ongoing R&D for DTC-link based parallel readout of EMCal/DCaL (ALICE)
replace obsolete GTL bus by DTC links
➔ DTC mezzanine plugged on existing FEE via SRU



Existing FEE electronics
(Altro and APD HV control)

Same as used by Atlas MM

Data Format for SRS

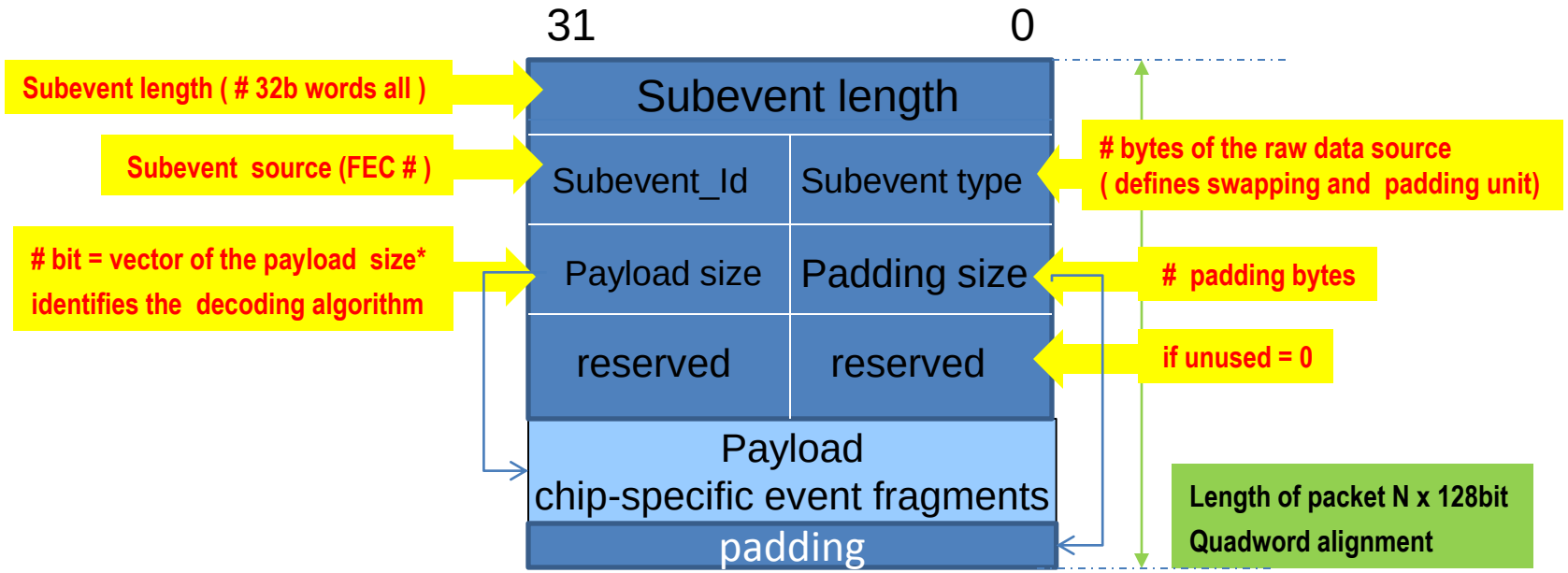
- Baseline for Scalable Readout Systems of RD51
  Subevent data format at the level of FEC cards:
  RHIC Data format of M.Purschke

  -> self identifying subevents allow for single unpacker software
  -> natural merging of different data flavors into a single stream
  -> large variety of detector types and event sizes are supported
- Compatibility with DATE Data acquisition system:

-> requires ALICE Common Data Header(CDH) format as Event format
-> we may have to strip down/generalize CDH for general purpose users

Subevent Packet Descriptor

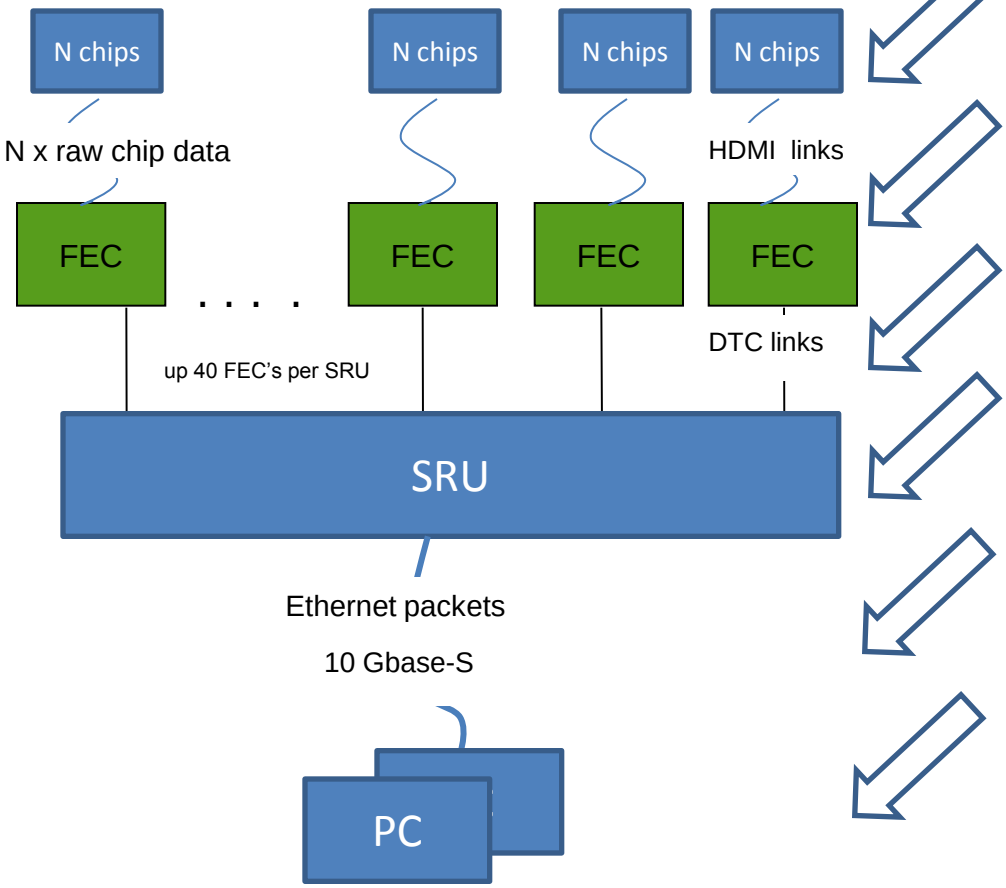
(to be confirmed)



*Payload (#32b) words = subevent lenght - header lenght (4) - padding(#)

Example : 6 means payload 2^6 , hence 64 x 32 bit words.

Formatted SRS streams



Trigger and Tansmit raw chip data to FEC
Here

Raw sub-sub-event fragments from chip

Make Data Packets
Here

Formatted Sub-event fragments in FPGA

Transmit Data Packets
Here

packet stream of sub-events via DTC links

Make Event and UDP payload
Here

Merged Events packed into UDP payload with CDH header for DATE

Transmit all subevent packets over UDP
Here

Event stream via UDP, eventually via switch

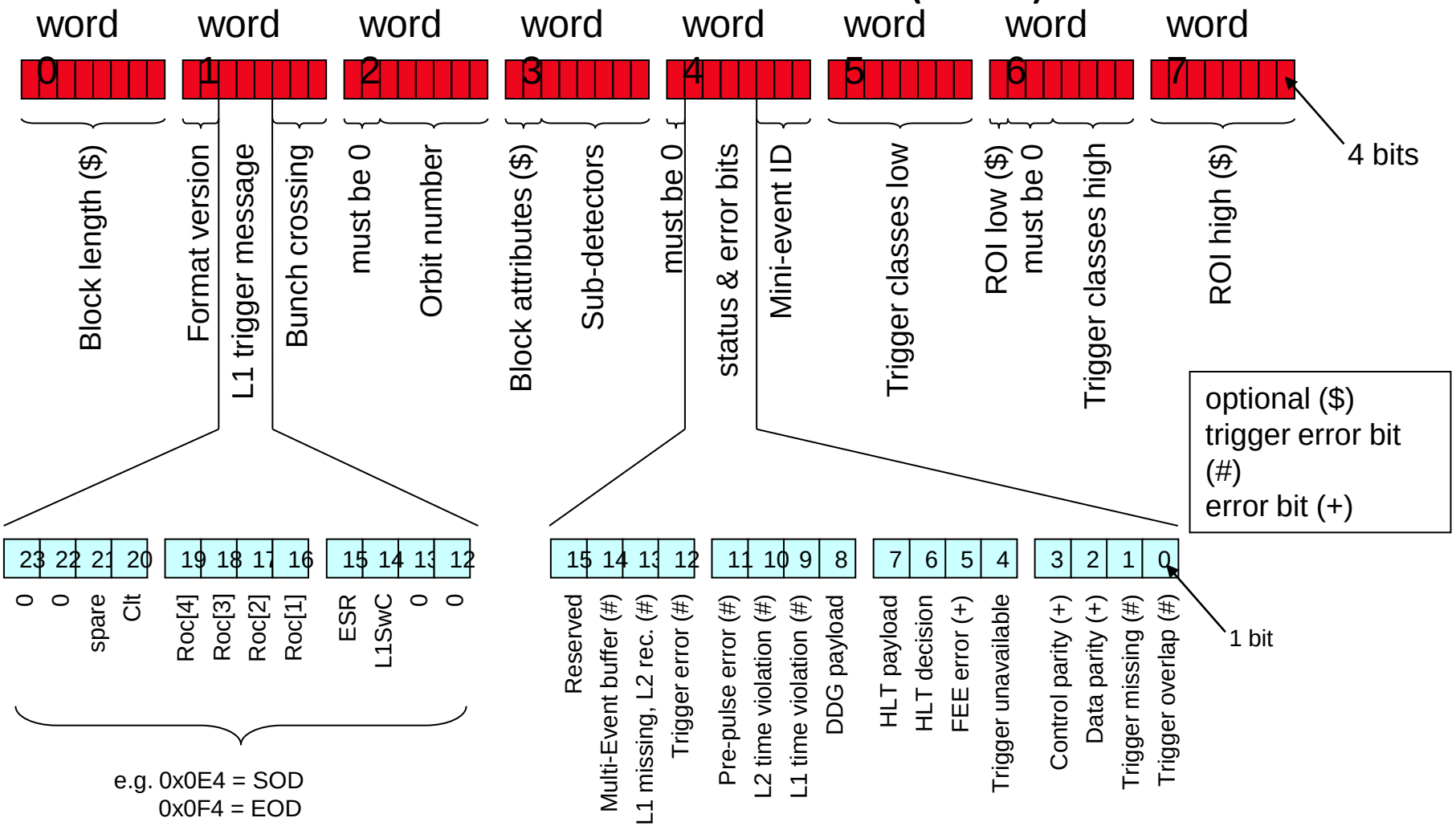
Unpack subevents & Make (Global*) Event*
Here

Events in DAQ PC

* Global if events are received from several SRU's

Event format for DATE:

Common Data Header (CDH)*



* to be adapted for RD51 SRS

Summary

- SRS system gives answers to 3 out of 5 WG5 mandates
- Small SRS systems up 16k channels may cost ~ 2.158 Eu/ch
- All SRS key components in advanced design/production status
- First SRS hybrid with APV was a success
- First applications for DTC links and SRU in the pipeline
- More adapter cards for SRS are under design
- More hybrid designs to be addressed with chips
  listed in the WG5 chip matrix (collaboration wanted)
- Discussions on Data formats are converging
- DATE is online via UDP packets made from Virtex FPGA's
  waiting for SRU

BACKUPS

SRS target

- Common system for MPGD detectors of RD51
- Upgrade of LHC detectors
- Common Readout Hard & Firmware
- Common DAQ system / Data format
- Exchange the chip frontend via common link interface (HDMI cable)
- No buses: more parallel BW, single-point failure tolerance, longer distance
- DTC link protocol for readout, control and triggering (CAT6 cables)
- Supports all RO architectures (push, pull, shared memory, triggerless ..)
- Scalability from very small to very large systems
- DAQ (farm/PC) connected via 10 Gbase-S (fiber) or 1000-Base-T (copper)
- cheap and versatile Eurocard size form-factor for FEC and adapter cards
- RD51-standard chip hybrids on detector, common Panasonic connector
- Detector readout via HDMI cable up 30 m to FEC interface
- Coming optical detector readout link on the horizon: Lightpeak from Intel

Scalable Readout Unit (SRU)

- Rack-mountable box 1U x 220
- 2x 10 Gbase-S, IEEE 802.3ae up 300 m over MM fiber via SFP+ (data)
- 1x 1000-Base-T (1 Gbit Ethernet) over standard network cables (controls)
- Fully bi-directional data and control streams via Gigabit ethernet
- Based on FPGA with integrated MAC cores and 6.5 Gbit GPX links
- DAQ / HLT data stream: uplink, Control and load scheduling: downlink
- Default readout and control system: DATE and DATE control software
- LHC applications: Optical TTCrx receiver for: LHC clock, Triggers, Broadcasts
  LED Monitoring Broadcast pre-pulse decoder from TTC
- Programmable NIM / LVDS trigger/clock interface with common BUSY generation
- 40 DTC links per SRU: Data / Trigger /Control via DTC protocol over shielded CAT6
- parallel DTC readout at max. bandwidth 40 x 240 Mbit/s ~ 10 Gbit/s
- Scalability from 1 to N DTC links (N>40 needs more SRU's)
- RHIC subevent data format on FEC level, ALICE CDH event format on SRU level

Frontend cards

(Eurocard sized 6U-220)

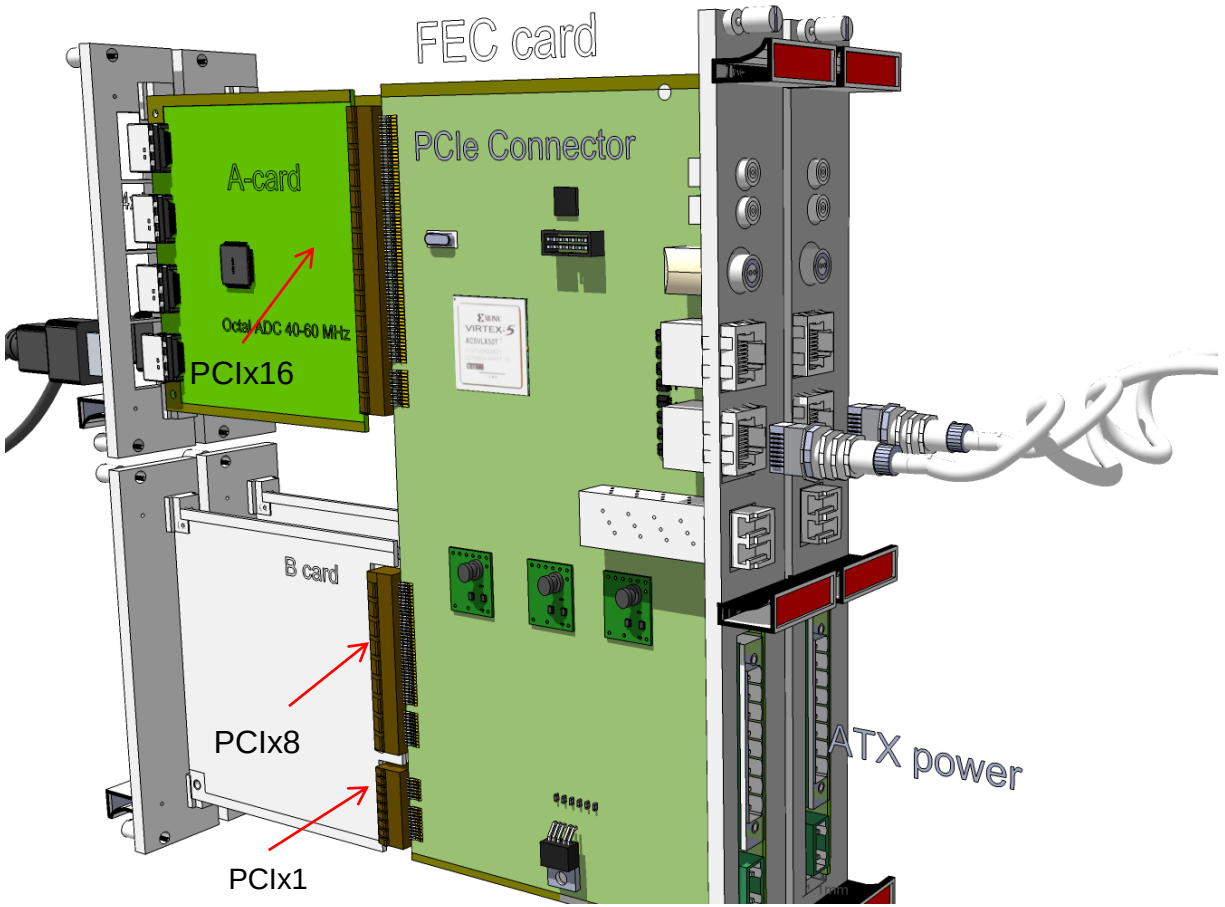
PCIe connectors used as interface to A B or C cards

-PCIx1: GND, LV and HV (optional)
-PCIx8: GND, I2C, 3Gigabit Rx-Tx-Clk, diff. IO
-PCIx16:GND, JTAG chain,3Gigabit Rx-Tx-Clk, diff IO

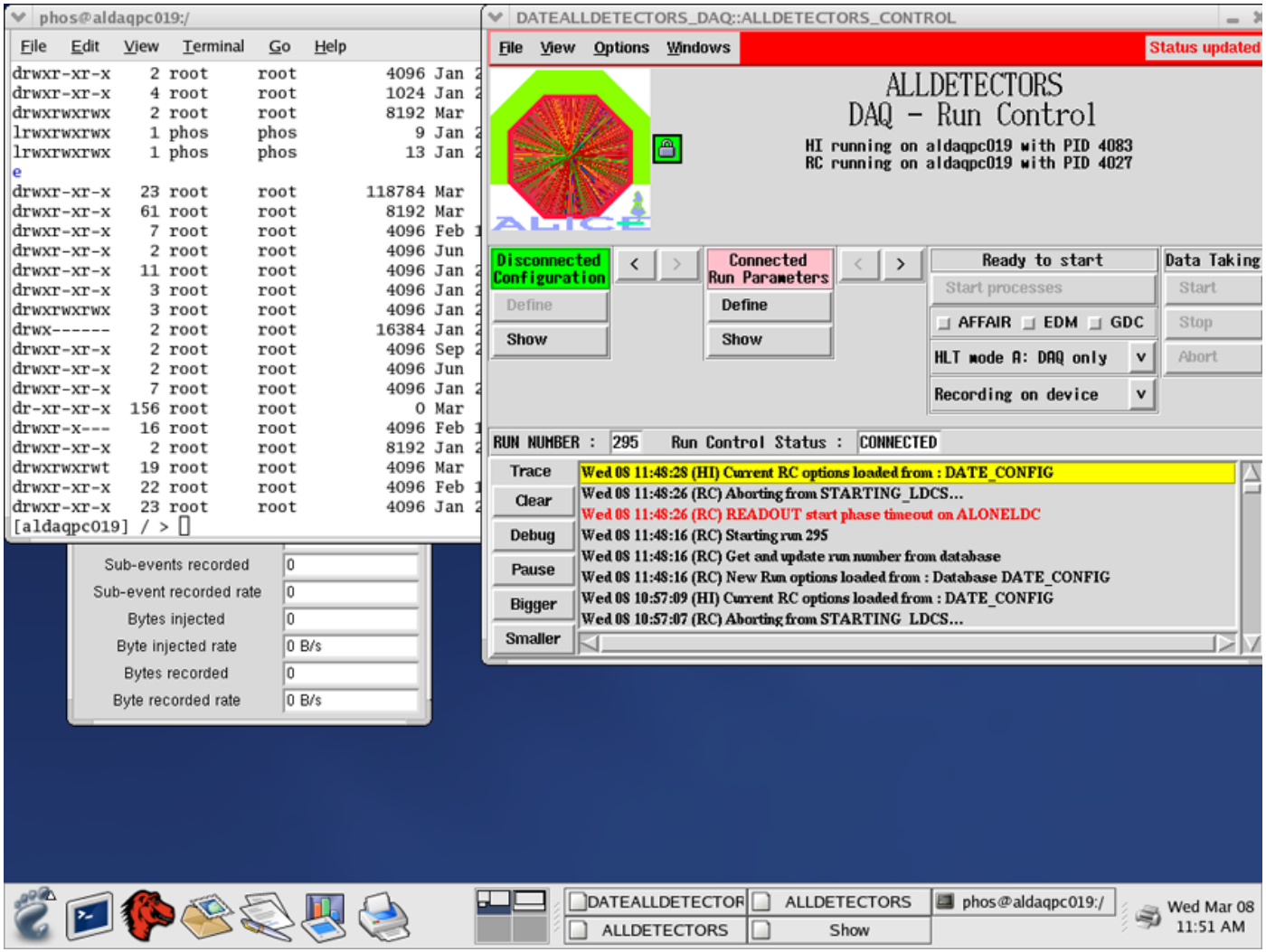
A –Cards: 3U for small detector interface logic

B –Cards: 3 U for miscellaneous extensions and LV-HV control

C – Cards: 6U for large detectors



Default User Interface: DATE



- Developed at CERN for ALICE Collaboration
- Runs on top of Scientific Li
- In daily operation and supported during LHC lifeti
- Very stable, many users
- Interface to Root file system for Data Analysis Framewor called "Root " http://root.cern.ch/drupal/ used by all physicists at CER