# Response to the NSW Trigger Processor PRR report

13 March 2020

This document addresses the issues to be clarified that were identified by the reviewers in the NSW Trigger Processor Production Readiness Review, 14 October 2019. Their report is at:
https://indico.cern.ch/event/862300/attachments/1943164/3223001/PRR-1-Trigger-Processor_final_20191104.pdf

## 1. Inter-FPGA Bit Error Ratio tests with the recovered BC clock

All links were tested by Bucharest with an external clock before the review. The reviewers requested that tests of the 4.8 Gb/s links be repeated with the recovered BC clock from FELIX/TTC. Almost all links of both Sector FPGAs on the Carrier were re-tested and found to be OK, with reasonable eye openings and zero errors in a test long enough to give a BER < E-12 or better. The links tested were:

- 4 bi-dir links between each of 4 mezzanine FPGAs and its Carrier FPGA → 16 bi-dir links
- 2 bi-dir links between the two Carrier FPGAs
- 4 Bi-dir links between each Carrier FPGA and the fibres connected to the RTM optical transceivers were tested with fibres connected from one link to another.

Links to the ZYNQ FPGA could not be tested due to lack of access on the ZYNQ side. The link to the Ethernet switch (1 Gb/s) was not tested. The two links for FELIX are used to provide the recovered clock. See:
https://espace.cern.ch/ATLAS-NSW-ELX/Shared%20Documents/NSW%20Trigger%20Processor/IBERT_tests.docx

During testing, one link showed a poor eye diagram and failed during an overnight test. Repeating the test after removing and replacing the mezzanine restored a good eye diagram with no failure and a BER <E-14. The assembly of the production blades with a carrier plus two mezzanines must include testing and re-seating a mezzanine until a good eye diagram with no failure and a BER < E-14 is attained. Hopefully once connectors are seated completely, there will be no problems later.

## 2. Carrier issues document

A list of all changes to the carrier was agreed upon. It was required that any change have minimal risk. See: https://edms.cern.ch/file/2306081/1/NSW_CarrierBoardChanges.docx

## 3. Thermal tests with fans at speed 10 out of 15

Thermal tests were revisited to study the use of lower fan speeds after confirming that the chosen version for the Trigger Processor optical transceivers (microPODs) supports up to 70°C. Fan speed level were safely brought down to 60% of the full speed (level 9 out of 15), with temperatures of FPGAs and microPODs under their specification values. It was demonstrated that the temperature of the microPODs is not significantly changed by lower fan speeds; being the FPGA devices are the limiting factor for lowering fan speeds.

Power consumption was measured for the actual Micromegas FPGA current implementation for a wedge of the detector. Extrapolating that value as reference for the full blade (four mezzanine FPGAs) instead of one, our final estimate is that a NSW Trigger Processor carrier board will use

around 167W, which agrees with 165W used during thermal tests. It is important to emphasize that sTGC algorithm uses much less power than the Micromegas one.

Therefore, there is enough cooling to absorb eventual power increases in the algorithms, since considerably lower than the maximum fan speed was adequate in this test. Note that the surrounding load boards were powered at 200W during the tests, which is higher than expected.

See: https://espace.cern.ch/ATLAS-NSW-ELX/Shared%20Documents/NSW%20Trigger%20Processor/tcpaiva-nswtp-prr_response.pdf

## 4. New heat sinks for the microPODs

The concern for overheating of the microPODs was based on a supposed maximum operating temperature of 50°C. After clarification that their maximum operating temperature was 70°C and the observation that a 60% fan speed resulted in an operating temperature below 60°C, there is no need for more efficient heat sinks.

## 5. Calculation of L1A data payloads for Phase-1

### Micromegas L1A data payload

The L1A data packet consists of RAW ADDC hit data and coincidence triggered segment data.

The ADDC data is in the form of raw un-decoded ADDC GBT packet, rather than the individual hits. This means that each GBT packet containing one or more hits will contribute 96 bits to the L1A packet. Packets with no hits are suppressed.

Using an average strip hit rate of 8 kHz for $\mathcal{L}$ = 2.8×10$^{34}$ (from a plot produced by Alex Tuna at $\mathcal{L}$ = 7×10$^{34}$ giving 20 kHz), the probability of an ART GBT packet containing at least one hit is

$$\lambda = 8\ KHz\ * 2048\ strips/GBT * 25\ ns\ =\ 0.41$$
$$1 - e^{-\lambda} = 34\%$$

The ART data contribution for a 5 BC window for 32 ART fibers would be

$$0.34 * 96 * 5 * 32 = 5.2\ Kb$$

For the coincidence triggered segment data, we currently collect 304 bits. Assuming we have five segments in a L1A window this will contribute 1.5 Kb. The total data size is then 6.7 Kb; a L1A rate of 100 kHz yields a required data rate capacity of 670 Mb/s. Six E-links, each providing 250 Mb/s after 8b/10b encoding, are available, providing a total of 1500 Mb/s.

Of the 96 bits in each ART GBT packet, many will be zeroes. Data compression should be able to significantly reduce the bandwidth.

### sTGC L1A data payload

For $\mathcal{L} = 5\times10^{34}$, the table below shows that the expected number of 320Mb/s E-links needed for the sTGC Trigger Processor is 1.36. Scaling to the expected Run 3 luminosity of $3\times10^{34}$, we require 0.8 320 Mb/s E-link. Note that six such E-links are available.

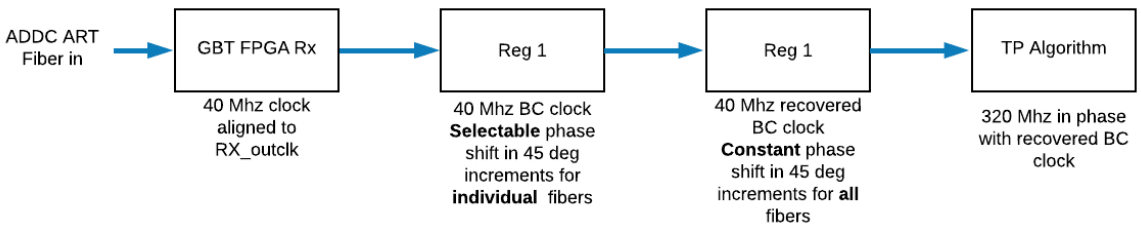
| | | |
|---|---|---|
| 16 | bits for header | |
| 104 | bits per input TDS | 104 means no compression |
| 8 | layers | |
| 1.33 | average no of bands per BC. This is an exaggeration. | |
| 3 | BCs per L1A | |
| 0.100 | L1A rate, MHz | |
| 348 | Mb/s | (435 bytes/L1A) |
| 435 | Mb/s with 8b/10b | |
| 1.36 | # E-links | @ $\mathcal{L} = 5\times10^{34}$ |

## 6. Redo BERT for the Pad Trigger input which has only a 43% eye

The two (redundant) links were retested with the recovered BC clock via the carrier on the Trigger Processor and an E-link BC clock on the Pad Trigger. Despite their non-ideal eye openings (33%, 40%), there were no transmission errors in three hours, corresponding to a BER < 8.5E-14. Both of the links showed similar behavior. We suspect that the non-ideal eye is due to the jitter of the E-link clock. The Pad Trigger will use the dedicated clock which will have substantially less jitter. The dedicated clock boards are not yet available.

## 7. Clarification of how MM crosses the 240 to 320 MHz boundary

The ADDC data from 32 fibers arrives via GBT FPGA on a 40 MHz clock that is aligned to the receiver's RX outclock. In order to align each fiber to a single recovered BC Clock, the data is registered twice using a clock that is phase aligned to the recovered BC clock. The first register uses a 40 MHz clock with settable phase adjustment in 45° increments specific to each fiber. This register will be used to account for any individual fiber length differences. The second register will also be a 40 MHz clock with settable phase adjustment but the phase will be a single constant set for all fibers. This register will align the data from all fibers and provide a fixed latency.




## 8. Carrier PCB stack-up and material choice

For the Carrier the PCB material is Megtron6.
See: https://espace.cern.ch/ATLAS-NSW-ELX/Shared%20Documents/NSW%20Trigger%20Processor/Schematics_layout/ATCA_Carrier_V2/Carrier_B16070-A%20Layers.doc

For the RTM the PCB material is FR408HR.
See: https://espace.cern.ch/ATLAS-NSW-ELX/Shared%20Documents/NSW%20Trigger%20Processor/Schematics_layout/RTM_V2/RTM_B16075-A_Layers.doc

## 9. Latency with respect to BCR of output to the Sector Logic

The start of transmission of the segment data from the Trigger Processor to the Sector Logic was measured to have fixed timing with respect to BCR across power cycles within 1 nsec. The de-serializers in the Sector Logic, however, present the data to the FPGA fabric with an uncertainty of ±1 user clock, 160 MHz, as expected. The Sector Logic handles this by waiting for the worst case before synchronizing the data to the BC clock. So although "fixed latency" across resets cannot be guaranteed, the latency is bounded. It is minimized by the fixed latency of the start of transmission from the Trigger Processor.

See Appendix A for details of the test.

## 10. Update calculation of the full Latency from IP to Sector Logic

A report as a separate document is in preparation.
Note that the latency budget is 1075ns, not 1025ns as reported in the review document.

## Appendix 1: Details of the test of Latency wrt BCR of output to the Sector Logic

The test was done as follows:

- Same TTC signal for Sector Logic and the Trigger Processor FELIX.
- The Trigger Processor ran on a clock recovered from FELIX, i.e. originating from the Sector Logic TTC system. This clock from FELIX and the TTC signals decoded have fixed latency with respect to the TTC system.
    - Note: The Trigger Processor transmits with a 320 MHz user clock, although the reference clock is 160 MHz. The Sector Logic uses a 160 MHz clock. All Trigger Processor clocks have edges aligned to the recovered BC clock.
- Sector Logic BCID was reset by BCR. BCR was monitored on an oscilloscope.
- When the Trigger Processor passed the last word of the segment packet with BCID=0 to its output serializer, it sent a pulse, P1, on a Lemo cable to an oscilloscope.
    - The time of P1 with respect to BCR was measured to be reproducible over power cycles and resets to within 1ns.
- When the Sector Logic received the segment packet with BCID=0, it sent a pulse, P2, on a Lemo cable to the oscilloscope.
- The measurements were:
    - DT1: Time between BCR and the Trigger Processor's start of transmission, P1.
    - DT2: Time between Trigger Processor's start transmission, P1, and Sector Logic's reception, P2.
- DT1 was fixed within 1 nsec over power cycles and resets
- As expected, resetting the SL receive deserializer can result in a shift of P2 with respect to BCR, i.e. P1, usually ±1 160 MHz clock, when the receiver resynchronizes. Power cycling or resetting the Trigger Processor, which deactivates and then reactivates the link, causes the Sector Logic receiver to re-synchronize.