ATLAS Note

ATLAS-INT-2020-XXX

5th May 2020

Draft version 0.2

New Small Wheel Trigger Processor

Hardware Acceptance Tests Specifications

NSW Trigger Processor Group

.

Contents

Revision History

Revision	Date	Author(s)	Description
0.1	27-04-2020	V. Martinez Outschoorn	Created. Ported document developed by R. Di Curzio Lera and T. Costa de Paiva
0.2	29-04-2020	T. Costa de Paiva	Released for review.

1 Introduction

This document outlines the testing areas and procedures required to declare the New Small Wheel Trigger Processor (TP) boards delivered by SAMWAY/IFIN suitable for operation. The acceptance tests described in this document cover only the functionality of the electronics and not the logic programmed into the boards' devices. These tests are intended to be performed on a full set of boards consisting of ATCA mezzanines, carrier board and RTM, or on system-wide arrangements with multiple of these sets. The tests perfomed by SAMWAY/IFIN after assembly of the boards and prior to these acceptance tests are summarized in Section 2.

All of the source code for the tests described in this specifications document is planned to be gathered in a common repository (link to repository in CERN Gitlab), which is distinct from the repository for the TP source code for operation. Raw and processed test results will be stored in the NSW database. In addition, reports summarizing the test results are planned to be prepared and included in the NSW TP SharePoint. These simplified reports will include some comparative analysis between boards to make sure no issue was missed during tests, the status of each board tested, as well as a pass-fail decision.

The acceptance tests described here are mostly standalone and can be carried out with a few essential resources in addition to the NSW TP hardware: Xilinx Vivado, Felix server (also used as a support computer), ATCA infrastructure and cabling. The tests are planned to be performed one board at at time by an experienced operator. The only tests that require multiple NSW TP boards are the thermal tests. These are planned to be conducted at the ATLAS ATCA Cooling Facility (in the Laser Room at Point 1).

The procedures involved in these tests are envisioned to cover each basic part of the system following an incremental approach. The goal is to reduce the likelihood of encountering major problems during the tests and by focusing on small portions for each test, facilitating the identification of potential defects. All steps described in this document have been tested with previous version of the hardware. In case a failure is identified during a test, a report is planned to be provided to the development team SAMWAY/IFIN for further instructions. One additional consideration is that the sequence of tests seeks to minimize the number of installations and removals of mezzanines on carrier boards. This is a delicate procedure and it is desirable to reduce all risk of damage. The set of carrier, mezzanines and RTM are planned to be assembled and tested as a unit without separating them unless there is a problem.

Section 3 describes the areas to be tested and the goals, while Section 4 describes each test procedure in more detail. Note that the procedures are being assembled in advance of receiving the final hardware, so they are evolving and are subject to change also once the final boards arrive.

1.1 Description of the Trigger Processor hardware

The Trigger Processor hardware consists of an AdvancedTCA (ATCA) carrier board and two mezzanine cards. The boards are an evolution of the SRS boards designed within the RD51 collaboration [1, 2]. Each mezzanine has two FPGAs, each with 36 bi-directional fiber optic links (microPODs) and 68 fast, low latency LVDS connections between the two FPGAs. The mezzanine FPGAs are Xilinx Virtex 7 XC7VX690T-FFG1158 FPGA's with GTH transceivers. The carrier FPGAs are Xilinx Kintex Ultrascale XCKU060, the carrier board manager is a Zynq XC7Z015 and the board includes gigabit Ethernet switch used has external connections to BASE I/F and the RTM, as well as internal connections to the IPMC,

Zynq and FPGA's. Figure 1 shows a block diagram of the Trigger Processor carrier board, mezzanines and RTM [3].

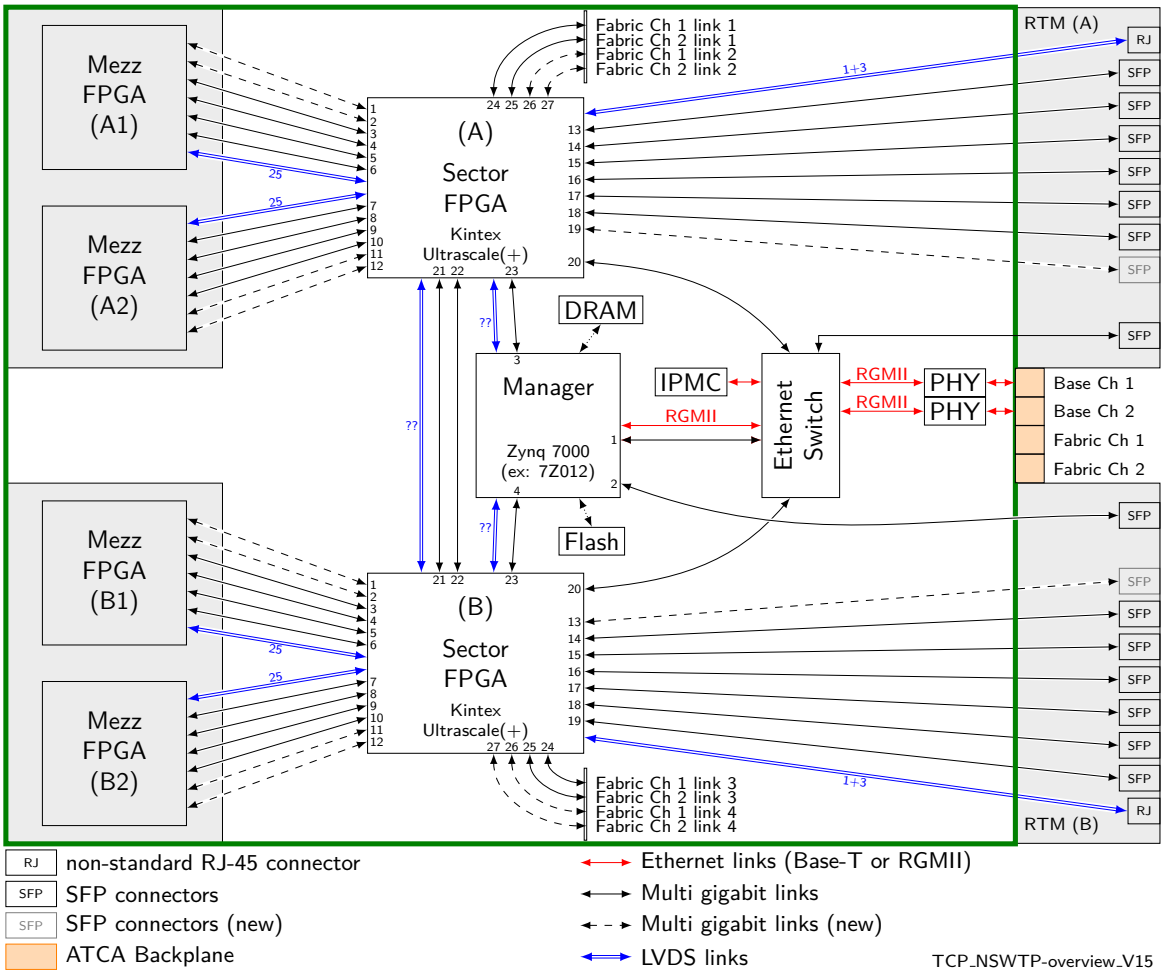

Figure 1: Trigger Processor carrier card, mezzanine cards and RTM highlighting the interconnections.

2 Tests Covered by SAMWAY/IFIN at Assembly

This section summarizes the tests perfomed by SAMWAY/IFIN after assembling the boards and before shipping them to CERN.

- Various tests of the power system
- Confirm that the FPGAs can be configured via JTAG for all combinations of the DIP switch options.
- Confirm I2C communication with the jitter cleaners and the connection to all the reference clock inputs to the gigabit transceivers
- Confirm proper operation of the clock and jitter cleaners.
- IBERT external loopback test at 10 Gb/s of the gigabit transceivers using fibers of the 36 optical pairs
- IBERT external loopback test at 10 Gb/s of the gigabit transceivers connections to the carrier FPGAs using jumpers on the mezzanine connector or two the carrier FPGAs.

- IBERT external test at 10Gb/s of the gigabit transceivers connections between the two FPGAs
- Transfer test at 1Gb/s of the LVDS connections between the two FPGAs
- Transfer test at 1Gb/s of the LVDS connections between the mezzanine and carrier FPGAs or in loopback using jumpers on the mezzanine connector
- Control and status readout of the optical transceivers using I2C

3 Areas for Testing

Test Topic	Priority	Test Procedures
3.1 Board Integrity	High	4.2, 4.3
3.2 Benchtop Operation	High	4.4
3.4 IPMC Configuration	High	4.7
3.5 ATCA Operation	High	4.8, 4.9
3.6 Device Programming	High	4.5, 4.6, 4.10, 4.12, 4.13
3.7 Ethernet Communication	High	4.11
3.8 High Speed Links	High	4.14, 4.15
3.3 Clocking	High	4.14, 4.15, 4.16
3.9 Environment Control and Monitoring	Medium	4.9, 4.17
3.10 Single-ended and Differential Signals	Low	4.16
3.11 Sector FPGA DRAM	Low	-
3.12 Backplane Communication	Low	-
3.13 Burn-in process	High	4.14, 4.15, 4.16, 4.17

3.1 Board Integrity

The carrier board and all of its components should be devoid of scratching, bending or any other form of physical damage that might impair its functions. The crate should also be dimensioned correctly so that the board fits smoothly without exerting unnecessary physical stress on in.

Covered by: Visual Inspection Test and Mechanical Test

Goal: avoid damages that can be caused by obvious problems.

3.2 Benchtop Operation

To ensure no short circuits or other electronic problems damage the board when fully powering it on, a benchtop test is run first. In this test a power supply source is connected through an adaptor to the mezzanines and the carrier board, one at a time. The voltage provide to the board under test can slowly be raised and any problems in the electronics can be pinpointed before any major damage is caused.

Covered by: Power-on and Control: Benchtop Setup Test

Goal: controlled bring-up of the boards.

3.3 Clocking

The clock is an essential resource in any digital design, and most functionalities are directly or indirectly related to clocks. This design has a very flexible and advanced clock specification, and much of it relies on proper configuration done by the programmable devices. Since it is so broadly spread through the functionalities of the board, there is no single test readily available that thoroughly evaluates the clock tree specifically. However, the verification of this resources is indirectly covered by several other tests.

Covered by: High Speed Links and Playback Test

Goal: This item assesses whether all clocking resources are functional, including generation, distribution, and jitter cleaning.

3.4 IPMC Configuration

The IPMC controls the board and can start up the other components. It has to be configured upon first use, overwriting the stock firmware. This is done over IPMI, with Shelf Manager support or directly, provided the IPMI service is available in the IPMC. There are also configurations available on the board through DIP switches and jumper headers that should be changed to make it compatible with the use of the IPMC.

Covered by: Power-on and Control: IPMC Configuration

Goal: proper IPMC operation.

3.5 ATCA Operation

The Shelf Manager controls and monitors the entire crate. In order to do so it exchanges information with the IPMC of each carrier board and, indirectly, with the MMCs (mezzanines and RTMs) on our system. These communications must be verified.

3.5.1 Hotswap and Power Negotiation

The ATCA standard defines mechanisms to hotswap Field Replaceable Units (FRU), which allows the NSWTP boards to be inserted and removed from ATCA crates without needing to power the whole system off. This feature is controlled by the Shelf Manager, which verifies if the power required by the boards to work is available. It is essential to ensure that these mechanisms are functioning.

Covered by: Power-on and Control: Hotswap Test

Goal: proper power-up of the boards in the ATCA context.

3.5.2 Sensor Monitoring

The IPMC collects important information about the blade, including temperature of components, current consumed, voltages applied and other overall flags. This data must be available for proper monitoring of the system. Since this information is obtained via I2C, accessing the information also confirms the functionality of the I2C bus tree.

Covered by: Power-on and Control - ATCA Monitoring and Control Test

Goal: Verify I2C communication and related devices/functionalities.

3.6 Device Programming

Every programmable device can be programmed in different ways depending on the situation (normal operation, recovery mode, etc). Testing these methods ensures that these resources are functioning.

3.6.1 Direct Connection

This is the most basic method. It is not planned to be used during the operation of the final system, but it guarantees that devices can be programmed in isolation. The configuration process occurs using a programming cable directly connected to the board. There is a connector to access the Zynq JTAG chain, and another connector for the other devices where the Zynq SoC is expected to route the JTAG chains to the other devices after its configuration.

Covered by: Device Configuration: Direct Access Test

Goal: Verify JTAG signals from the connector to the programmable devices:

- JTAG connector to Zynq JTAG pins.
- JTAG connector to Zynq GPIO pins.
- JTAG signals between Zynq and the other FPGAs (include mezzanine interface).
- JTAG jumper bypass connectors.

3.6.2 via RTM USB Connector

In the RTM, there is an on-board USB-to-JTAG adapter that can be used to access the main devices on the board using signals routed by the Zynq. This is important to operate boards inside of crate, where physical constraints prevent the use of programming cables connected to the boards.

Covered by: Device Configuration: Access via RTM USB Connector

Goal: verify JTAG signals between the RTM USB connector and the carrier board (local JTAG chain already covered in the previous description).

3.6.3 via on-board configuration memory

There is a flash memory attached to every programmable logic device, where the configuration can be stored. This is used to load these devices automatically with a default configuration immediately after they are powered on.

Covered by: Device Configuration: On-board Memory Test

Goal: verify communication between programmable devices and their configuration memories, as well as the memories themselves.

3.6.4 Alternative recovery path

The Zynq device is attached to two Flash memories for its configuration. They are connected to the same port, separated by a multiplexer controlled by the IPMC. As a backup measure, the memory path can be swapped between memories by the IPMC in order to change the configuration used by the Zynq device during boot. This can be done by accessing the IPMC through XVC using its Ethernet connection.

Covered by: Recovery Path Test: Secondary Zynq Configuration Memory

Goal: IPMC operation is already guaranteed by a previous stage. This test, together with those described in via on-board configuration memory, ensures the availability of IPMC control signals for the multiplexer, as well as functional memory devices.

3.6.5 Remotely via Xilinx Virtual Cable

Xilinx specified a very basic protocol to provide JTAG communication via internet called Xilinx Virtual Cable (XVC), which is directly supported by their tools. XVC facilitates remote operation. This test must be performed after the internet links are verified.

Covered by: Recovery Path Test: XVC for Zynq Configuration

Goal: Since JTAG signals are already covered by Direct Connection, this test focuses on the JTAG signals between the IPMC and the Zynq device.

3.7 Ethernet Communication

The blade possesses an on-board network switch that can be used to send data packets through an internet connection to the many ports available. For this acceptance test, the most important are to verify remote access to the Zynq and to the IPMC. This is essential to ensure remote recovery paths are viable.

3.7.1 Zynq and IPMC Ethernet links

Both the embedded Linux OS available for the Zynq device and the CERN IPMC system support internet (TCP/IP) communication. Access is provided via RTM through an on-board network switch. The Zynq and IPMC must be fully operational, as covered by previous sections.

Covered by: Ethernet Communication: Zynq and IPMC Test

Goal: to verify

- The RTM optical interface;
- The link between RTM and the on-board network switch;
- The network switch device and its configuration;
- The link between the Zynq and the network switch device;
- The link between the IPMC and the network switch device.

3.7.2 Sector FPGAs Ethernet links

Both Sector FPGAs are connected to the on-board network switch by design. However, this form of communication is provided only as an alternative means of access for development purposes.

Covered by: None, since it a non-essential feature, it is not included in the acceptance results.

3.8 High Speed Links

There are multiple gigabit links on the carrier board, allowing for very fast communication:

- 4 links between sector and mezzanine FPGAs (up to 10 Gbps)
- 8 links between mezzanine FPGAs (up to 10 Gbps)
- 1 link between the Zynq and each sector FPGA (up to 5 Gbps)
- 6 links from sector FPGAs through SFP connectors in the RTM (up to 5 Gbps)
- 36 links from each mezzanine FPGA through MTP connectors in the front panel (up to 6.4 Gbps)
- 2 links between sector FPGAs (up to 16 Gbps)

Since high speed links are essential in the NSW TP design, multiple tests are envisioned to test each part of the system. These tests are based on the Integrated Bit Error Ratio Tester (IBERT) provided by Xilinx and are planned to run for an extended period in order to accumulate statistics about the link operation. Proper cooling is required to perform these tests.

Covered by: IBERT Link Loopback: Mezzanine – Front-Panel, IBERT Link Loopback: Carrier Board Transceivers

Goal: test each of the high speed links in the design.

3.9 Environment Control and Monitoring

During regular operation, all components must be kept within their specifications regarding temperature, current, voltage and other flags. This can be monitored through the Shelf Manager, supported by the IPMC. From a system-level point of view, it is also important to understand the behavior of the environment when all the boards are operating together in the final configuration.

Covered by: Most of the tests. The full crate setup evaluates the system's behavior as a whole (see Full-ATCA Shelf Operation – Thermal Test).

Goal: Ensure cooling capabilities and long term reliable operation of the system.

3.10 Single-ended and Differential Signals

Programmable devices provide single-ended and differential signals for general purposes.

Covered by: No complete verification is available to evaluate these resources specifically, but the most relevant of them are part of the implemented functionalities of the this design. Thus, single-ended and differential signals will be indirectly evaluated.

3.11 Sector FPGA DRAM

Every Sector FPGA is accompanied by a DRAM memory, which would be used for buffering if required. These components were included for a worst case scenario and their use is not envisioned in the current plans.

Covered by: None, since it a non-essential feature, it is not included in the acceptance results.

3.12 Backplane Communication

The ATCA standard specifies resources for intra-crate communication between boards. These are included in the NSW TP project as alternative resources for extended functionalities, but is currently not planned to be used.

3.12.1 Base Interface

The possibility exists of using an ATCA hub to access the network of the blade, in contrast to an external network switch.

Covered by: None, since it a non-essential feature, it is not included in the acceptance results. It can be easily verified as an extension of the current procedure using an ATCA network switch.

3.12.2 Fabric Interface

High speed communication between blades. Some extra multi-gigabit transceivers are available on the sector FPGAs and the NSW TP group decided to connect them for this purpose.

Covered by: None, since it a non-essential feature, it is not included in the acceptance results.

3.13 Burn-in process

Burn-in is a very important process to cover in the acceptance tests and give confidence about general aspects of the hardware. Since the procedures envisioned for this acceptance tests are long and extensive, the burn-in stage is considered to happen during the procedures established, mainly during the high speed link and playback tests.

Covered by: IBERT Link Loopback: Mezzanine – Front-Panel, IBERT Link Loopback: Carrier Board Transceivers, Playback Test, Full-ATCA Shelf Operation – Thermal Test

4 Testing Procedures

4.1 Carrier Board Identification

The first step is to identify each board uniquely. All tests shall be associated to this identifier.

Information to be stored

- Serial and product number of each component.
- Any other relevant details about the boards or the setup.

Required material

- NSW TP carrier board
- NSW TP RTM
- NSW TP mezzanines (if available)
- CERN IPMC

4.2 Visual Inspection Test

Many forms of damage on the board either from the transport or overlooked during the manufacturing stage can be identified visually upon arrival of the board. This test should be done in a lab setting in case other materials are needed (magnifying glass, soldering devices, multimeters, etc).

Procedure

1. Check that every operator is wearing anti-static gear during the entire procedure
2. Check for scratches, scrapes or lacerations on the board
3. Check for corrosion of any metal on the board

4. Check for any loose soldering or overly-soldered connections
5. Check for loose, damaged, crooked or missing components
6. Check for bending of the board, that can possibly damage internal links

Information to be stored

- Photograph both sides of the board.
- Photograph the interface connectors to mezzanines, RTM, IPMC, and shelf manager.
- Report of the DIP switch and jumper headers configuration received.
- Any other relevant detail about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- NSW TP carrier board and RTM
- NSW TP mezzanine
- Possibly other inspection tools

4.3 Mechanical Test

The dimensions of the board must meet the requirements of the ATCA standard. The boards must not suffer any undue physical stress when placed inside the crate.

Procedure

1. Check the crate is powered off.
2. Position the board in front of the crate and insert it. It should fit in and slide smoothly until reaching the end of the course.
3. Turn the levers located on the sides of the carrier board until the latch locks in place, as indicated by the handle switches on the levers being lowered.
4. Raise the handle switches to unlock the board and remove them.
5. Check for any physical stress caused by the insertion/removal process.

Remarks

- Handles should not show any sign of mechanical instability when attaching and removing the board from the backplane.

Information to be stored

- Any other relevant detail about the boards or setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- NSW TP carrier board and RTM
- NSW TP mezzanine

- ATCA crate
- Possibly other electronic tools

4.4 Power-on and Control: Benchtop Setup Test

This test requires a voltage source of at least 38V and that can provide at least 2-3 amps of current. Before this operation, the carrier board DIP switches and jumper headers must be configured, as they control the proper power and activation of the board's devices.

Procedure

1. Ensure the IPMC is not installed.
2. Ensure DIP switches and jumper connectors are configured to allow power on of the devices without support from the IPMC.
3. Ensure the source utilized is set to zero voltage and current.
4. Place the carrier boards securely on a benchtop workplace.
5. Ensure fan is on and correctly positioned to cool the carrier board.
6. Plug the standalone power adapter in to the Zone-1 connector of the carrier board.
7. Connect the red and black cables to the power supply, making sure positive and negative are correct.
8. Limit the current to a reasonable value (500 mA) and start raising the voltage slowly. The current increase should follow. Watch for close to 0 V on the indicator of the power supply, current peaks, or any signs of short circuits in the board.
9. Raise the current limits if nothing is suspicious.
10. This process should be continued until the carrier board is fully powered on. Continue raising the voltage slowly until it reaches around 40 V.
11. Turn the power supply off. Remove the power supply connector from the carrier board.
12. Make sure the mezzanine has the correct JTAG chain configuration (DIP switches on the mezzanines). Install it and repeat this procedure.
13. Repeat for the other mezzanine.

Remarks

- If no mezzanine is available at the moment of this test, this sequence must be repeated later.
- If only one mezzanine is available, this procedure should be repeated for both sides, one at a time.

Information to be stored

- Current measurements when no mezzanines are connected
- Current measurements when one mezzanine is connected
- Current measurements when both mezzanines are connected (or for each side if just one mezzanine is available)
- Any other relevant detail about the boards or the setup (number of mezzanines, for instance).
- Equipment used.

- Report any issues found. Success otherwise.

Required material

- NSW TP carrier board
- 2 NSW TP mezzanines
- Voltage and Current adjustable power supply (minimum of 40V and 2A)
- Benchtop fan

4.5 Device Configuration: Direct Access Test

Since the on-board connectors are easy to access during the benchtop setup, and after checking no showstoppers are found during the previous stage, this test verifies the programmable device configuration is possible via direct access.

Procedure

1. Make sure the JTAG related jumper headers are configured in accordance with the availability of the mezzanines.
2. Make sure the carrier board is powered on and healthy as in the previous procedure
3. Connect the programming cable to the JTAG connector close to the IPMC.
4. Open Vivado, ensure the Zynq device is recognized.
5. Start the programming procedure of the Zynq Device
6. In case of error, re-try with slower frequencies.
7. Move the cable to the JTAG connector close to the RTM connector (Zone-3). JTAG chain to the other devices should be available since the Zynq is configured.
8. Program all the FPGA devices.
9. Powering off the blade, change the configuration of the JTAG bypass jumpers on the carrier board and check if the visible devices in Vivado follows that accordingly.

Information to be stored

- Devices available and devices visible in the chain
- Maximum working programming cable frequencies and configuration duration for each device.
- Any other relevant detail about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Remarks

- Very basic configuration binaries are needed for the FPGAs. Do not use fully featured designs since cooling is not appropriate.
- To install linux in the carrier board follow the instructions in this link.
- If the programming is completed without error, the test is completed.

Required material

- NSW TP carrier board and RTM
- NSW TP mezzanine
- CERN IPMC
- Computer with Xilinx Vivado IDE
- Programming cable

4.6 Device Configuration: On-board Memory Test

Since the programming cable is a reliable way to program the FPGAs (when compared to remote accesses), this setup is appropriate to program the FPGA on-board memories.

Procedure

1. Make sure the JTAG related jumper headers are configured in accordance with the availability of the mezzanines.
2. Make sure the carrier board is powered on and healthy as in the previous procedure
3. Connect the programming cable to the JTAG connector close to RTM connector (Zone-3).
4. In Vivado hardware interface, make the memories attached to the FPGAs visible.
5. For each device, program its on-board memory with the same basic binary used in previous tests.
6. In case of error, re-try with slower frequencies.

Information to be stored

- Devices available and devices visible in the chain
- Part number of the memory devices found, maximum working programming cable frequencies and configuration duration.
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Remarks

- If the programming is completed without error, the test is completed.

Required material

- NSW TP carrier board and RTM
- NSW TP mezzanine
- CERN IPMC
- Computer with Xilinx Vivado IDE
- Programming cable

4.7 Power-on and Control: IPMC Configuration

Jumper Headers should be left in a position that prevents any components from being turned on without the IPMC commands. The IPMC is programmed and the board should be powered on after insertion in the crate.

Procedure

1. Ensure IPMC is installed on the NSW TP carrier board.
2. Ensure DIP switches and jumper connectors are configured to allow power on of the devices with support from the IPMC.
3. Ensure ATCA shelf is powered off.
4. Insert carrier board into the ATCA shelf.
5. Ensure board is attached to the backplane, with handles closed but unlocked.
6. Power the ATCA shelf on
7. Ensure that only the blue LED on the carrier board front panel is on (payload power is off, no errors indicated by the red LED).
8. Program the IPMC via shelf manager (`ipmitool hpm`)
9. If no error encountered, lock (click) the carrier board handles and watch for the power negotiation process to happen (blue LED solid, then blinking, then off).

Remarks

- Handle should be unlocked during ATCA shelf power up since the IPMC will be programmed with stock firmware. Since it is hard to avoid latching the ejector handles when inserting the board, the recommendation is to do it with the ATCA shelf powered off and then to make sure that handles are unlocked before powering the crate on.
- IPMC firmware is generated per card, according to which carrier board it will be connected to.

Information to be stored

- Version of the IPMC firmware programmed. Name of the binary file used.
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- NSW TP carrier board
- CERN IPMC
- ATCA shelf
- Computer

4.8 Power-on and Control: Hotswap Test

Power negotiation is an important aspect of the ATCA standard. This resource is available not only for the carrier board, but also for mezzanines and RTM. Correct behavior is tested in multiple scenarios.

Procedure

1. Ensure that the ATCA shelf is off and that there is no RTM or other blades inserted.
2. Turn the ATCA shelf on.
3. Insert carrier into the ATCA shelf and latch (click) the handle watching for any indication of short circuits or other electronic problems (sparks, sounds, smoke, flickering LEDs).
4. Watch power negotiation process (blue LED solid, then blinking, then off).
5. Release ejector handles (click sound) and watch power negotiation process (blue LED off, then blinking, then solid). Every component should automatically deactivate.
6. Lock the front ejector handles again. Watch the LED operation as before, until everything is stable.
7. Insert the RTM at the back of the ATCA shelf, closing its handles fully (click sound). Watch the power negotiation process. The carrier board status should remain unchanged.
8. Release the RTM ejector handles and watch it deactivate. The carrier board status should remain unchanged.
9. Lock the RTM eject handles once more. Wait for it to activate.
10. Unlock the carrier board ejector handles. The blade and the RTM should both deactivate (blue LED on).
11. Lock the blade ejector handles. RTM and blade should re-enter normal operation (blue LED off).

Remarks

- Blue LED misbehavior seen on the RTM might indicate IPMC firmware problems, in contrast to hardware problems. It will require further investigation.

Information to be stored

- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- NSW TP carrier board and RTM
- 2 NSW TP mezzanines
- CERN IPMC
- ATCA shelf
- Computer

4.9 Power-on and Control - ATCA Monitoring and Control Test

After performing the previous tests, the board is on and the IPMC is functioningl. It is now possible to check the availability of basic ATCA control and monitoring resources.

Procedure:

1. Ensure ATCA shelf in powered on and the NSW TP blade is activated (blue LED off).
2. Ensure the support computer is connected to the shelf manager via network.
3. List all sensors via shelf manager (IPMI commands)
4. Compare list of sensors and reference values for sensors, it must include sensors from all modules (mezzanines, carrier boards, RTM).
5. Repeat process from item 3 at least 5 times to get a sense of average results and to ensure I2C communication is reliable. The process can be repeated further if automated.

Remarks

- Instructions about how to get the information of the sensors via shelf manager will be available as support.
- Sensor reference list will be provided as well.

Information to be stored

- A representative list of the sensors reported by the Shelf Manager.
- Any failure or values that are out of the expected range should be reported.
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found, success otherwise.

Required material

- NSW TP carrier board and RTM
- 2 NSW TP mezzanines
- CERN IPMC
- ATCA shelf
- Computer
- Network cables

Required software

- `ipmitool`

4.10 Device Configuration: Access via RTM USB Connector

Most of the local JTAG chain has already been tested, the only missing part is the link provided on the RTM trough a USB-JTAG adapter. Since the RTM is now installed in the shelf after the successful power negotiation processes, the RTM USB-JTAG chain should also be available.

Procedure

1. Make sure the NSW TP blade and RTM are properly installed in the ATCA shelf, with all the elements active.
2. Connect one side of the micro USB cable into the RTM slot (at the rear of the ATCA shelf).
3. In Vivado, look for the FPGA devices, which should be accessible in a similar way as was done before.
4. Configure all devices.

Information to be stored

- Devices available and devices visible in the chain
- Maximum working programming cable frequencies and configuration duration for each device.
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Remarks

- Same configuration files should be used.
- Since the programming cable is changed (it is using one directly provided by the RTM design), the description of the link in Vivado will change slightly as well.
- If the programming is completed without error, the test is completed.

Required material

- NSW TP carrier board and RTM
- NSW TP mezzanine
- CERN IPMC
- Computer with Xilinx Vivado IDE
- Programming cable

4.11 Ethernet Communication: Zynq and IPMC Test

Issuing ping commands through the Network Switch to the Zynq and IPMC devices is sufficient to test the communication. Note the operation of the Zynq and IPMC is verified in previous tests. This test validates the path including access through the RTM and on-board network switch.

Procedure

1. Ensure the NSW TP carrier board and RTM are correctly inserted and activated in the ATCA shelf manager.
2. Connect the SFP-RJ45 adapter to the proper SFP interface on the RTM.

3. Connect the network cable between the support computer and the RTM using the interface prepared above.
4. Make sure the corresponding interface in the computer is configured with a compatible IP address.
5. Start the Wireshark software in the support computer, monitoring the interface connected to the NSW TP.
6. Perform ping requests for the Zynq and IPMC systems.
7. Interrupt the Wireshark monitoring and save the log.
8. Using SCP, transmit a reasonably-sized file to the Zynq Linux OS. Repeat this process a few times to obtain an average transmission period.

Information to be stored

- A Wireshark log of at least 3 minutes of duration of the monitored interface.
- Report about the file transmission with average duration of the process.
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Remarks

- Static IP addresses for the IPMC and for the Zynq Ethernet interfaces will be available in the support documentation.
- Instructions related to the file to be transmitted will be available in additional documentation, as well as Zynq Linux OS log in information.
- Different IP addresses might be needed in the support computer interface to communicate with both systems. In Linux OS, more than one IP address can be configured to an interface.
- A DHCP server might be needed in the support computer to distribute dynamic IP addresses to the IPMC and to the Zynq interfaces.

Required material

- NSW TP carrier board
- NSW TP RTM
- SFP-RJ45 adapter
- Support computer
- Copper network cable

Required software

- Ping client
- Wireshark
- SCP

4.12 Recovery Path Test: XVC for Zynq Configuration

Most of the Zynq recovery path is verified when testing the internet access to the IPMC (see Ethernet Communication: Zynq and IPMC Test) and when configuring the Zynq with direct access (see Device Configuration: Direct Access Test). The only part missing is the JTAG link between the IPMC and Zynq.

Procedure

1. Make sure the NSWTP carrier board is activated and network configured properly, as done in the previous stages.
2. Ensure ATCA shelf manager monitoring is happening as usual.
3. Open an XVC endpoint in Xilinx Vivado Hardware Server pointing out to the XVC service in the IPMC.
4. Reconfigure the Zynq with the proper configuration image.
5. Watch the reboot process and ensure that the Linux OS is fully operational again.

Remarks

- IPMC IP address and XVC TCP port will be available in additional documentation.
- Zynq Linux OS image and configuration instructions are the same as provided in the link in Section 4.5.

Information to be stored

- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- ATCA shelf
- NSW TP carrier board
- NSW TP RTM
- SFP-RJ45 adapter
- Copper network cable
- Support computer

Required software

- Vivado

4.13 Recovery Path Test: Secondary Zynq Configuration Memory

As a last option for remote recovery attempts, the NSW TP design provides a secondary memory for the Zynq to store a golden firmware version. The choice of which memory is used is controlled by the IPMC (see Alternative recovery path). As before, most of the required resources are already tested by previous stages. This step also prepares the secondary memory with a valid configuration.

Procedure

1. Make sure the NSWTP carrier board is activated and network configured properly, as done in the previous stages.
2. Ensure ATCA shelf manager monitoring is happening as usual.
3. Open an XVC endpoint in Xilinx Vivado Hardware Server pointing out to the XVC service in the IPMC.
4. Select the Zynq device (it should be the only one on the list) and expose its configuration memory.
5. Change the enabled memory via IPMC command.
6. Reboot the Zynq system via IPMC command and realize that the Zynq boot fails (red LED or `ping` request via internet after some tens of seconds). See related comment in remarks.
7. Using the Xilinx Vivado interface, reconfigure the selected Zynq memory.
8. Reboot the Zynq device via IPMC command and observes system to be available again.

Remarks

- Instructions to select the memory used by Zynq via IPMC is available as support material.
- IPMC IP address and XVC TCP port will be available in additional documentation.
- Zynq Linux OS image and configuration instructions are the same as provided in the link in Section 4.5.
- If Zynq boot does not fail after changing target memory, it means that both memories were previously configured. For this test, one of the memories should be erased and than it should be proven that the Zynq boots with one of them and it does not with the other. This is important to prove that the IPMC signal is delivered correctly.

Information to be stored

- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- ATCA shelf
- NSW TP carrier board
- NSW TP RTM
- SFP-RJ45 adapter
- Copper network cable
- Support computer

Required software

- Vivado
- `ipmitool` or `netcat`

4.14 IBERT Link Loopback: Mezzanine – Front-Panel

This set of tests not only aim to evaluate whether the fast communication channels work, but also how well they work. Eye-diagrams will be generated for each link and related configuration. The mezzanine transceivers on the front panel can be tested independently of other transceivers. The tests must be performed for all new mezzanines. It relies on the IBERT cores provided by Xilinx.

Procedure

1. Ensure the ATCA shelf, NSW TP set of boards (carrier, mezzanines and RTM) are inserted and activated.
2. Plug loopback cables on the MTP24 interfaces of the mezzanines.
3. Ensure network is properly configured to access the shelf manager.
4. Ensure NSW TP board is monitored by the shelf manager, specifically the mezzanine temperature sensors (FPGAs and transceivers).
5. Configure the NSW TP Thermal Tests GUI to track the environment of the board and log information each minute.
6. Ensure USB cable is connected to the RTM providing access to the JTAG chains in the carrier board.
7. Open the Vivado Hardware Manager and establish connection with the NSW TP JTAG chain
8. Ensure reported FPGA temperatures in Vivado are similar to what has been seen by the shelf manager
9. Program one mezzanine FPGA with the IBERT configuration and wait for its temperature to stabilize.
10. Program the other mezzanine FPGA with the IBERT configuration and wait for its temperature to stabilize.
11. Repeat the process starting from item 8 for the second mezzanine if available.
12. Configure the IBERT parameters (bandwidth, pattern) via Vivado GUI for all links.
13. Use the Vivado debug interface to reset error counting for all the links.
14. Let it run for at least 4 hours. The setup must not be left without in-person supervision for more than 15 minutes.
15. When the test is done, save all reports from Vivado (IBERT) and from the Thermal GUI
16. Export the eye diagram provided by Vivado for each link.

Remarks

- Configuration files for the mezzanine FPGAs are available from the main NSW TP Gitlab group area.

- If more than one board is tested at a time, extra care should be taken with the temperature of the components, mainly when the carrier board environment is not refrigerated.
- Extra information about IBERT configuration will be provided as support.

Information to be stored

- IBERT reports from Vivado
- Eye diagrams for the links
- Logs from Thermal GUI
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- NSW TP carrier board
- NSW TP mezzanine
- NSW TP RTM
- CERN IPMC
- ATCA shelf
- MTP loopback cables
- USB cable

Required software

- Vivado
- NSW TP Thermal Tests GUI

4.15 IBERT Link Loopback: Carrier Board Transceivers

This set of tests not only aim to evaluate whether the fast communication channels work, but also how well they work. Eye-diagrams will be generated for each link and related configuration. The Sector FPGA transceivers are exposed in two main interfaces, the mezzanine and the RTM. The RTM interfaces can be tested directly with loopback cables, but in order to test the Mezzanine links, a support configuration binary on the mezzanine FPGA is required to enable the corresponding transceivers and setup the clocks. This test must be performed for all new carrier boards. It relies on the IBERT cores provided by Xilinx.

Procedure

1. Ensure ATCA shelf, NSW TP set of boards (carrier, mezzanines and RTM) are inserted and activated.
2. Plug loopback cables on the relevant SFP interfaces of the RTM.
3. Ensure network is properly configured to access the shelf manager.
4. Ensure NSW TP board is monitored by the shelf manager, specifically the mezzanine and sector FPGA temperature sensors.
5. Configure the NSW TP Thermal Tests GUI to track the environment of the board and log information each minute.
6. Ensure USB cable is connected to the RTM providing access to the JTAG chains in the carrier board.

7. Open Vivado Hardware Manager and establish connection with the NSW TP JTAG chain
8. Ensure reported FPGA temperatures in Vivado are similar to what has been seen by the shelf manager

9. Program one mezzanine FPGA with the support configuration binary and wait its temperature to stabilize.
10. Program the other mezzanine FPGA with the support configuration binary and wait its temperature to stabilize.
11. Program the related sector FPGA with the IBERT configuration and wait its temperature to stabilize.
12. Configure IBERT parameters (bandwidth, pattern) via Vivado GUI for all links.
13. Repeat the process starting from item 8 for the second mezzanine if available. If not available, after finishing this test, the mezzanine should be swapped to other interface on the carrier and the tests repeated.
14. Use the Vivado debug interface to reset error counting for all the links.
15. Let it run for at least 4 hours. The setup must not be left without in-person supervision for more than 15 minutes.
16. When test is done, save all reports from Vivado (IBERT) and from the Thermal GUI
17. Export the eye diagrams provided by Vivado for each link.

Remarks

- Configuration files for the mezzanine FPGAs are available from the main NSW TP Gitlab group area.
- Extra information about IBERT configuration will be provided as support.
- If more than one board is tested at a time, extra care should be taken with the temperature of the components, mainly when the carrier board environment is not refrigerated.

Information to be stored

- IBERT reports from Vivado
- Eye diagrams for the links
- Logs from the Thermal GUI
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- NSW TP carrier board
- NSW TP mezzanine
- NSW TP RTM
- CERN IPMC
- ATCA shelf
- MTP loopback cables
- USB cable

Required software

- Vivado
- NSW TP Thermal Tests GUI

4.16 Playback Test

This is essentially a TP algorithm operation test, and will consist of configuring one mezzanine to be an ADDC emulator and sending GBT hit data from it. The GBT data will be received as if sent from the ADDCs with no special accommodations made. The mezzanine that serves as the ADDC emulator does not need to be on the same carrier or even in the same ATCA shelf as the targets. The full MM algorithm will be used, including all 32 input fibers. This is a full level test and can be considered a burn-in process.

Procedure

1. Before starting, ensure that the carrier board and RTM are properly engaged in the ATCA shelf, Zynq and IPMC are programmed, and that all sector and mezzanine FPGAs that will be tested are programmed and under normal operation.
2. Ensure all the required optical links between mezzanines are connected and functional.
3. Ensure all the required optical links between the FELIX server and the NSW TP boards are connected and functional.
4. Ensure all the access to shelf manager is available.
5. Start NSW Thermal GUI to track environment information from the ATCA shelf each minute.
6. Prepare FELIX core environment and start it.
7. Start SCAX OPCUA server connected to the FELIX core.
8. Start the OPCUA client connected to the SCAX OPCUA server
9. Run executable tests prepared with the swROD framework
10. Process received results and make sure tests finished as expected.

Remarks

- Instructions assume that the swROD-based executable tests are prepared beforehand and no other new test is needed.
- Extra support information about dealing with FELIX, SCAX, and swROD framework will be provided with this guide.

Information to be stored

- All the tests results should be stored.
- Thermal GUI logs should be stored.
- Any other relevant details about the boards or the setup (FELIX core, SCAX, etc).
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- NSW TP mezzanine

- NSW TP carrier board and RTM
- CERN IPMC
- ATCA ATCA shelf
- FELIX computer
- MTP24 optical cables
- LC Optical fibers
- SFP-RJ45 adapters
- MTP24/LC breakout cable (box)
- USB cable

Required software

- FELIX Core
- SCAX OPCUA server
- SCAX OPCUA client
- Tests
- Vivado
- NSW TP Theraml GUI

4.17 Full-ATCA Shelf Operation – Thermal Test

This test uses the thermal FPGA configuration for a full crate operation with 8 NSW TP board sets (carrier, mezzanines and RTM). Programming files are available from tests performed previously with prototypes. This test can only be performed at CERN in the ATLAS ATCA Cooling Test Facility. This is a system-level test and can be considered a burn-in process.

Although this test is prepared as standalone, all the configuration files of the FPGAs were prepared to mimic the resource utilization of the actual algorithms, including speed links and power consumption on the FPGAs. The design is divided into hundreds of small blocks in a way that it can be activated in step-by-step way, preventing damage of the system, for example in case the cooling is insufficient.

Procedure

1. Ensure ATCA shelf, NSW TP set of boards (carrier, mezzanines and RTM) are inserted and activated.
2. Plug loopback cables on the MTP24 interfaces of the mezzanines.
3. Ensure network is properly configured to access the shelf manager.
4. Ensure NSW TP board is monitored by the shelf manager, specifically the mezzanine temperature sensors (FPGAs and transceivers).
5. Configure the NSW TP Thermal Tests GUI to track the environment of interesting NSW TP boards in the ATCA shelf (sides or centrally positioned blades) and log information each minute.
6. Ensure USB cable is connected to the RTM providing access to the JTAG chains in the carrier board.
7. Open Vivado Hardware Manager and establish connection with the NSW TP JTAG chain
8. Ensure reported FPGA temperatures in Vivado are similar to what has been seen by the shelf manager

9. Configure each and every FPGA with appropriate thermal configuration binaries (mezzanine or sector FPGA version).
10. Configure ATCA setup to run with expected power and airflow.
11. Once the temperatures of all boards are stable, enabling of the resources of the FPGAs is needed and should be performed for each FPGA.
12. Let it run for at least 6 hours. The setup must not be left without in-person supervision for more than 15 minutes.
13. When test is done, save all the environment log generated by the Thermal GUI.

Information to be stored

- Environment log generated by the Thermal GUI.
- Any other relevant details about the boards or the setup.
- Equipment used.
- Report any issues found. Success otherwise.

Required material

- 16 NSW TP mezzanines
- 8 NSW TP carrier boards
- 8 NSW TP RTMs
- 8 CERN IPMCs
- 1 14-slot ATCA shelf
- MTP24 optical cables
- USB cable
- Support computer

Required software

- NSW TP Thermal GUI
- Vivado

References

[1] eicSys GmbH, *EATCA-100, FPGA based ATCA blade for RD51 SRS system, User Manual*, (2014), URL: https://edms.cern.ch/file/1476256/1/NSW_TriggerProcessor_SRS_ATCA_PDR_20150209.pdf (cit. on p. 4).

[2] Sorin Martoiu, *High-Density Optical Receiver Mezzanine board for ATCA-SRS*, (2015), URL: https://edms.cern.ch/file/1476256/1/NSW_TriggerProcessor_SRS_Mezzanine_PDR_20150209.pdf (cit. on p. 4).

[3] ATLAS New Small Wheel Trigger Processor Group, *NSW Trigger ProcessorCarrier Board Version 2 Specification*, (2018), URL: https://espace.cern.ch/ATLAS-NSW-ELX/Shared%20Documents/NSW%20Trigger%20Processor/NSWTP_NewCarrierBoardRequirements.pdf (cit. on p. 5).