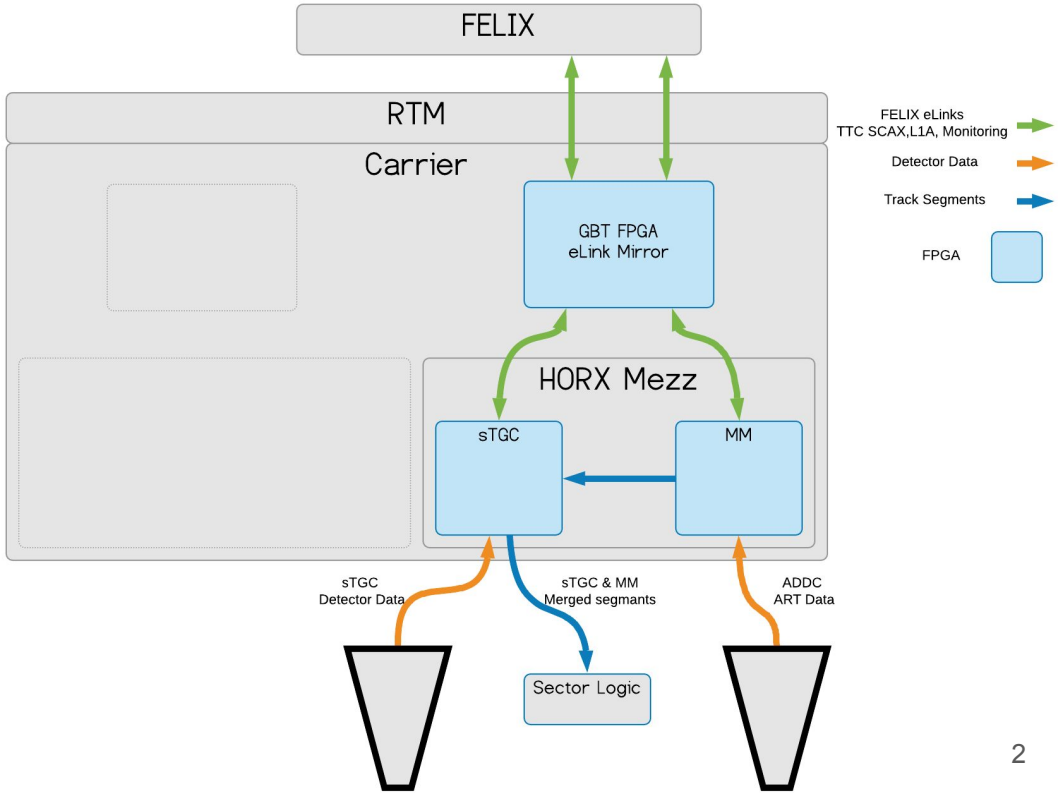
PRR of the NSW Trigger Processor

# Micromegas: L1A and readout (thru carrier). Algorithms and time alignment.

Nathan Felt
With everyone in the TP group
PRR of the NSW Trigger Processor 2020 May 06

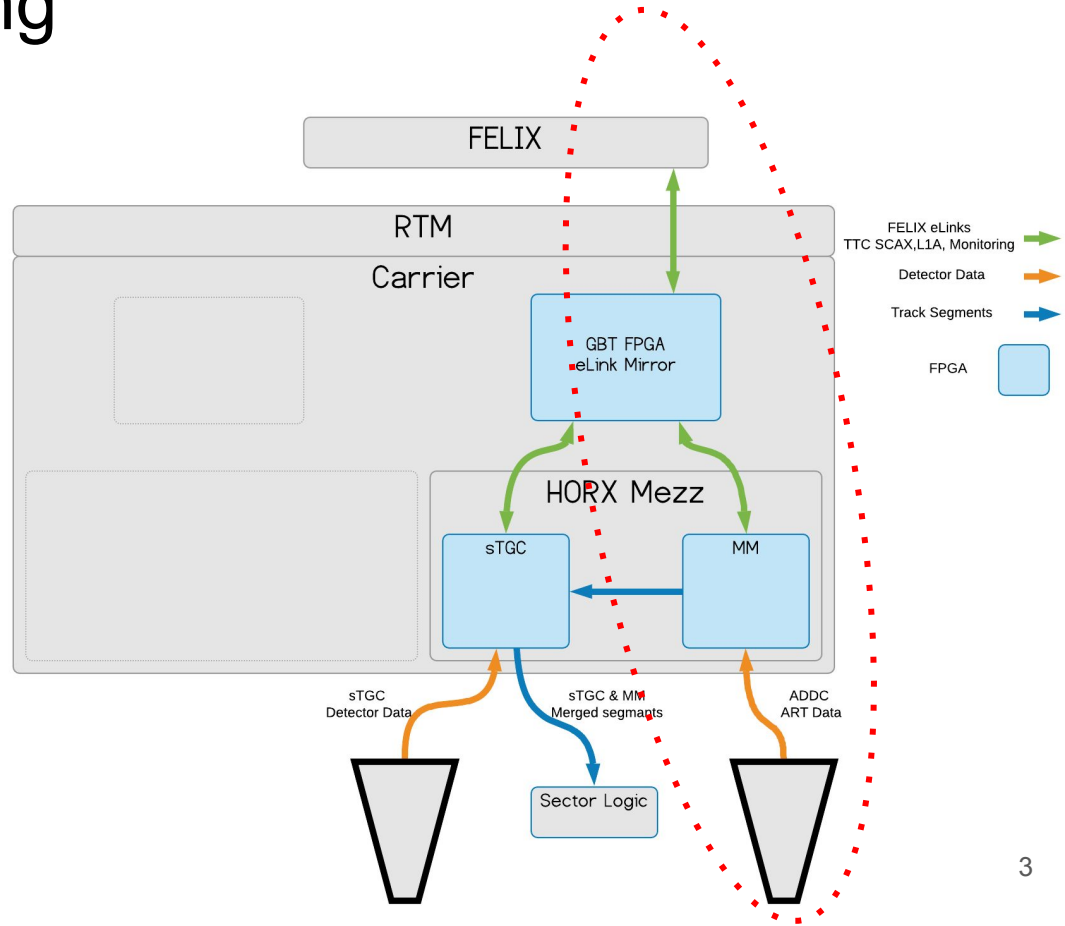
# Overview / Data Paths

- FELIX Communication via RTM
  - SCAX configuration, Register R/W
  - BC clock recovery at carrier
  - TTC received / distributed at carrier
  - L1A and Monitoring packets
- Front panel fiber detector data
- MM track segment lateral transfer to sTGC for merging

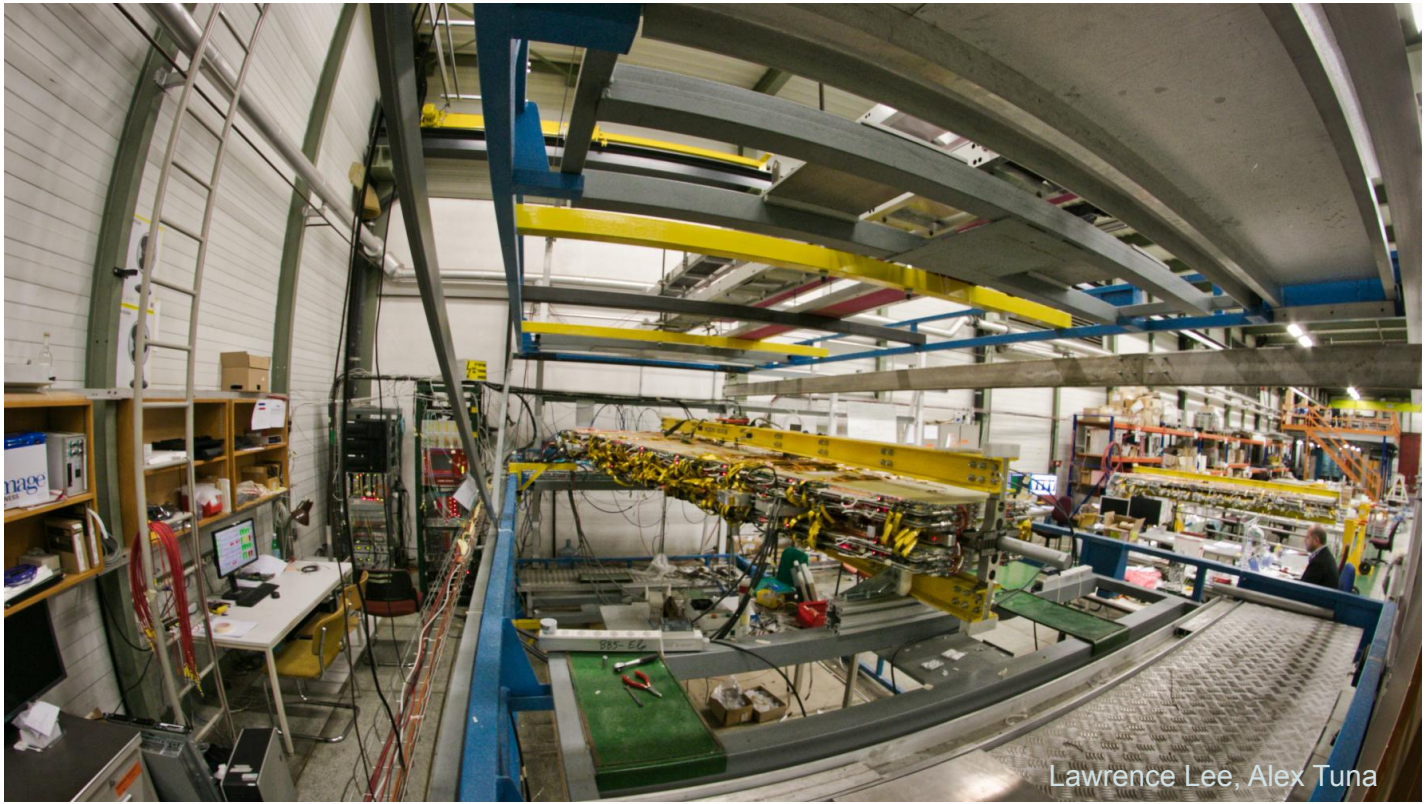


# BB5 MM Commissioning

- FELIX Communication via RTM
  - SCAX configuration, Register R/W
  - BC clock recovery at carrier
  - TTC received / distributed at carrier
  - L1A and Monitoring packets
- Front panel fiber detector data
- Full sector MMTP algorithm

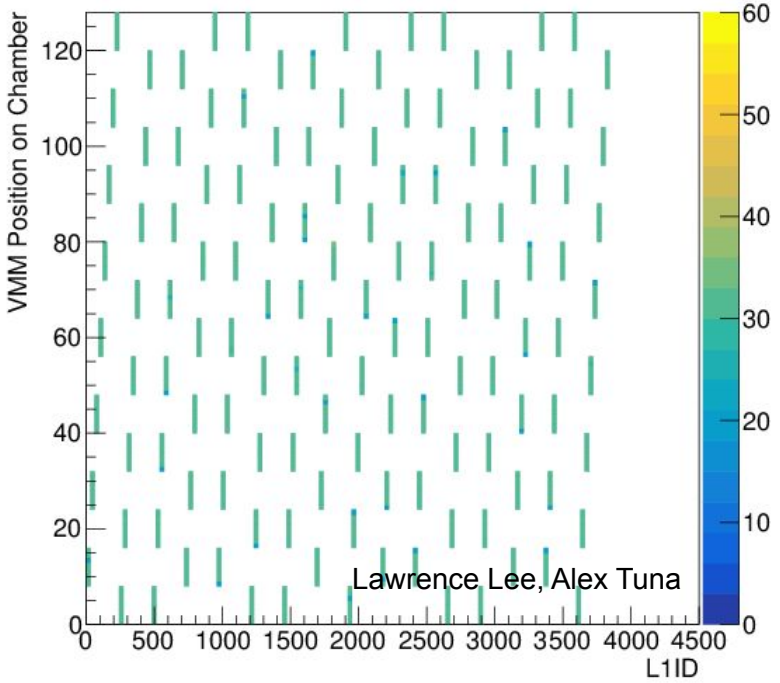


# BB5 MM Commissioning



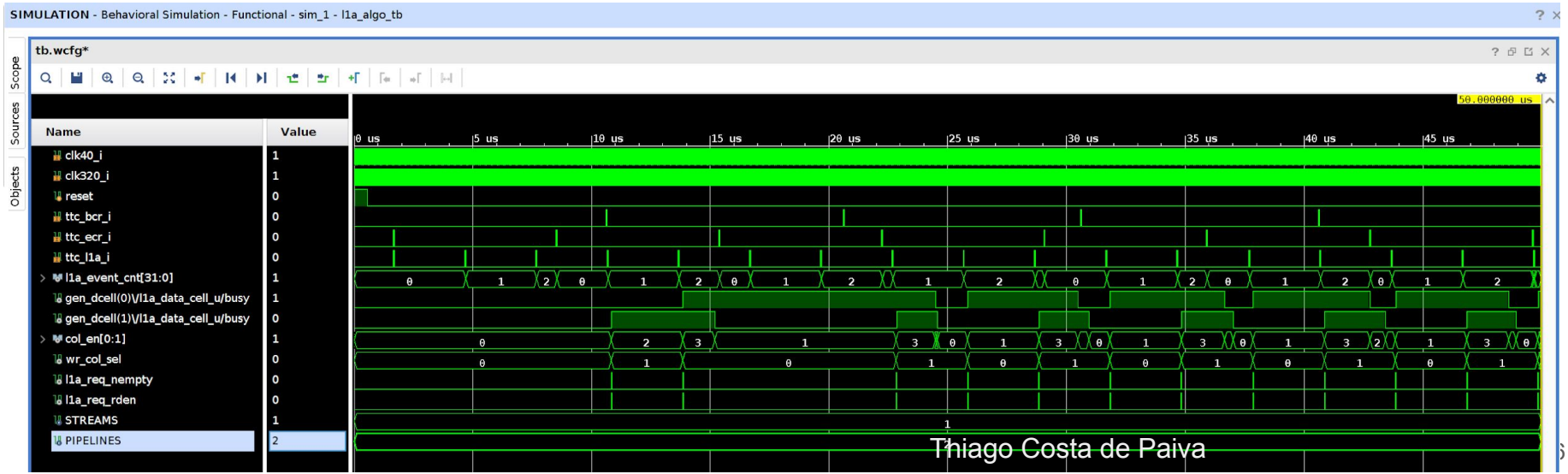
# BB5 ART path connectivity tests using L1A packets

- Sector A14
- All VMMs on entire sector independently pulsed synchronous to L1A
- Raw ART data taken from L1A packets
  - Data in plot read out through front panel fibers
  - Have since started using eLinks through the carrier
- Packets recorded with the swROD to disk.
- All VMMs on sector are accounted for in L1A packet data



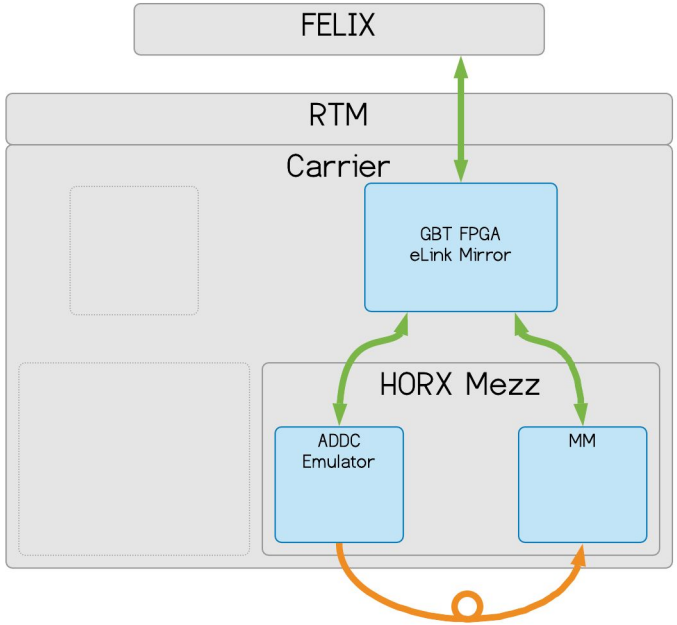
# L1A Packet Builder Firmware update

- Key improvements
  - Handling of multiple L1A's in a readout window (parameterized)
  - Event Count Reset is available
- Currently being tested at the "Massachusetts" test stand.



# Massachusetts NSW Hardware Remote Testing

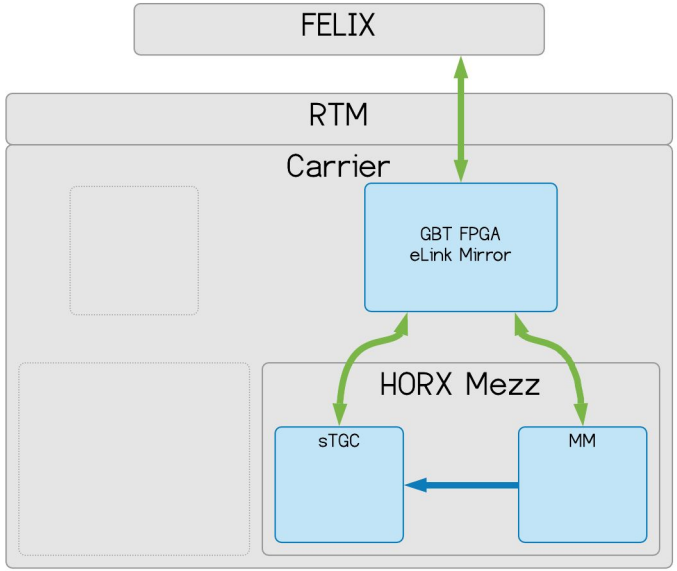
- ADDC Emulator is now standalone and can be run on a different Mezz / carrier
- eLinks from 1 FELIX fiber is shared between two Mezz FPGAs
  - Second FELIX fiber has been implemented and currently being tested
- 36 front panel fibers between FPGAs
- Currently transitioning the MMTP playback tests to use the NSWConfiguration Software
  - Firmware development
  - Production board testing
- Remote testing hardware has been working well



# Massachusetts NSW Hardware Remote Testing

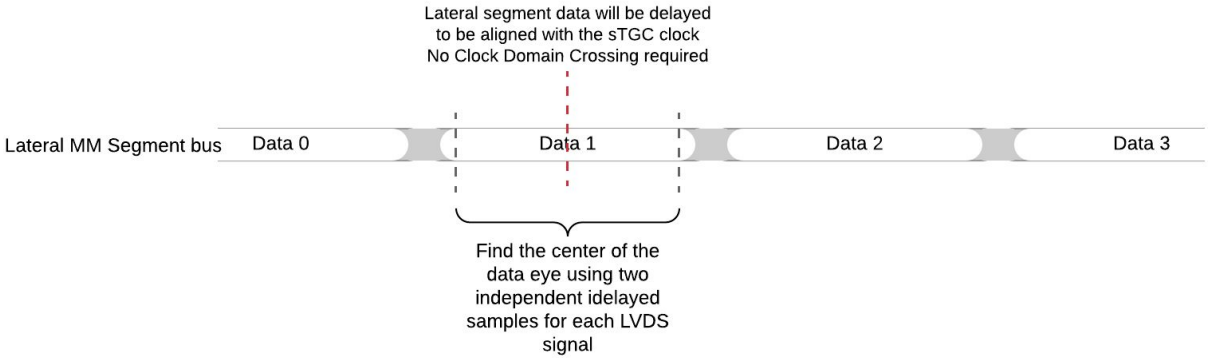
# Lateral Transfer of MM Segments to sTGC FPGA

- Initial testing of interface using pattern data Tx in MMTP
- Further pattern data testing on the sTGC side by George Chatzianastasiou
- With access to hardware, we can test using coordinated playback testing with emulated detector data on the front panel fibers



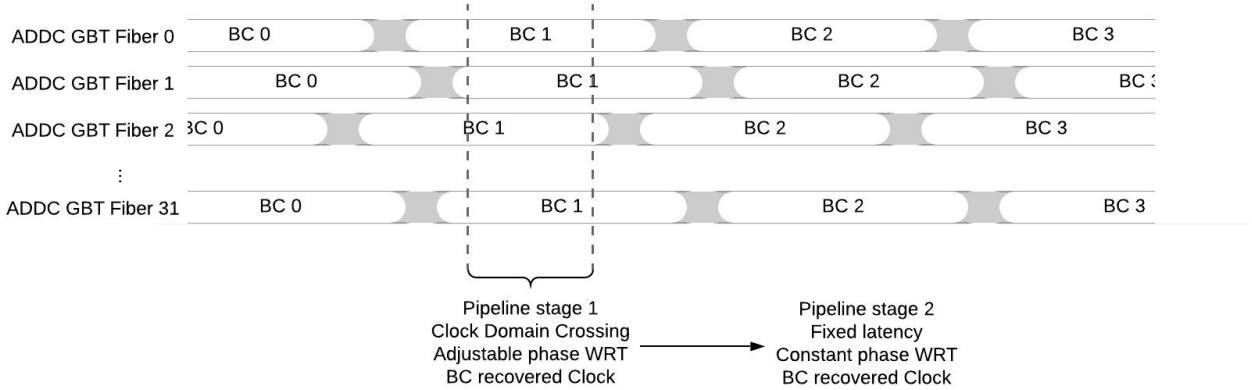
# Lateral Transfer of MM Segments to sTGC FPGA

- Data transfer on 16 x 640 MS/s LVDS - up to 8 segments / BC
- The data bus is delayed by the receiver such that the center of the data eye is aligned with the sTGC 320MHz clock.  No Clock Domain Crossing.
- The receiver continuously looks for data errors and can adjust the delay.
  - Two independent idelays per signal

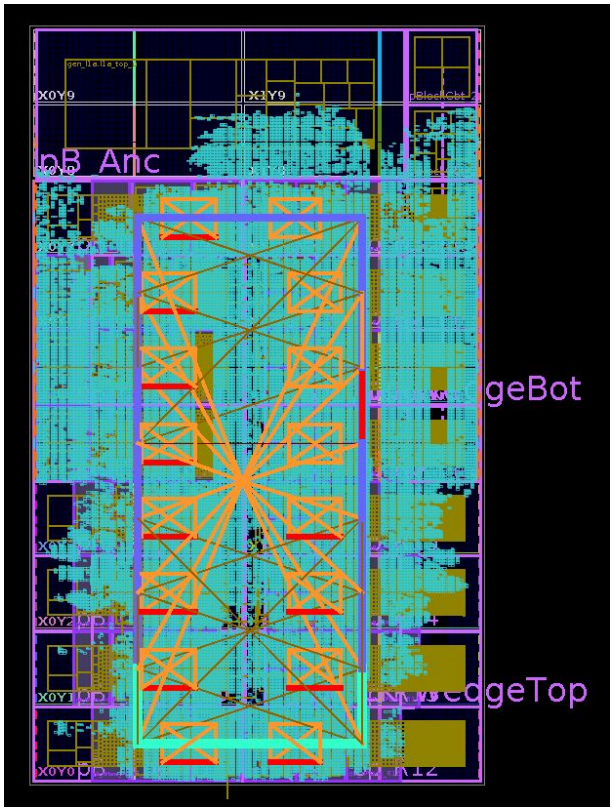


# ADDC ART Data Fiber Alignment

- ADDC Fibers are aligned using two 40 MHz pipeline stages phase locked with the BC clock
  - The first stage is the Clock Domain Crossing automatically set by the TP to latch the data within the “aligned” window
  - The second is a manual setting to provide a fixed latency
- For details of the ART ASIC alignment and calibration please refer to Alex Tuna’s recently presented talk [Calibrating ART]



# Current MMTP Placement




- 65% LUT resource usage
  - congestion / latency requirement is the real limiting factor
- TP algorithm updated to accommodate detector cabling
  - Previous version minimizes the front end electronics needed to produce a coincidence trigger
  - Much more difficult placement
  - Impact on timing
- Interactive physical optimization used to re run the Vivado place after initial physical optimization
  - Second place step now knows about replication
- Full design still has ~ -100ps WNS that is expected to be solved with better placement constraints … and a pipeline stage if necessary

# Power Requirement (Measured)

- Carrier board and RTM power consumption: 41.73 W
- Mezzanine power consumption: 11.13 W
- Sector FPGA power consumption: 1.39 W
- Mezzanine FPGA power consumption, µPod included: 25.04 W
- Estimated total power consumption: 166.92 W

# Micromegas Trigger Processor Latency

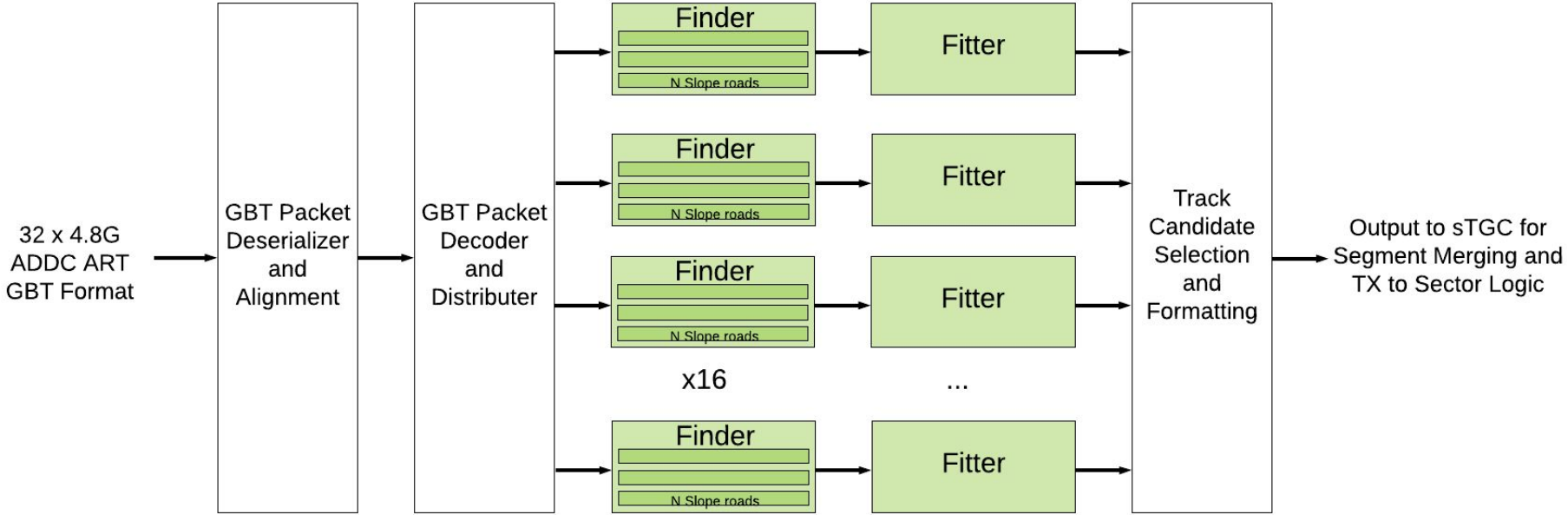
- The latency from VMM output to Trigger Processor track segment coincidence trigger (finder) have been measured during a hardware integration workshop.
- Timing measurements for the Micromegas track segment fitter components and segment lateral transfer are taken from behavioral simulations.
- At a latency of 904 ns, the MM segments will arrive at the sTGC merge block before the sTGC segments, 959ns.
    - This estimate assumes a three bunch crossing hit integration window.
    - Studies suggest the hit integration window will need to be increased to four or more bunch crossings.
    - Each additional bunch crossing will increase the latency by 25ns.

# MMTP Firmware ToDo List

- Resolving the last -100ps WNS
- MM Finder algorithm duplicate track removal
- Track fit parameter adjustment
- Testing recently added features
  - Multiple L1A's in a readout window
  - ADC fiber clock phase auto align
  - Adding new data types to the L1A / Monitoring packets
  - Automatically suppressing hot VMM channels
- Firmware and bug fixes needed for the commissioning effort

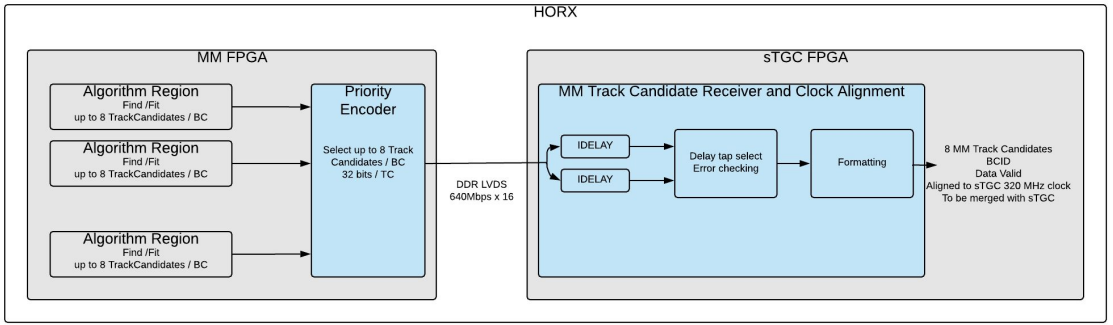
# “Backup” slides

# MM Trigger Processor Algorithm



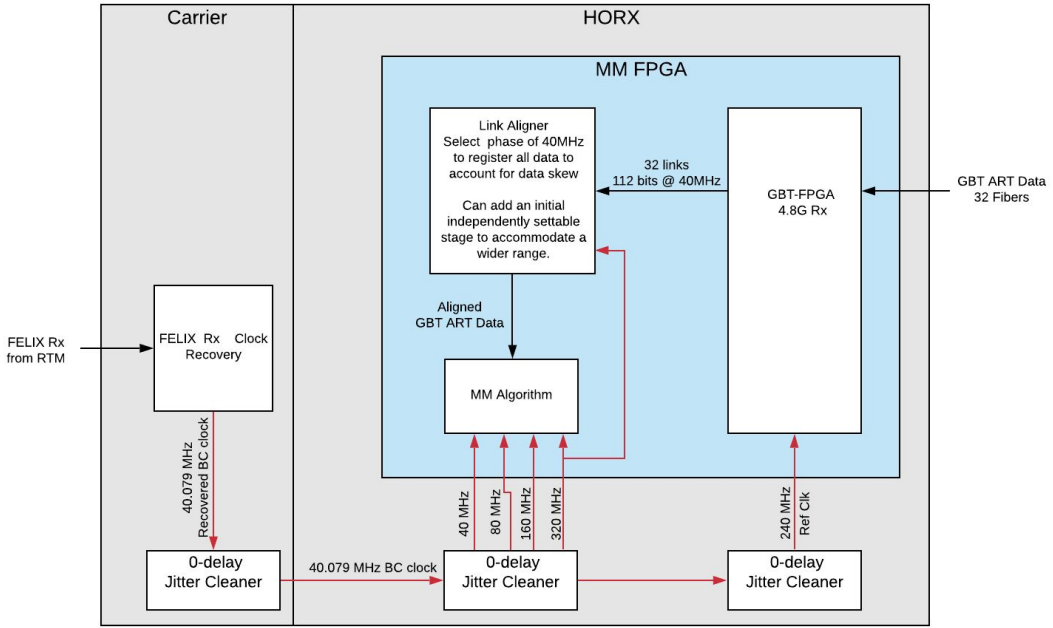
# MM to sTGC segment transfer

- Collects up to 8 MM segments from MMTP algorithm regions each BC
- Segments transferred to the sTGC FPGA using 16x 640 Mb/s LVDS signals
- The segment receiver in the sTGC FPGA uses independently delayed versions of the same signal
  - Set the sampling point to the center of the data eye
  - Check for errors
  - Provide segment data to the sTGC logic that will be aligned to the sTGC clock with no additional clock domain crossing necessary.



# MMTP Clock Network and ADDC Alignment

Link aligner uses two 320Mhz pipeline stages to selectively delay fiber data and align data from 32 ADDCs

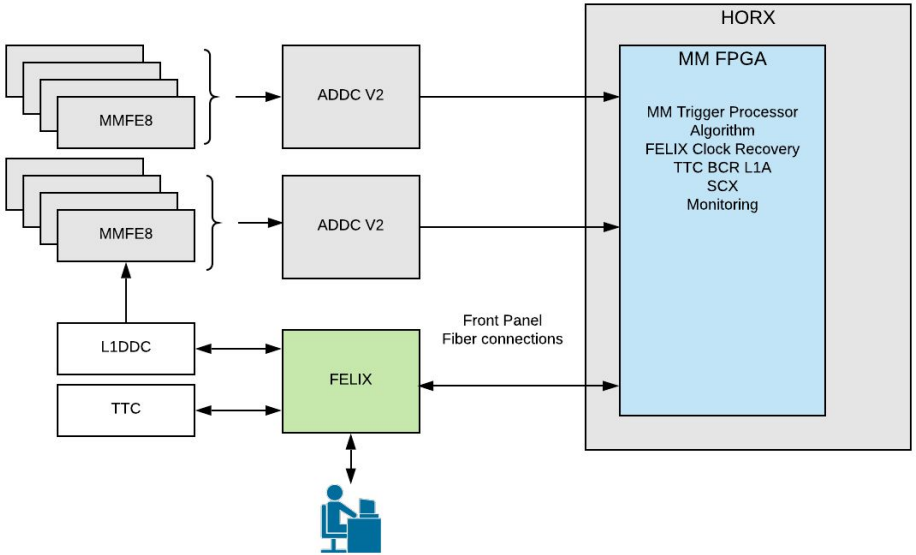


# Hardware Implementations

- VC707 development board implementation
  - 1/8 th wedge algorithm slice.
  - Python/UDP DAQ.
  - Algorithm evaluation
    - in a cosmic ray test stand and documented in ATL-COM-MUON-2018-003 https://cds.cern.ch/record/2302523 (Alex, Ann, Paolo)
    - Test-beam (Alex, Ann)
- HORX implementation
  - Full wedge algorithm.
  - Tcl/JTAG DAQ Transitioning to a FELIX based DAQ
  - Tested using
    - internally generated ART data that is sent through a loopback fiber.
    - CERN vertical slice ART data chain.

# CERN Vertical Slice  ART Data Chain

- HORX clock recovered from FELIX in MMTP
- Configuration / Monitoring via FELIX / SCX
- MMTP synchronization using TTC Bunch Crossing Reset and L1A signals via FELIX
- ART data chain
  - 8 MMFE8
  - 2 ADDC
- Track candidates from pulsed VMMs collected from Trigger Processor using the FELIX / monitoring functionality
- Latency measurement in past VS from VMM ART flag to coincidence trigger matches calculated estimate.
  - Total latency  event to sector logic input 1026ns with a 4 BC window

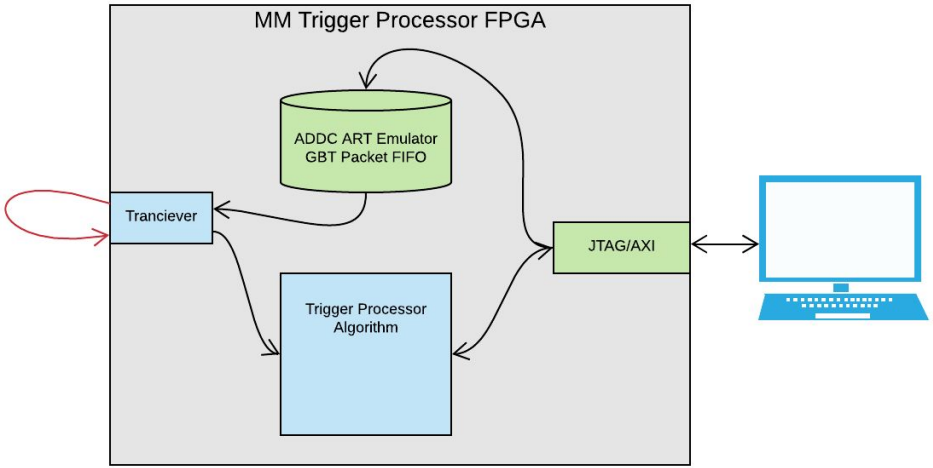


# MM Remaining Tasks

- Finder track duplicate removal
  - Include ART Data in monitoring data path
- Monitoring / L1A data path implementations are currently being tested on hardware using ⅛ wedge algorithm implementation.  This needs to be scaled up to the full algorithm implementation
  - Implementation size is a selectable parameter but may need some pipelining and placement constraints to meet timing requirements
- GBT ART data packet alignment to account for different fiber lengths
- Alignment correction for rotation and twist
- Mapping GBT data to match ADDC to MMFE8 cabling
  - Current mapping MMFE8s in Z to minimize number of ADDCs needed to produce a trigger
- Adjusting fit parameters to accommodate “diamond” finder algorithm

# MM Current Loopback Hardware

- JTAG AXI interface used for FPGA DAQ communication
- Python, Tcl, Matlab used for data formatting, DAQ, and verification
- ADDC ART data loaded into FIFO
- Receives loopback fiber as if sent from ADDC
- Option to bypass transceiver inside FPGA

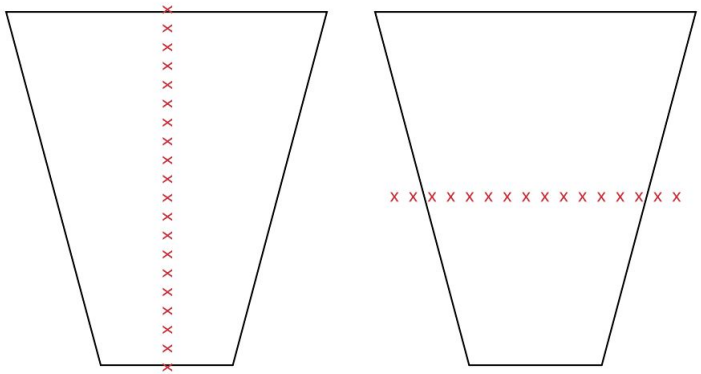


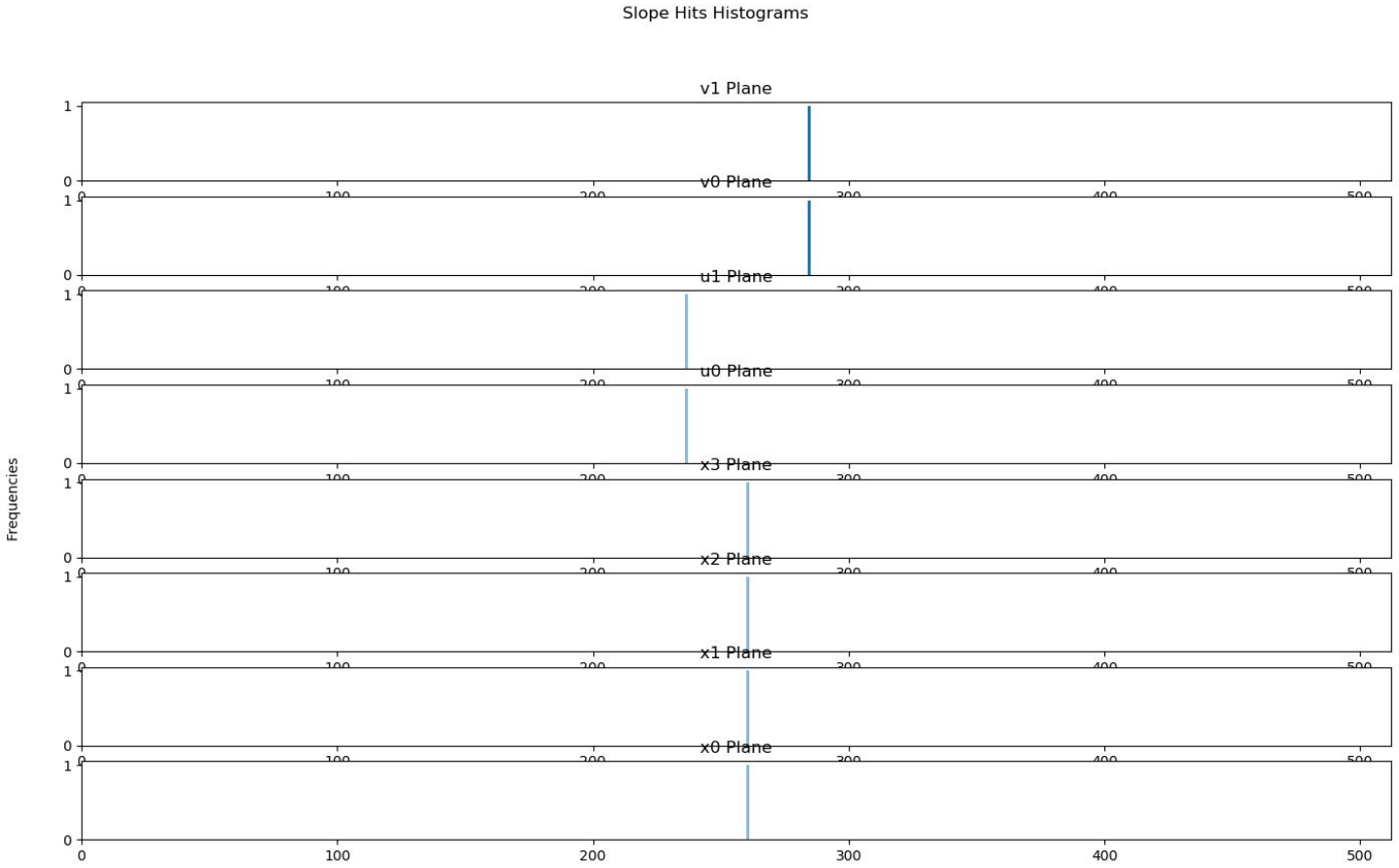
# MM Loopback Data Sources

- Athena generated with no background hits
  - Athena hits are formatted into an ADDC ART data packet
- Hits collected from cosmic ray test stand
  - Each coincidence trigger will store a window of raw GBT data
  - Raw GBT data is used to “replay” an event in simulation or hardware
- Pattern data to emulate tracks anywhere on the detector
  - GBT Packets are generated using a Python script
  - Hit strips from track candidates are histogrammed, problems become easy to spot.
  - Currently testing the full wedge implementation with pattern data
- Firmware simulations and hardware tests use same hit data source.

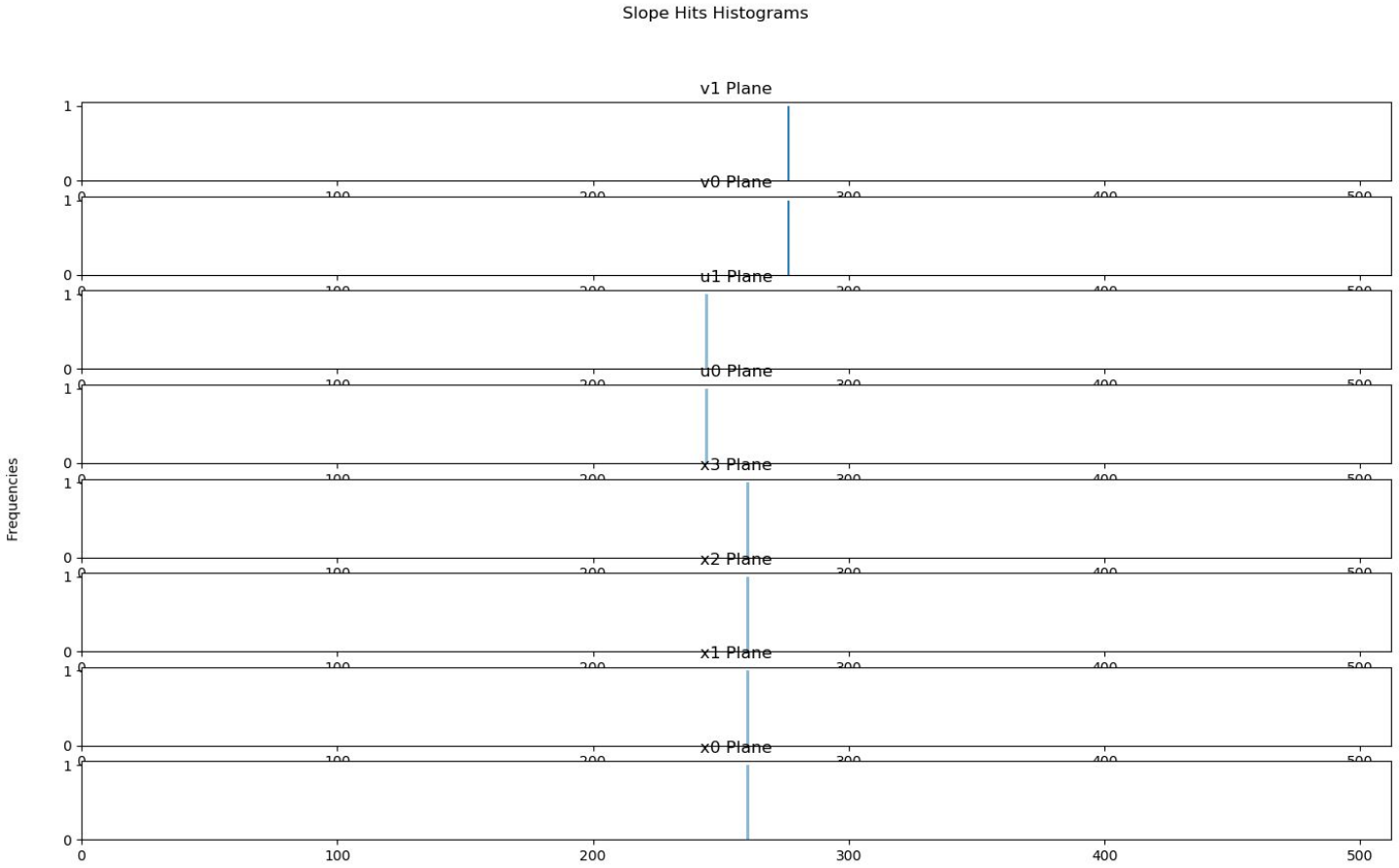
# Example Pattern Data

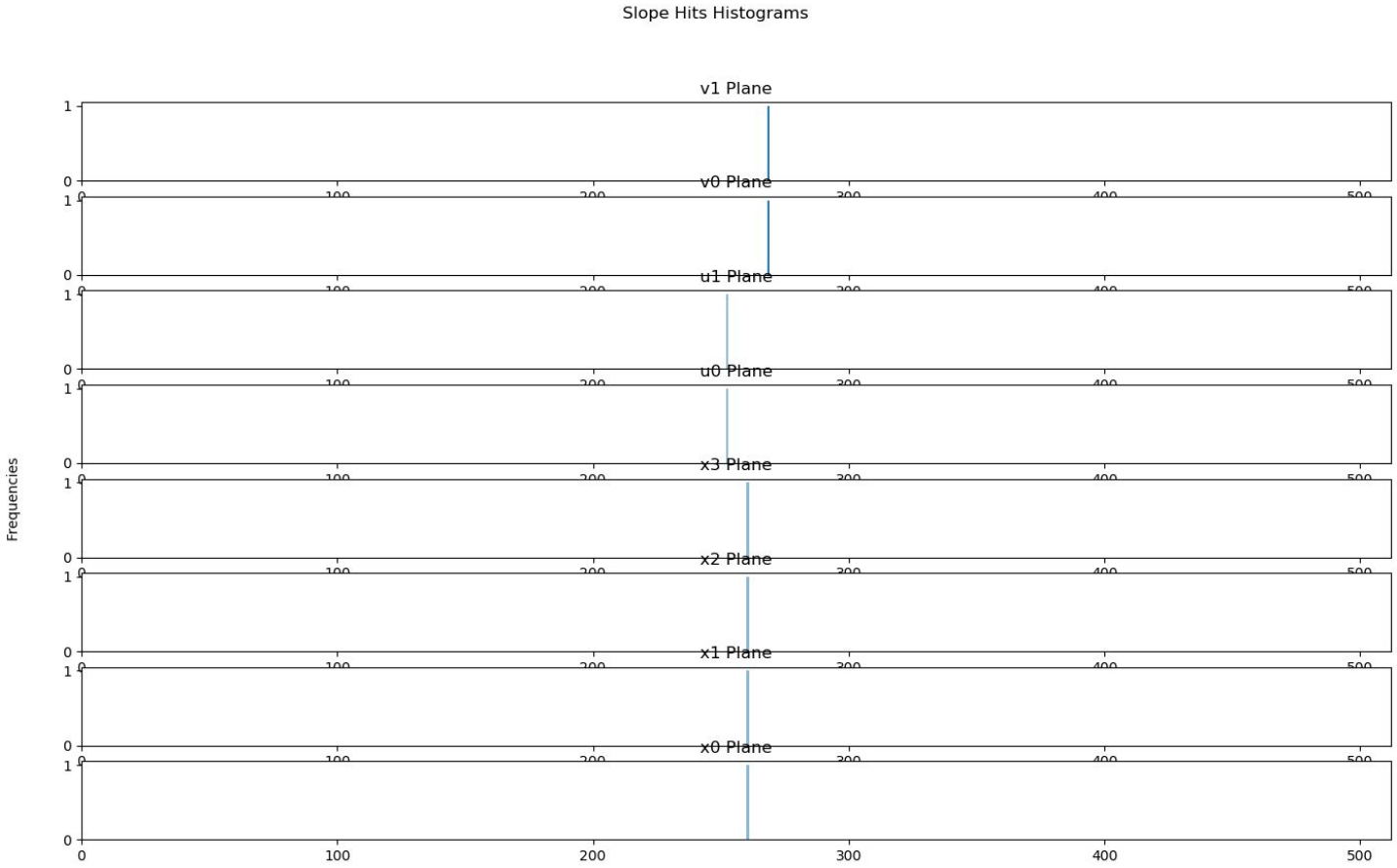
- Tracks with the same slopes for X,U, and V planes (scanning up the center)
- Tracks with the same X plane slopes but offset UV plane slopes (scanning across)



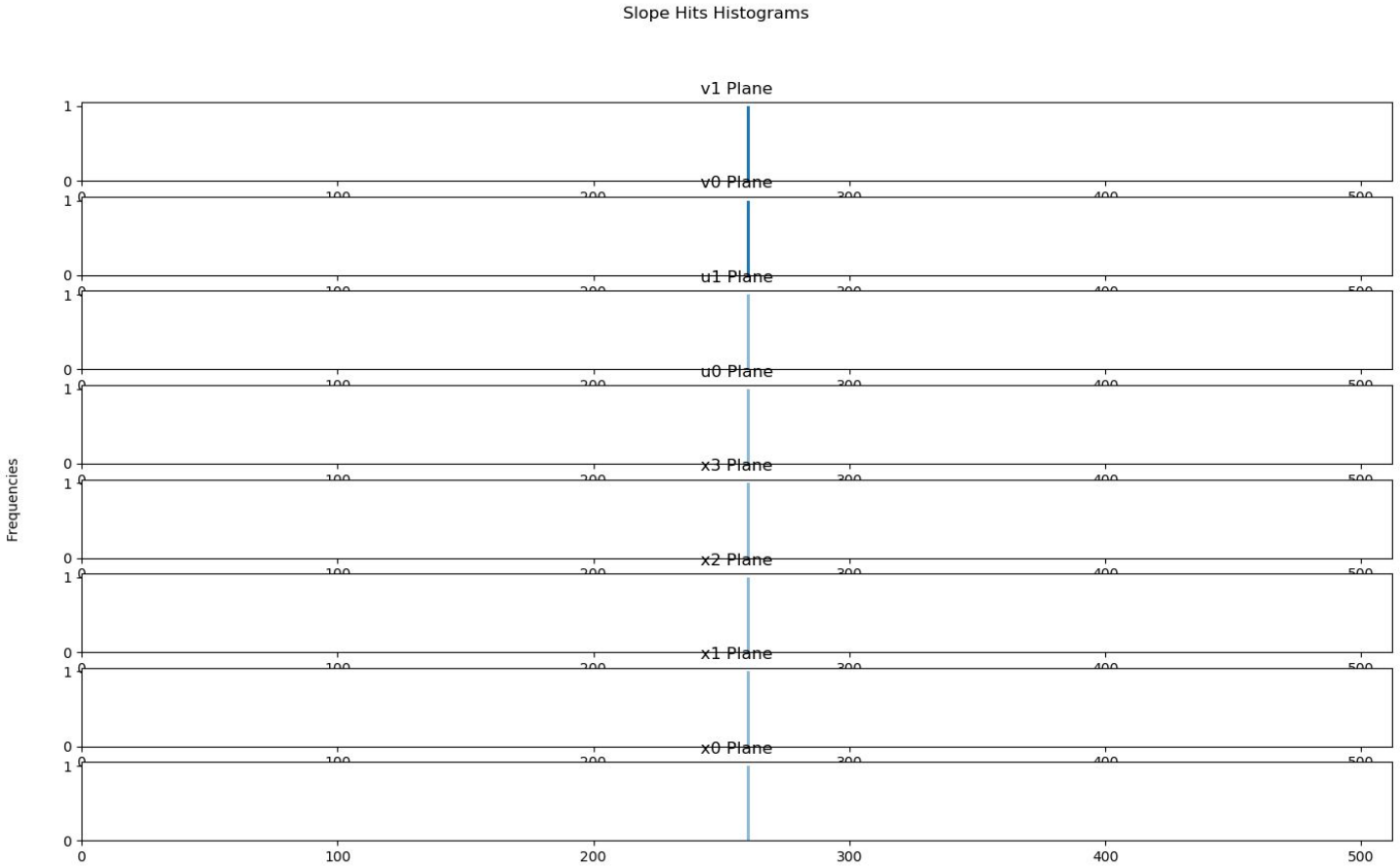



x=162.015 y=0.613189

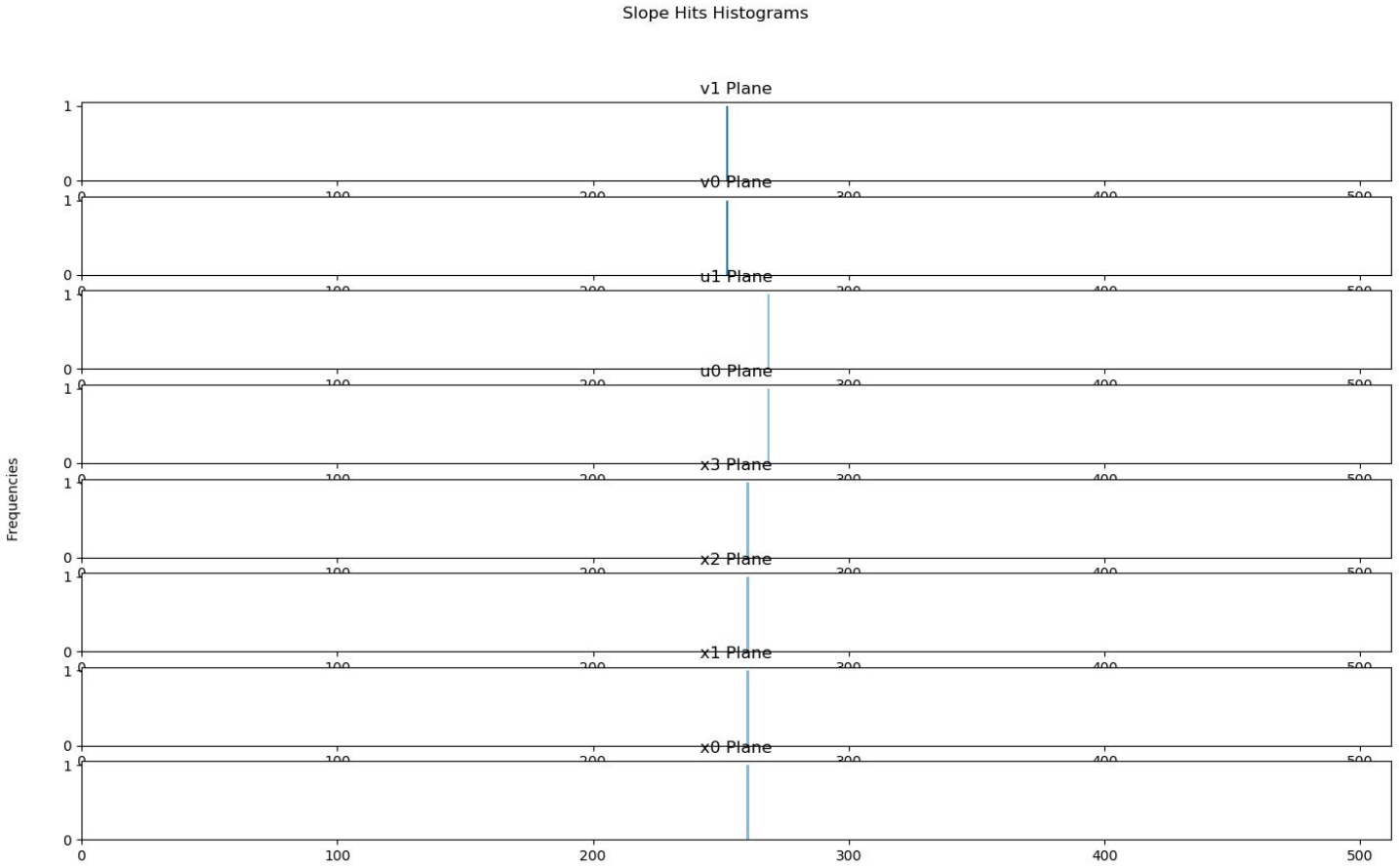




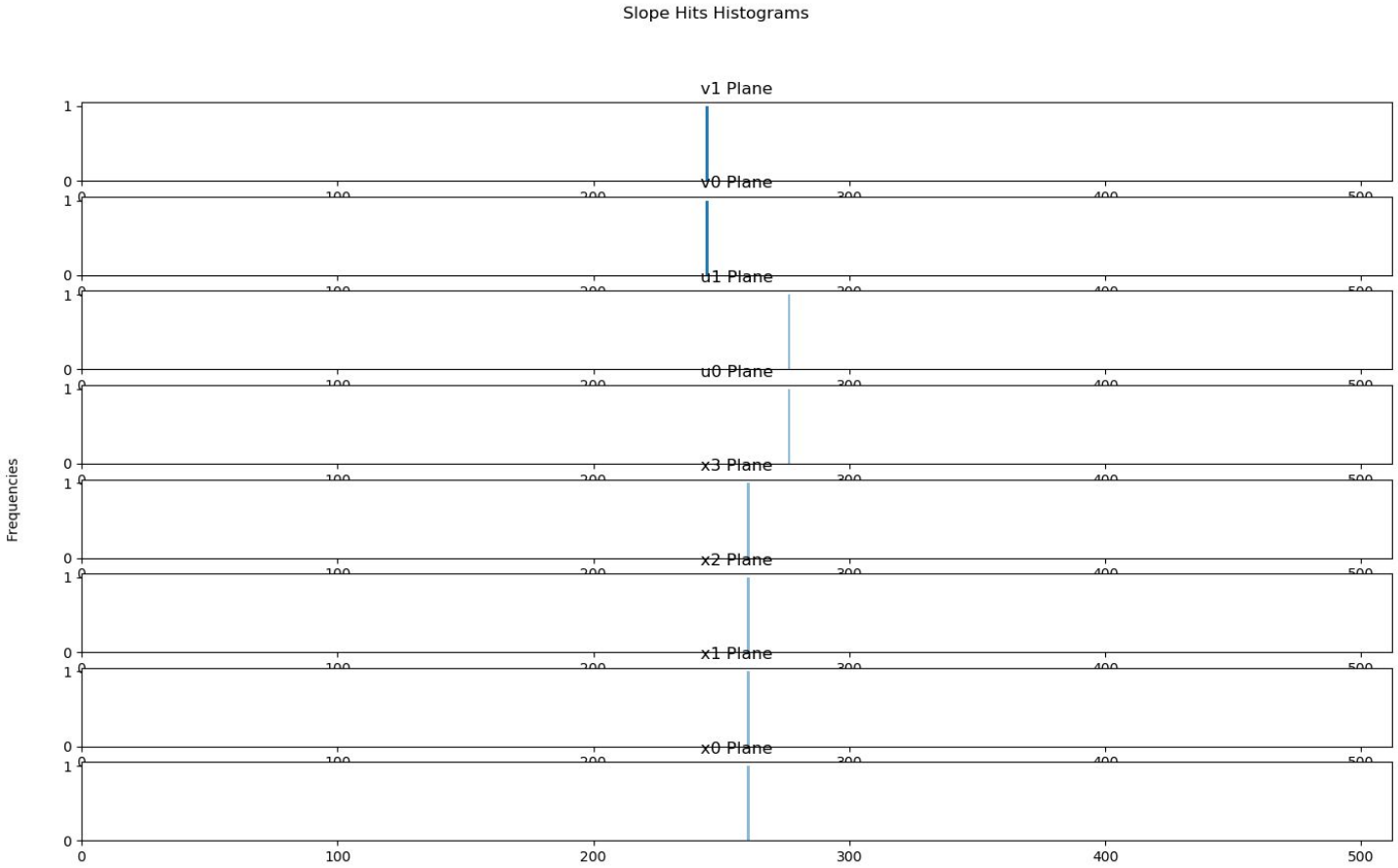

x=166.734 y=0.928533

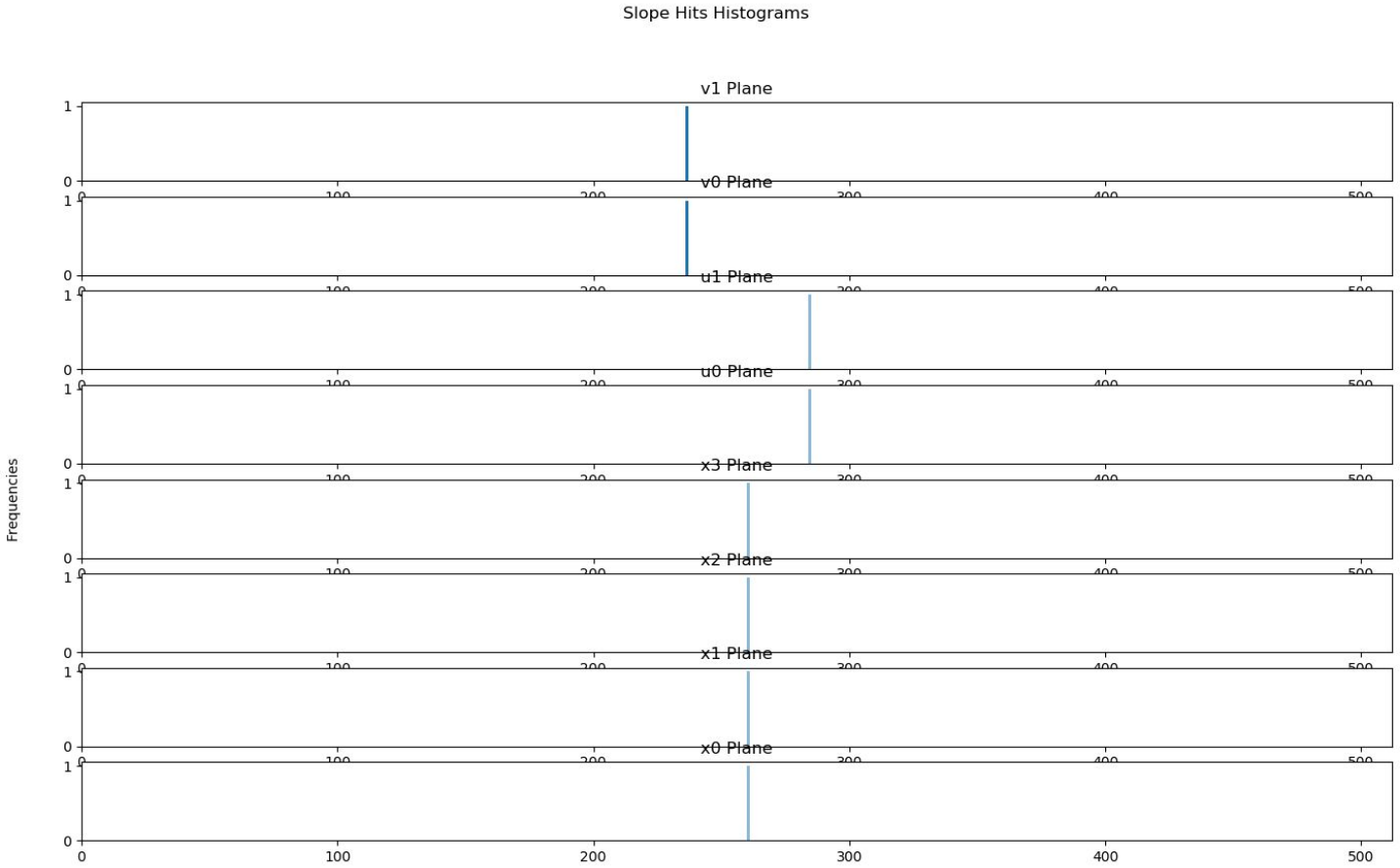

Slope Hits Histograms
v1 Plane
v0 Plane
u1 Plane
u0 Plane
x3 Plane
x2 Plane
x1 Plane
x0 Plane
Frequencies
0
100
200
300
400
500
1
0

x=161.622 y=0.201451

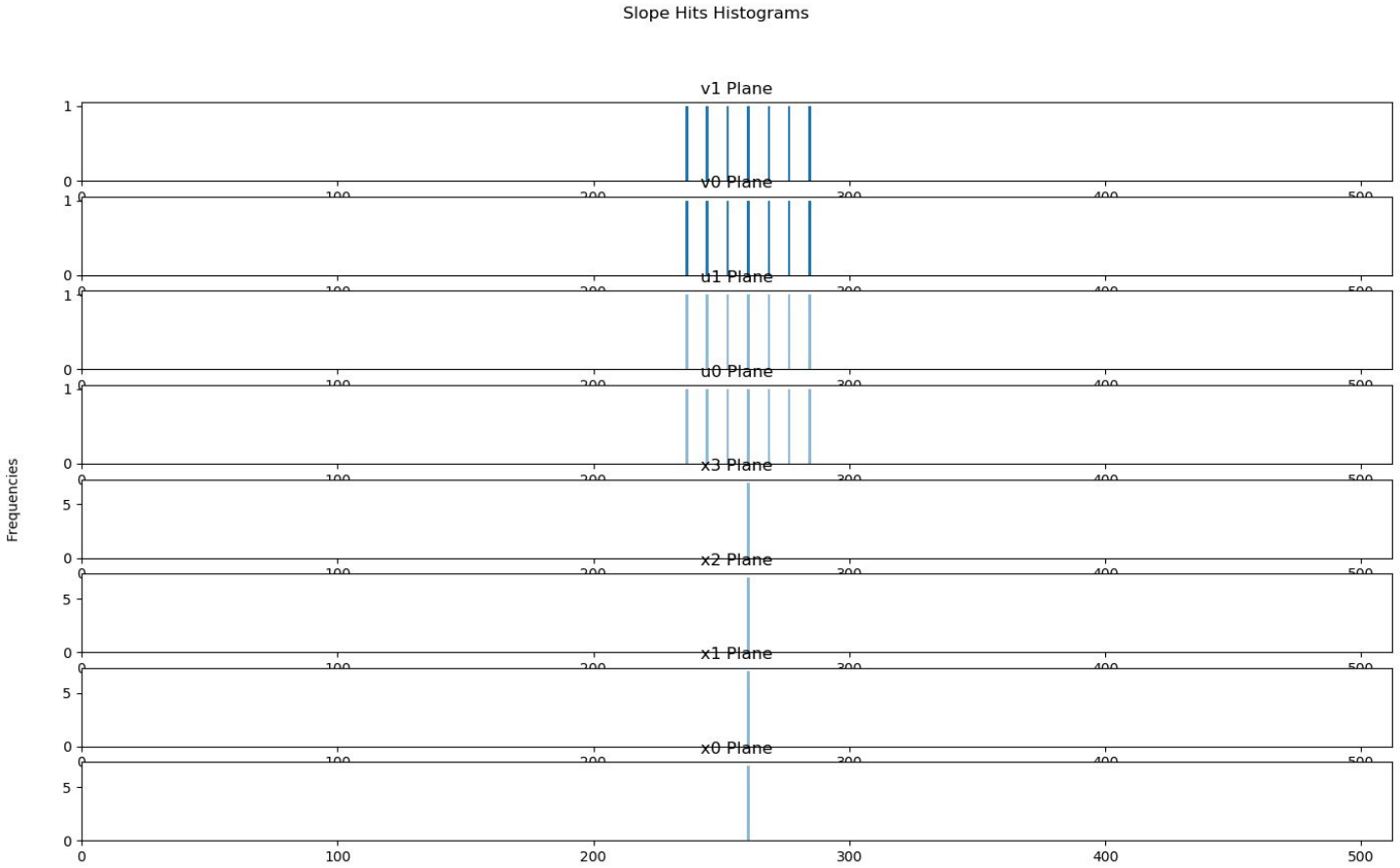



x=296.111 y=0.907265


Slope Hits Histograms
v1 Plane
v0 Plane
u1 Plane
u0 Plane
x3 Plane
x2 Plane
x1 Plane
x0 Plane
Frequencies
0
100
200
300
400
500
1
0




x=164.768 y=0.874675




x=165.161 y=0.826478

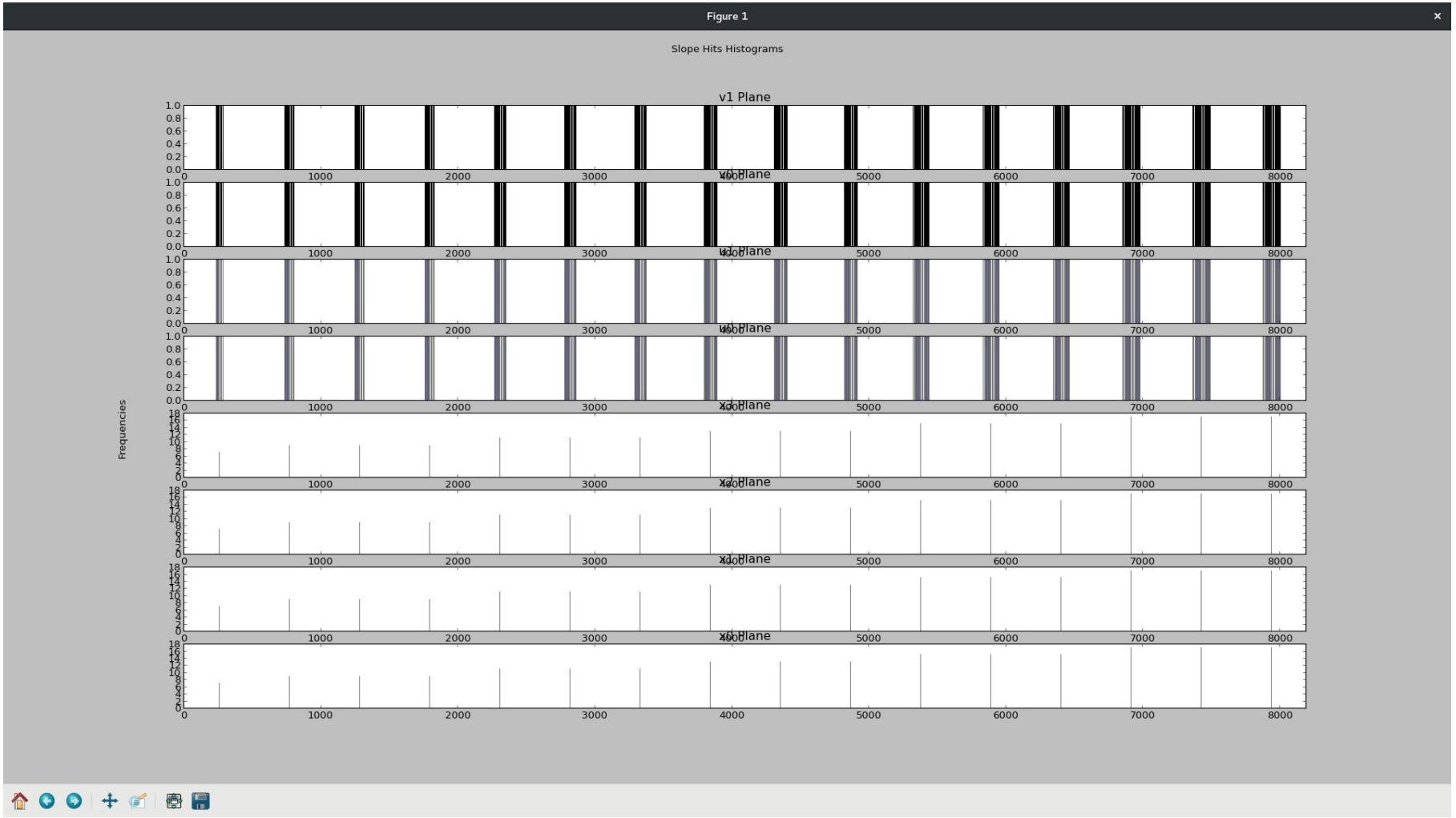


Figure 1
Slope Hits Histograms
v1 Plane
v0 Plane
u1 Plane
u0 Plane
x1 Plane
x0 Plane
Frequencies


Figure 1
Slope Hits Histograms
v1 Plane
x0 Plane
u0 Plane
x00 Plane
x1 Plane
x2 Plane
u1 Plane
Frequencies

# ADDC Interface testing

- 36 front panel transceivers have been IBERT tested
- Full MMTP algorithm using 32 fibers has been tested
  - Loopback fibers
  - Data Tx Rx in same FPGA
  - Limited statistics
- Integrated in vertical slice with 2 ADDCs (4 fibers) and ART data from pulsed MMFE8s
  - FELIX clock recovery implemented in MMTP FPGA