

# sTGC: Stage 0 and L1A readout

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For the NSW trigger processor team

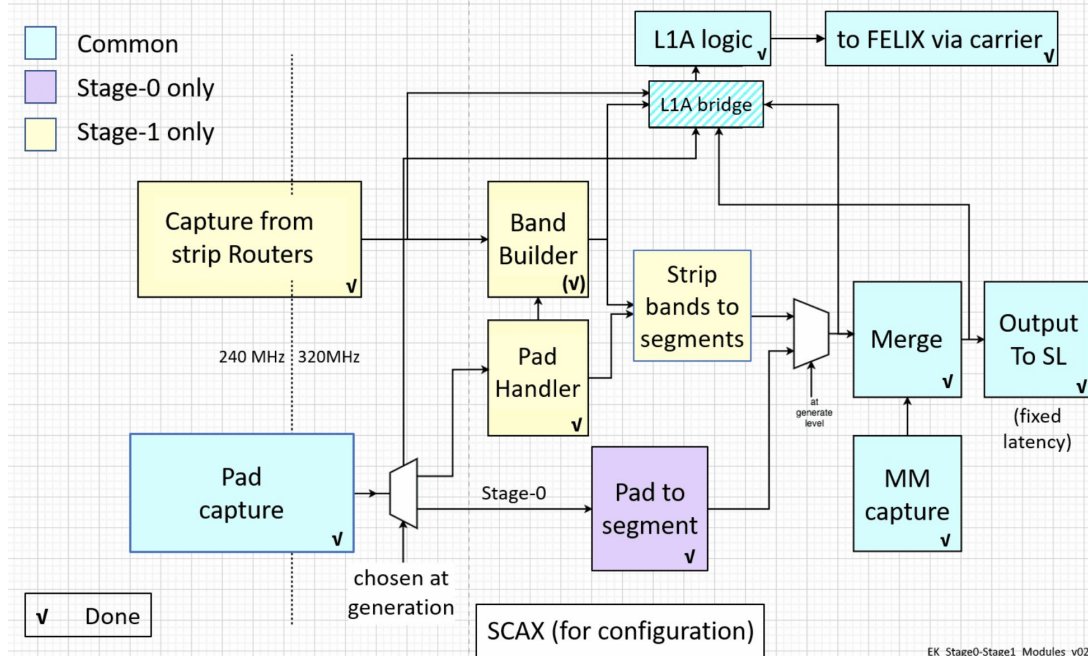
# sTGC firmware

Stage-0: produce segments for SL based on pad trigger

- George's talk: detailed discussion on Stage-0 modules
- Lorne's talk: detailed discussion on SL testing
- **This talk: L1A Readout**

\*Stage-0: essential parts of stage-1 with the exception of purple box

Stage-0 / Stage-1 schema

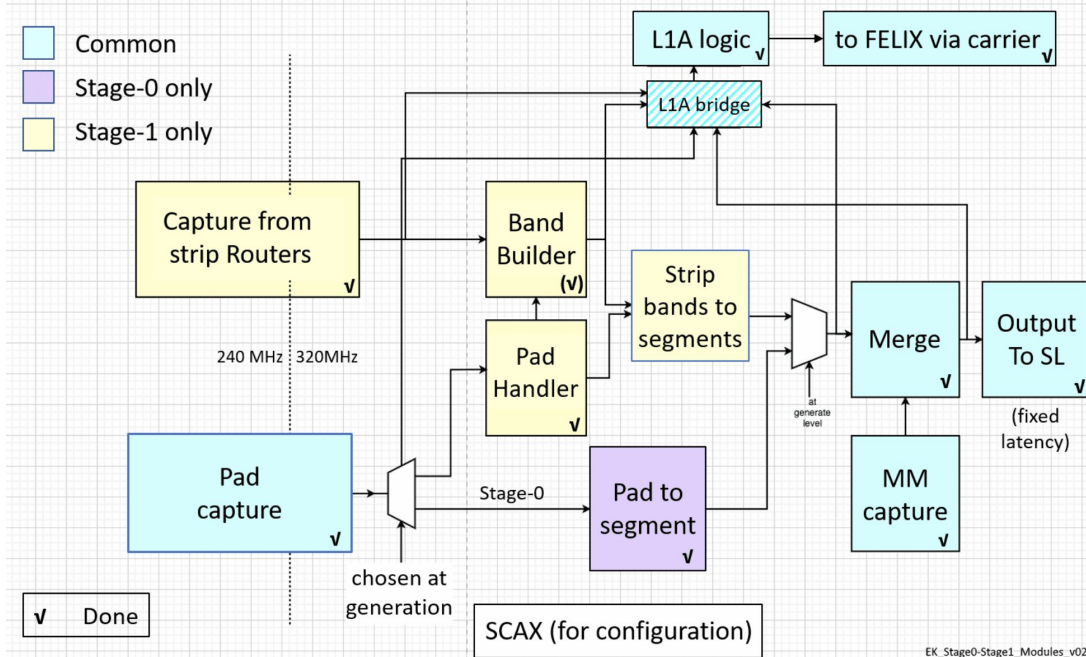


EK\_Stage0-Stage1\_Modules\_v02

# sTGC firmware resource utilization

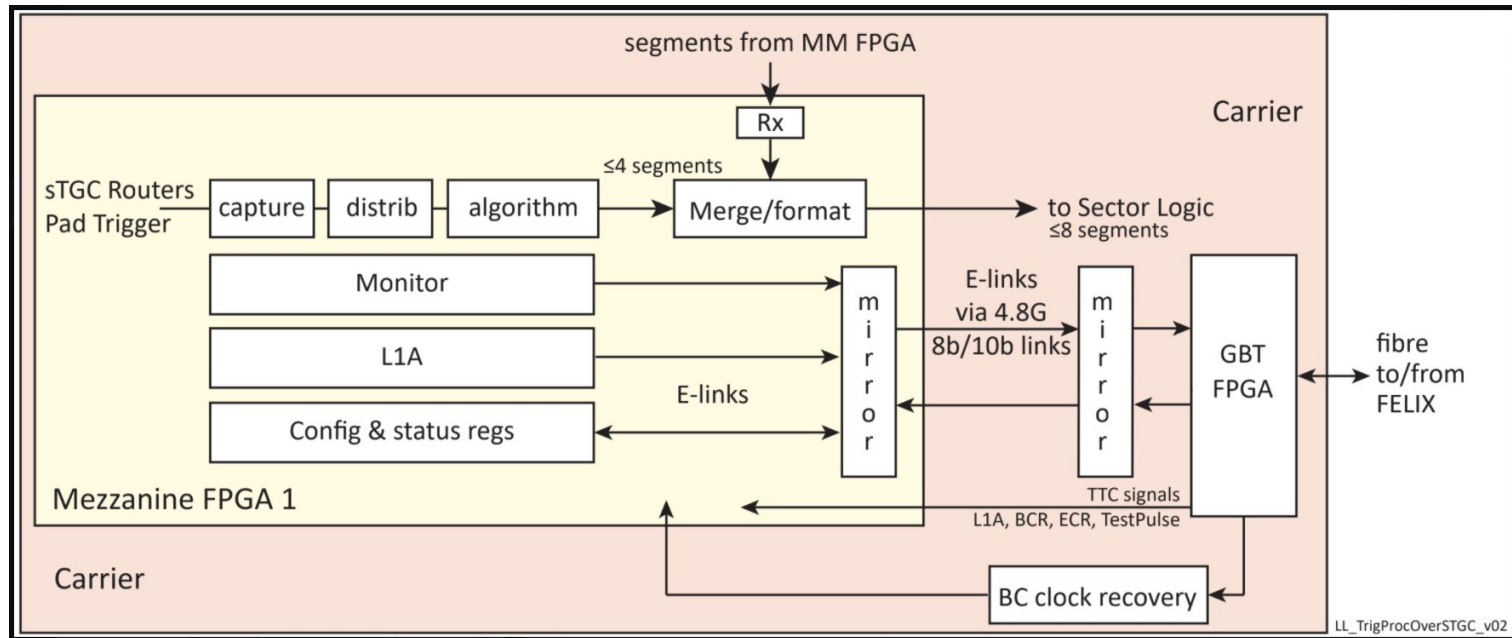
Stage- 1		Stage- 0	
Resource	Utilization %	Resource	Utilization %
LUT	18.8	LUT	3.1
LUTRAM	3.7	LUTRAM	0.6
FF	12.9	FF	3.3
BRAM	45.8	BRAM	4.6
DSP	7.1	DSP	0.0
IO	18.0	IO	na
GT	83.3	GT	66.7
BUFG	43.8	BUFG	28.3
MMCM	5.0	MMCM	5.0

Stage-0 / Stage-1 schema



# Readout path \* See Nathan's talk

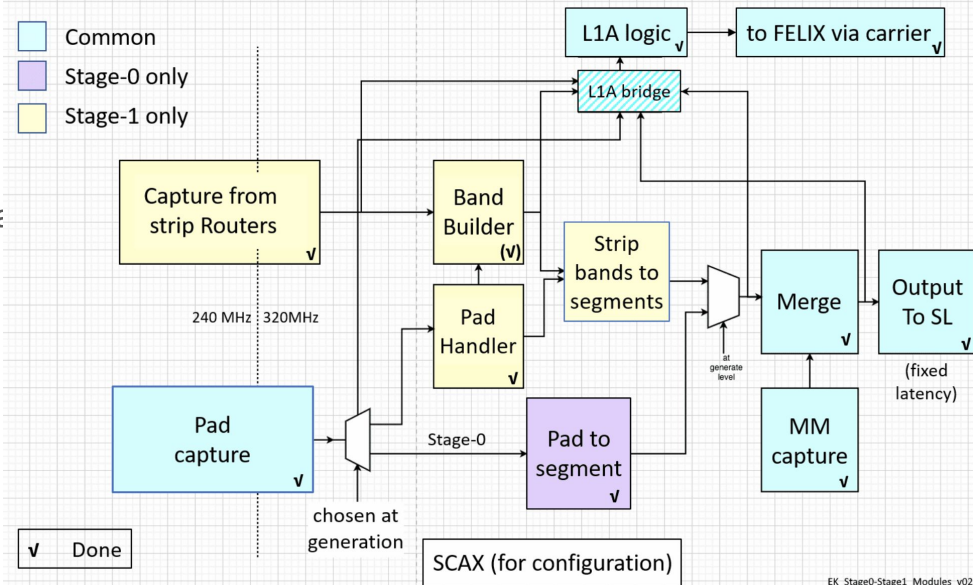
- Readout data is sent to FELIX through RTM
- **Common firmware:** L1A packet builder (MM/sTGC)
- **sTGC firmware:** bridge between sTGC data and L1A packet builder



# Status of readout path bridges

- Each bridge is a FIFO to match latencies along the pipeline
- Testing at VS
  - TTC signal: from ALTI via FELIX
  - Pad-data: Trigger Processor and Pad-Trigger hardware
  - Router data: Trigger Processor and playback data
- Integrated in the version tested in hardware:
  - Raw pad trigger data
  - Raw router data (stage-1)
- Implemented in development branch:
  - Stage-1 pipeline, including algorithm
  - Merge

Stage-0 / Stage-1 schema



# Readout path commissioning status

- Readout path is working
- Packets are correct length and L1ID increases as expected
  - Issue - some large packets that includes data + large garbage tail (Bug fix released)
- Rest of data is hard to interpret (swapped perhaps, and some bit changes)

**ILA Status: Idle**

Name	Value
U_2/u_trngproc11a_#/...if_pad_inst/din[87:0]	#####f001f
U_2/u_trngproc11a_#/...if_pad_inst/out[87:0]	0000000000000000000000
U_2/u_trngproc11a_#/...rigger_data_dbg[87:0]	#####f001f
U_2/u_trngproc11a_#/...a_raw_bcid5_dbg[11:0]	00a
U_2/u_trngproc11a_#/...1a_bcid_cnt_reg[11:0]	d7f
U_2/u_trngproc11a_#/...data_o_reg[17:17:0]	00060
U_2/u_trngproc11a_#/...11a_if_pad_inst/empty	1
U_2/u_trngproc11a_#/...11a_algo_uf2e_wren_o	0
u_11a_o_full	0
U_2/u_trngproc11a_#/...rigger_data_valid_dbg	0
U_2/u_trngproc11a_#/...11a_if_pad_inst/rd_en	0
U_2/u_trngproc11a_#/...11a_if_pad_inst/nw_en	0
U_2/BCR_cred	0

**Trigger Setup - hw\_11a\_5**

Name	Operator	Radix	Value	Port	Comparator Usage
U_2/u_trngproc11a_#/...11a_algo_uf2e_wren_o	==	[8]	R	probe7[0]	1 of 1

```

22 00 00 00 91 02 00 00 00 00 00 00 00 6e 82 f4 00 70 01 00 10 09 00 00 00 00 00 00 00 00
>>> message from 128.141.214.253:59398 size=34
22 00 00 00 91 02 00 00 00 00 00 00 00 6e 82 f5 00 70 01 00 10 09 00 00 00 00 00 00 00 00
>>> message from 128.141.214.253:59398 size=34
22 00 00 00 91 02 00 00 00 00 00 00 00 6e 82 f6 00 70 01 00 10 09 00 00 00 00 00 00 00 00
>>> message from 128.141.214.253:59398 size=34
22 00 00 00 91 02 00 00 00 00 00 00 00 6e 82 f7 00 70 01 00 10 09 00 00 00 00 00 00 00 00

```

# Summary and next steps

- Stage-0 / Stage-1 schema
  - Most Stage-0 blocks are an essential part of Stage-1, in-tandem development for stage-0 and stage-1
  - Functional Stage-0 implemented and tested (to be discussed by George)
- Readout path is working
  - Remaining issues are being addressed
- Router data through readout path - will be used for commissioning
  - So far tested with playback data transmitted from second FPGA in Mezz.
  - \* timing issues (most probably at the playback emulator side)