sTGC:
Stage 0 and L1A readout

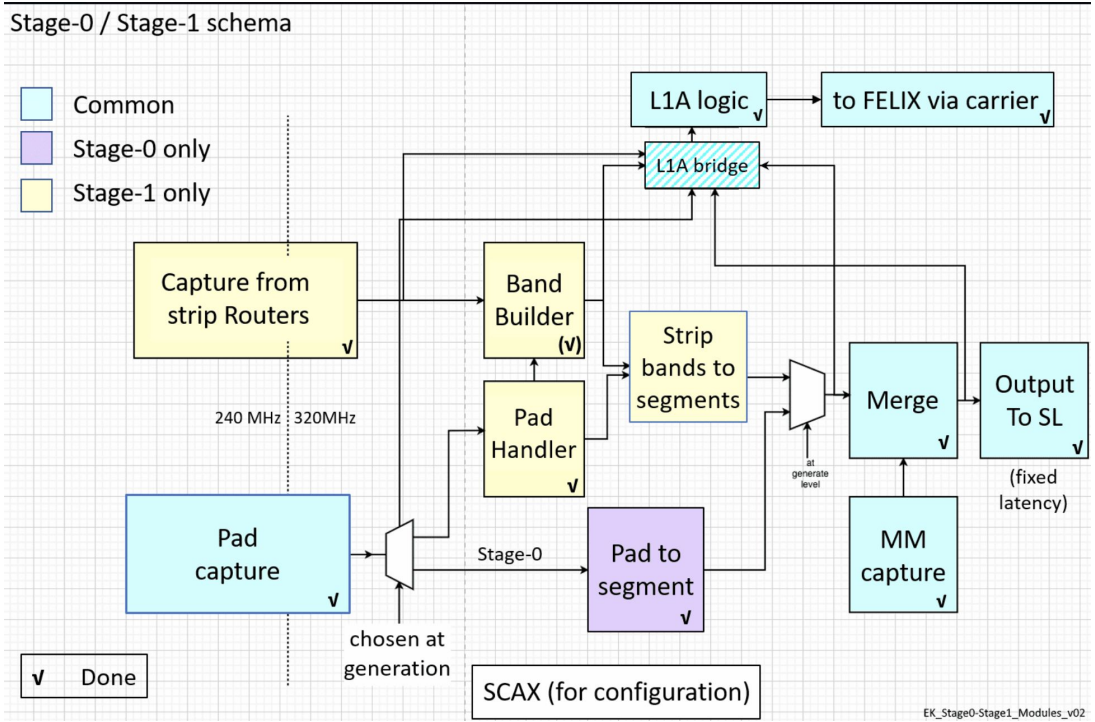
Enrique Kajomovitz Ken
For the NSW trigger processor team

sTGC firmware

Stage-0: produce segments for SL based on pad trigger

- George's talk: detailed discussion on Stage-0 modules
- Lorne's talk: detailed discussion on SL testing
- **This talk: L1A Readout**

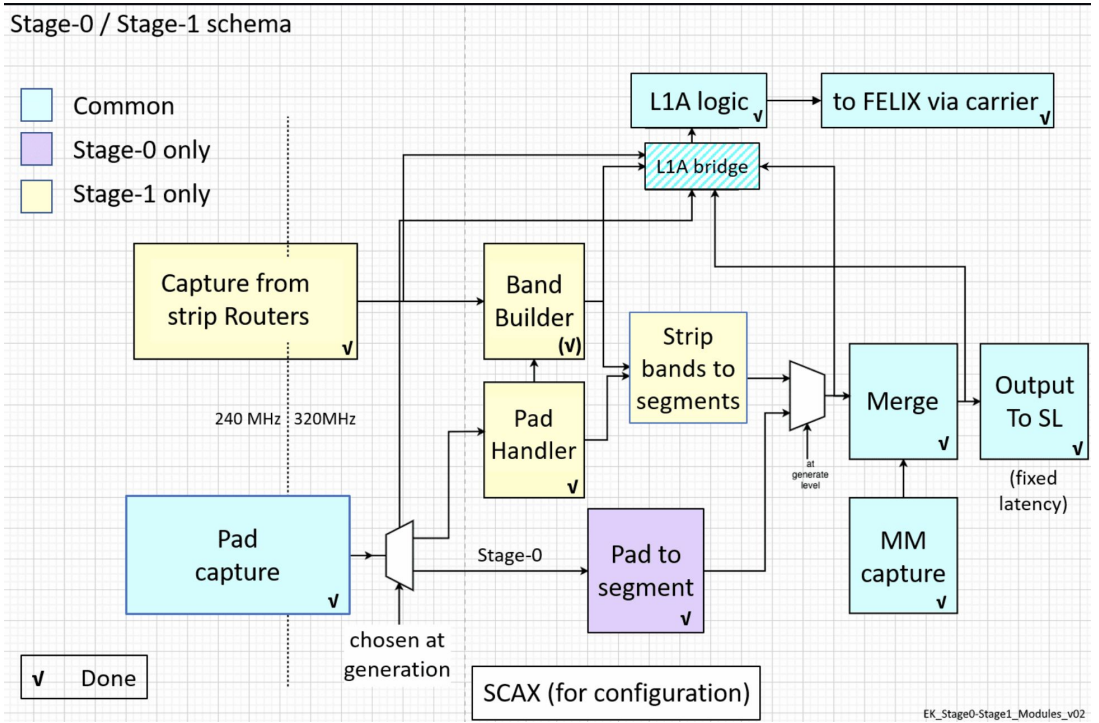
*Stage-0: essential parts of stage-1 with the exception of purple box



sTGC firmware resource utilization

Stage- 1	
Resource	**Utilization %**
LUT	18.8
LUTRAM	3.7
FF	12.9
BRAM	45.8
DSP	7.1
IO	18.0
GT	83.3
BUFG	43.8
MMCM	5.0

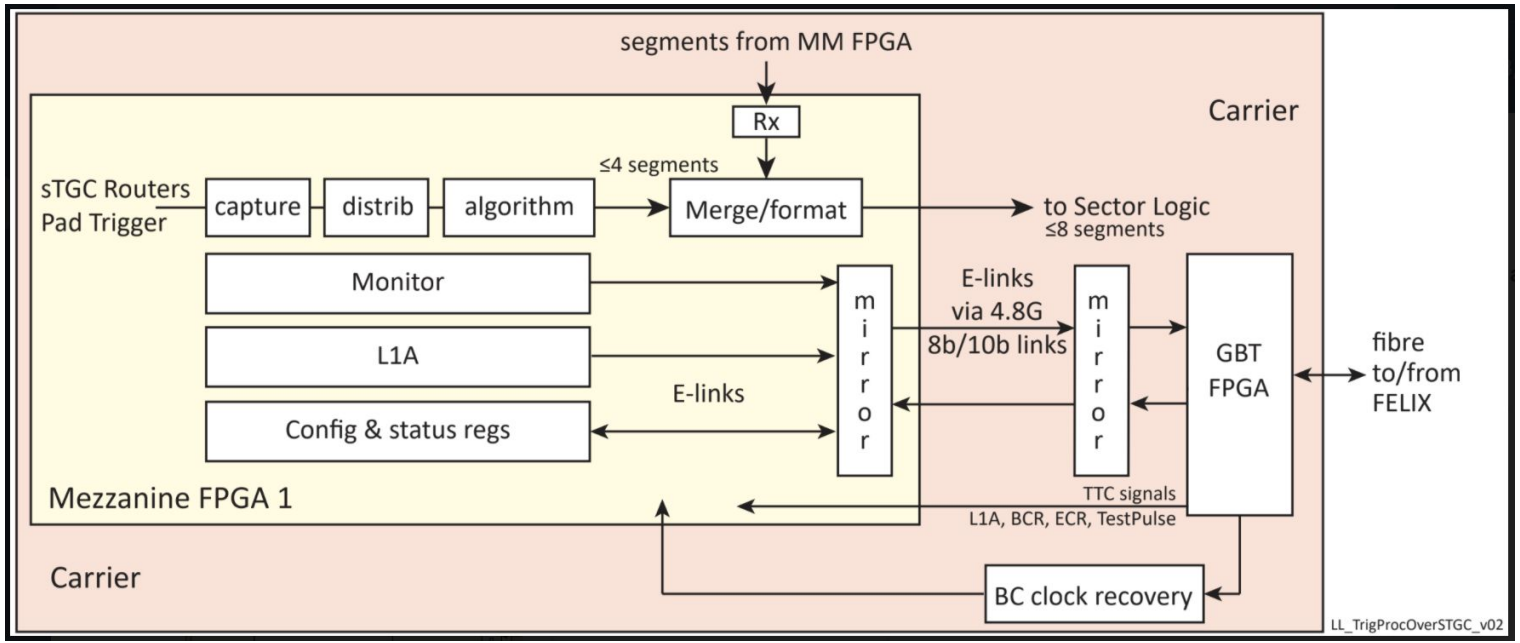
Stage- 0	
Resource	**Utilization %**
LUT	3.1
LUTRAM	0.6
FF	3.3
BRAM	4.6
DSP	0.0
IO	na
GT	66.7
BUFG	28.3
MMCM	5.0



Readout path

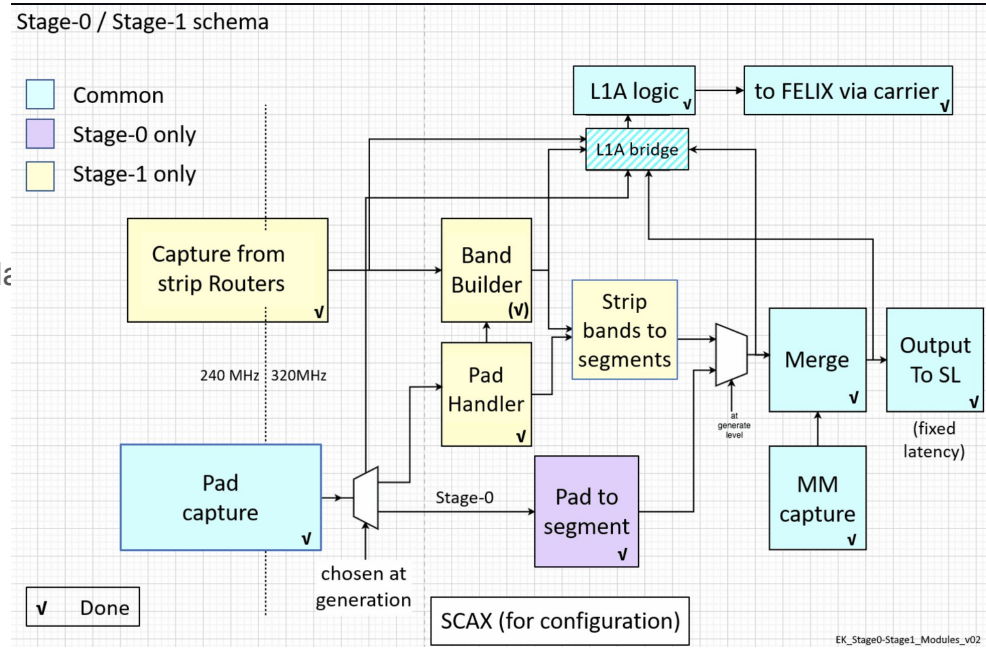
* See Nathan's talk

- Readout data is sent to FELIX through RTM
- **Common firmware:** L1A packet builder (MM/sTGC)
- **sTGC firmware:** bridge between sTGC data and L1A packet builder



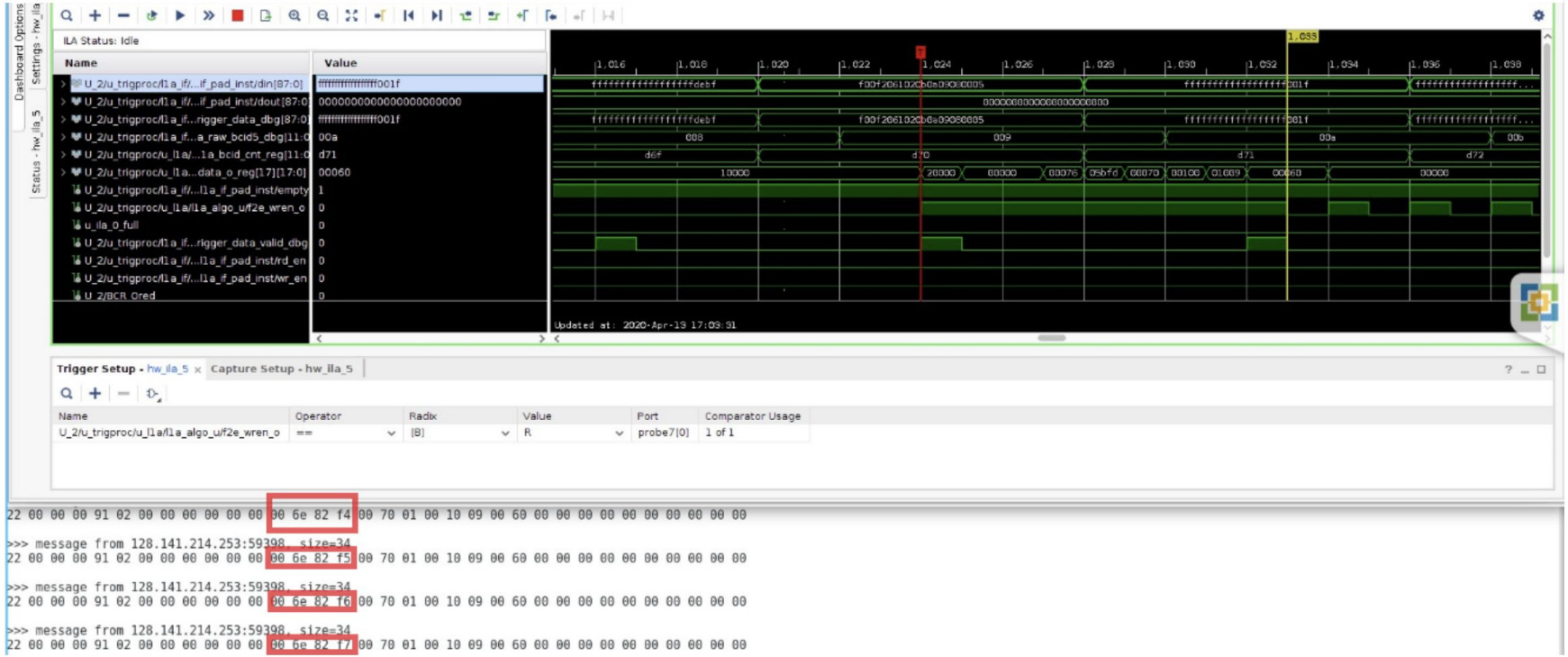
Status of readout path bridges

- Each bridge is a FIFO to match latencies along the pipeline
- Testing at VS
  - TTC signal: from ALTI via FELIX
  - Pad-data: Trigger Processor and Pad-Trigger hardware
  - Router data: Trigger Processor and playback da
- Integrated in the version tested in hardware:
  - Raw pad trigger data
  - Raw router data (stage-1)
- Implemented in development branch:
  - Stage-1 pipeline, including algorithm
  - Merge



Readout path commissioning status

- Readout path is working
- Packets are correct length and L1ID increases as expected
  - Issue - some large packets that includes data + large garbage tail (Bug fix released)
- Rest of data is hard to interpret (swapped perhaps, and some bit changes)



Summary and next steps

- Stage-0 / Stage-1 schema
  - Most Stage-0 blocks are an essential part of Stage-1, in-tandem development for stage-0 and stage-1
  - Functional Stage-0 implemented and tested (to be discussed by George)
- Readout path is working
  - Remaining issues are being addressed
- Router data through readout path - will be used for commissioning
  - So far tested with playback data transmitted from second FPGA in Mezz.
  - * timing issues (most probably at the playback emulator side)