PRR of the NSW Trigger Processor Part 2

Report of Contributions

https://indico.cern.ch/e/894588

Contribution ID: **1** Type: **not specified**

Review procedure

Wednesday 6 May 2020 14:00 (5 minutes)

Presenter: CHEN, Hucheng (Brookhaven National Laboratory (US))

Contribution ID: **2** Type: **not specified**

Introduction & Review Scope

Wednesday 6 May 2020 14:10 (10 minutes)

Presenter: ZIMMERMANN, Stephanie Ulrike (Albert Ludwigs Universitaet Freiburg (DE))

Contribution ID: **3** Type: **not specified**

Carrier v3 design.Validation/test results (Bucarest/Samway, standalone)

Wednesday 6 May 2020 16:35 (20 minutes)

Presenters: SCURTU, Andrei (Samway SRL); MARTOIU, Sorin (Horia Hulubei National Institute of Physics and Nuclear Enginee)

Contribution ID: **4** Type: **not specified**

Board test protocol and procedures (for series production); acceptance criteria

Wednesday 6 May 2020 17:00 (20 minutes)

Presenters: DI CURZIO LERA, Ricardo (University of Massachusetts (US)); COSTA DE PAIVA, Thiago (University of Massachusetts (US))

Contribution ID: **5** Type: **not specified**

Production plan and schedule

Wednesday 6 May 2020 17:30 (20 minutes)

Presenters: SAVU, Mihai (Samway Electronic); MARTOIU, Sorin (Horia Hulubei National Institute of Physics and Nuclear Enginee)

Contribution ID: **6** Type: **not specified**

Installation plans @ P1 and commissioning

Wednesday 6 May 2020 18:05 (20 minutes)

Presenter: TUNA, Alexander Naip (Harvard University (US))

Contribution ID: **7** Type: **not specified**

Results of combined tests with SL. Fixed latency. Latency measurements.

Wednesday 6 May 2020 15:55 (15 minutes)

Presenter: LEVINSON, Lorne (Weizmann Institute of Science (IL))

Session Classification: Trigger Processor Firmware

Contribution ID: **8** Type: **not specified**

Micromegas: L1A and readout (thru carrier). Algorithms and time alignment.

Wednesday 6 May 2020 14:25 (20 minutes)

Presenters: FELT, Nathan (Harvard University (US)); FELT, Nathan (Unknown); COSTA DE PAIVA, Thiago (University of Massachusetts (US))

Session Classification: Trigger Processor Firmware

Contribution ID: **11** Type: **not specified**

sTGC stage-0: L1A and readout (thru carrier). Stage-0 algorithm; time alignment

Wednesday 6 May 2020 14:55 (15 minutes)

Presenters: KAJOMOVITZ MUST, Enrique (Department of Physics); KAJOMOVITZ MUST, Enrique (Technion, Israel Institute of Technology)

Session Classification: Trigger Processor Firmware

Contribution ID: **12** Type: **not specified**

Merge block, and output formatter to SL.

Wednesday 6 May 2020 15:25 (20 minutes)

Presenter: CHATZIANASTASIOU, George (University of Innsbruck (AT))

Session Classification: Trigger Processor Firmware