PRR of the NSW Trigger Processor Part 2

Wednesday, May 6, 2020

Trigger Processor Firmware - Vidyo Only (2:20 PM - 4:20 PM)

time	[id] title	presenter
2:25 PM	[8] Micromegas: L1A and readout (thru carrier). Algorithms and time alignment.	FELT, Nathan FELT, Nathan COSTA DE PAIVA, Thiago
2:55 PM	[11] sTGC stage-0: L1A and readout (thru carrier). Stage-0 algorithm; time alignment	KAJOMOVITZ MUST, Enrique KAJOMOVITZ MUST, Enrique
3:25 PM	[12] Merge block, and output formatter to SL.	CHATZIANASTASIOU, George
3:55 PM	[7] Results of combined tests with SL. Fixed latency. Latency measurements.	LEVINSON, Lorne