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The powering scheme of the CBM Silicon Tracking System: concept and first implementations

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The Silicon Tracking System (STS) is planned to be the principal tracking detector of the future CBM experiment at FAIR. It will perform charged-particle track measurement with momentum resolution better than 2% in a 1 Tm dipole-magnetic field. A main challenge for the STS is to maintain high track reconstruction efficiency throughout the projected lifetime of the experiment which means being exposed to an accumulated fluence of up to 10^{14} n_{eq}/cm^2, expected to be reached in beam-target interaction rates of 10 MHz. Therefore, front-end electronics with self-triggering architecture needs to have sufficient signal-to-noise ratio (S/N>10) which requires an ultra-low noise system design.
The STS will consist of eight tracking stations comprising 876 double-sided silicon detector modules installed onto 106 carbon fibre ladders with a total of 1.8 million readout channels. Operation of the system requires a detailed understanding of the electrical scheme at different hierarchical levels, including: low and high voltage systems, copper data lines from the front-end electronics to the read-out and data combiner boards, signal path, as well as grounding and shielding concepts. The performance parameter of the system is equivalent noise charge (ENC) value measured by the front-end electronics.
The electrical scheme of the system as well as its experimental validation in the laboratory and beam will be presented.

Author: LYMANETS, Anton (GSI - Helmholtzzentrum fur Schwerionenforschung GmbH (DE))

Presenter: LYMANETS, Anton (GSI - Helmholtzzentrum fur Schwerionenforschung GmbH (DE))

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