Optimization of the calibration of the Silicon Tracking System front-end electronics

Rodríguez Garcés, Dairon (d.rodriguezgarces@gsi.de), GSI Helmholtzzentrum, *for the CBM Collaboration*

ABSTRACT

The CBM is a next-generation experiment to be operated at FAIR facility, currently under construction in Darmstadt, Germany. The setup is designed as a forward multipurpose detector capable to measure hadrons, dileptons, and muons with high precision. To achieve the high rate capability CBM will be equipped with fast and radiation hard detectors employing free-streaming readout electronics. Inside a 1 Tm superconductive dipole magnet is placed the Silicon Tracking System (STS), the main detector for charged particle measurements and momentum determination. The STS is designed as 8 tracking layers built from 876 modules. The custom-designed front-end electronics for reading out the double-sided silicon sensors is the SMX ASIC: analog front-end with CSA, slow and fast shaper paths, ADC, digital part with hit generation and readout.

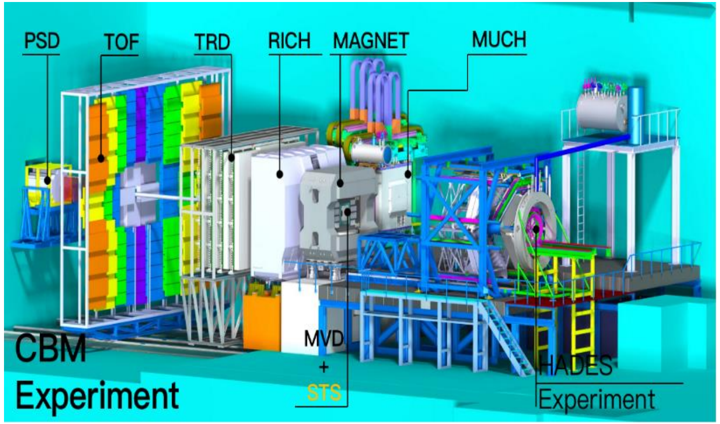
The characterization of the chip is an extensive procedure that includes multiple functional tests such as proper amplitude and time calibration. These are necessary steps to correctly interpret the collected data. The design of the analog front-end, with a double processing path for independent time and energy measurements, implies that the calibration should consider not only the ADC linearity aspects but also a homogeneous time response among all channels, and a well-known correlation of the threshold in both measuring paths. This work describes the characterization of the timing discriminator of the ASIC, the optimization of other-related chip parameters, and their effect on the measured data.

THE COMPRESSED BARYONIC MATTER (CBM) EXPERIMENT

The **GOAL** is to explore the QCD phase diagram in the región of high baryons densities using high-energy in nucleus-nucleus collisions for searching:

- **EoS** of nuclear matter.
- Phase transition.
- Chiral symmetry restoration.
- Exotics form of QCD matter.

High interaction rates (10^5-10^7 Hz); ideal for systematic, high precision studies of high-density nuclear matter.



HIGH SPEED DATA ADQUISITION

Readout electronics

- Fast, radiation hard detectors and self-triggered.

Powerful computing farm

- 4D(x,y,z,t) online event reconstruction.

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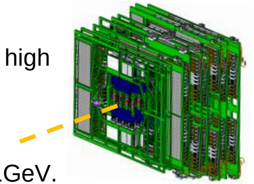
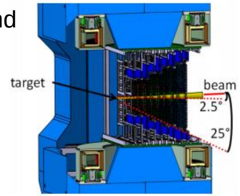
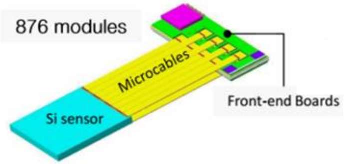
THE SILICON TRACKING SYSTEM

The STS characteristics:

- Tracking and reconstruction of high rate collisions.
  - Multiplicities up to 1000 particles/collision.
- High efficiency ~97%, for p > 1GeV.
- Excellent momentum resolution, < 2%.
- Low material budget design,front-end electronics out of the physics acceptance.
- Physics aperture: $2.5^{o} \leq \theta \leq 25^{o}$.
- Radiation hard: withstand up to 10^{14} 1 MeV $n_{eq}\,cm^{2}$.







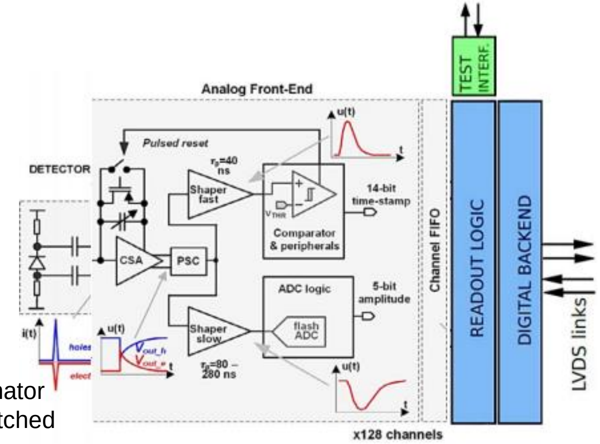
- 8 tracking stations.
- 876 modules, built from double-sided micro-strip silicon sensors.
- 2 front-end boards with 8 ASICs each one.

SMX ASIC

The **SMX** is a custom designed Application Specific Integrated Circuit for reading out the silicon sensors.

Features:

- Self-triggered ASIC.
- 128 readout channels.
- Double path for signal proccesing:
  - time measurements (time resolution < 5ns)
  - energy measurements (5 bit flash ADC/channel)
- 14 fC dynamic range determined by two reference potential: **Vref_P** and **Vref_N**.
- The common threshold of the discriminator are generated by a resistor ladder stretched between these potentials.



The fact that the chip possesses a double path is not a simple coincidence; this construction allows to establish a more elaborated scheme to suppress the noise keeping a very good time resolution.

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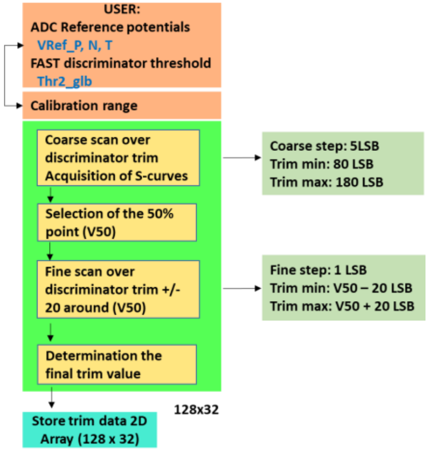
STANDARD METHOD

Current method for calibrating of **SMX ASIC**

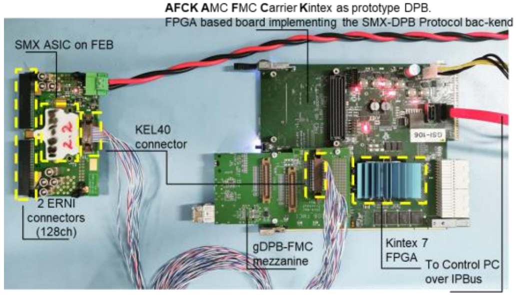


Coarse scan: the goal is to get the S-curves and find the inflection points (V50).

- Time in this step depends strongly of the numbers of pulses injected.

MOTIVATION

- The calibration matrix is not applicable to other ASICs.
- The time for calibrating one ASIC on the current test setup at 40 injected pulses:
  - ~30 min

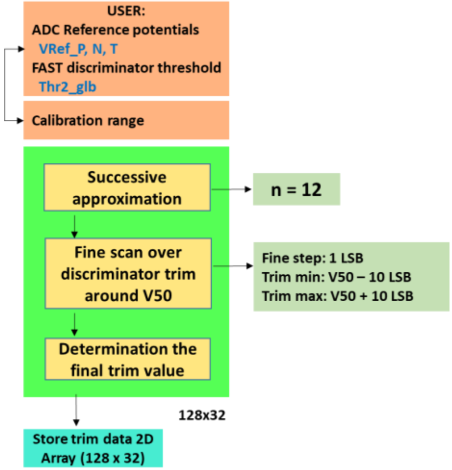


- STS will use ~14000 ASICs:
  - 290 days

NEED TO OPTIMIZE THE CALIBRATION PROCESS WITH THE GOAL TO IMPROVE THE CALIBRATION TIME WITHOUT LOSING PRECISION

SUCCESSIVE APPROXIMATION

The proposal is to replace the coarse scan for successive approximation



The results was obtained for 12 iterations, but this is a parameter that can be optimize in the future.

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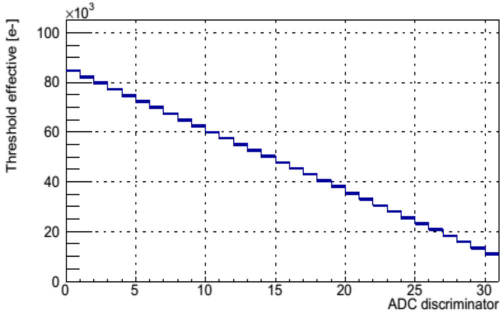
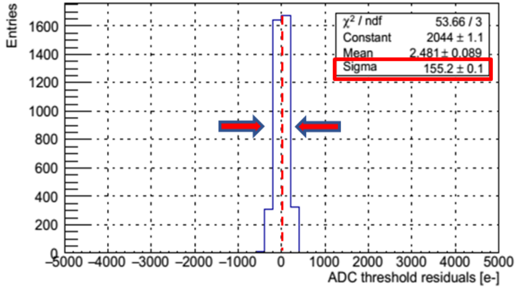
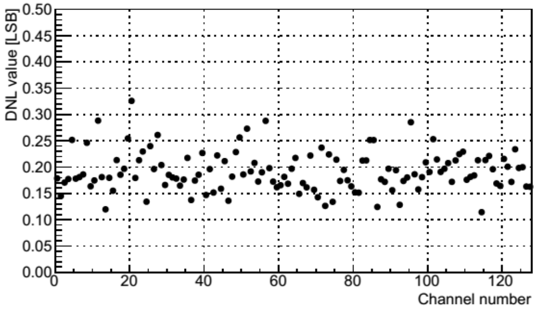
THRESHOLD RESIDUAL

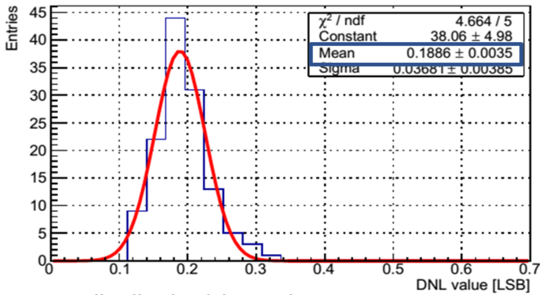




- Centered at zero.
- Sigma is a parameter that say how good was the calibration.

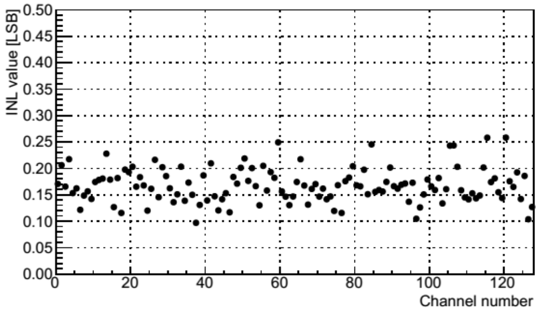
DIFFERENTIAL NON-LINEARITY

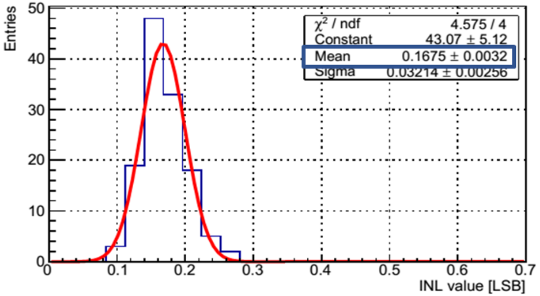




- DNL distribution/channel.
- Mean value is the DNL value of the ASIC.

INTEGRAL NON-LINEARITY





- INL distribution/channel.
- Mean value is the INL value of the ASIC.

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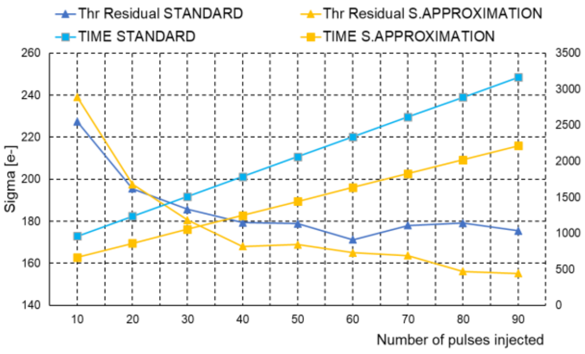

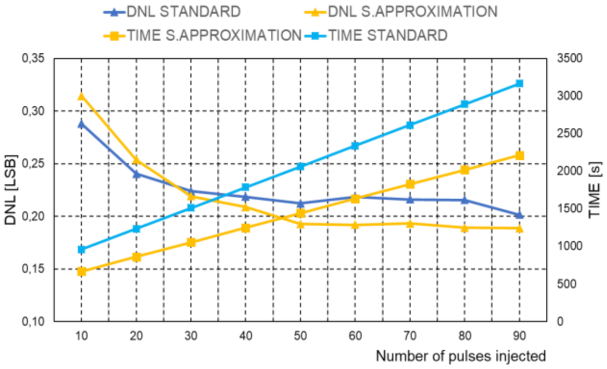

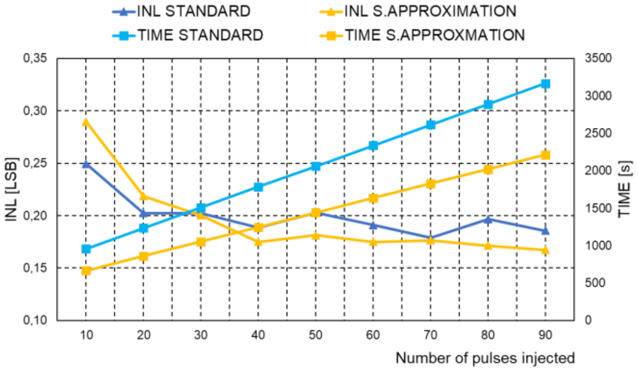

SUMMARY

- The successive aproximation method showed a better performance than the standard method.
- The successive approximation method reduced the calibration time in 30%.
- We recommend to calibrate at 50 injected pulses since we obtained the best relation precision/calibration time.

OUTLOOK

- The next step is a scan over the number of iterations of the successive approximation looking the best relation precision/calibration time.
- To implement the successive approximation method in a different hardware platform (EMU board with different firmware).