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Optimization of the calibration parameters for the font-end electronics of the Silicon Tracking System of the CBM experiment

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The CBM is a next-generation experiment to be operated at FAIR facility, currently under construction in Darmstadt, Germany. Its goal is to investigate the phase diagram of strongly interacting matter in the region of high baryon-net densities and moderate temperatures, using high-intensity nucleus-nucleus collisions. The setup is designed as a forward multipurpose detector capable to measure hadrons, dileptons, and muons with high precision. To achieve the high rate capability CBM will be equipped with fast and radiation hard detectors employing free-streaming readout electronics. Inside a 1 Tm superconductive dipole magnet is placed the Silicon Tracking System (STS), the main detector for charged particle measurements and momentum determination. The STS is designed as eight tracking layers built from 876 modules. The custom-designed front-end electronics for reading out the double-sided silicon sensors is the STS-XYTER ASIC: analog front-end with CSA, slow and fast shaper paths, ADC, digital part with hit generation and readout.
The characterization of the chip is an extensive procedure that includes multiple functional tests such as proper amplitude and time calibration. These are necessary steps to correctly interpret the collected data. The design of the analog front-end, with a double processing path for independent time and energy measurements, implies that the calibration should consider not only the ADC linearity aspects but also a homogeneous time response among all channels, and a well-known correlation of the threshold in both measuring paths. This work describes the characterization of the timing discriminator of the ASIC, the optimization of other-related chip parameters, and their effect on the measured data.

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