



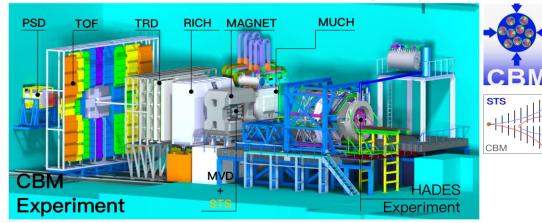
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ABSTRACT:

The Compressed Baryonic Matter (CBM) experiment is a fixed-target heavy-ion physics experiment at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany. The CBM physics program aims at exploring the QCD phase diagram at very high baryon densities, where a first-order phase transition from hadronic to partonic matter and a chiral phase transition is expected to occur. For highstatistics measurements of rare probes, CBM is designed to cope with very high interaction rates up to 10 MHz. Therefore, the experiment will be equipped with fast and radiation hard detectors employing freestreaming readout electronics.

The Silicon Tracking System (STS) is the essential component for tracking up to 1000 charged particles per event in nucleus-nucleus collisions. The experimental conditions pose demanding requirements in terms of channel density and read-out bandwidth to be met by the front-end electronics. An essential component is the STS-XYTER, a dedicated ASIC for the readout of the double-sided silicon micro-strip sensors. It is a low power, self-triggering ASIC with 128 channels, 5-bit ADC charge and 14-bit timing information. It needs to be fully integrated into a very confined space and it should perform in a high radiation environment. Several tests have been carried out to check the chips functionalities, the performance of modules as well as integration aspects. This contribution summarizes the characterization procedures of the final STS front-end electronics for different data taking scenarios.

THE COMPRESSED BARYONIC MATTER (CBM) EXPERIMENT



- · Fixed target experiment
- High interaction rates up to 10 MHz
- Free-streaming readout chain:
- Self-triggered Front- end electronics
- Powerful computing farm for 4D (x, y, z, t) tracking and online event reconstruction.
- Aim to explore the QCD phase diagram at high net-baryon densities and moderate temperatures.
- Unprecedented interaction rate is ideal for systematic, high precision studies of high-density nuclear matter.
- Multi-strange hyperons and hyper-nuclei reconstruction with complex decay topology.





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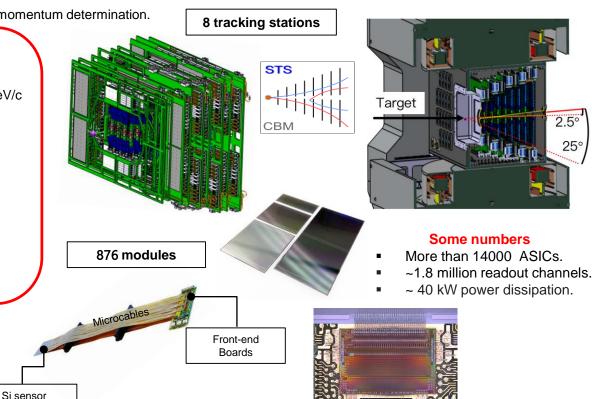
Main CBM detector for charged particle measurement & momentum determination.

THE SILICON TRACKING SYSTEM

- High track efficiency ~97% for p > 1 GeV/c.
- Excellent momentum resolution < 2% for p > 1 GeV/c
- Radiation hardness up to 10¹⁴ 1 MeV n_{eq} /cm².
- Low material: $\approx 0.3\% 1.5\% X_0$ per station
- Physics aperture, position in dipole magnet: $2.5^{\circ} \le \Theta \le 25^{\circ}$, $0.3 \text{ m} \le z \le 1.0 \text{ m}$
- 8 tracking stations
 - double-sided silicon microstrip sensors
 - − hit spatial resolution \approx 25 µm
- self-triggering front-end electronics
 - time-stamp resolution ≈ 5 ns

DETECTOR MODULE :

- Double-sided silicon microstrip sensor.
- Stack of Al-polyimide readout cables (up to 50 cm).
- 2 front-end boards (2 × 8 ASICs).

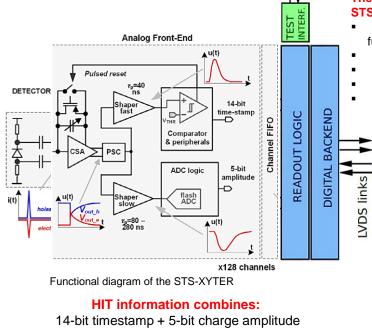






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Designed by K. Kasinski et al at AGH, Cracow; fabricated in UMC 180 nm technology

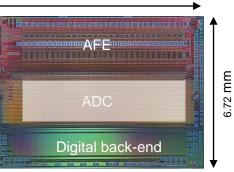


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7-bit channel address + 1-bit event missing flag

The STS-XYTER ASIC:

- STS + X, Y coordinates + Time and Energy Readout
- Self triggered ASIC that combines analog and digital functionalities.
- 128 + 2 test channels staggered with 58 µm pitch.
- 14 fC dynamic range.
- Radiation hard layout.
- Backend compatible with the GBTx data concentrator



10.00 mm

The STS-XYTERv2 ASIC under the microscope.

Main features for every channel:

- A charge sensitive amplifier (CSA) with gain switching to address different dynamic ranges.
- Polarity selection circuit (PSC) to have a single polarity in the preceding stages.
- Two parallel signal paths:
 - FAST shaper and a comparator for the arrival time determination (Time resolution ~5 ns)
 - SLOW shaper with a 5-bit flash ADC and ~14 fC dynamic range with digital peak detector.
 - The ADC uses 31 comparators, each of them with 8-bit trimming and 12-bit auxiliary counters.
- AFE control registers implemented as radiation hard DICE cells.
- The AFE circuits use ELT NMOS transistors to improve the TID immunity.

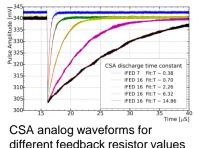


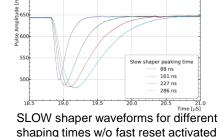


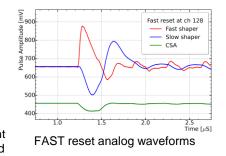
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TESTING PROCEDURES:

- Acquisition and evaluation of the waveforms in the test channels for different polarities.
- Waveforms for different ASIC register settings.
- Analog waveforms from FAST and SLOW shapers for different injected charges.
- Estimation of the CSA discharging constant, shaper's gain, linearity.
- Verification of the fast reset functionality.





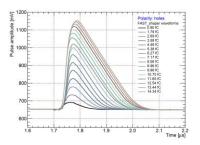


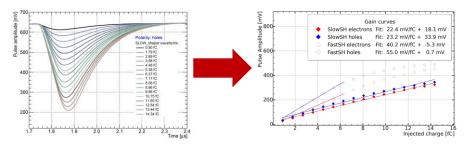
@THE FEB-C WAVEFORMS



FINDINGS:

- Characteristics as expected & previously measured.
- The fast reset functionality is not working properly.





VERIFICATION:

- Shapers linearity and gain characteristics as expected (similar to previous versions).
- FAST shaper linearity achieved up to ~7 fC.
- SLOW shaper linearity achieved up to ~14 fC (full ADC range).





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ASIC ENC studies performed at the FEB-C:

- Register settings optimized for operation:
 - CSA current scan.
 - Feedback resistance values.
 - Shaping time.
- ENC vs input capacitance.

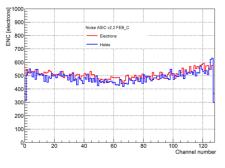


@THE FEB-C ENC studies



STS-XYTERv2.1

STS-XYTERv2.2



FINDINGS:

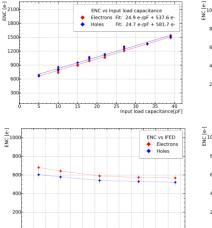
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- Results are in the expected level and comparable with its predecessor.
- ENC levels stable and similar across different register settings.

0 120 Channel number

ENC dependence with capacitance (~25 e-/pF) for both polarities.

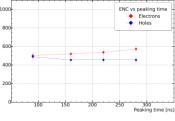
Noise studies for different operational settings

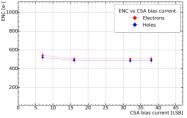


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