Operational Experience and Performance with the ATLAS Inner Detector at the Large Hadron Collider at CERN

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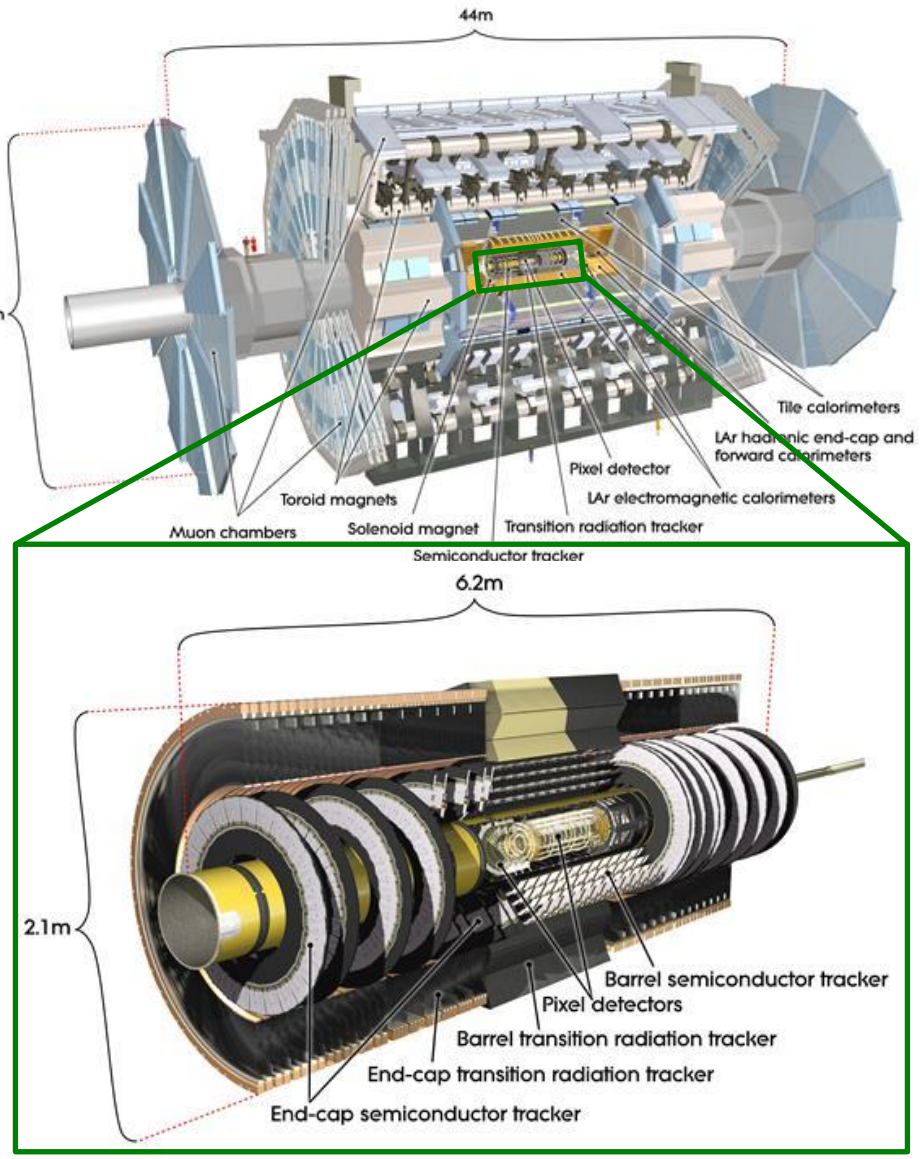
On behalf of the ATLAS Collaboration

ATLAS Inner Detector

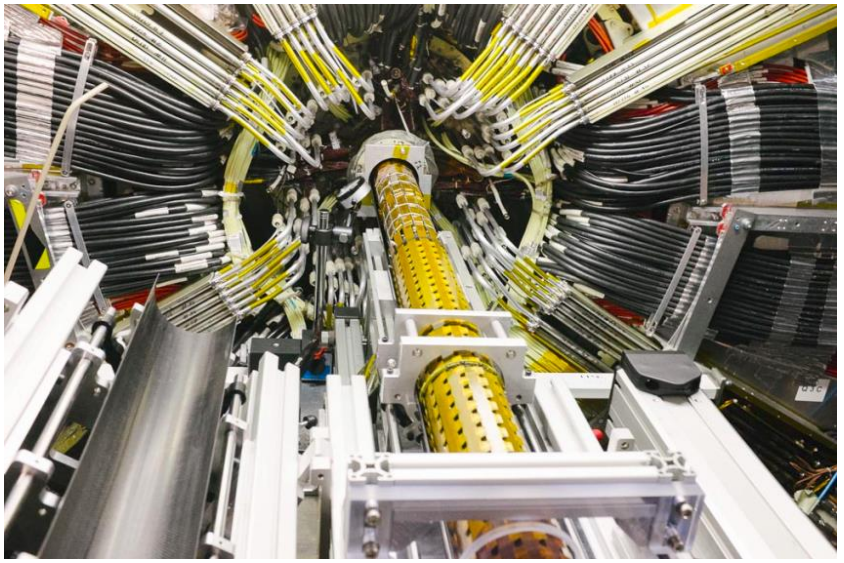
- IBL/Pixel
  - 92 million channels
  - 8 um/40 um resolution (IBL)
  - 10 um/115 um resolution (Pixel)
- SCT
  - 6.3 million channels
  - 17 um/570 um resolution
- TRT (Transition Radiation Tracker)
  - 35,000 channels
  - 130 um resolution

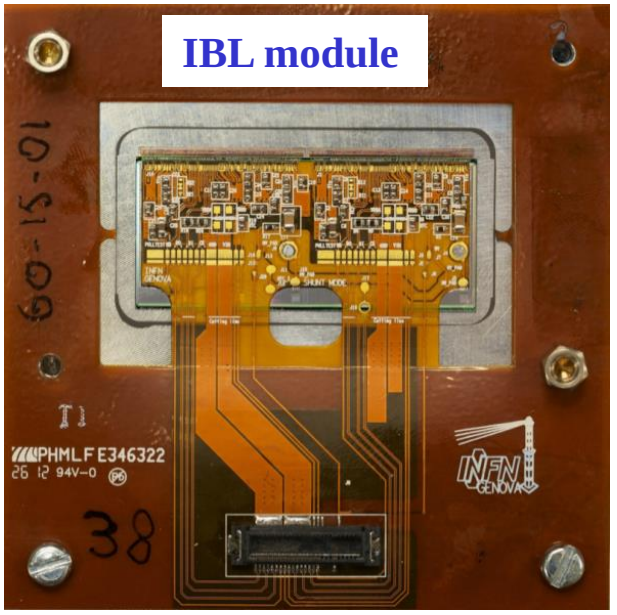
This talk focuses on IBL/Pixel and SCT in Run 1/Run 2 operation.



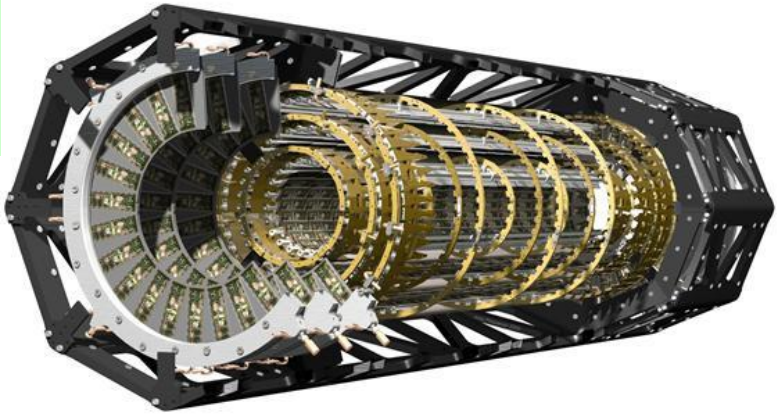
IBL (Insertable B-Layer)

- Innermost pixel barrel layer installed in 2014 (Radius: 3.3 cm)
- Sensor technology: n-in-n planar (75%) and 3D (25%)
  - IBL is the first detector to use 3D sensor in HEP experiments.
- Pixel size: 50 x 250 um^2
- FE-I4 front-end ASIC
  - 130 nm CMOS technology
  - Provides charge info with 4-bits ToT
- CO_2 evaporative cooling
- Radiation tolerance: up to 5 x 10^{15} n_{eq}/cm^2

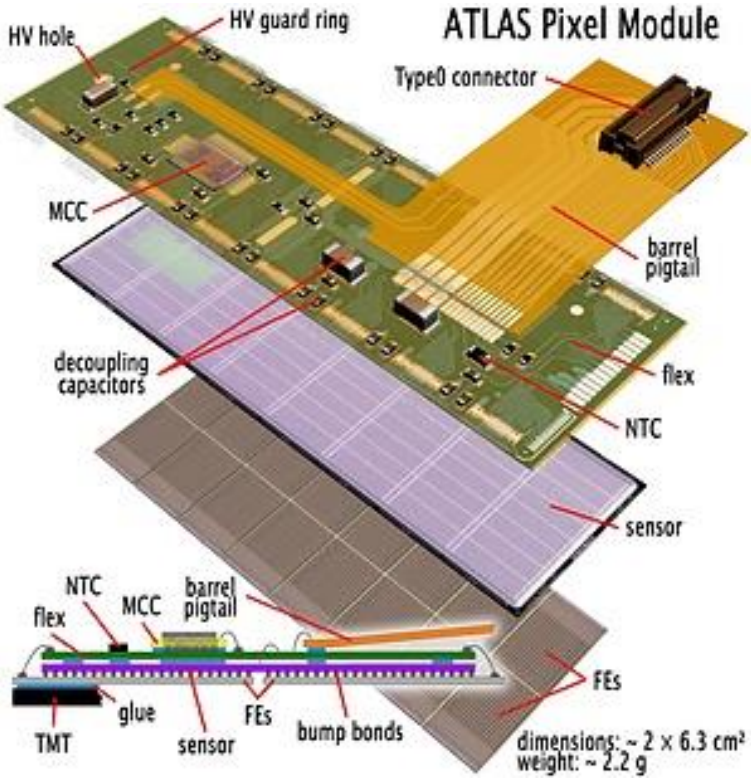




Pixel

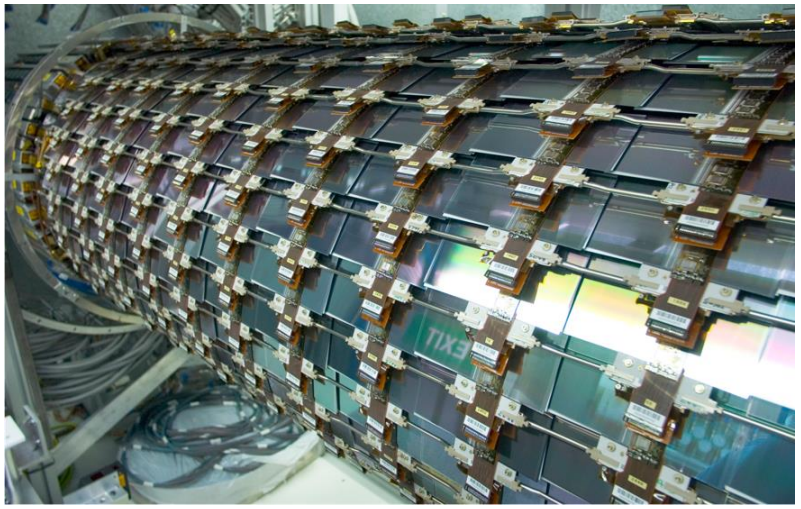


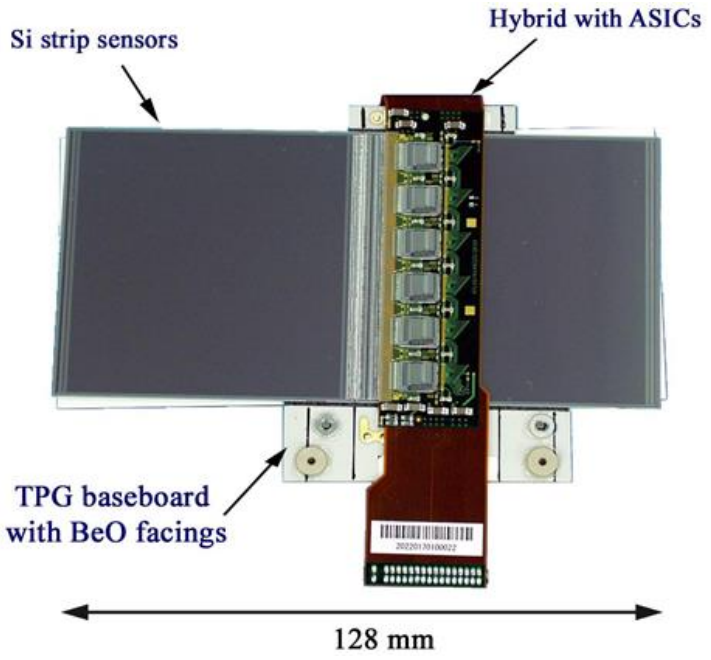
- Pixel detector existing since Run 1 with 3 barrel layers and 3 x 2 endcap disks
  - B-Layer, Layer1, Layer2 in barrel
- n-in-n planar sensor technology
- Pixel size: 50 x 400 um^2
- FE-I3 front-end ASIC
  - 250 nm CMOS technology
  - Provides charge info with 8-bits ToT
- One Pixel module with 16 FE-I3s and 1 MCC (controller chip).
- C_3F_8 evaporative cooling
- Radiation tolerance: up to 1 x 10^{15} n_{eq}/cm^2



SCT (SemiConductor Tracker)

- Silicon strip detector with 4 barrel layers and 9 x 2 endcap disks
  - The detector is operated since Run 1.
  - Barrel 3/4/5/6 in barrel
- 80 um strip pitch with 12.8 cm length
- One module consists of top/bottom sensor layers with 40 mrad stereo angle.
  - 768 x 2 strips/module
- 12 ABCD front-end chips/module
  - Provides binary hit pattern with 3-bits





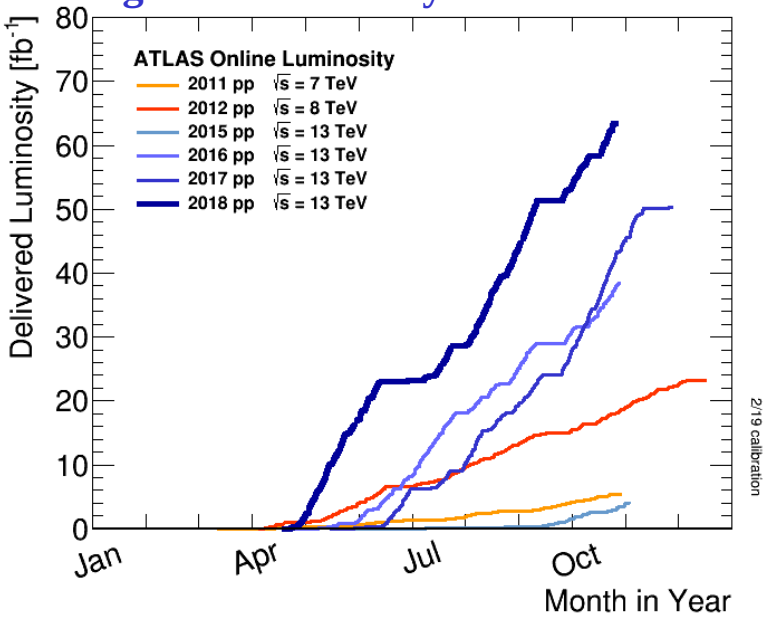
Overview of Run 1/Run 2 operation

ATLAS Run 1/Run 2 data-taking

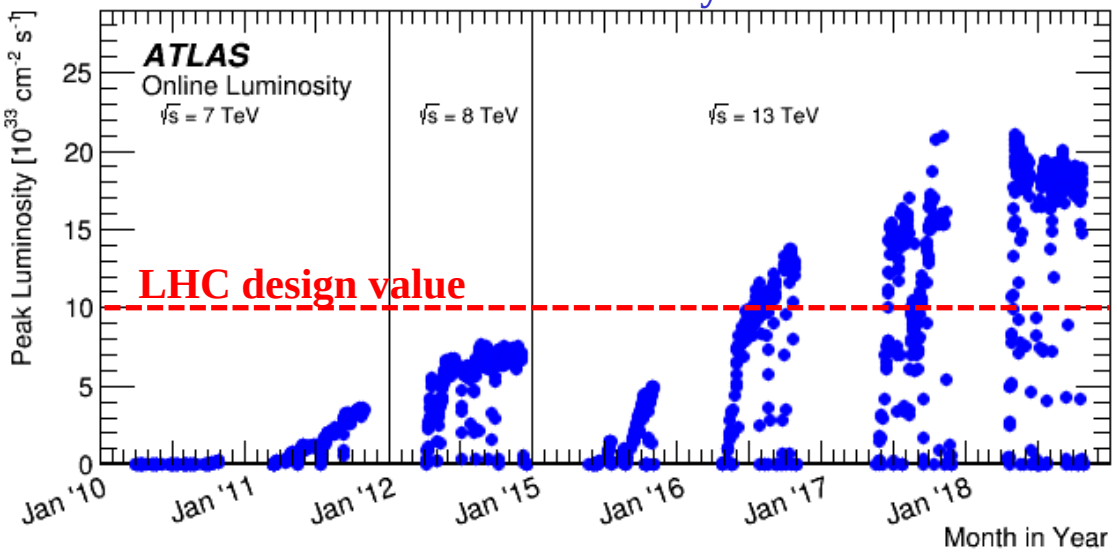
- ATLAS collected 5.1/21.3 fb^{-1} with 7/8 TeV in Run 1 (2010 - 12) and 149 fb^{-1} with 13 TeV in Run 2 (2015 - 18).
- The instantaneous luminosity reached 2 times larger than LHC design value in Run2 (LHC design value: 1.0 x 10^{34} $cm^{-2}s^{-1}$).

Inner detector was operated successfully with high data-taking efficiency even in high luminosity condition.

Integrated luminosity in Run1/Run2



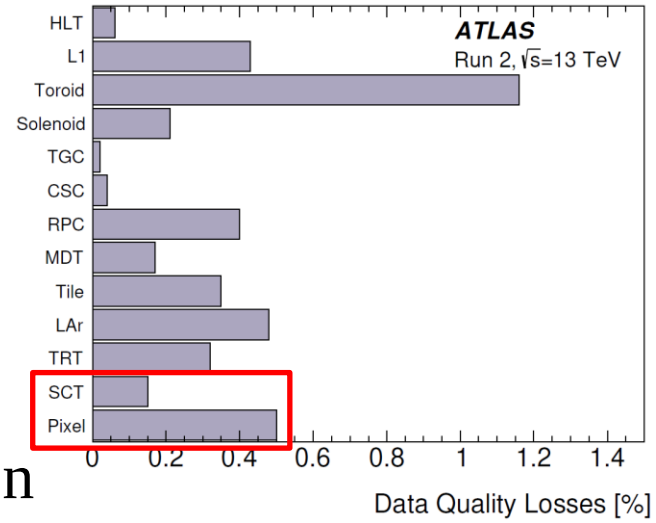
Instantaneous luminosity in Run1/Run2



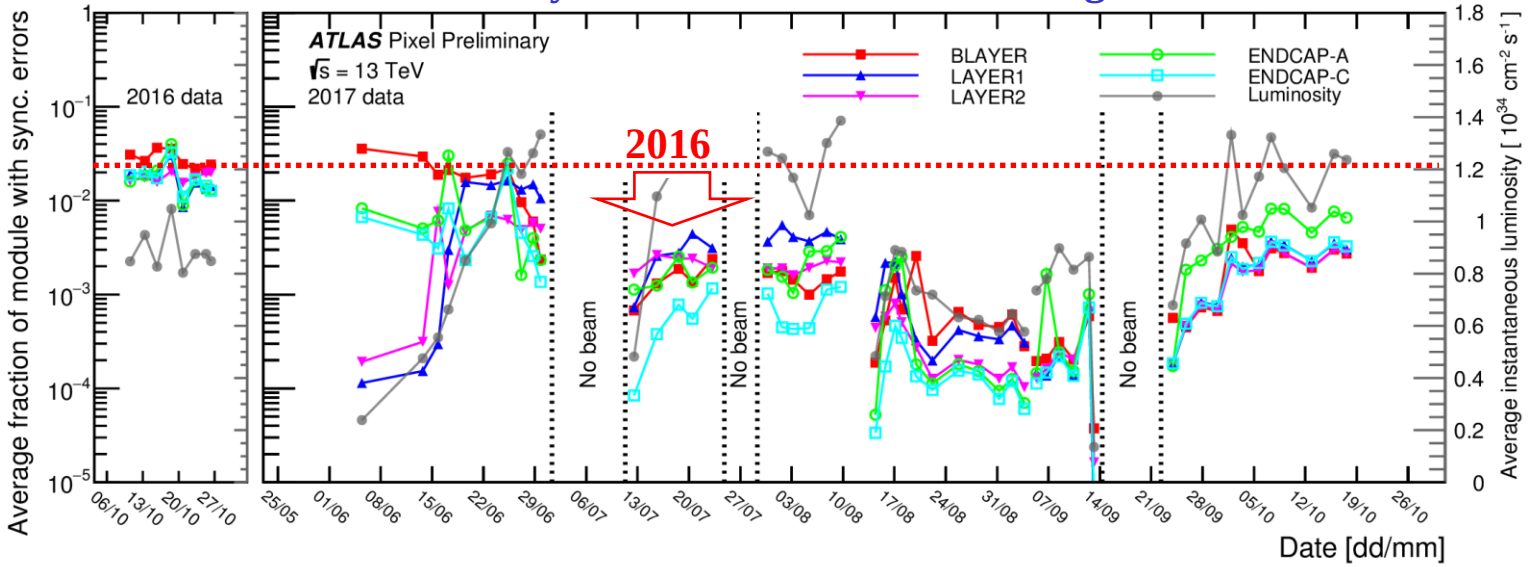
Detector stability

- Fraction of data used for physics analyses:
  - IBL/Pixel: 99.5%, SCT: 99.9%
  - Total fraction in ATLAS: 95.6%
- Stability of Pixel was improved by modification of DAQ hardware/firmware/software.
- SCT achieved constantly stable operation.

Fraction of data rejected for physics analyses in Run 2



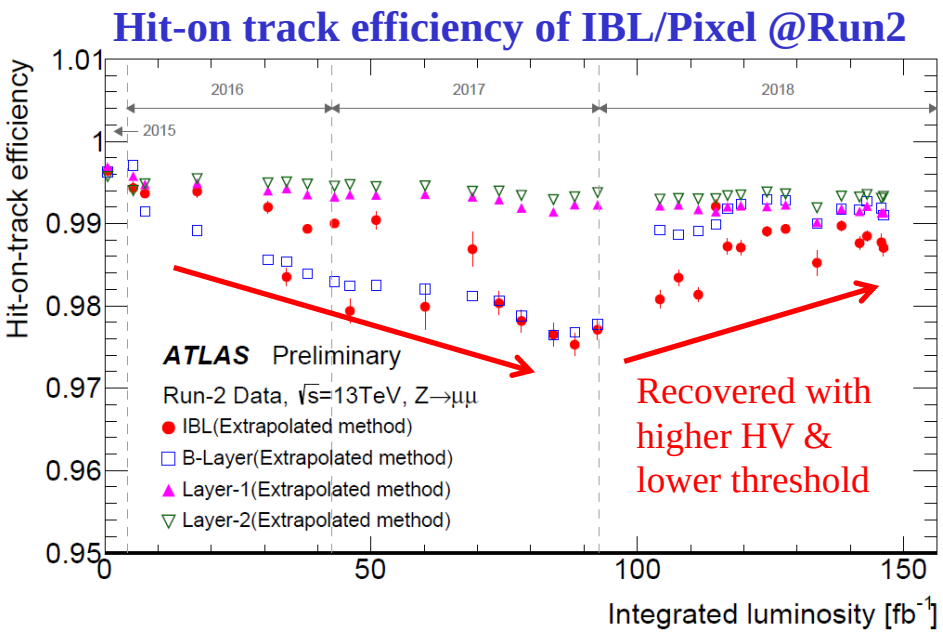
Fraction of desynchronization in Pixel during 2016-2017



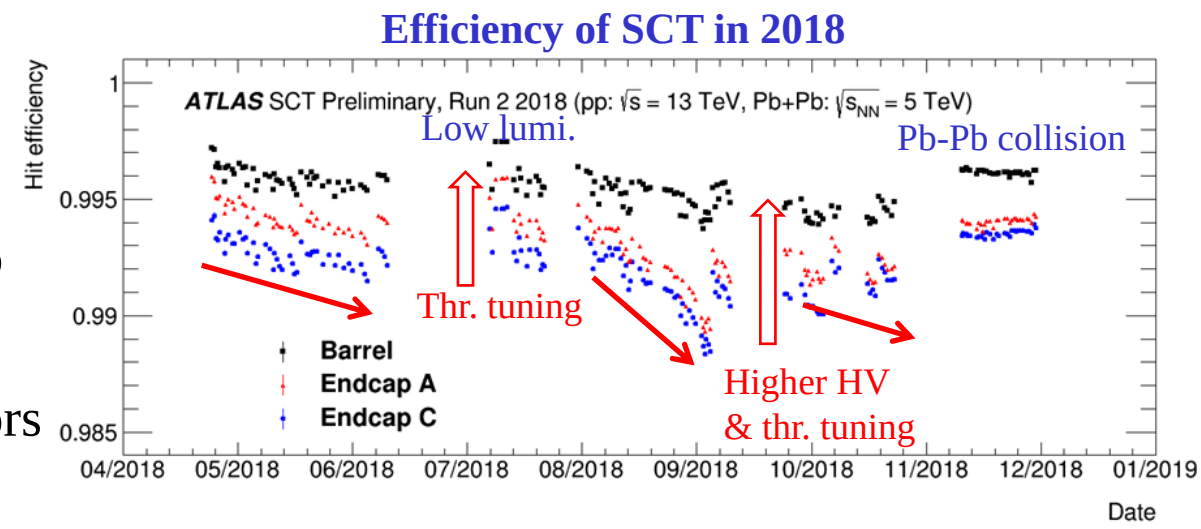
Hit-on-track efficiency

- Hit-on-track of efficiency dropped in IBL & B-Layer before ~90 fb^{-1}.
  - IBL: under depletion before ~45 fb^{-1} and only the rad. damage after then
  - B-Layer: radiation damage

→ Recovered with higher HV and lower threshold.

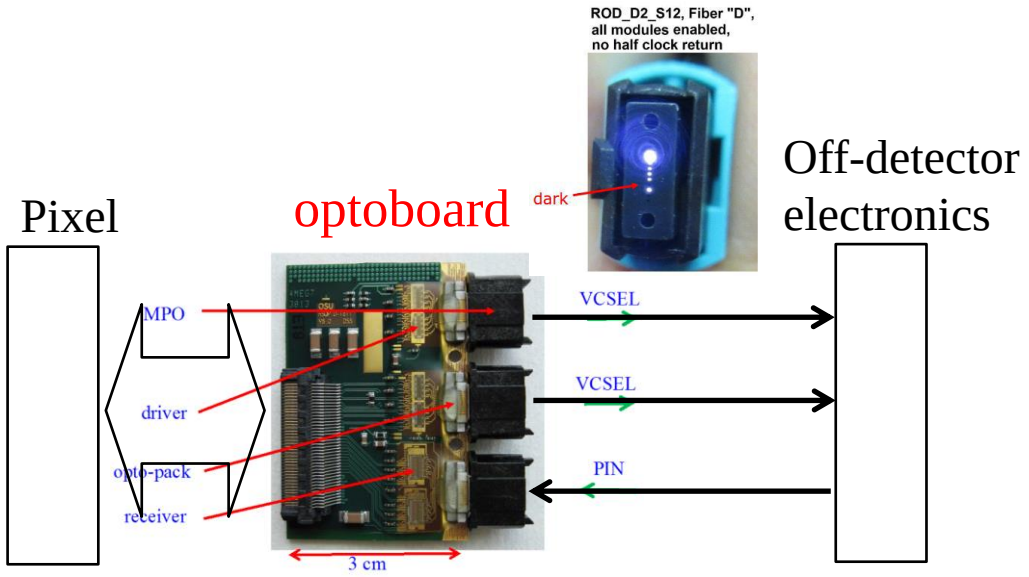


- Increasing noise caused efficiency loss in SCT.
  - Detuning of threshold due to TID (Total Ionization Dose).
  - Under depletion of the sensors also contributes.



Failure of optoboards in Pixel

- Pixel had issue of a high failure rate of the VCSELs on optoboard, which is used for data transmission on the detector.
- The cause of the failure is not known, possibly humidity.
- ~30 boards were replaced before 2018 run, but ~30 additional VCSELs have died since then.
- In February 2021, all suspicious optoboards will be replaced.



Radiation damage on silicon sensor

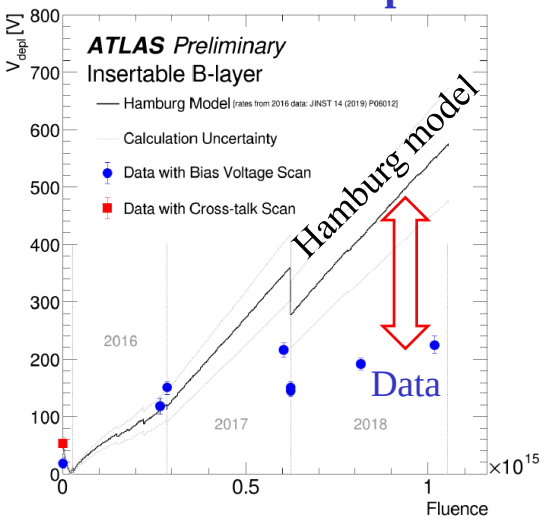
Depletion voltage

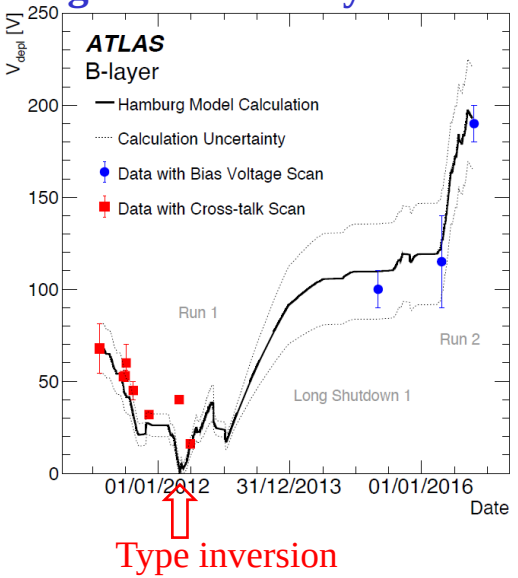
- IBL/Pixel/SCT use n-type bulk, and type inversion to p-bulk is caused by radiation.

- Expected date of type inversion:
  - IBL: 2015
  - B-Layer: 2012
  - SCT Barrel 3: 2016
  - SCT Barrel 4/5/6: 2017

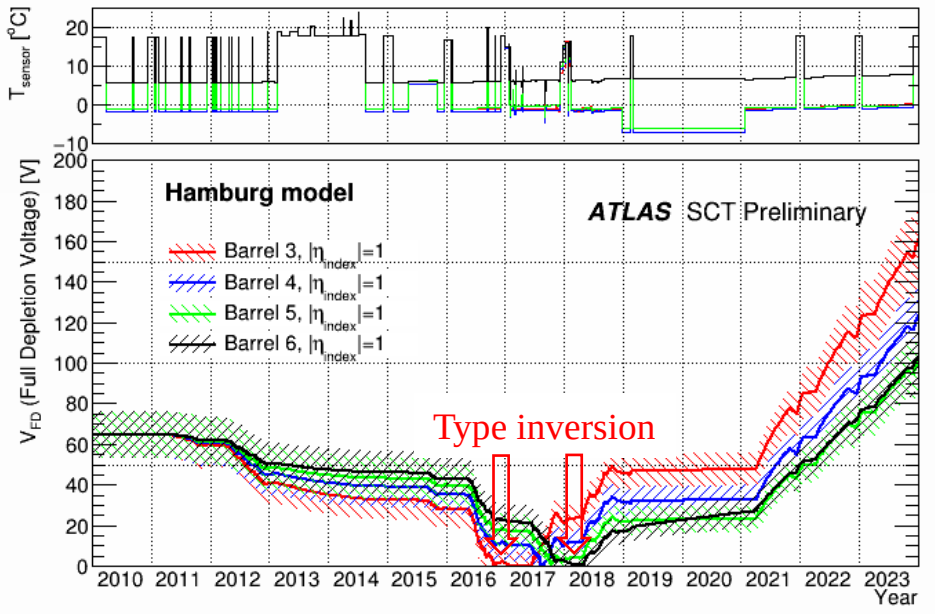
- Agreement of depletion voltage is not good with Hamburg model in IBL (the reason is still unclear).

Variation of depletion voltage in IBL/B-Layer





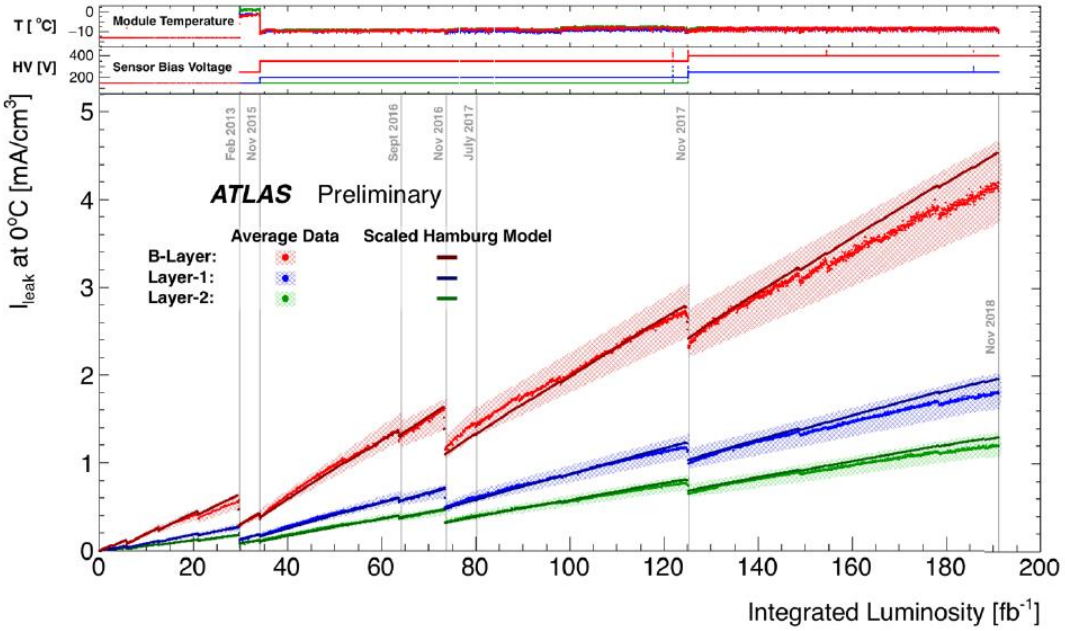
Simulated depletion voltage in SCT



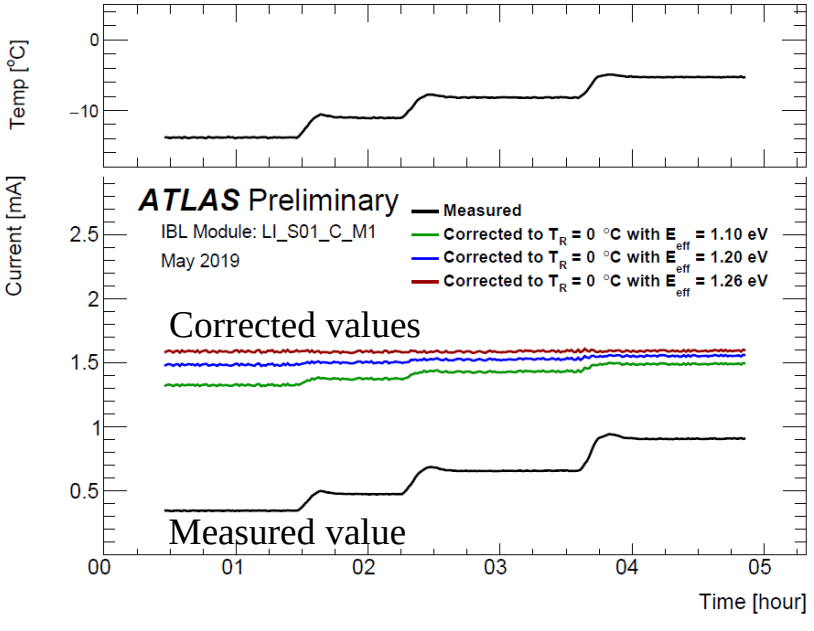
Leakage current in silicon sensor (IBL/Pixel)

- Leakage current of the silicon sensors has been increasing as a function of radiation dose.
- Prediction with Hamburg model is higher than data in Pixel.
- The current corrected to 0 deg. is scaled with different effective silicon band gap energy (normally, E_g = 1.21 eV is used).

Leakage current in Pixel

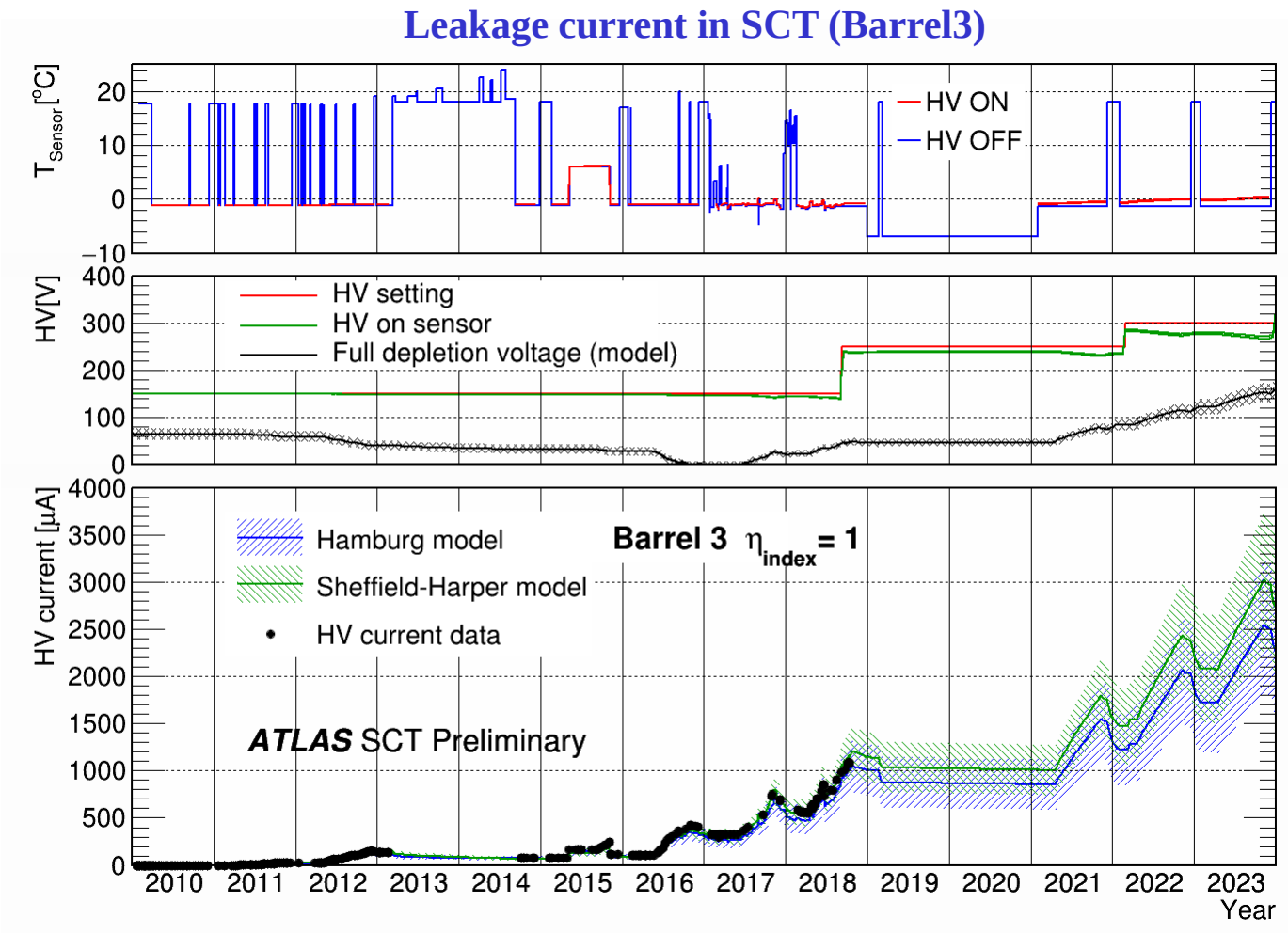


Leakage current with different E_g (IBL)



Leakage current in silicon sensor (SCT)

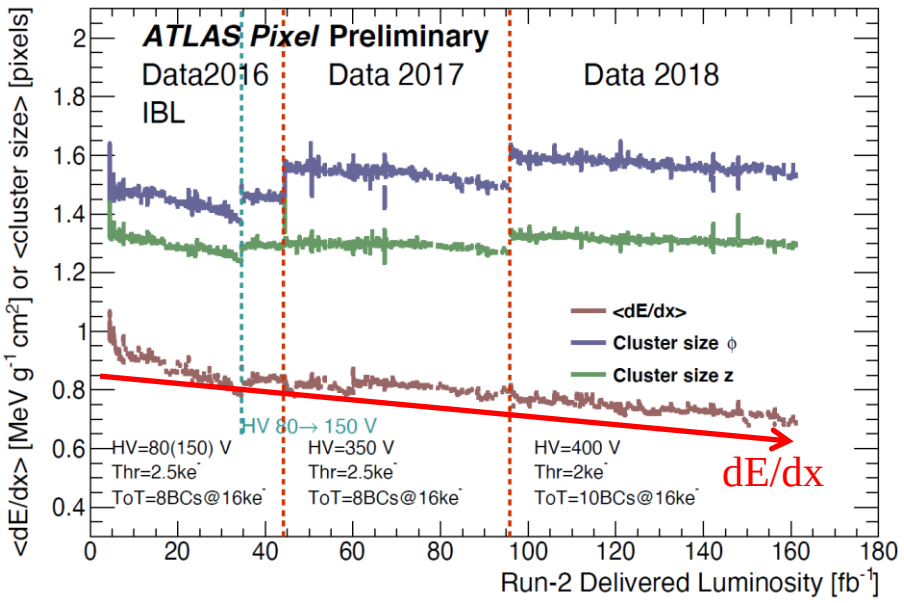
- The current is consistent both with Hamburg model and Sheffield-Harper model in SCT.



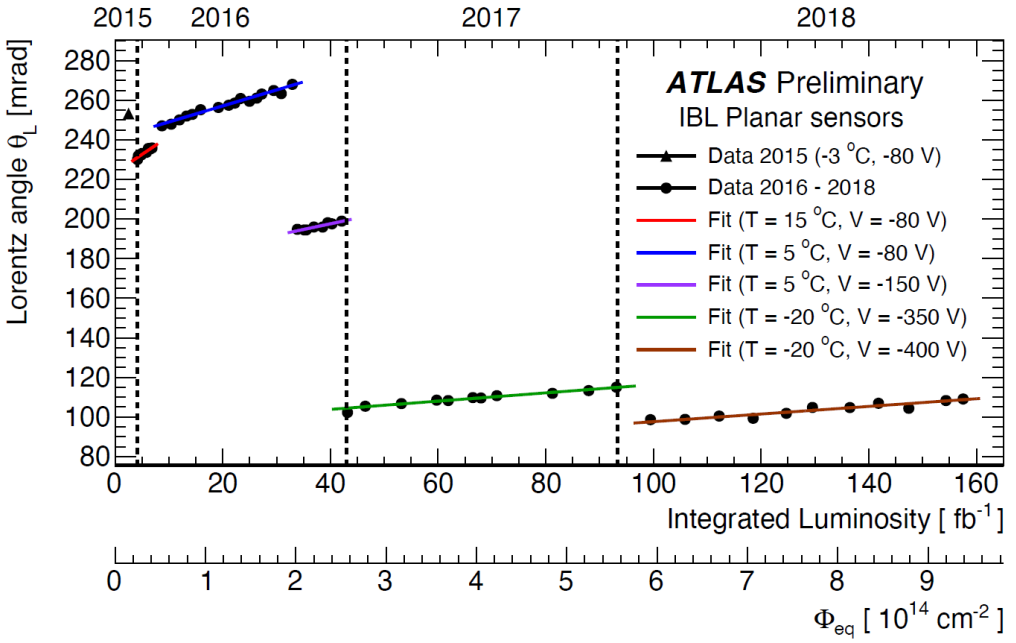
Charge collection & Lorentz angle (IBL)

- 30% decrease of measured dE/dx in IBL shows loss of the charge collection due to charge trapping caused by radiation damage on the sensor bulk.
- Lorentz angle is sensitive to deformations in the electric field within a sensor, and IBL shows clear dependence of Lorentz angle on temperature, voltage, and radiation damage.

Measured charge and cluster size @IBL



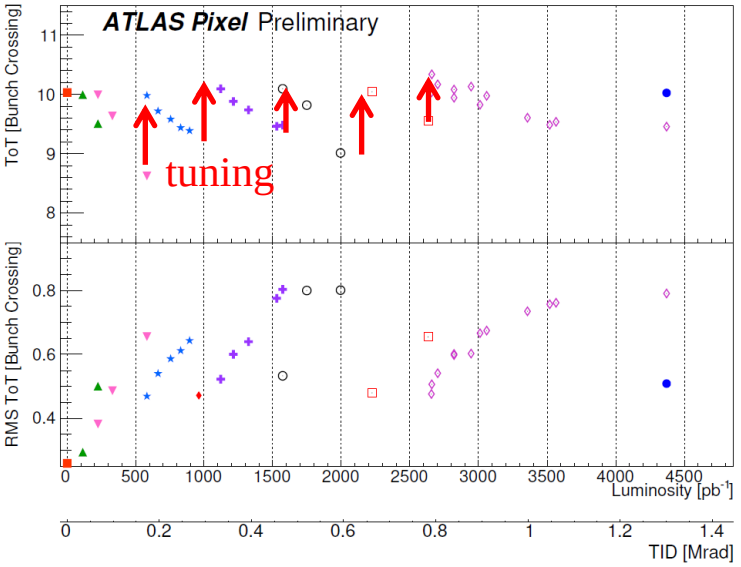
Lorentz angle v.s. fluence @IBL



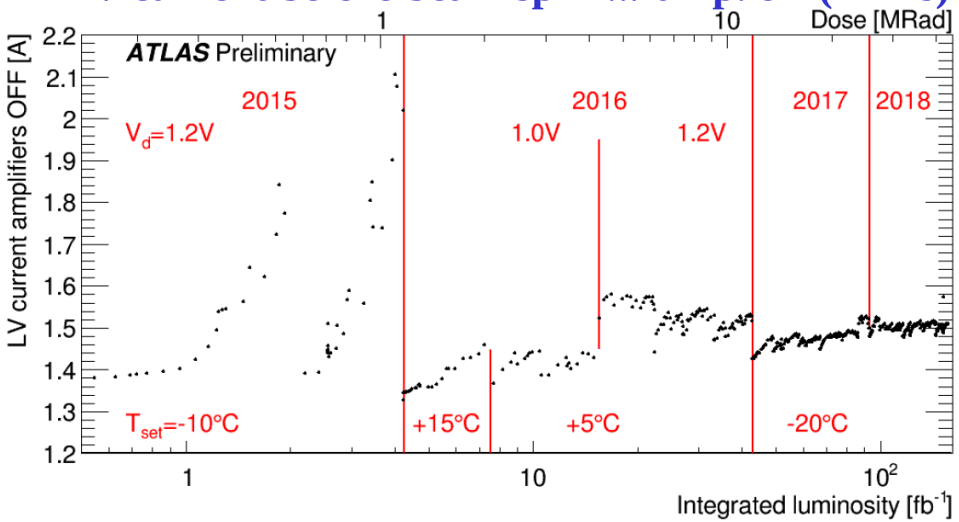
TID effect (IBL)

- Effect of TID (Total Ionization Dose) on FE-I4 chip was visible in IBL soon after operation of the detector started.
  - Detuning of ToT/threshold
  - Increase of LV current
- The effect was mitigated with lower digital voltage/temperature and frequent tuning.

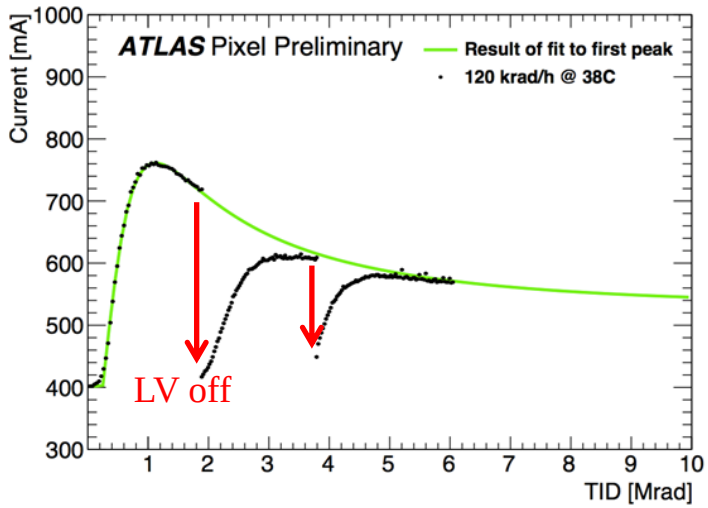
ToT drift v.s. int. lum. (TID)



LV current before beam spill w/ amp. off (4 FEs)

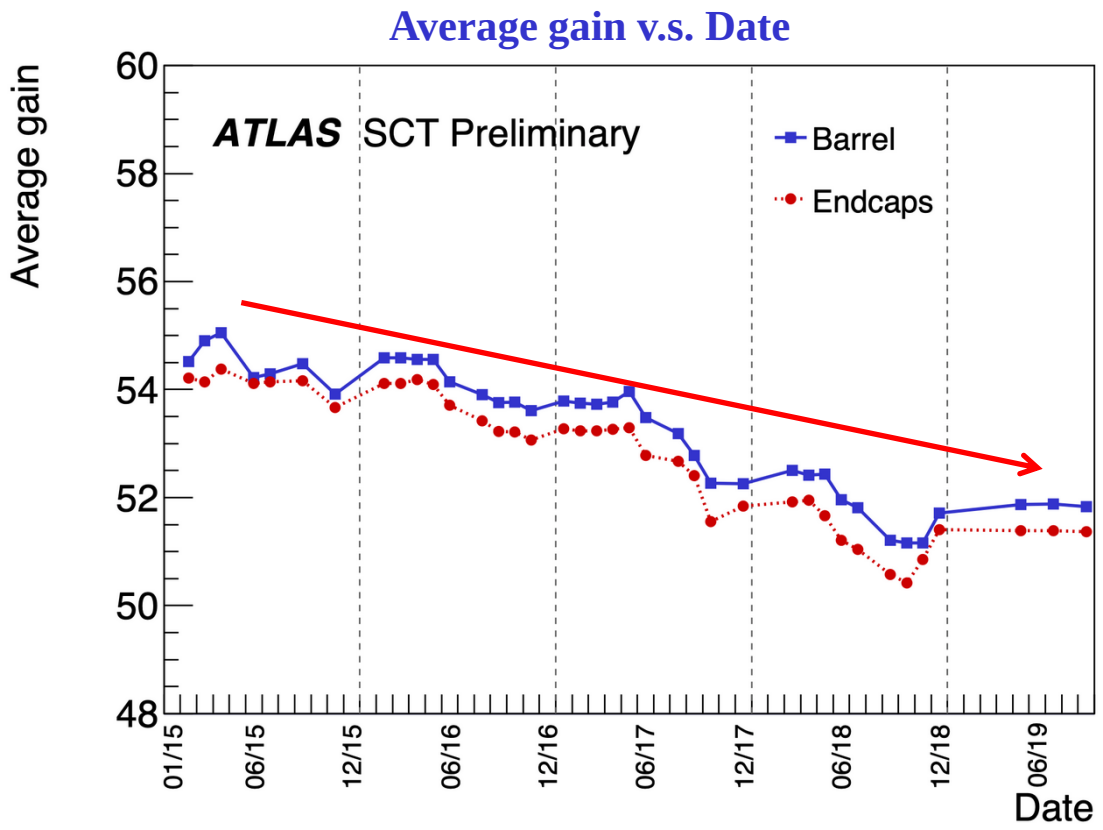


LV current v.s. TID measured at Lab. (1 FE)



TID effect (SCT)

- TID effect is also visible in decrease of the amplifier gain of ABCD chips in SCT during Run 2.
- The gain drop is not problematic for the operation yet and recoverable by tuning.

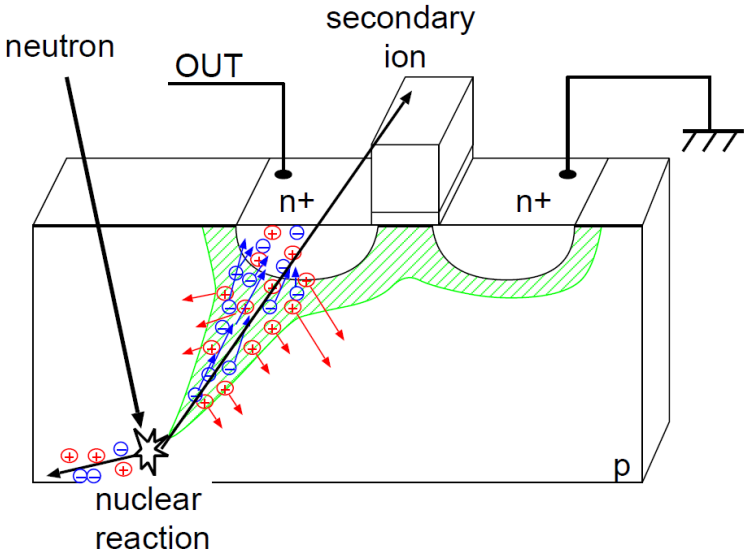


Single event effects on front-end ASIC

Single event effects

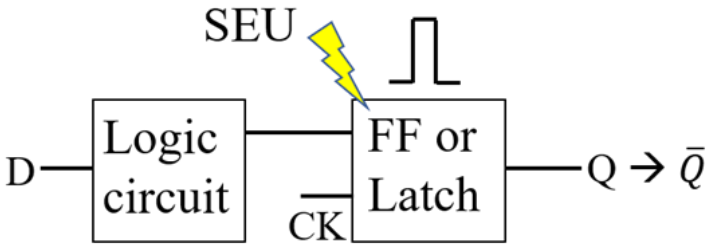
Single Event Upset (SEU)

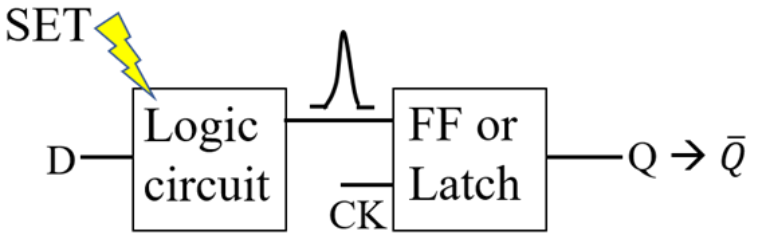
- The charges caused by a charged/neutral particle alter the state of memory.
- On-chip memory corruption leads to detuning and reduction of hit efficiency.



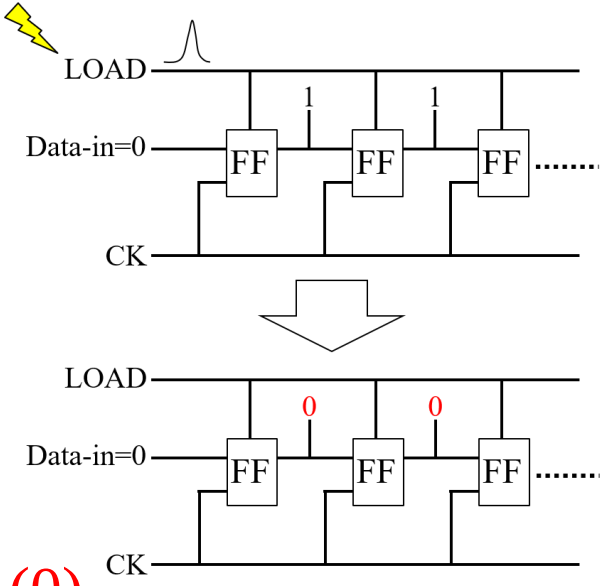
Single Event Transient (SET)

- A glitch caused by single event effect travels through combinational logic and is captured into storage element.





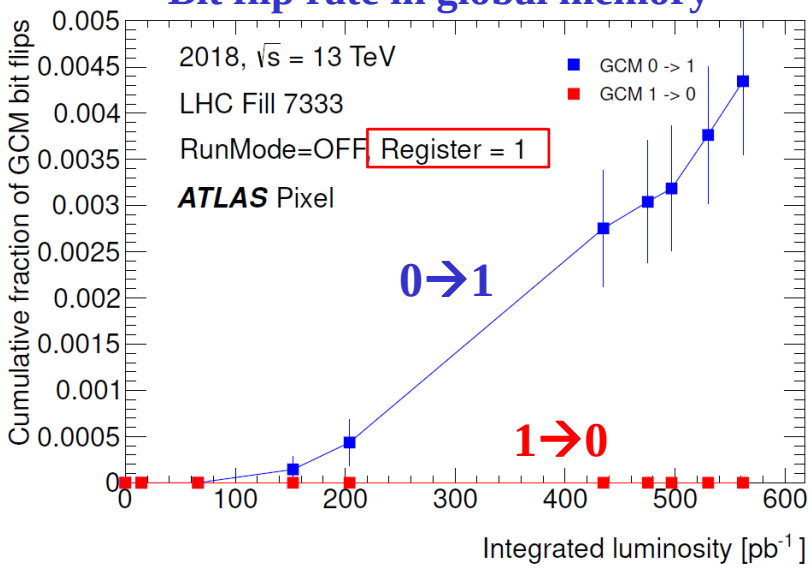
SEU v.s. SET (IBL)



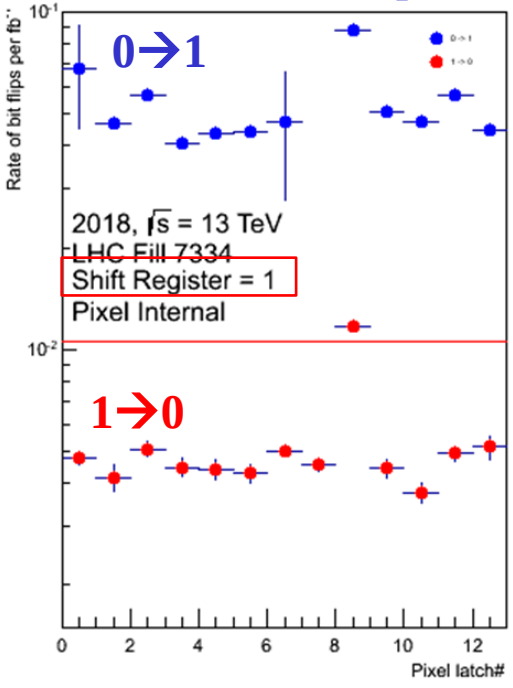
- Bit flip rate in FE-I4 chip was studied.
  - global memory: chip level configuration
  - pixel cell memory: pixel level configuration
- 0→1 (1→0) flips dominate for register input = 1 (0).

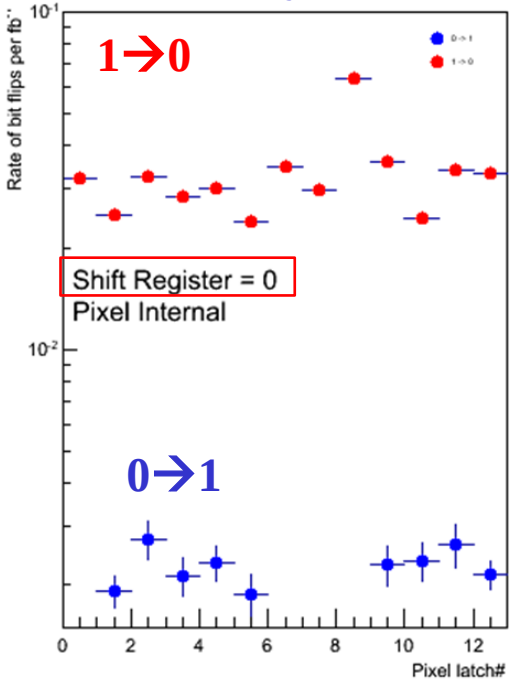
⇨ SET (glitches) is the primary source of bit flips.

Bit flip rate in global memory



Bit flip rate in pixel cell memory



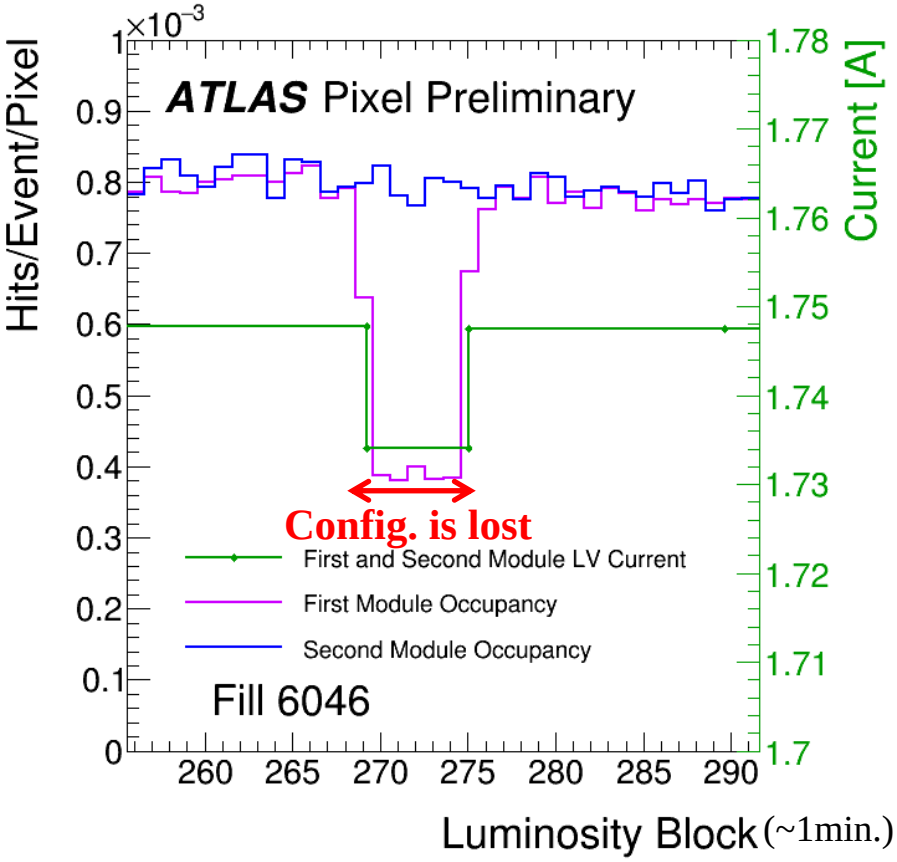


Global configuration recovery (IBL)

- Global memory corruption causes change of LV current consumption, quiet modules, desynchronization, etc..
- Mechanism to refresh global memory every 5 s was deployed in 2017.
  - No extra dead time is added.

Proper function of the module could be restored by re-configuration.

Hit rate and LV current in IBL module

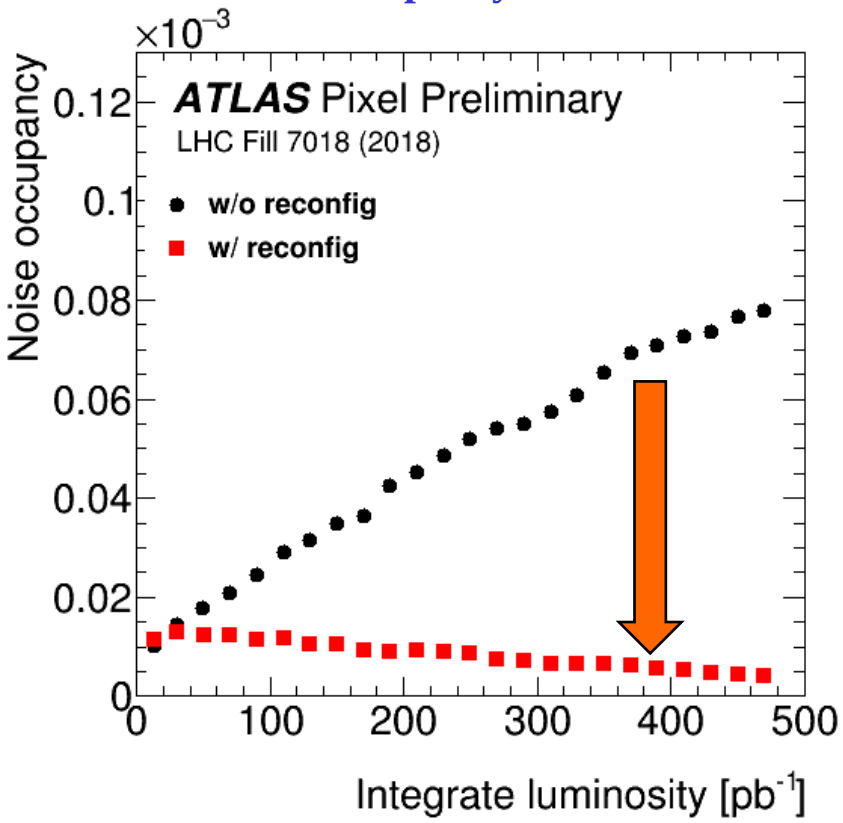


Pixel configuration recovery (IBL)

- The auto mechanism to reconfigure pixel cell memory was tested in 2018 data-taking.
- A fraction of the chip is refreshed every 5 s, resulting in complete reconfiguration of the chip after 11 min.

Noise hits caused by SEU/SET could be suppressed to negligible level.

Noise hit occupancy v.s. Int. lumi.

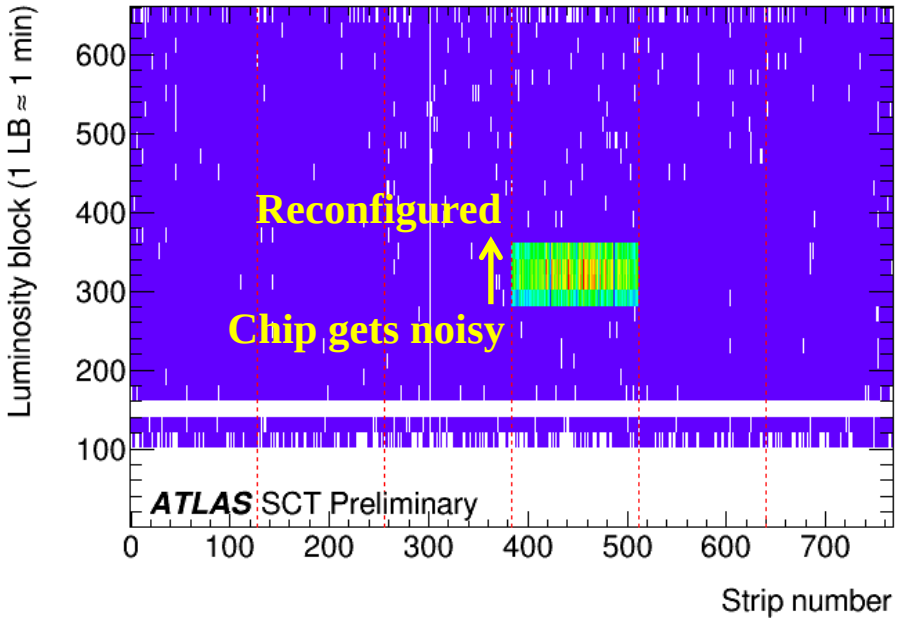


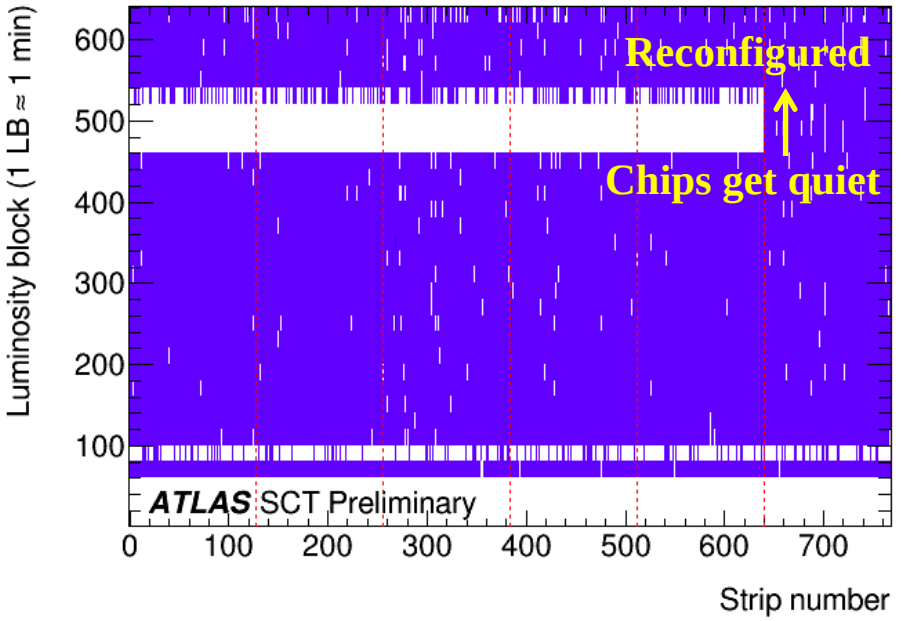
Single event effects (SCT)

- Single event effects were visible in operation of ABCD chips in SCT.
- The strips became noisy or quiet by bit-flip of the threshold registers.
- Automatic mechanism of reconfiguration at every 90 minutes was implemented in Run 2.

→ The functionality of the chips could be restored by reconfiguration.

Hits map in SCT (strip ID v.s. Luminosity block)





Summary & Conclusions

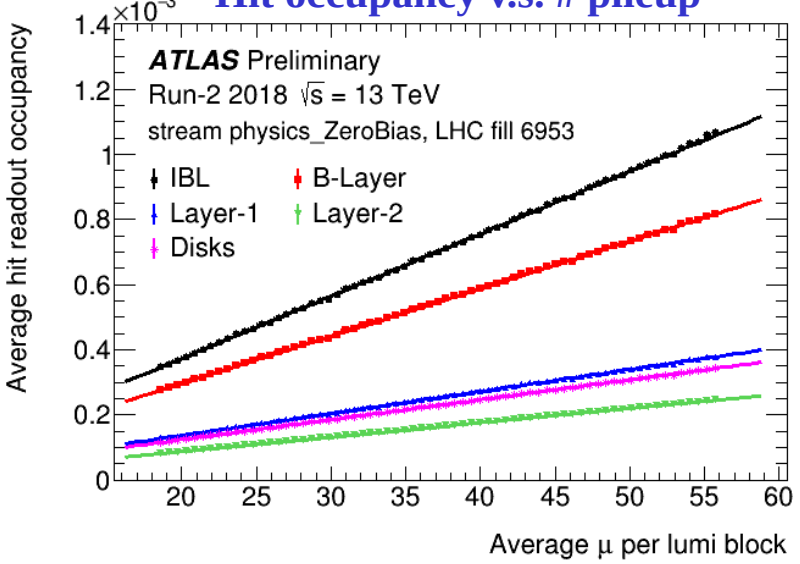
- IBL/Pixel and SCT were operated successfully in stable condition during Run 1/Run 2.
- The effect of radiation damage on silicon sensor appeared both in IBL/Pixel and SCT.
  - higher leakage current, higher depletion voltage, lower charge collection efficiency.
  - Modeling of radiation damage on IBL/Pixel is summarized in JINST 14 (2019) P06012.
- A significant number of Pixel VCSELs has failed during Run2, and all suspicious optoboards will be replaced in February 2021.
- TID caused detuning of chip parameters (gain, threshold and ToT), and the effect can be recovered by frequent tuning.
- Single event effects became visible in IBL (JINST 15 (2020) P06023) and SCT, that could be mitigated by re-configuring the chips.

Backup

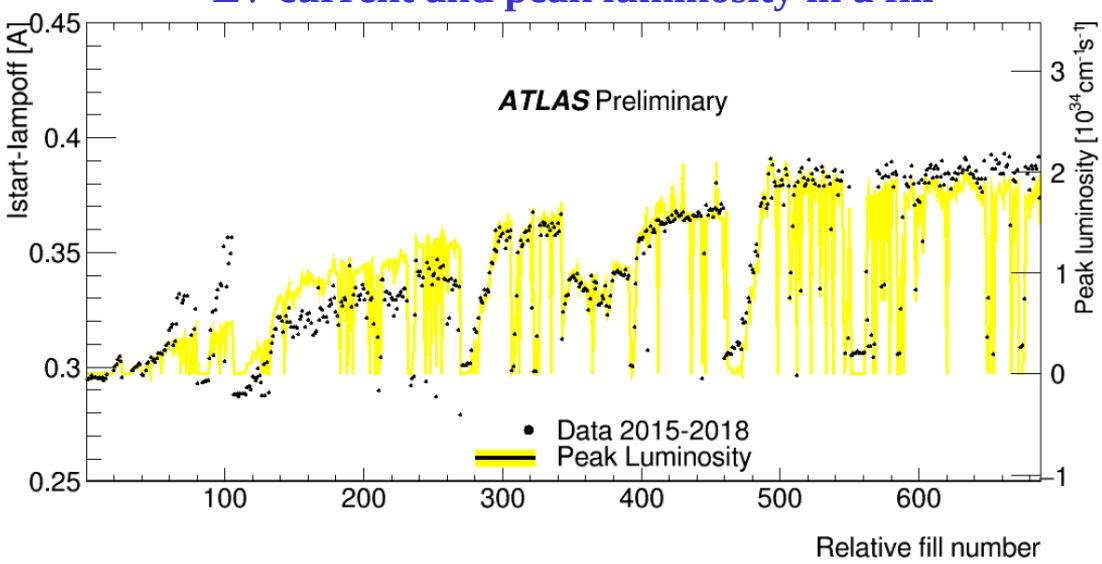
High luminosity operation (IBL/Pixel)

- The hit occupancy of IBL/Pixel linearly increased as a function of the luminosity and became more than 10^{-3} at the maximum in IBL.
  - No occupancy saturation even with high pileup condition.
- LV current in IBL shows good correlation with peak luminosity in a fill due to activities in the front-end.

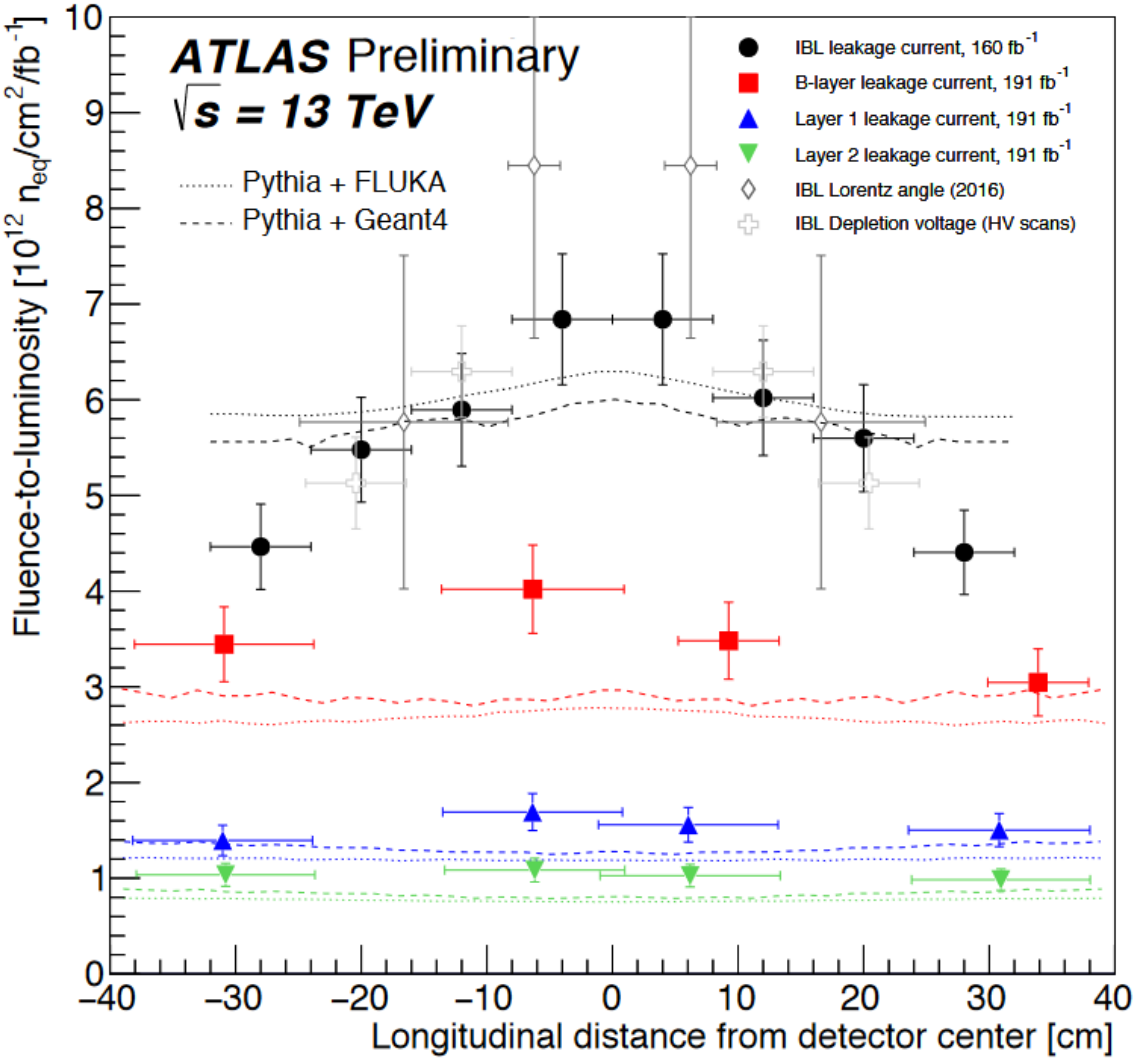
Hit occupancy v.s. # pileup



LV current and peak luminosity in a fill



Fluence in IBL/Pixel



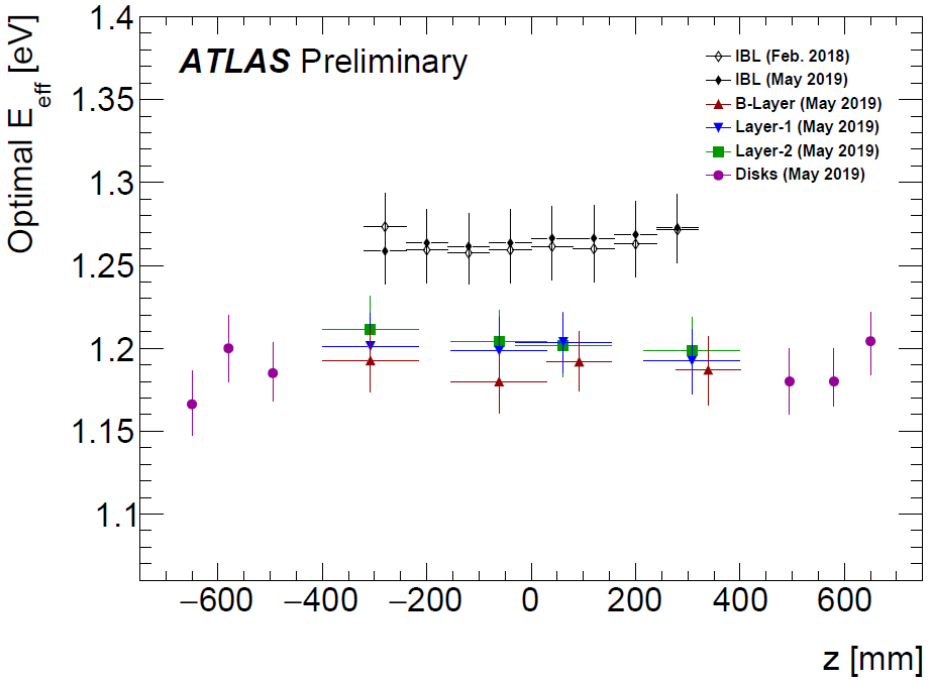
Effective band gap in IBL/Pixel

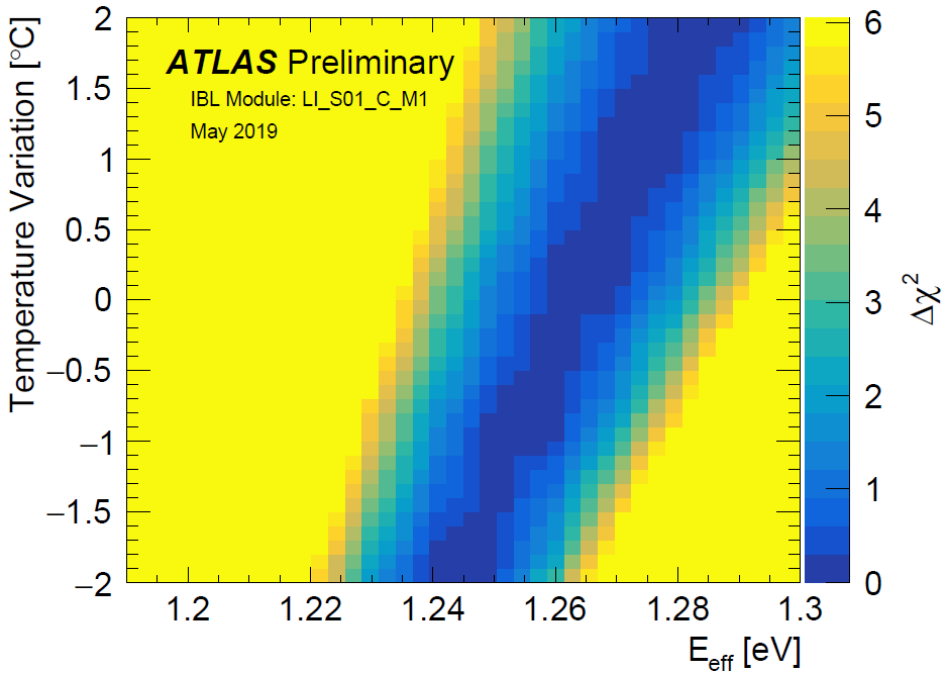
- The leakage current is corrected to the reference temperature (T_R):

$$I(T) = I(T_R)/R(T)$$

$$R(T) = (T_R/T)^2 \exp\left(-(E_{\text{eff}}/2k_B) \times (1/T_R - 1/T)\right)$$

- The optimal silicon effective band gap (E_{eff}) is determined by χ^2 fitting in the rage of systematic error of temperature measurement (± 2 deg.)

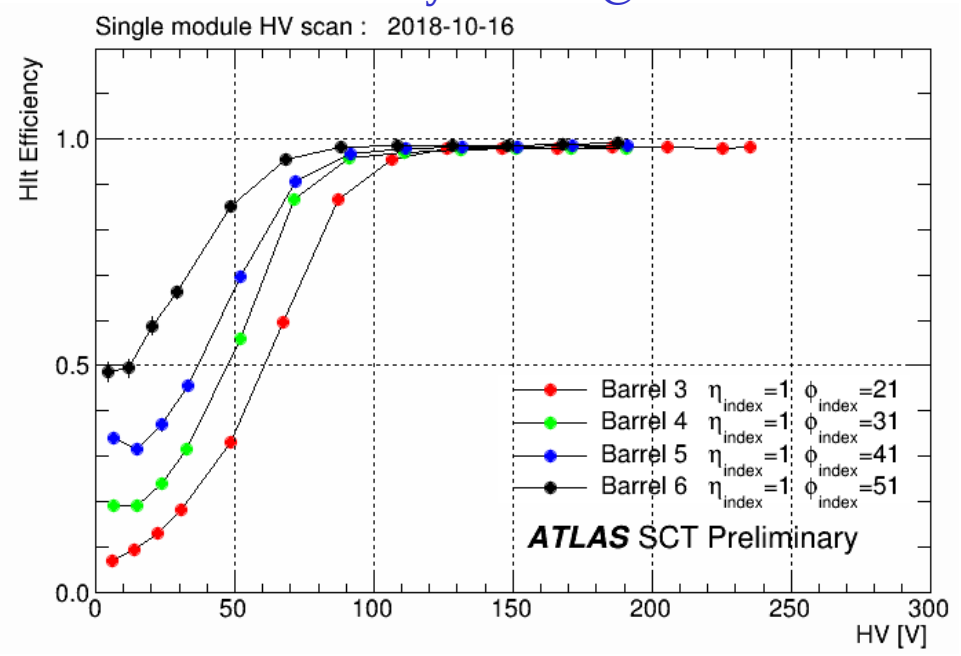




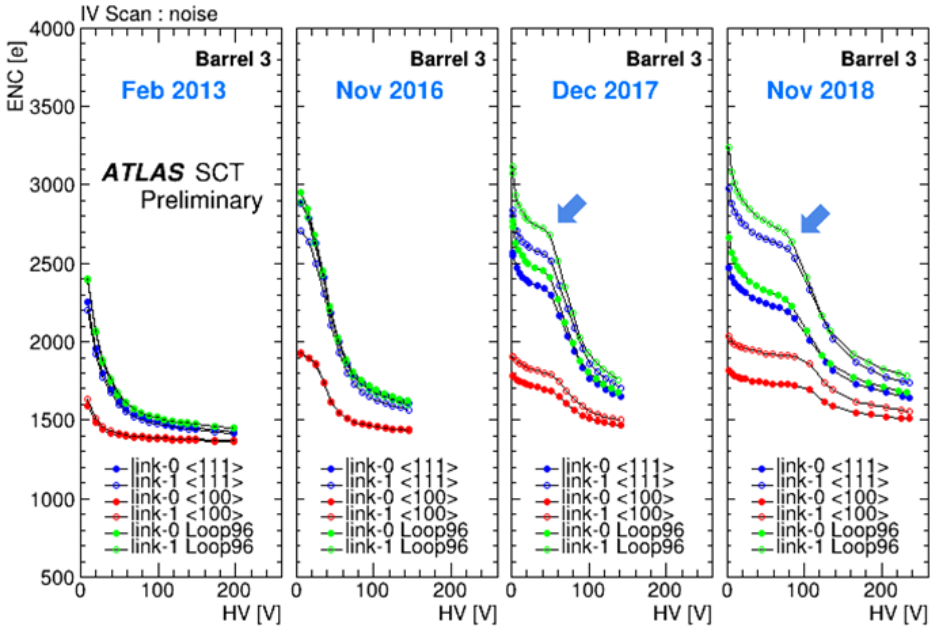
Depletion voltage (SCT)

- The shift of hit efficiency as a function of HV indicates higher depletion voltage due to radiation damage on the sensor.
- ENC (Equivalent Noise Charge) is used to identify depletion voltage of the sensor in SCT.
  - Knee position shows depletion voltage of the sensor.

Hit efficiency v.s. HV @SCT

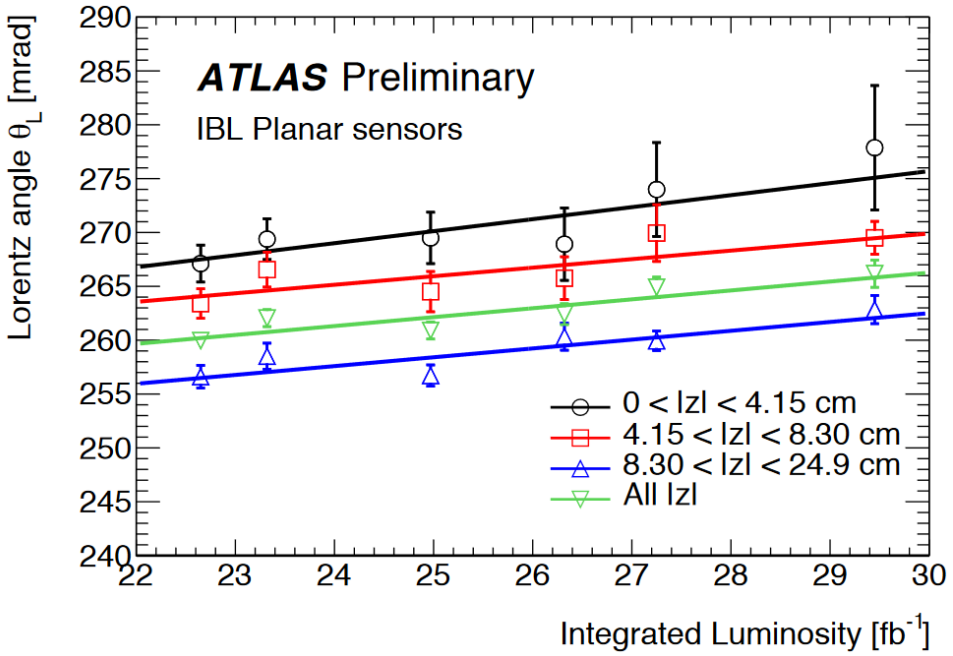


ENC v.s. HV @SCT

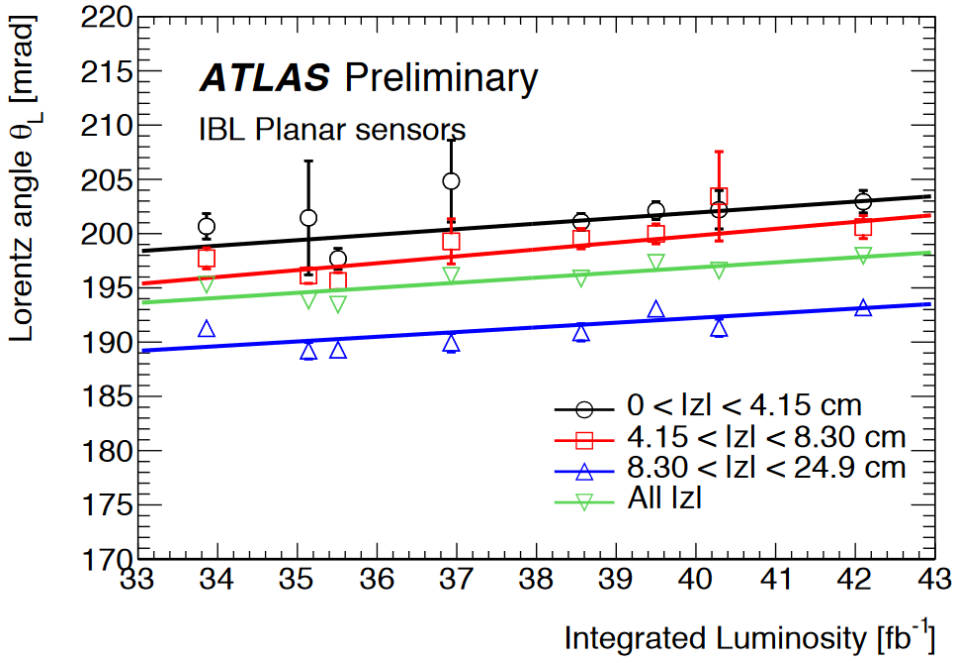


Lorenz angle in 2016 (IBL)

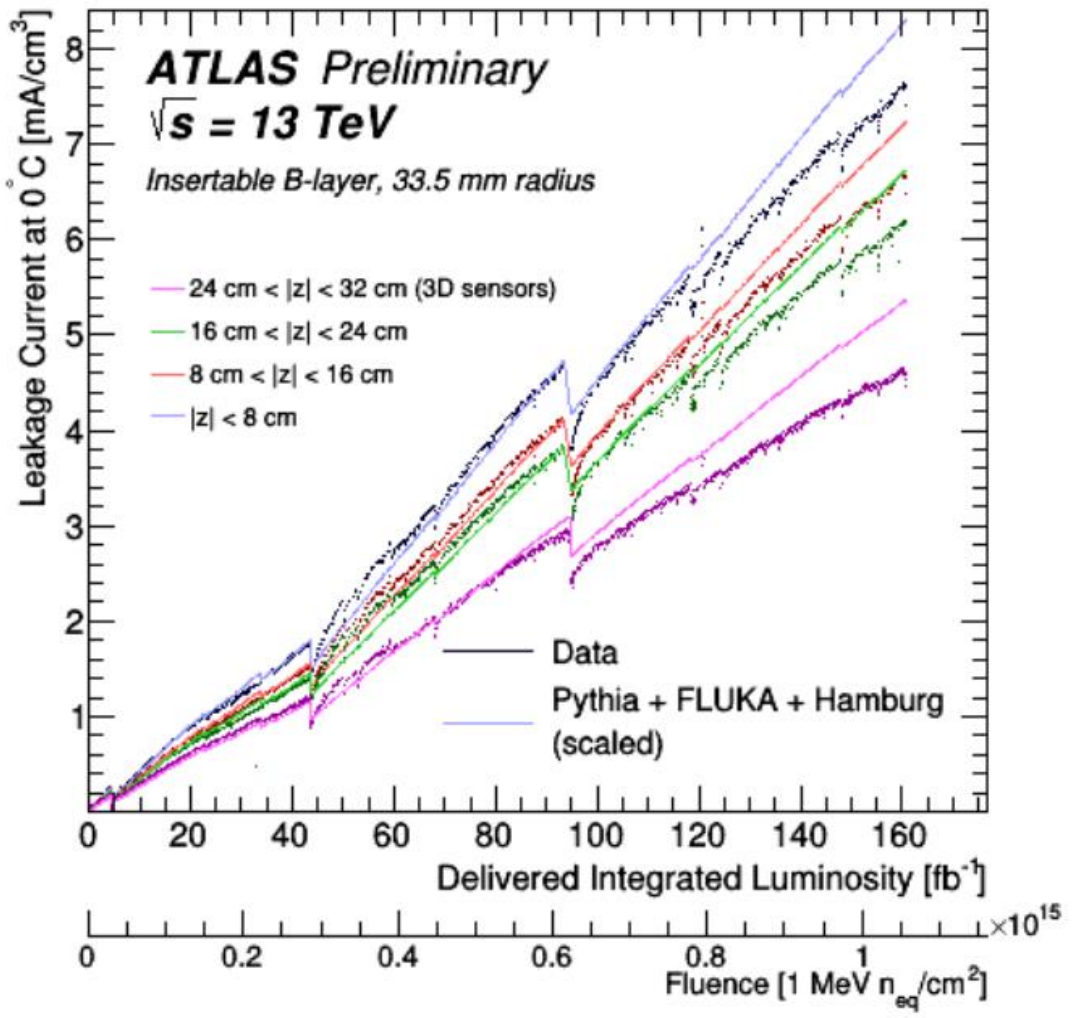
5 deg, -80V



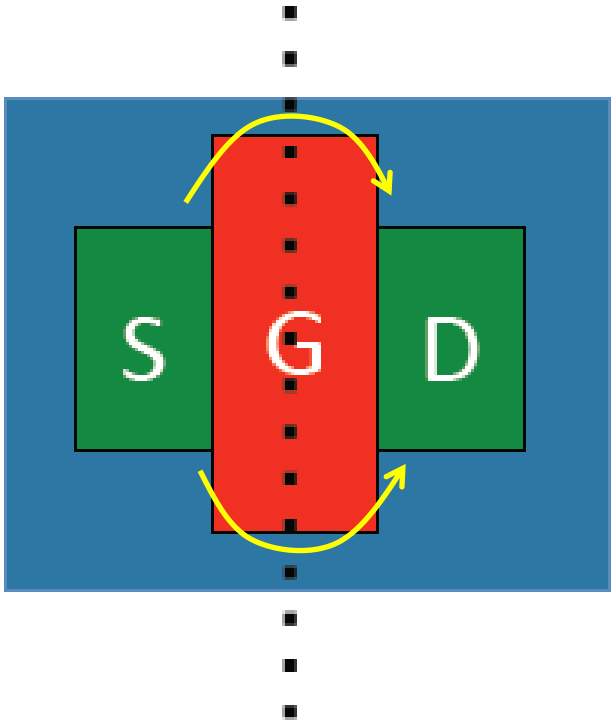
5 deg, -150V

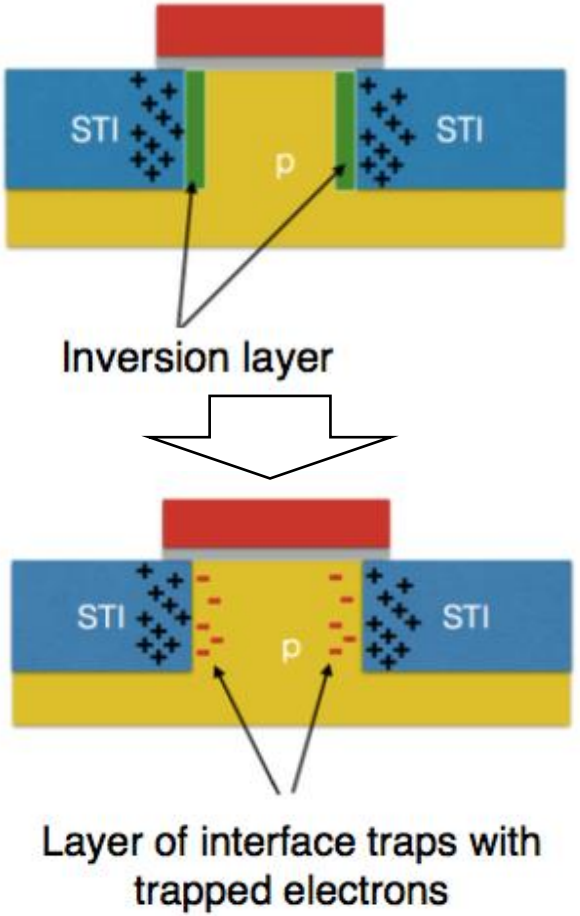


Leakage current in z-position (IBL)



Mechanism of total ionization dose

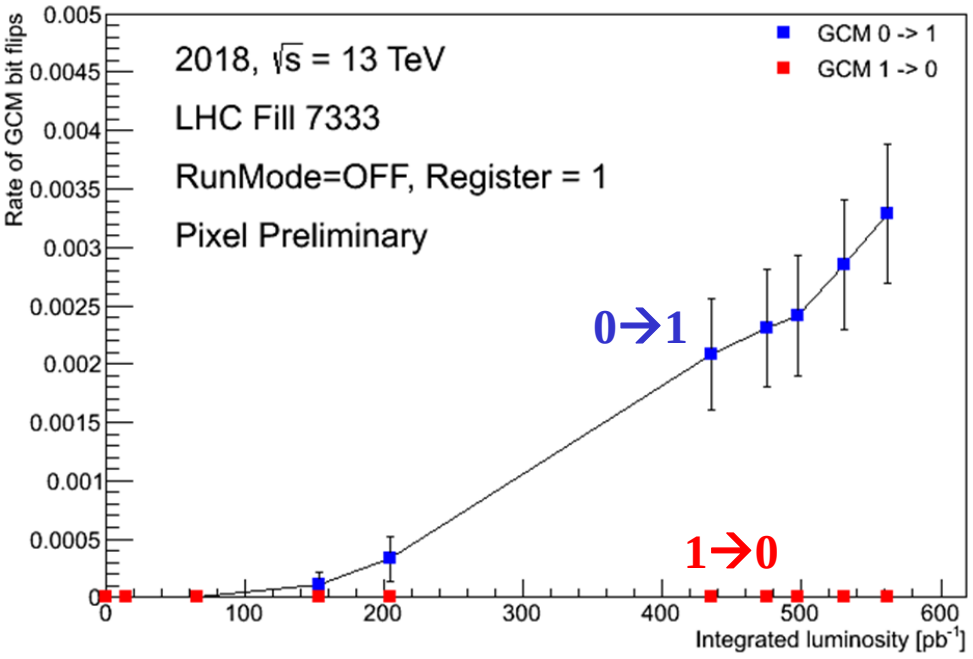


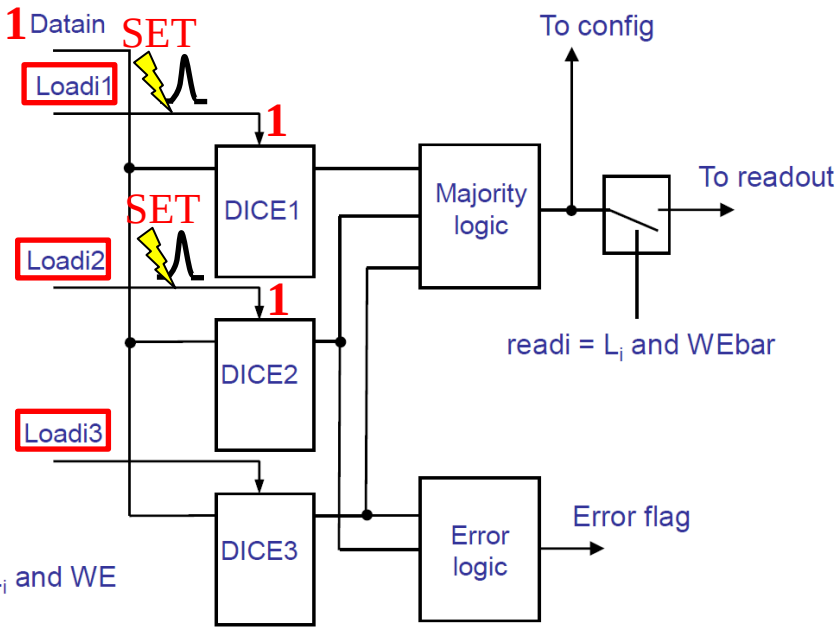


SEU/SET rate in Global memory

- The cumulative rate of bit flips in Global memory was investigated to see effect of SEU/SET.
- High rate of 0→1 flips indicate SET (glitches) on the LOAD line with Data-In = "1".
- No 1→0 transitions are observed due to the triple redundant logic.

Bit flip rate in Global memory (Data-In = 1)



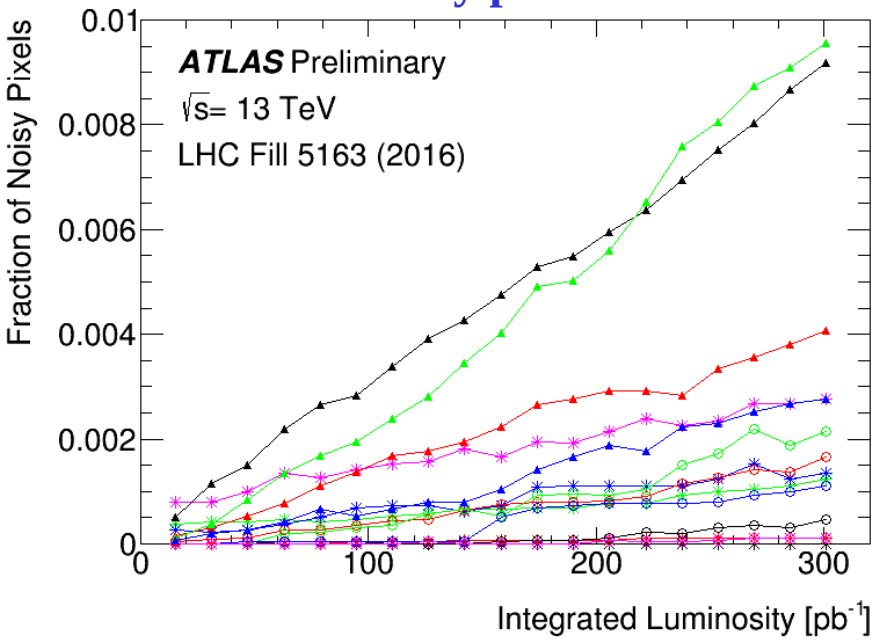


SEU/SET in Pixel memory (threshold)

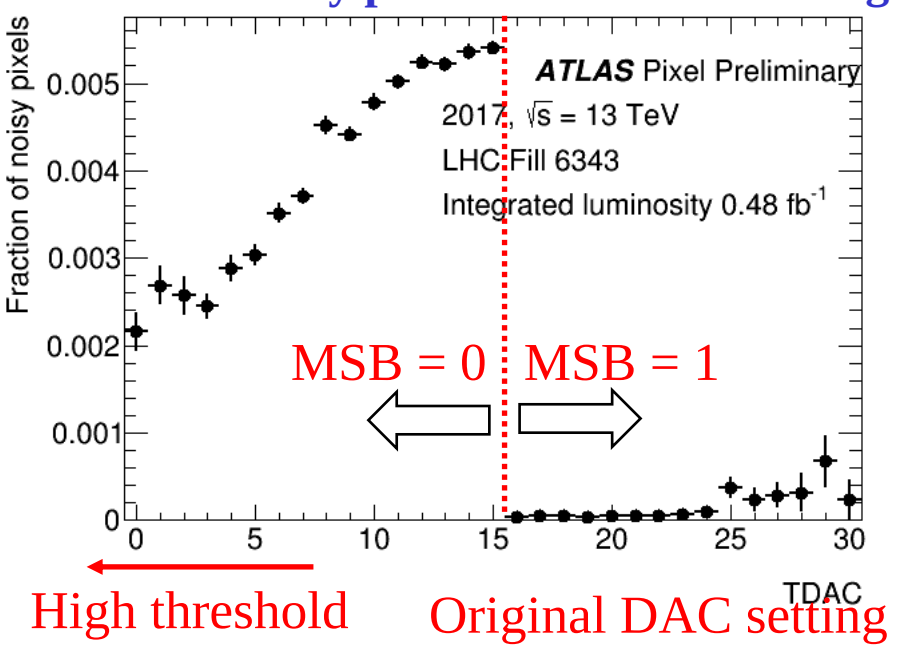
- Even with SEU tolerant logic, Pixel memory is affected by SEU/SET.
- The number of noisy pixels increases during a run.
- The noisy pixels concentrate in high original threshold setting.

→ The biggest effect comes from bit flip of MSB (Most Significant Bit) in threshold DAC (TDAC).

Fraction of noisy pixel v.s. Int. lumi.



Fraction of noisy pixel v.s Thr. DAC setting

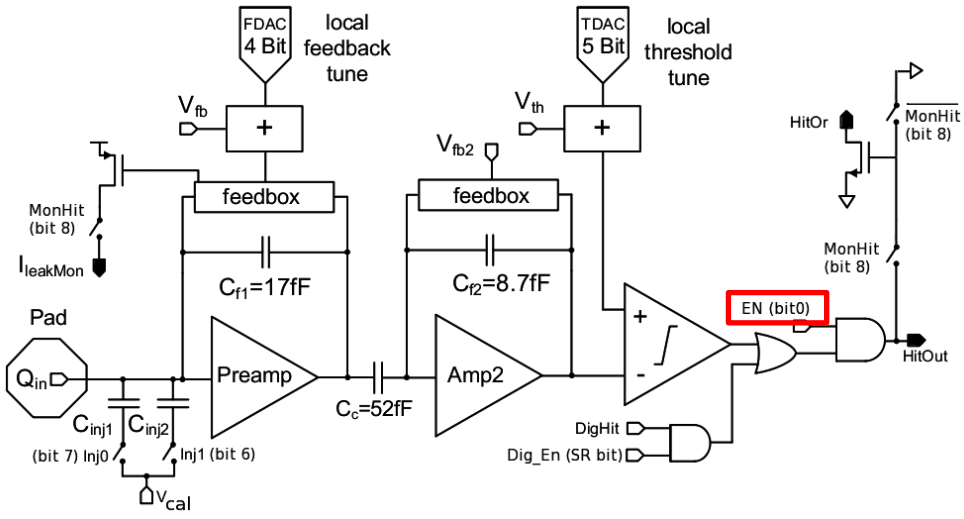


High threshold

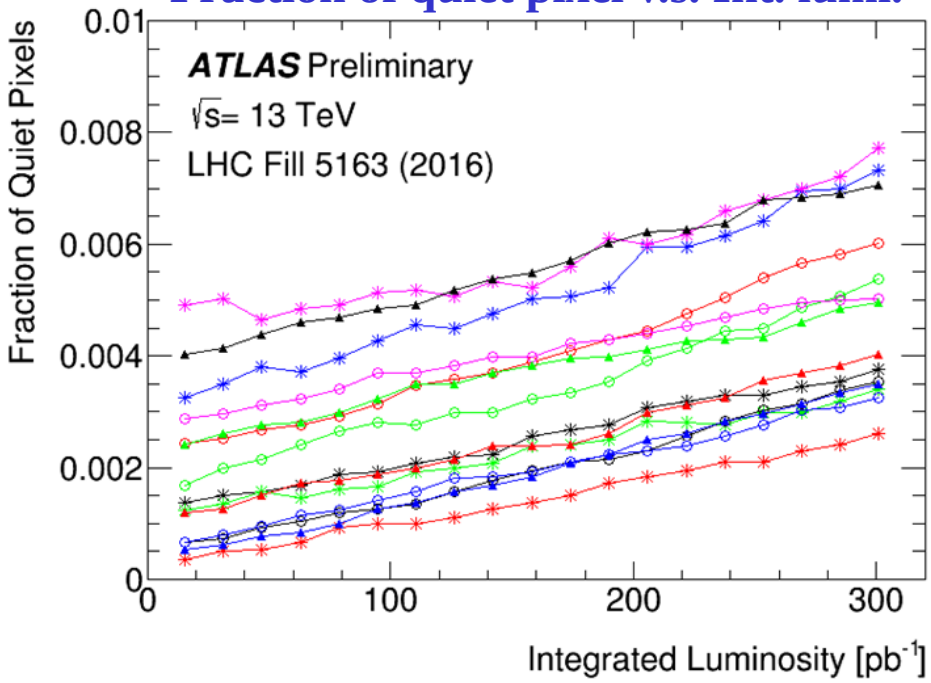
Original DAC setting

SEU/SET in Pixel memory (Enable bit)

- The number of quiet pixels also increases during a run.
- The enable bit in Pixel memory would be disabled by SEU/SET.
- Offset is from disabled pixels.

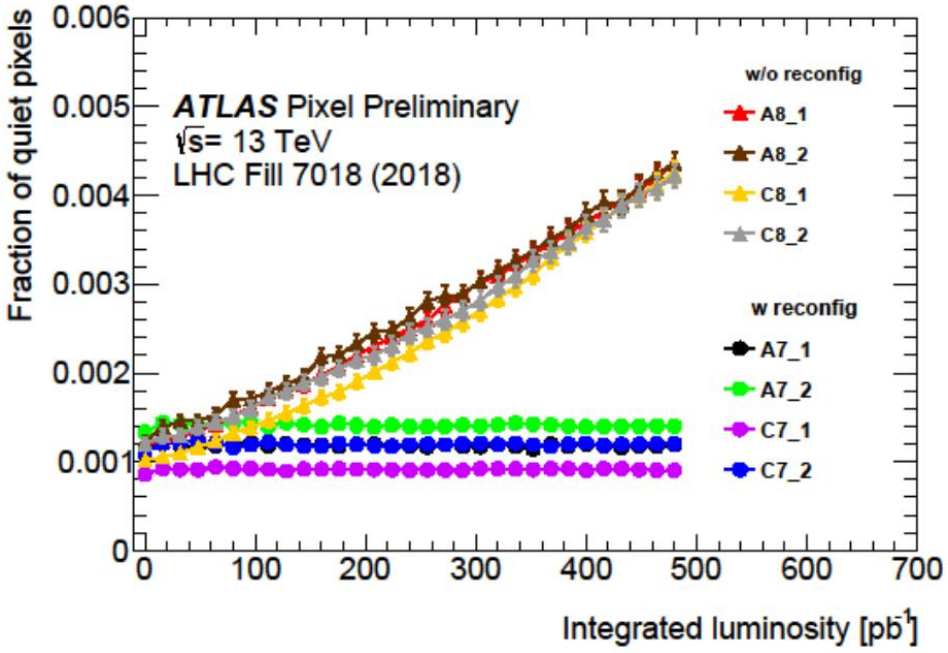


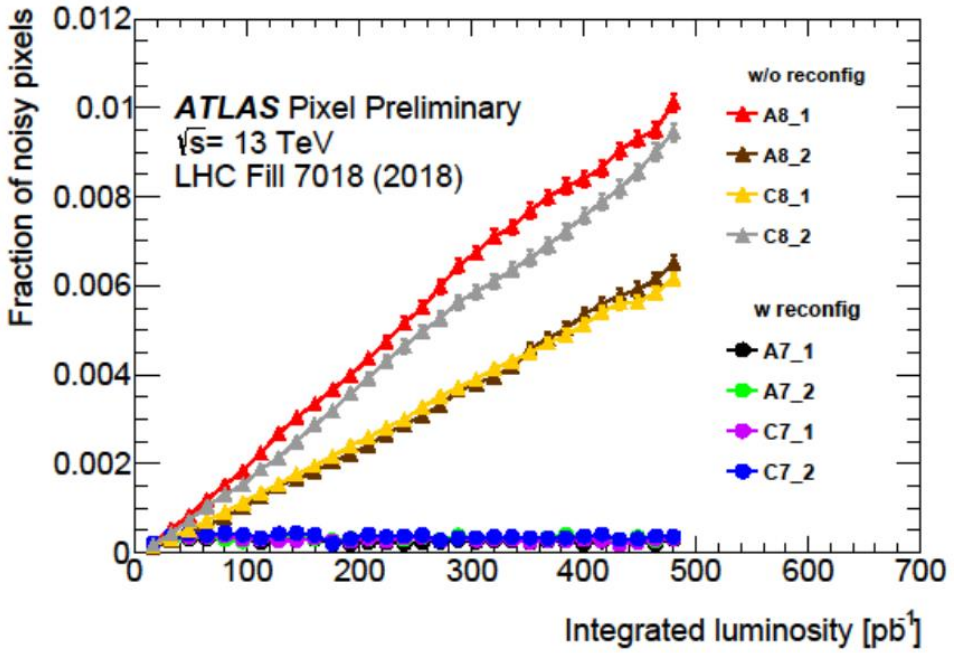
Fraction of quiet pixel v.s. Int. lumi.



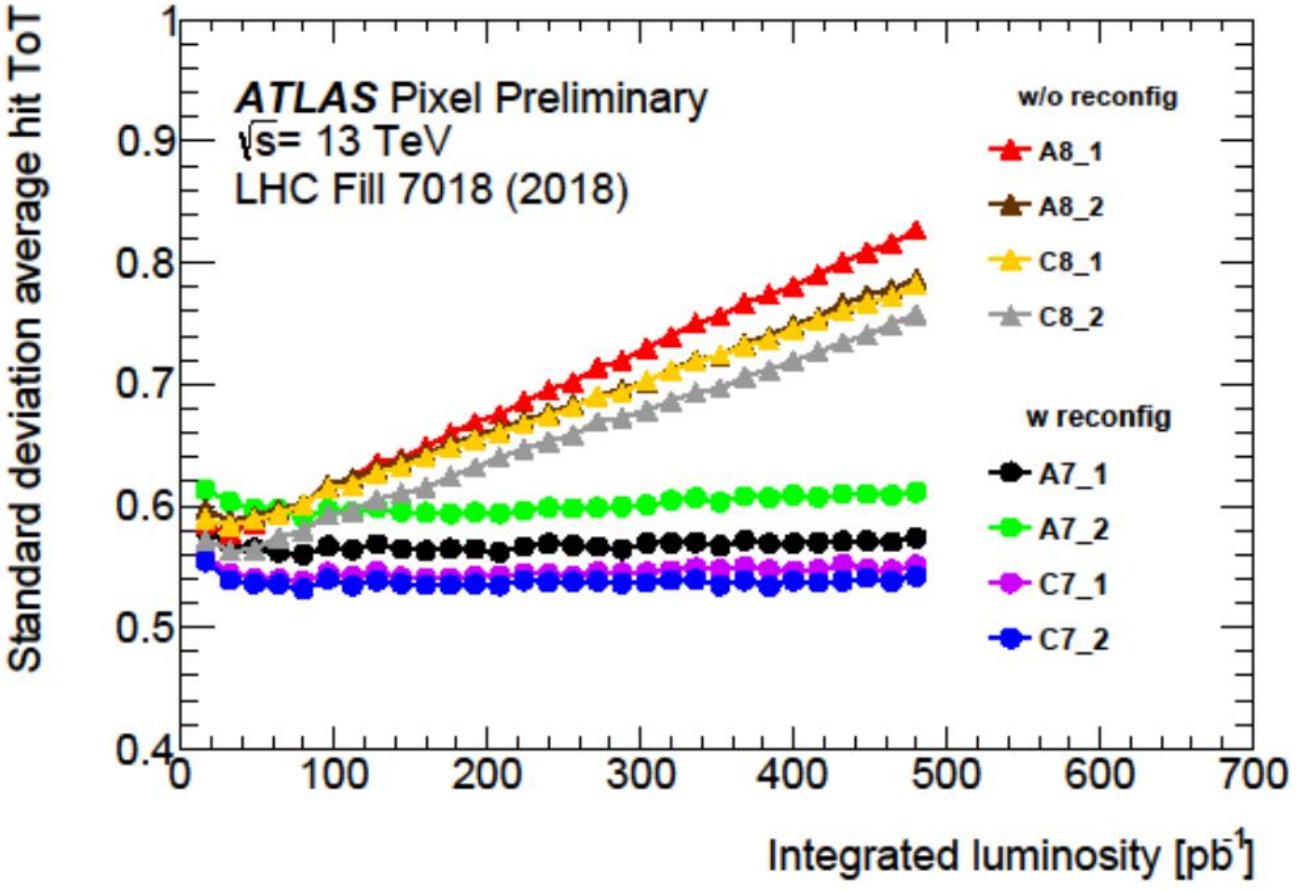
Quiet/Noisy pixels by SEE (IBL)

- The number of quiet pixels also increases during a run.
- The enable bit in Pixel memory would be disabled by SEU/SET.
- Offset is from disabled pixels.
- The noisy and quiet pixels are decreased by reconfiguration action of Pixel memory during a run.





ToT drift by SEE (IBL)



Configuration recovery (IBL/Pixel)

- ECR (Event Counter Reset) timing is used for reconfiguration of Global/pixel memory.
- There is 1 ms dead time before/after ECR.
- Reconfiguration mechanism utilize 1 ms dead time after ECR not to introduce extra dead time.