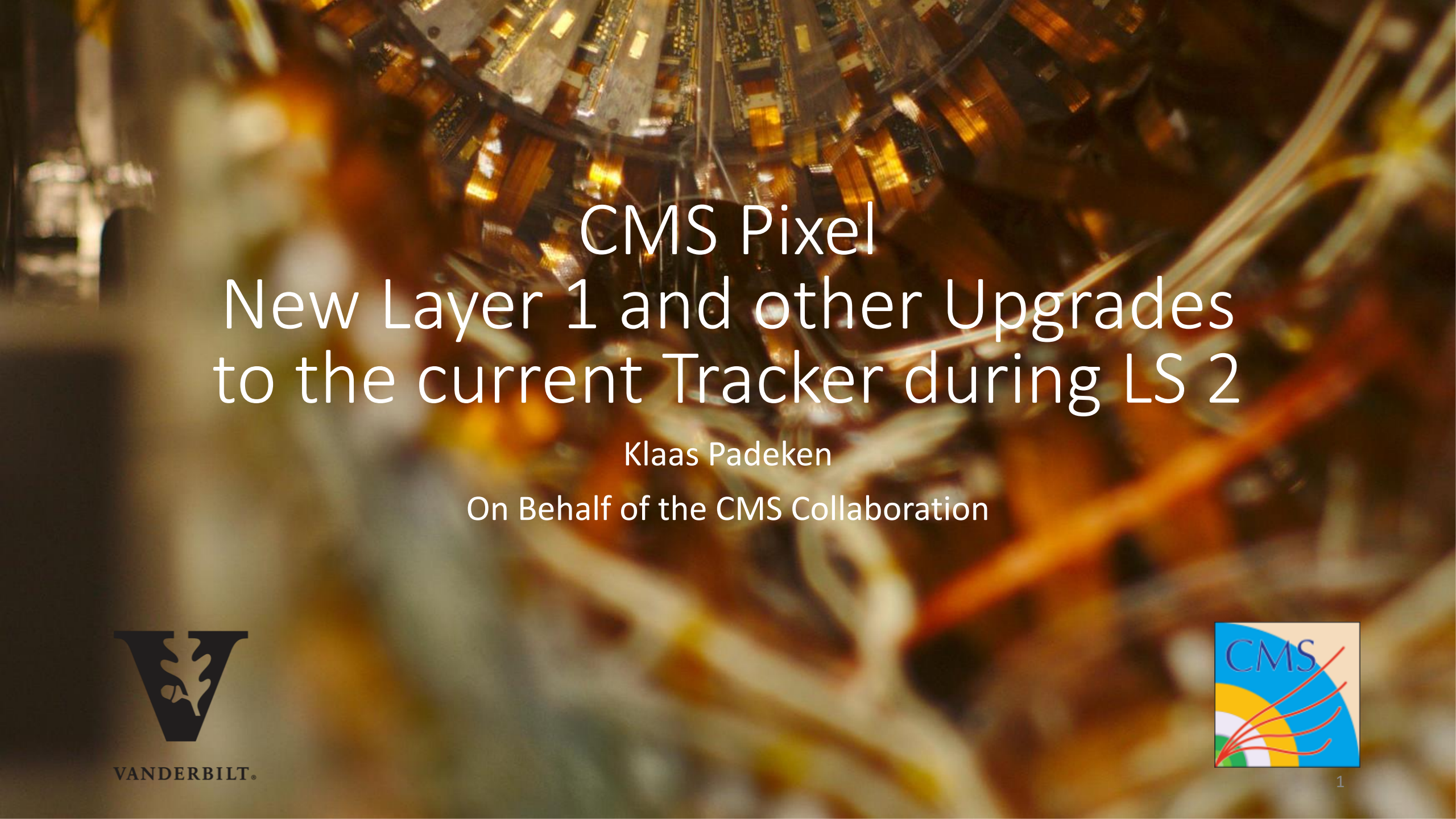


CMS Pixel
New Layer 1 and other Upgrades to the current Tracker during LS 2

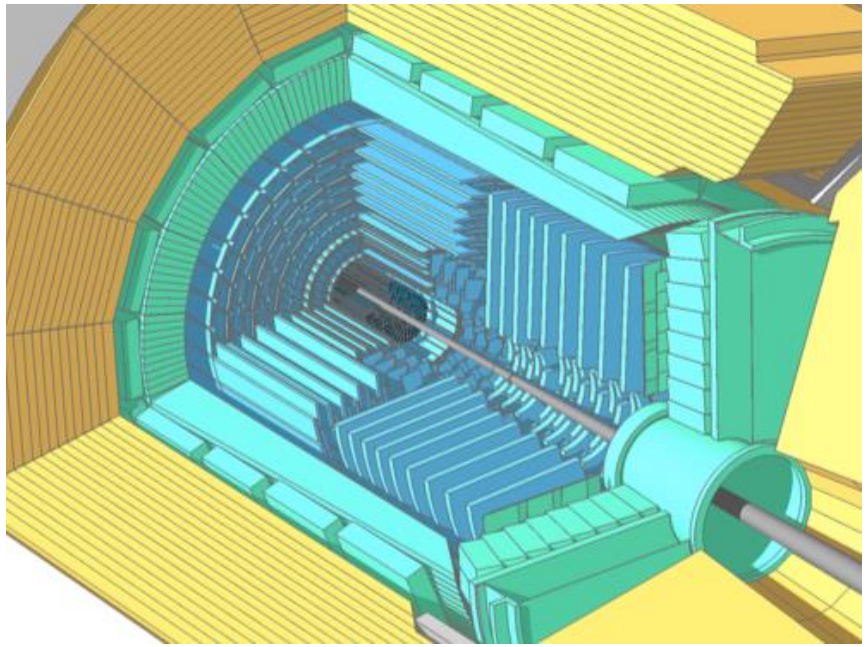
Klaas Padeken

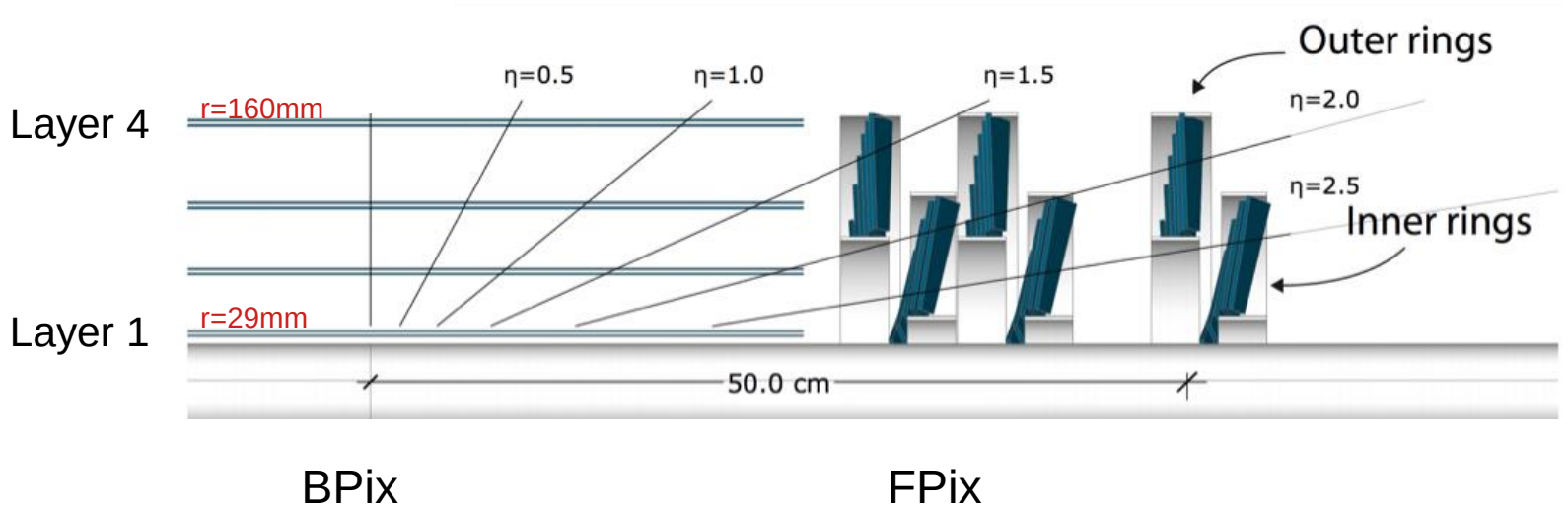
On Behalf of the CMS Collaboration

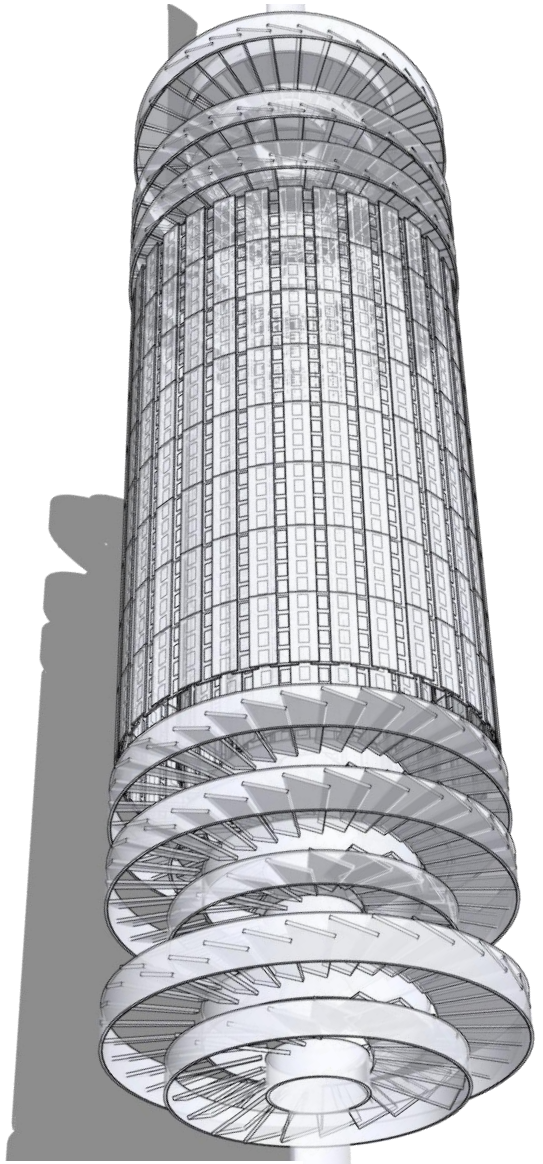
VANDERBILT.

CMS Phase 1 Pixel

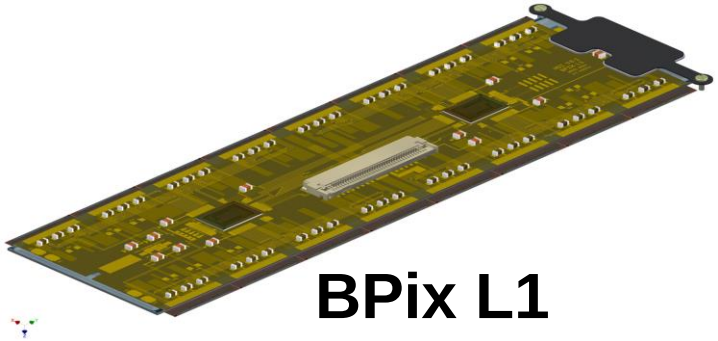
- Installed in EYETS 16/17
- Newest active Subdetector of CMS
- ~1.9 m^2 pixel area ~124 M channels
- 4 hit coverage up to η=3



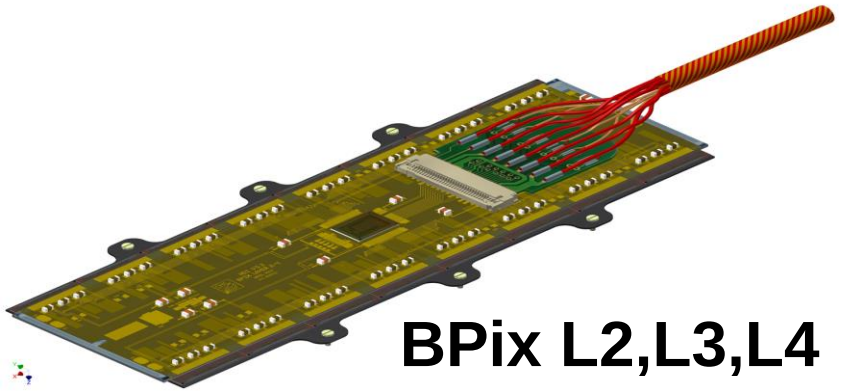




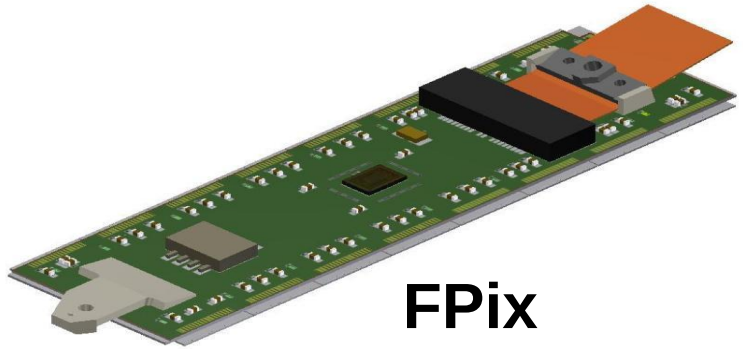
Module Concept



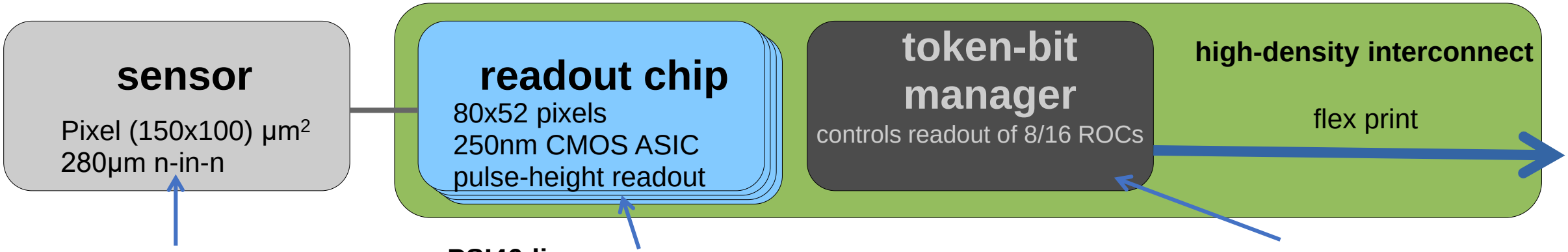
BPix L1



BPix L2,L3,L4



FPix



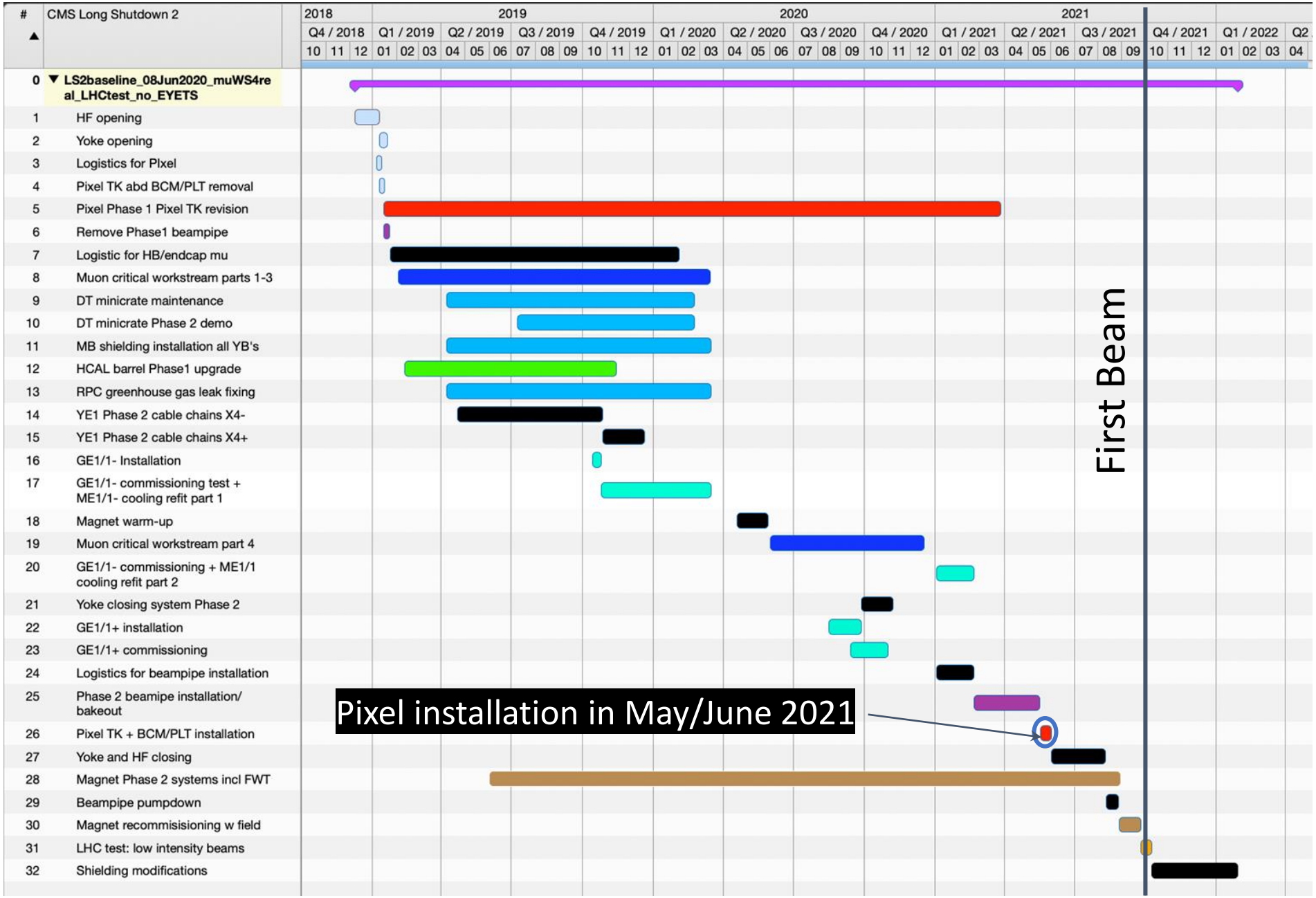
unchanged compared to Phase-0

- **PSI46dig**
  - same architecture as Phase 0
  - Digital readout with double column draining
  - >90% efficient up to 400MHz hit rate
- **PROC600**
  - Dedicated for Layer 1
  - Dynamic cluster drain
  - >90% efficient up to 600MHz hit rate

- **new digital TBM**
- old: 40MHz analog coding
  new: 160Mbit/s digital
- module out-bound data stream: 400Mbit/s

all components suited for high integrated & instantaneous luminosities

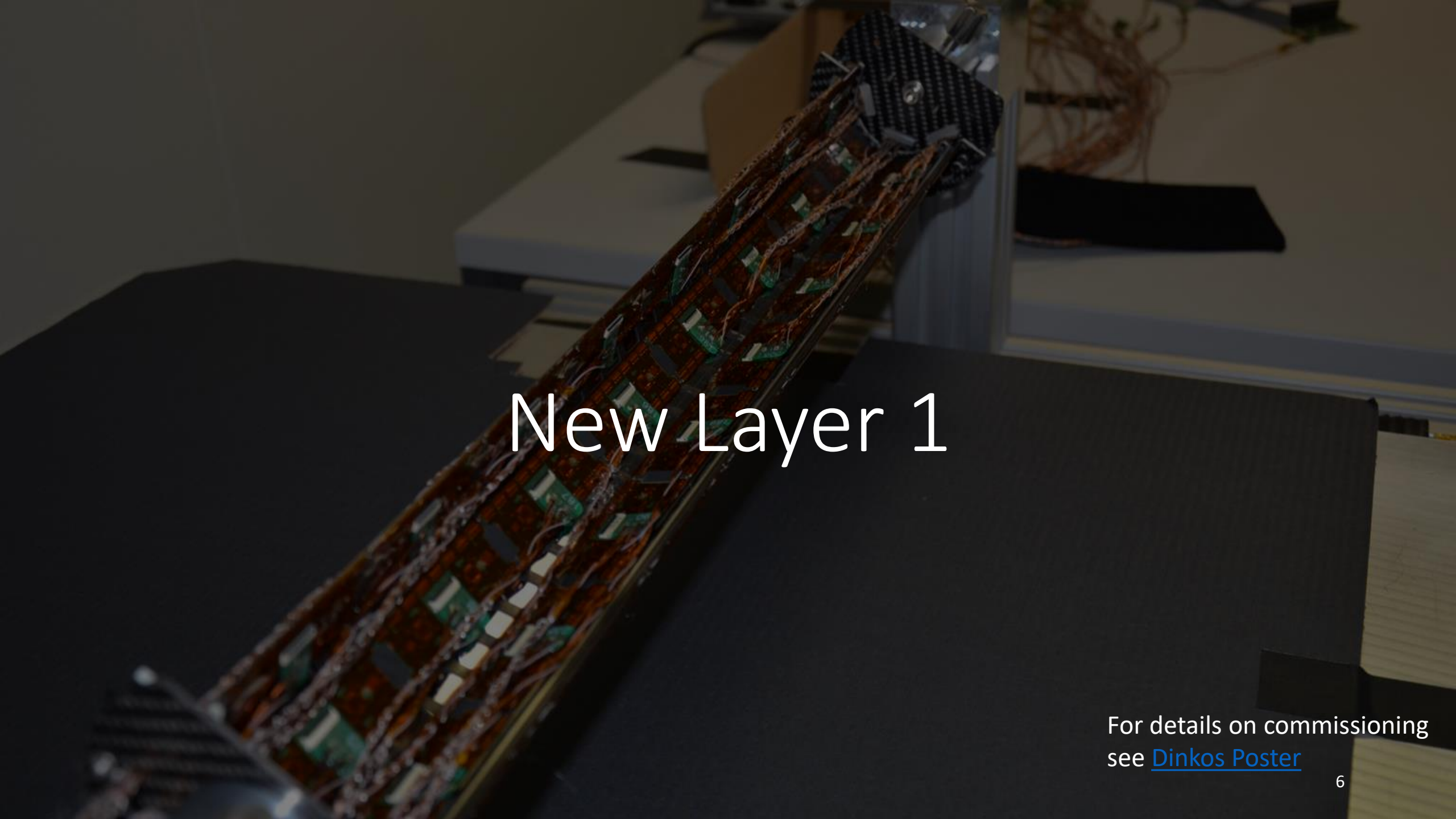
CMS Schedule



Pixel Timeline

Main Objective for LS2:

- New Layer 1
- New DCDC Converter
- Consolidate FPix CO_2 cooling connection
- HV Powersupply Upgrade to 800V



New Layer 1

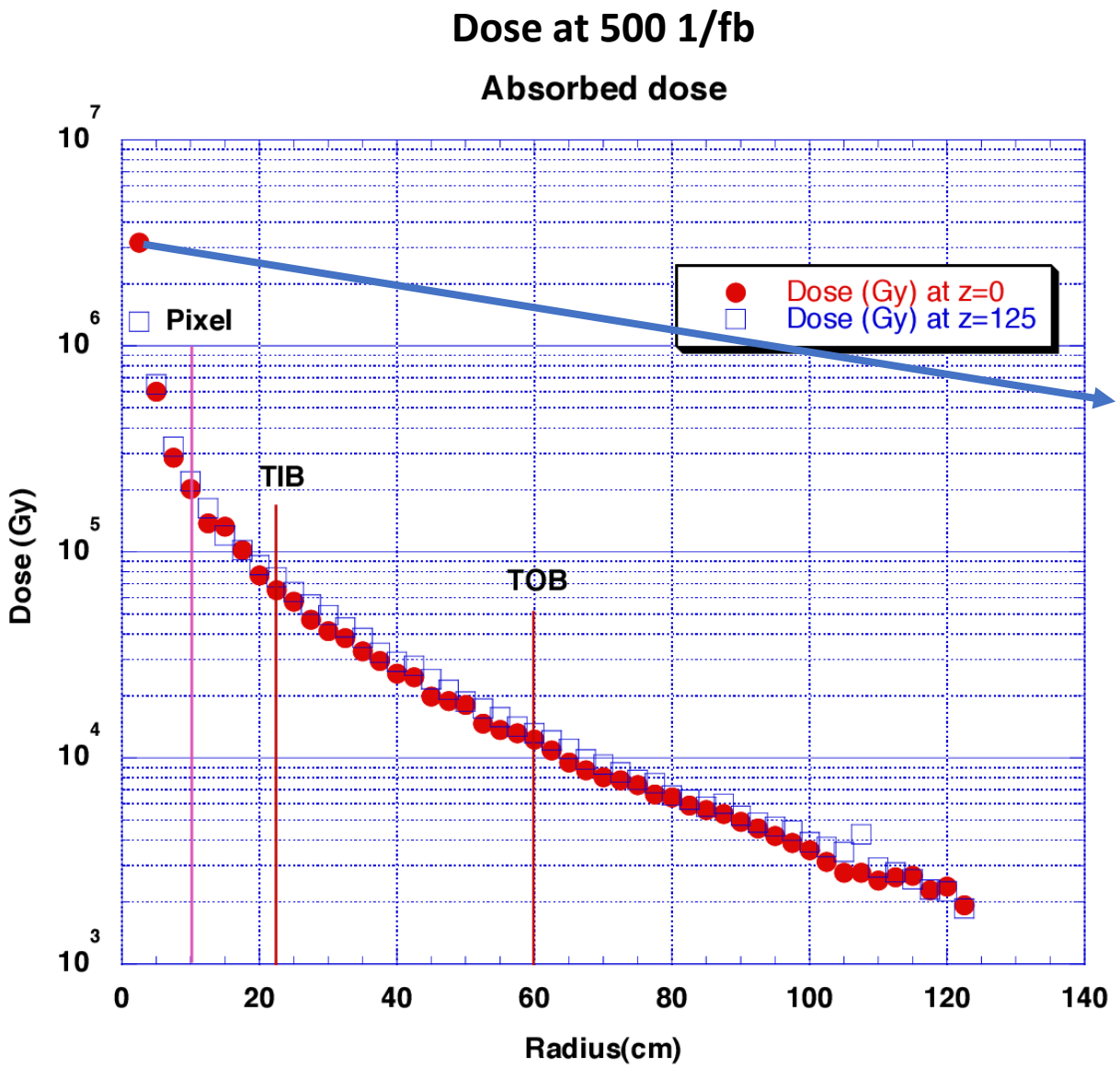
For details on commissioning see Dinkos Poster

Radiation

For Layer 1
Per fb $^{-1}$ 0.34 Mrad/3.4 kGray
$7 \cdot 10^{12}$ particles/cm^2 (*)

End of 2018
41 Mrad/410 kGray
$0.83 \cdot 10^{15}$ particles/cm^2

→ Pixel Layer 1 was needed for CMS Run 3



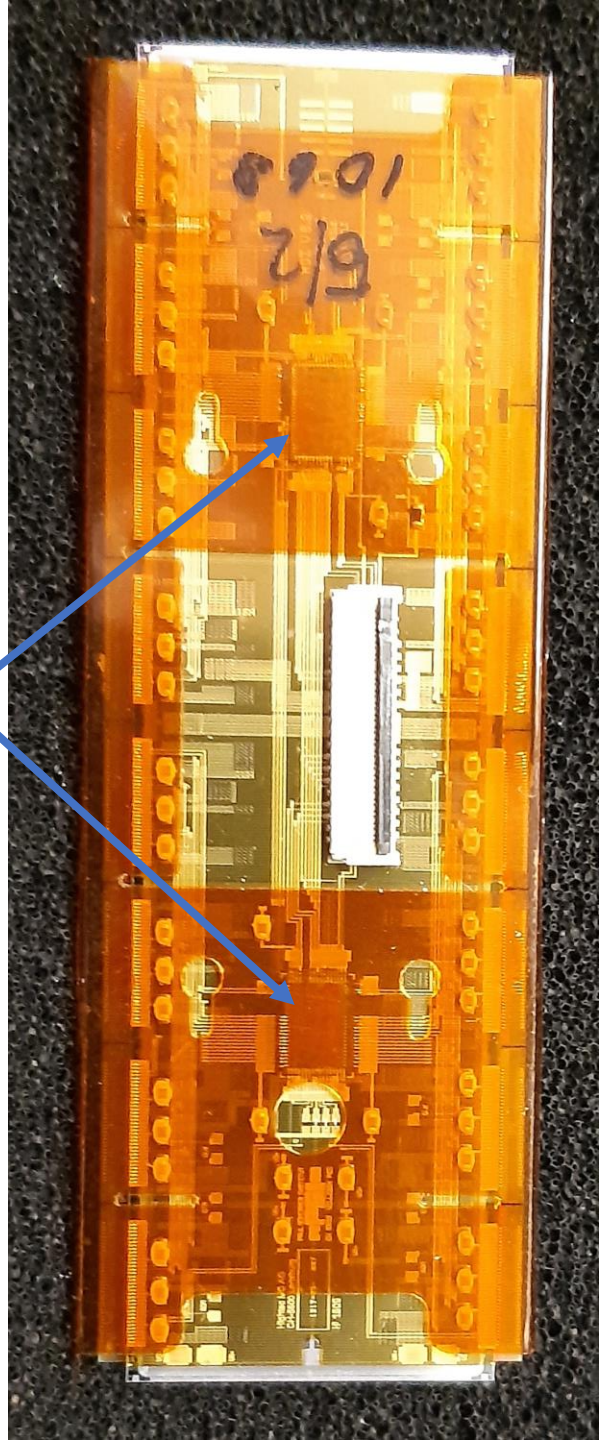
→Layer 1 new Readout chip PROC600

→Layer 2-4 +Disks digital version of the PSI46(dig)

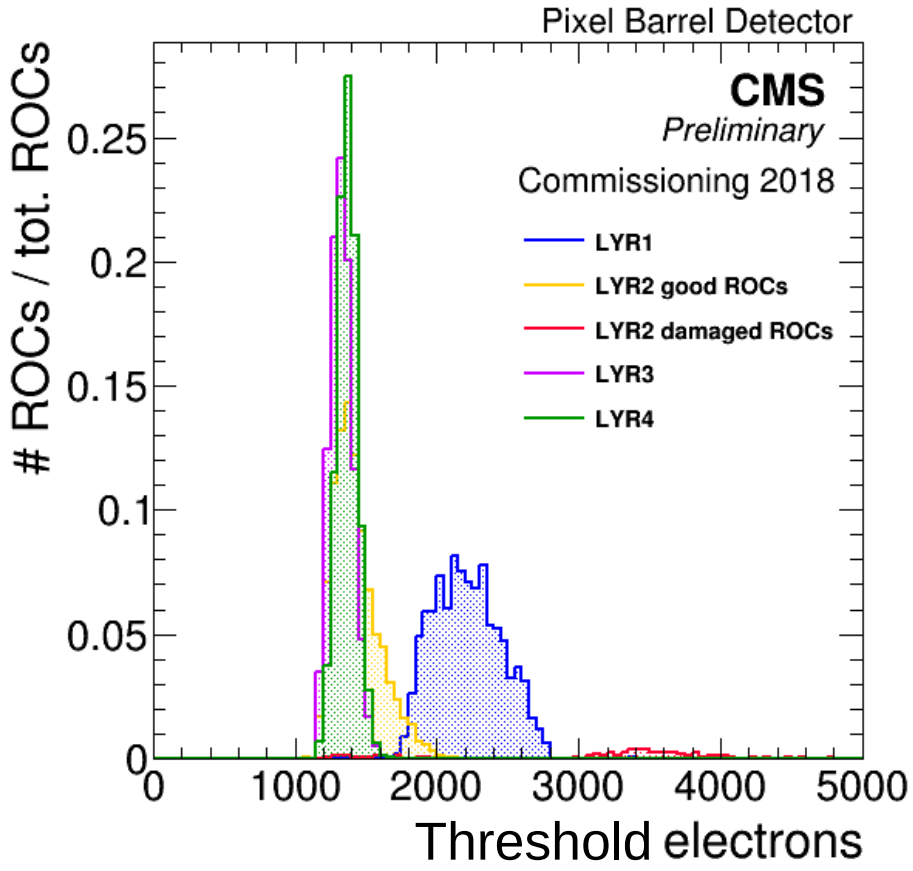
(*) Particles/cm^2 are usually represented by something called "1MeV neutron equivalent", requires scaling!

If you build a new one anyway…

- Improve with new version for PROC 600
- Improve with new version for TBM (Token Bit Manager)
- Decorrelate Layer 1 and 2 timing
- Make sure 800V bias voltage is ok



Crosstalk

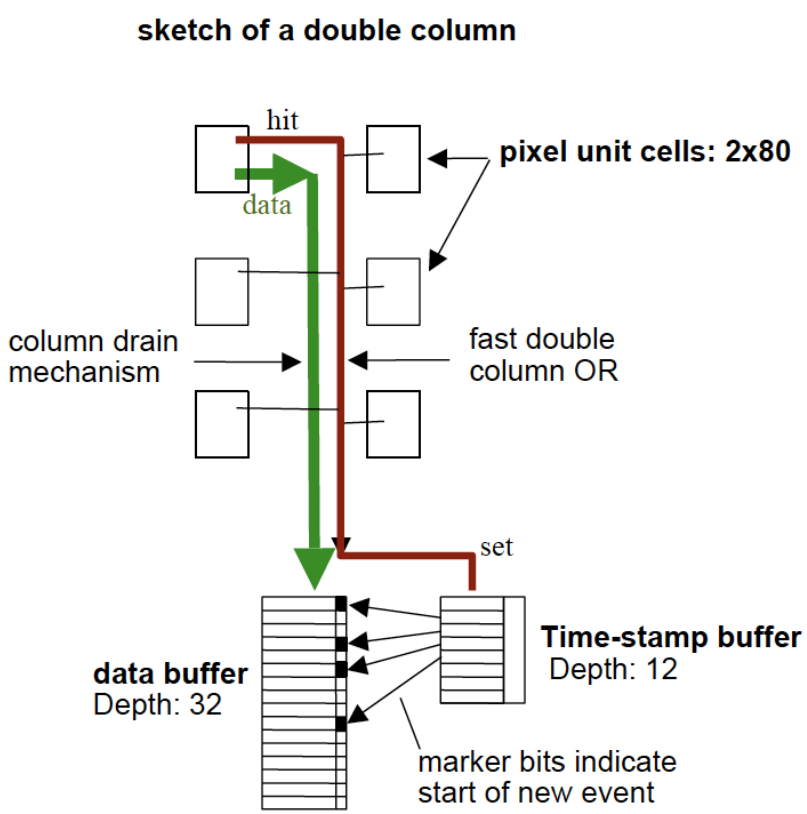


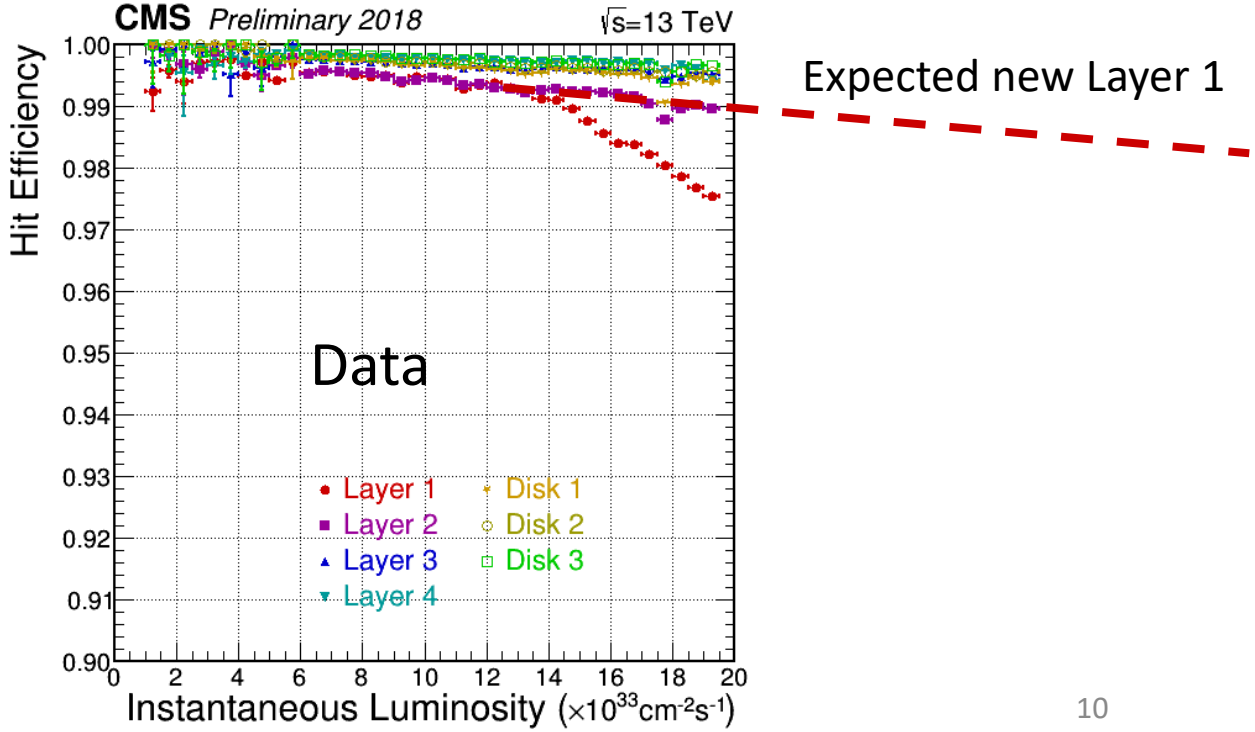
Layer 1 shows a worse crosstalk than expected, which was mainly due to electronics crosstalk.

The injection capacitor was too close to the trim lines of the pixel.
The source could be mitigated via “programming”, but a layout change solved the problem.

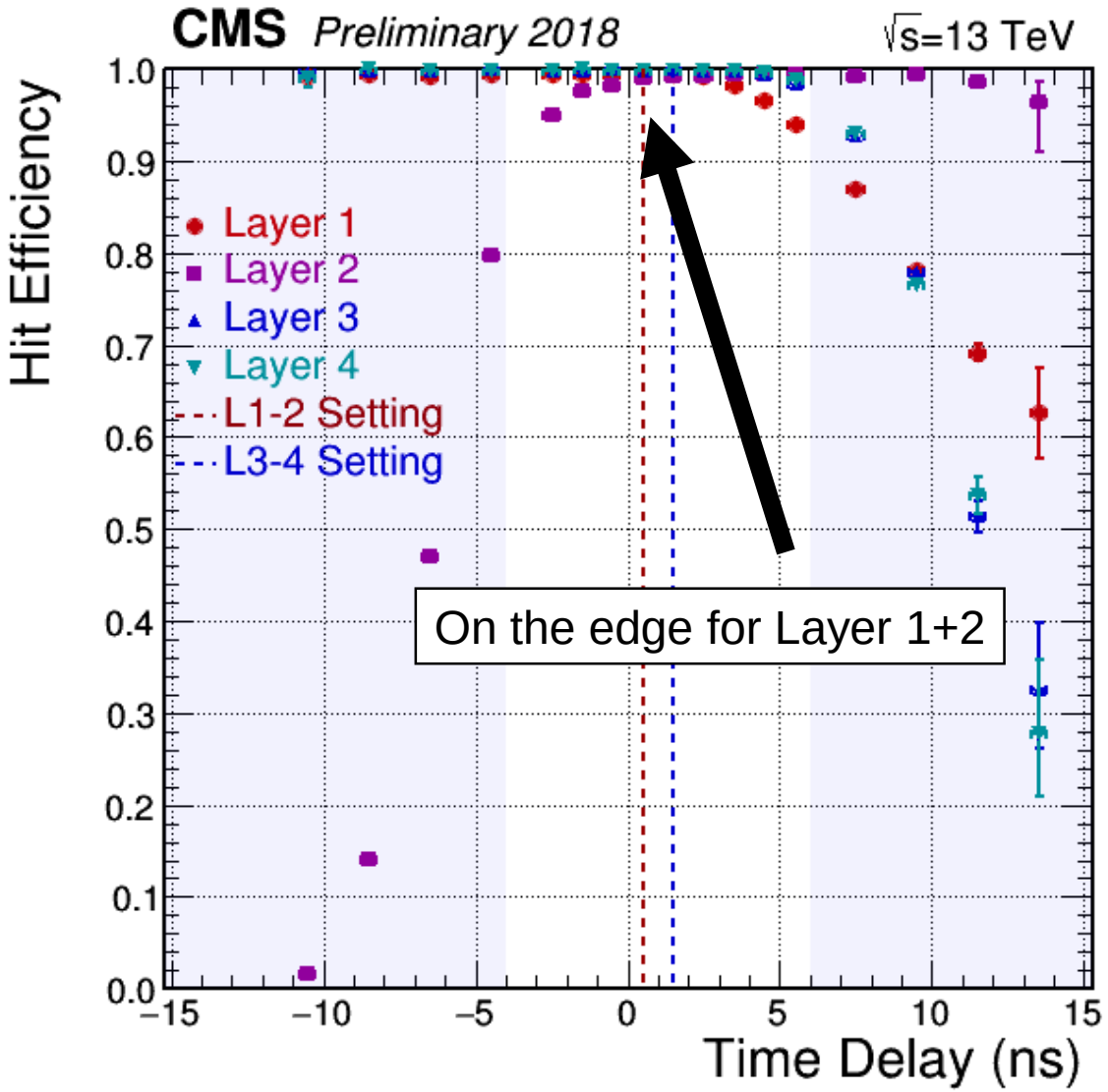
Dynamic inefficiency

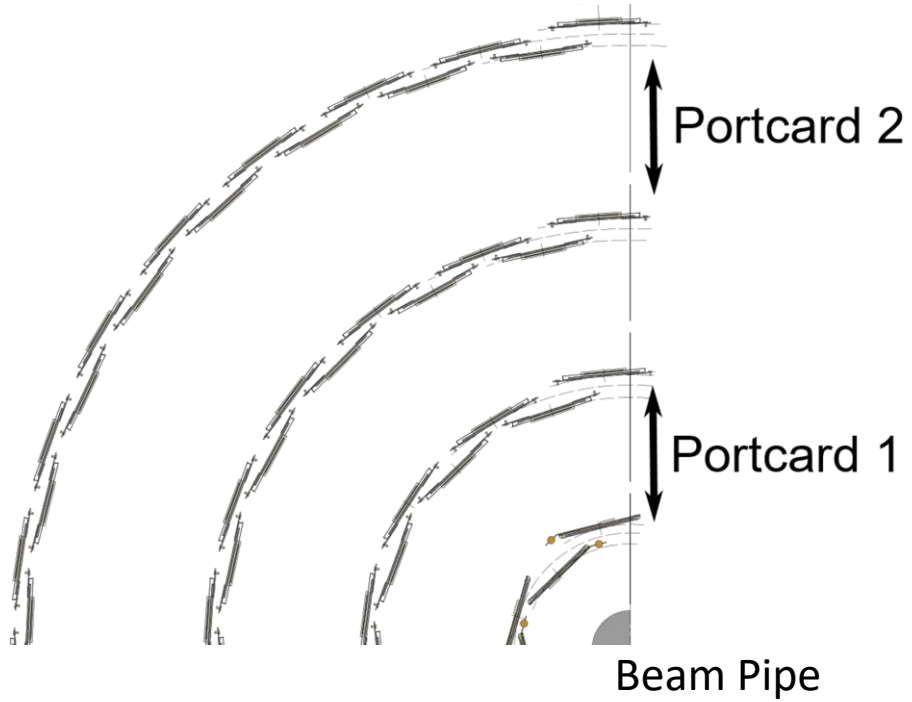
The hits are stored in the chip periphery:
timestamp – in the time-stamp buffer
data – in the data buffer.
Due to a glitch the synchronisation between time and data was lost.
This could be solved in the new PROC600.





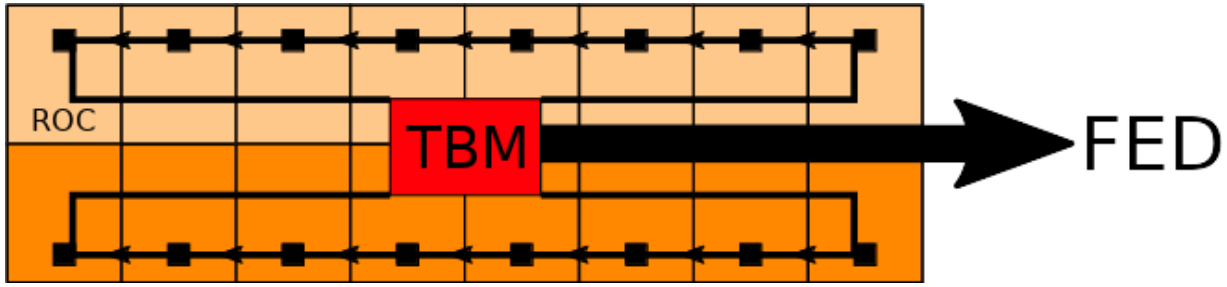
Pixel Timing





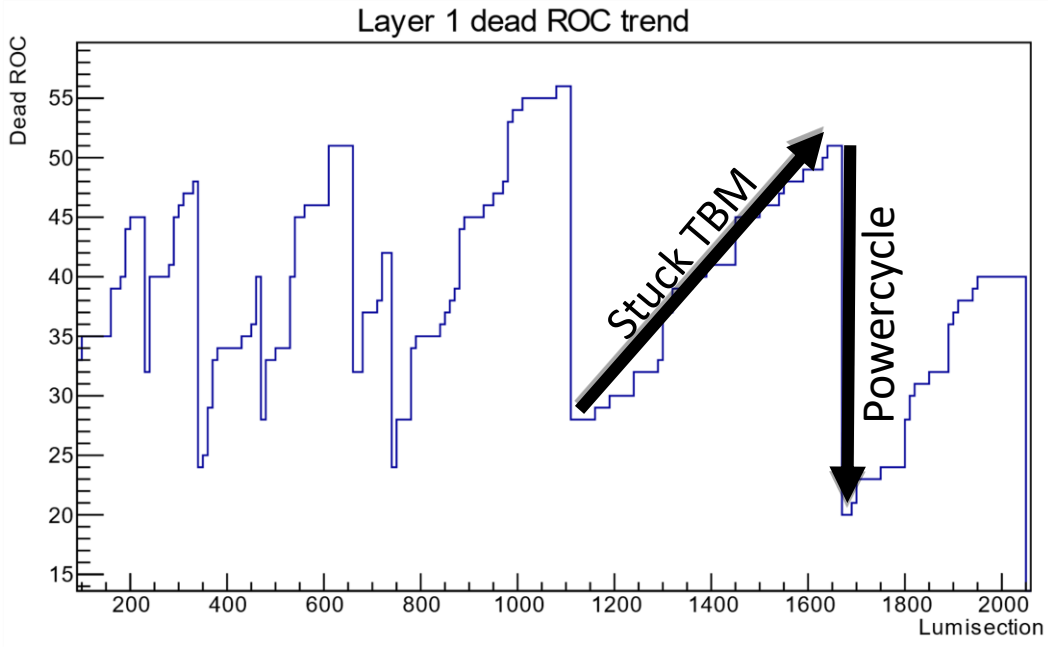
- Same portcard (delay) for Layer 1 and Layer 2 → One timing shift for both layers
- New TBM will have an **additional delay**, that will allow to shift Layer 1 vs Layer 2 (and even shift each module)

Token Bit Manager (TBM)



TBM collects data from all Readout chips if a L1 trigger is received.

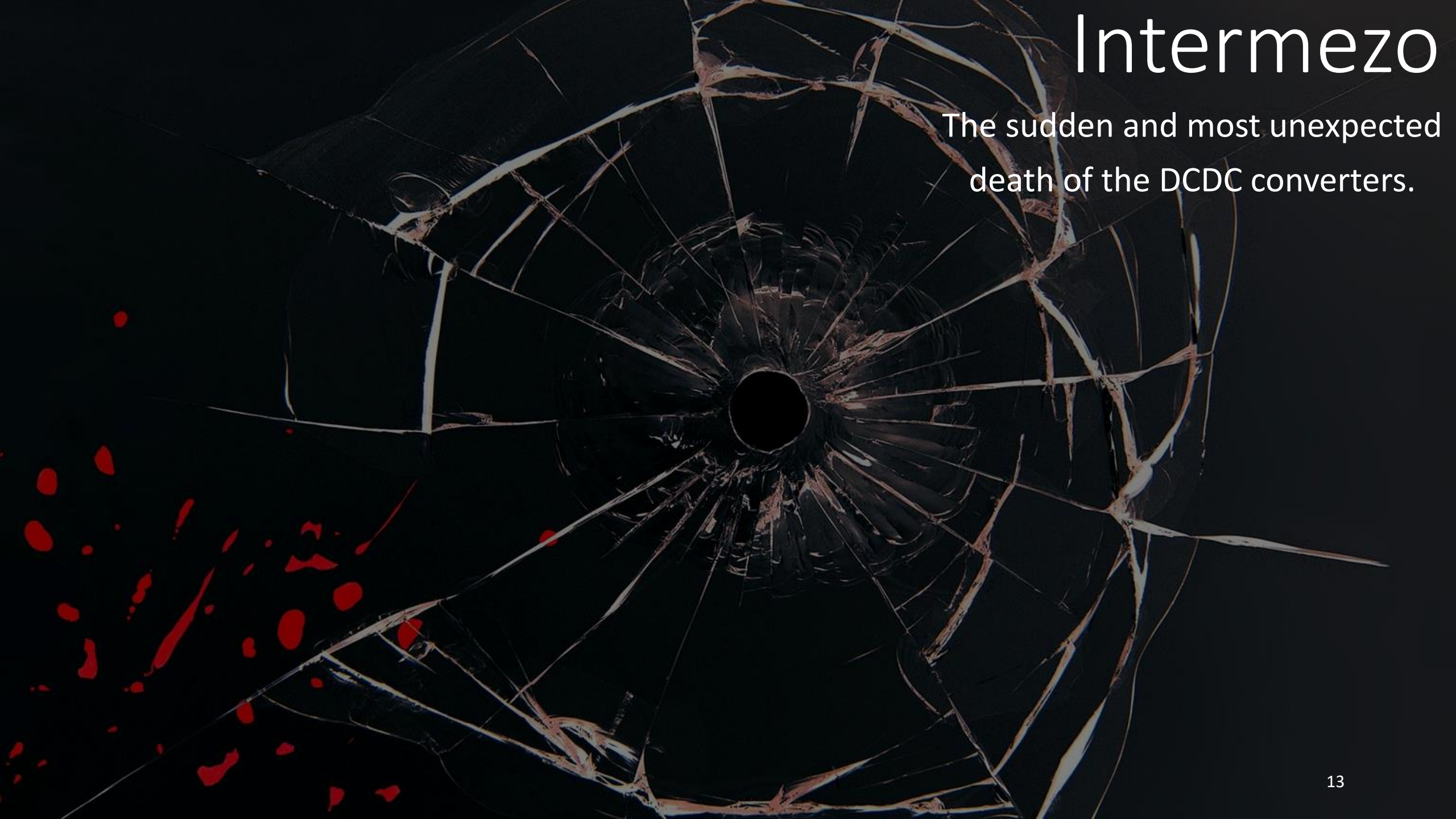
Run 303838 Sep. 2017



- The TBM can get stuck in one state
- Lose data from one core
- No way to reset except to **powercyle**

SEU rate during 2018: ~ 3/100 pb^{-1}

- **New TBM for Layer 1 fixes this issue**
- **Reset of the TBM possible in new version (for Layer 1)**

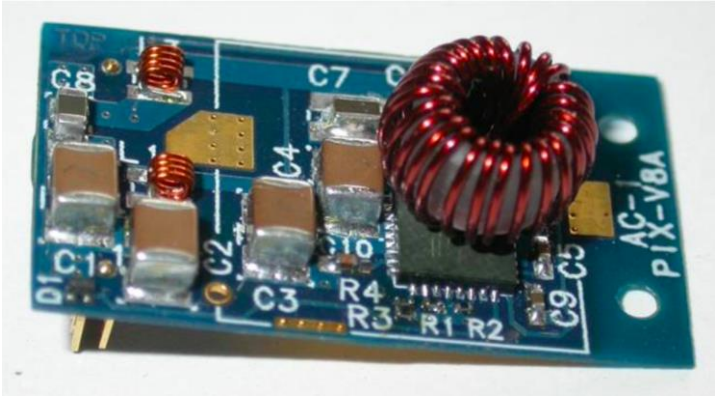


Intermezo

The sudden and most unexpected death of the DCDC converters.

DCDC

How do DCDCs break?:
If the DCDC is **irradiated** and **disabled** -> a **current** can be **amplified** and **break** the DCDC



Mar. 2017

Phase-1 upgrade done, Started data taking with 95.6% active detector

5th Oct. 2017

1st DCDC Converter Broke

Dec. 2017

5% converters not working, 11% detector not active

YETS 2017/2018

Detector Extracted, Replaced all DCDC with bigger fuse, problem not yet understood

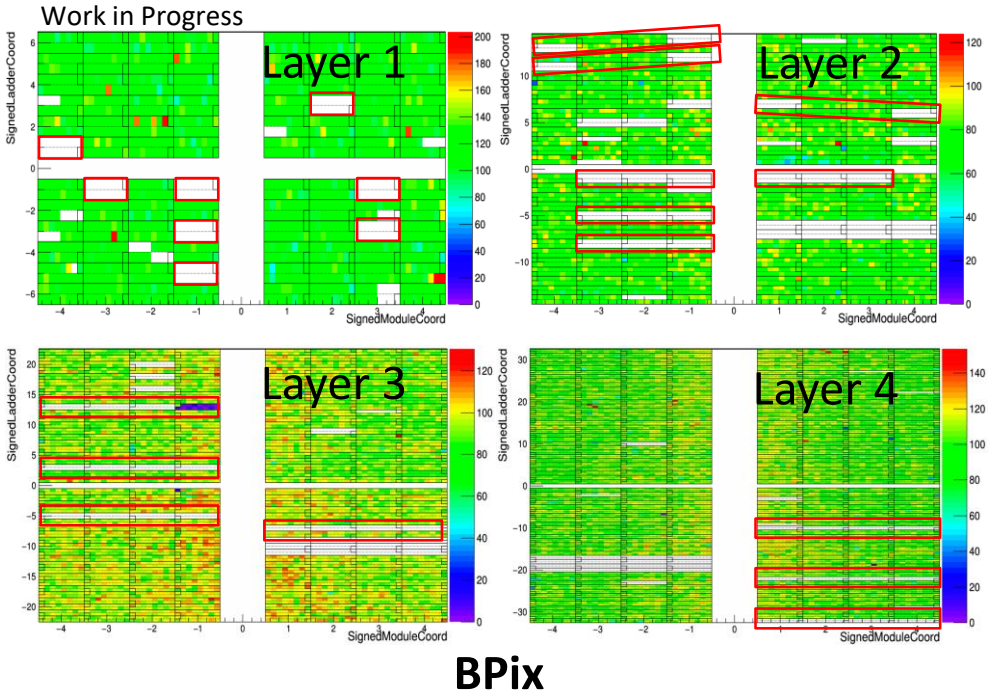
May 2018

Problem reproduced in the lab (IRAD,X-ray), reason understood

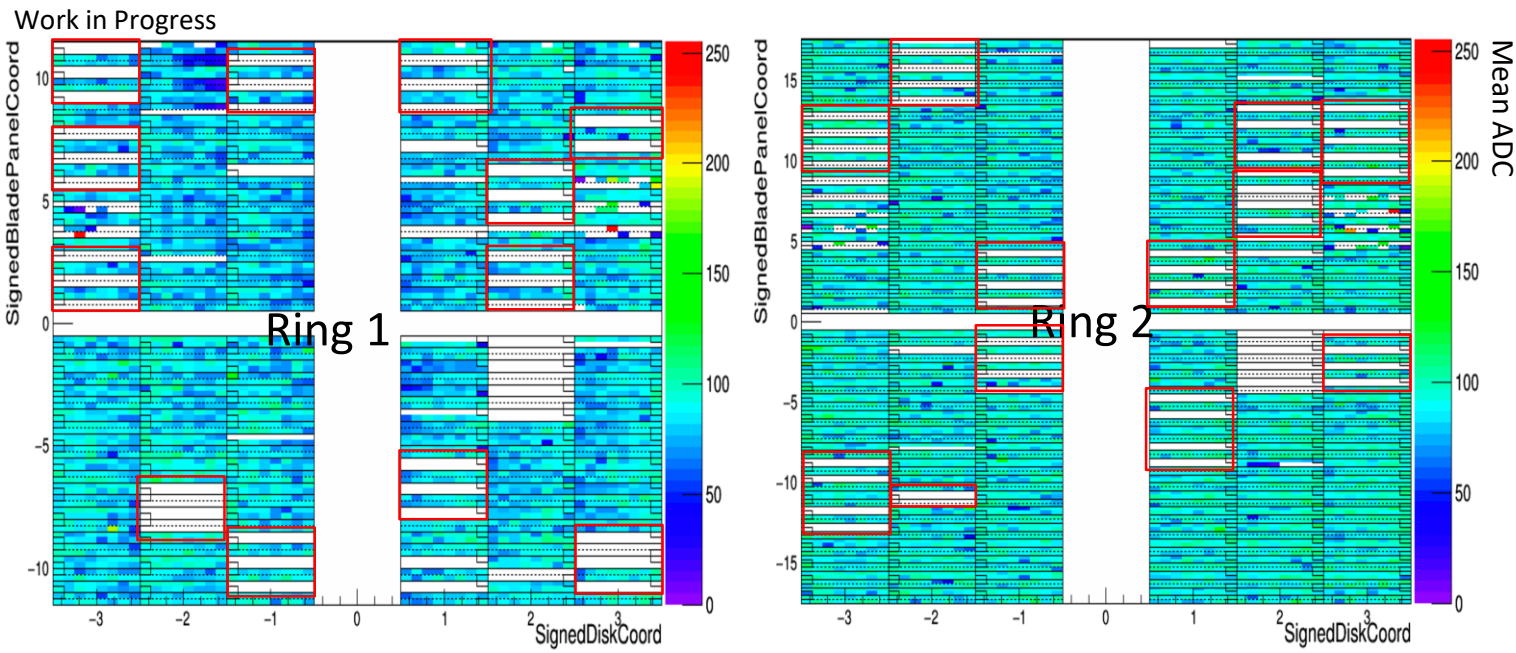
- We ran 2018 without using the DCDC converters to cut the power to the modules
- Powercycling needed for the stuck TMBs
- Reduced the supply voltage to 9V
- Use powersupplies to powercycle between beam
- The turn on current of the modules is very high
  - We did have to disable a few DCDCs in order to turn on the detector/powercycle the powersupplies --> **none broke in 2018**

	Tot. ROC	Inactive	%activate
Layer 1	1536	56	96.4
Layer 2	3584	224	93.7
Layer 3	5632	88	98.4
Layer 4	8192	48	99.4
Ring 1	4224	290	93.1
Ring 2	6528	88	98.7

Pixel active fraction end 2017



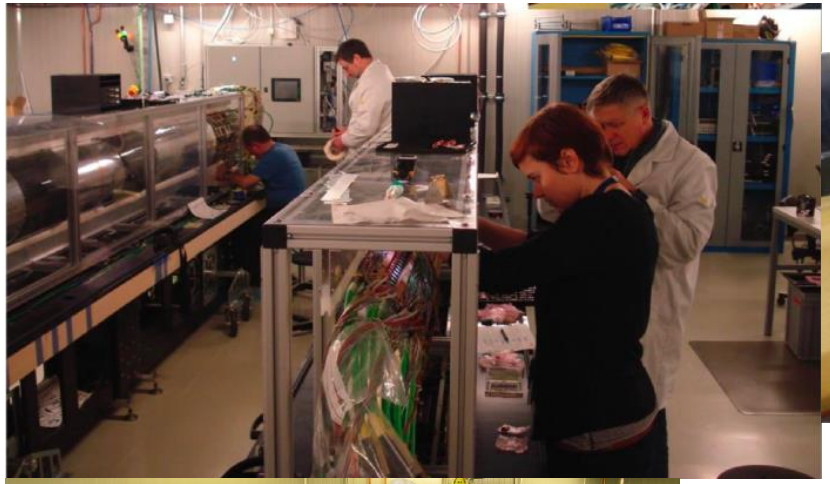
BPix



FPix

Broken DCDC Converter

YETS 2017/2018



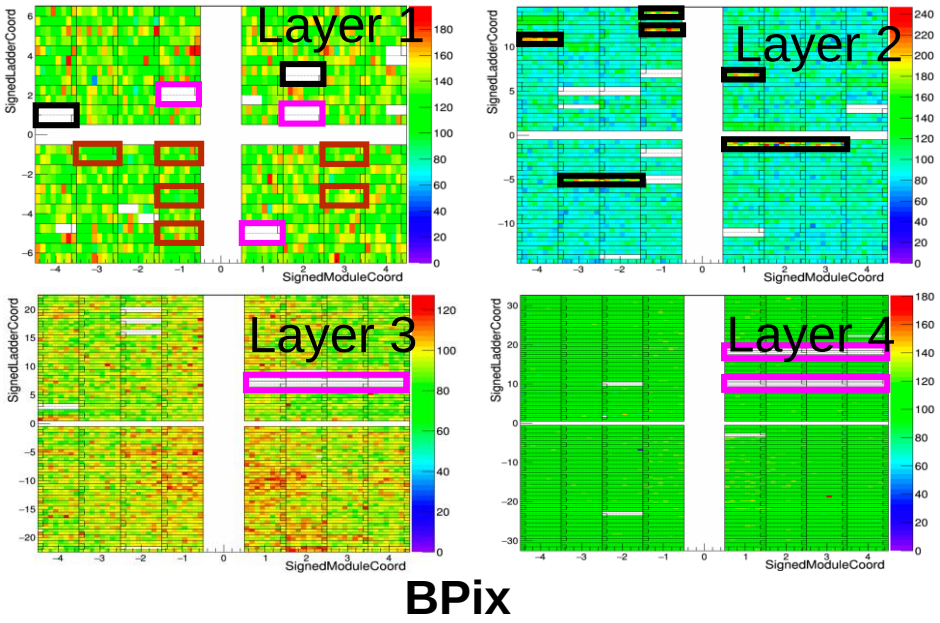
Pixel active fraction end 2018

Other Problems

New modules

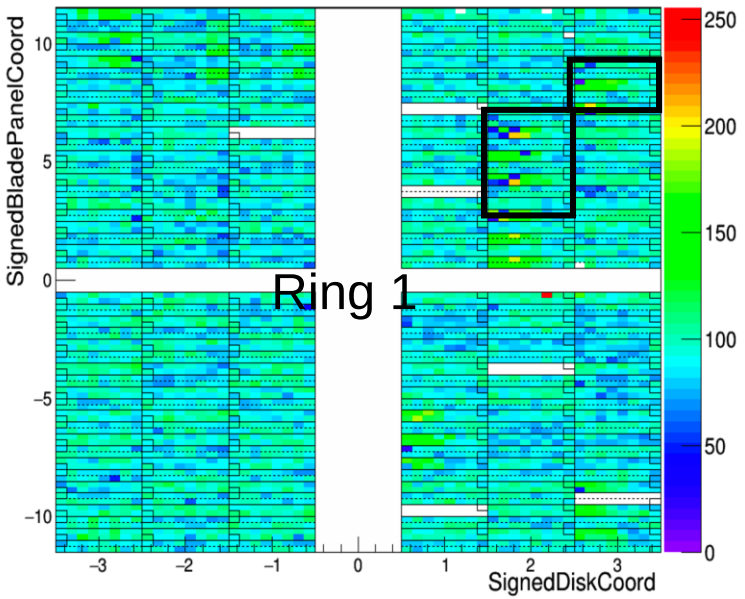
Damaged modules from 2017

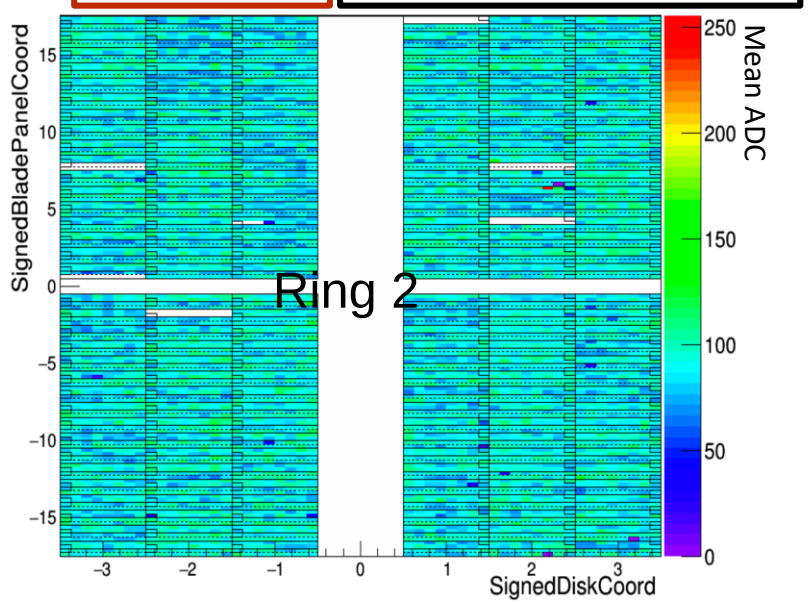
Work in Progress



BPix

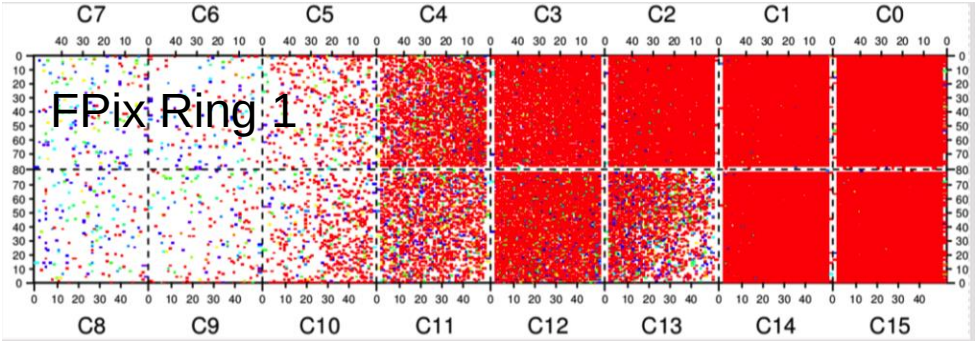
Work in Progress





Work in Progress

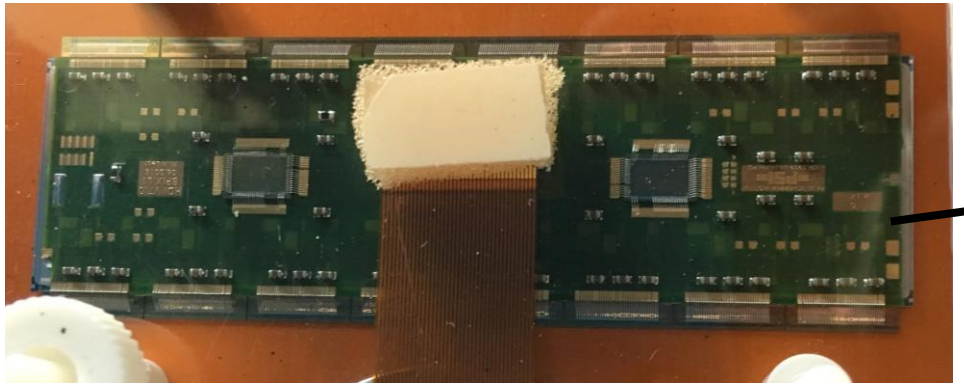
FPix

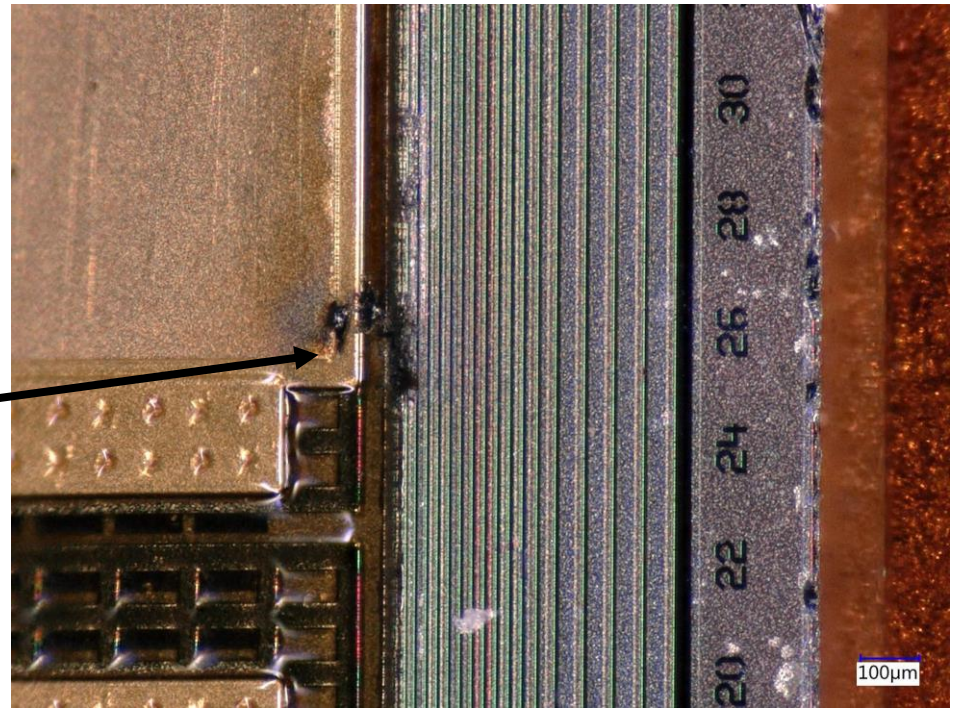


- Reason for DCDC failure discovered in May/June
- Active channel fraction at end of 2018 : 94.5%
- Layer 1 HV breakdown of 2 modules at >400V
- Layer 3/4 connection LV problems
- No modules lost in FPix

Damages due to HV on and LV off

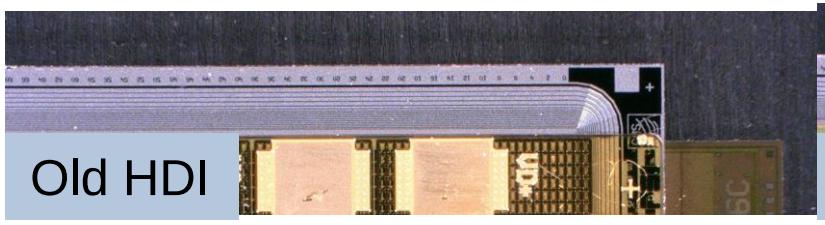
HV problems

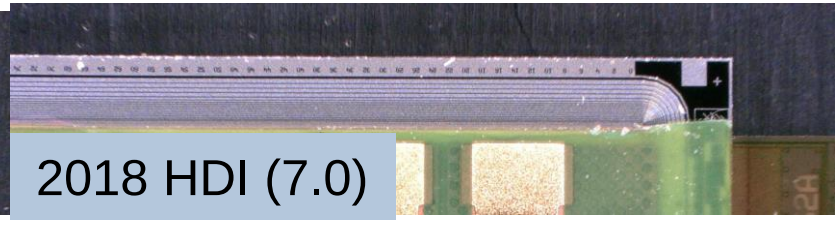


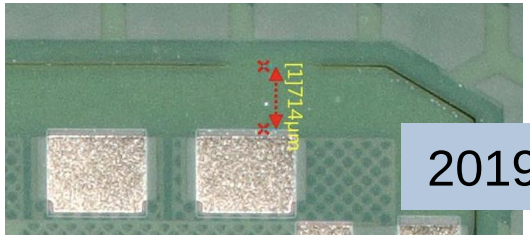


Problem:
The edge of the L1 HDI was not covering the sensor enough, so a HV spark to pad ground could damage the module.

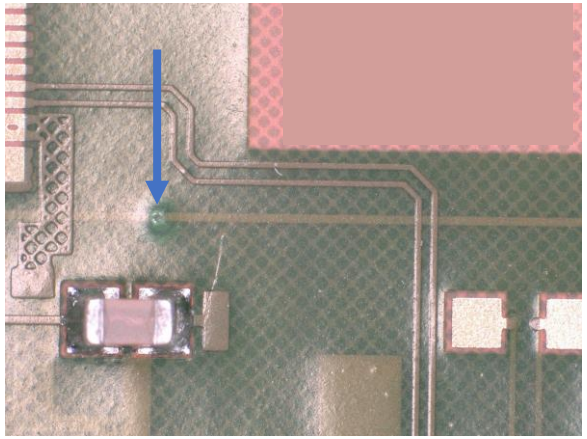
Solution:
For the new L1 the HDI boarder was increased to cover the guard rings completely.

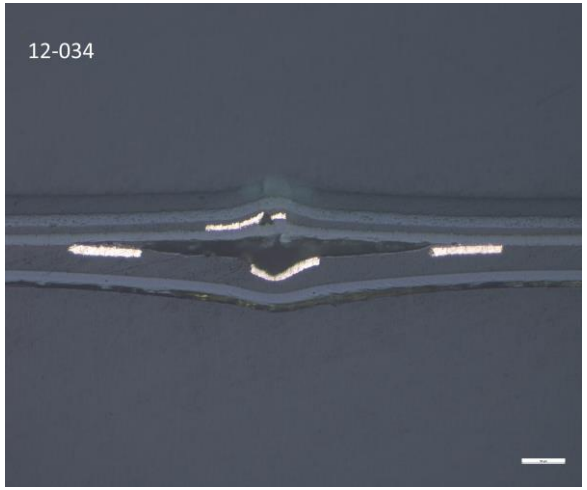






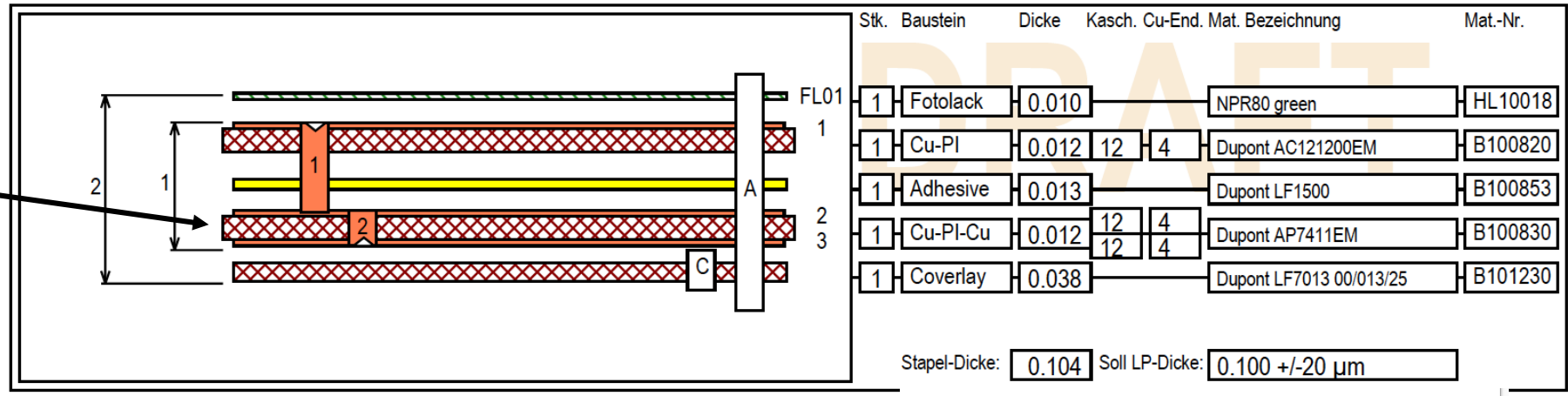
(other) HV problems



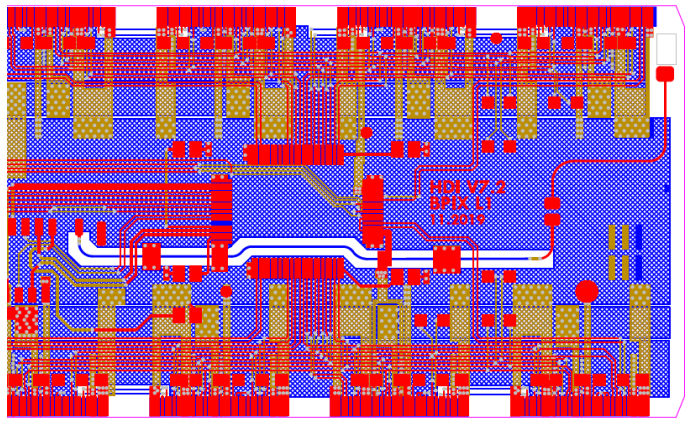


On testing the new HDIs at 1100V (800V maximum in the detector originally designed for 600V) a short occurred

Insulator should hold 3kV



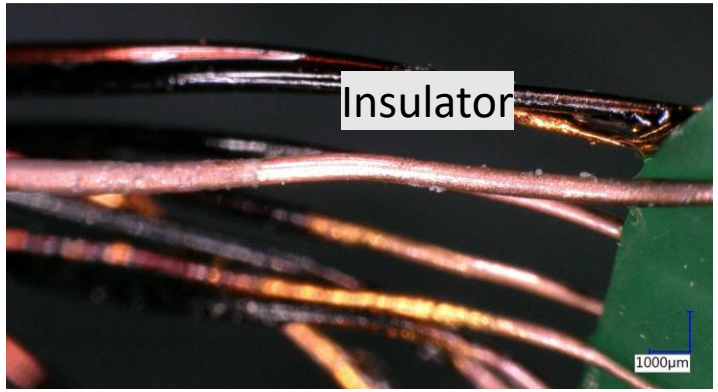
Further test showed that you can break any HDI if you try. Humidity probably has an effect (or opening the test box)

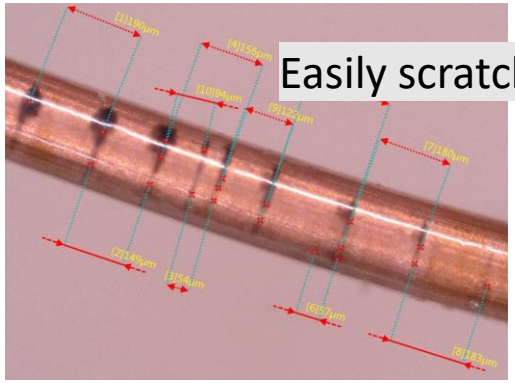


- **New HDI** without a ground grid around the HV line
- No problems observed for long testing at 1100V

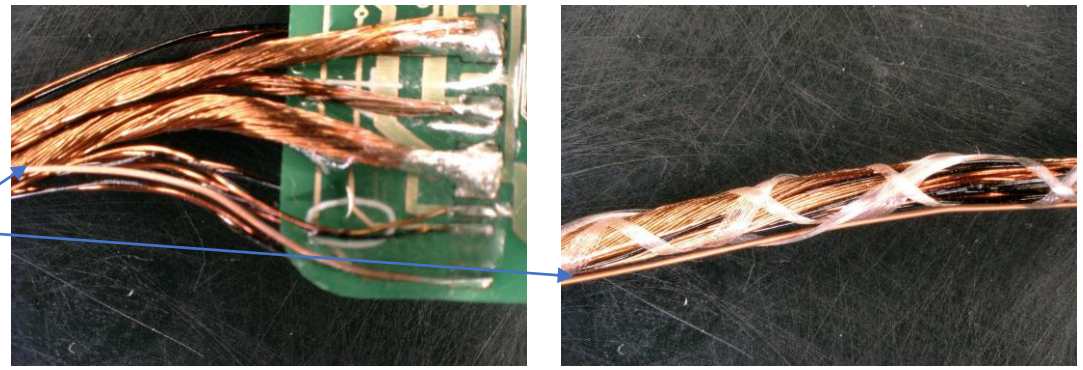
(and one more) HV Problem

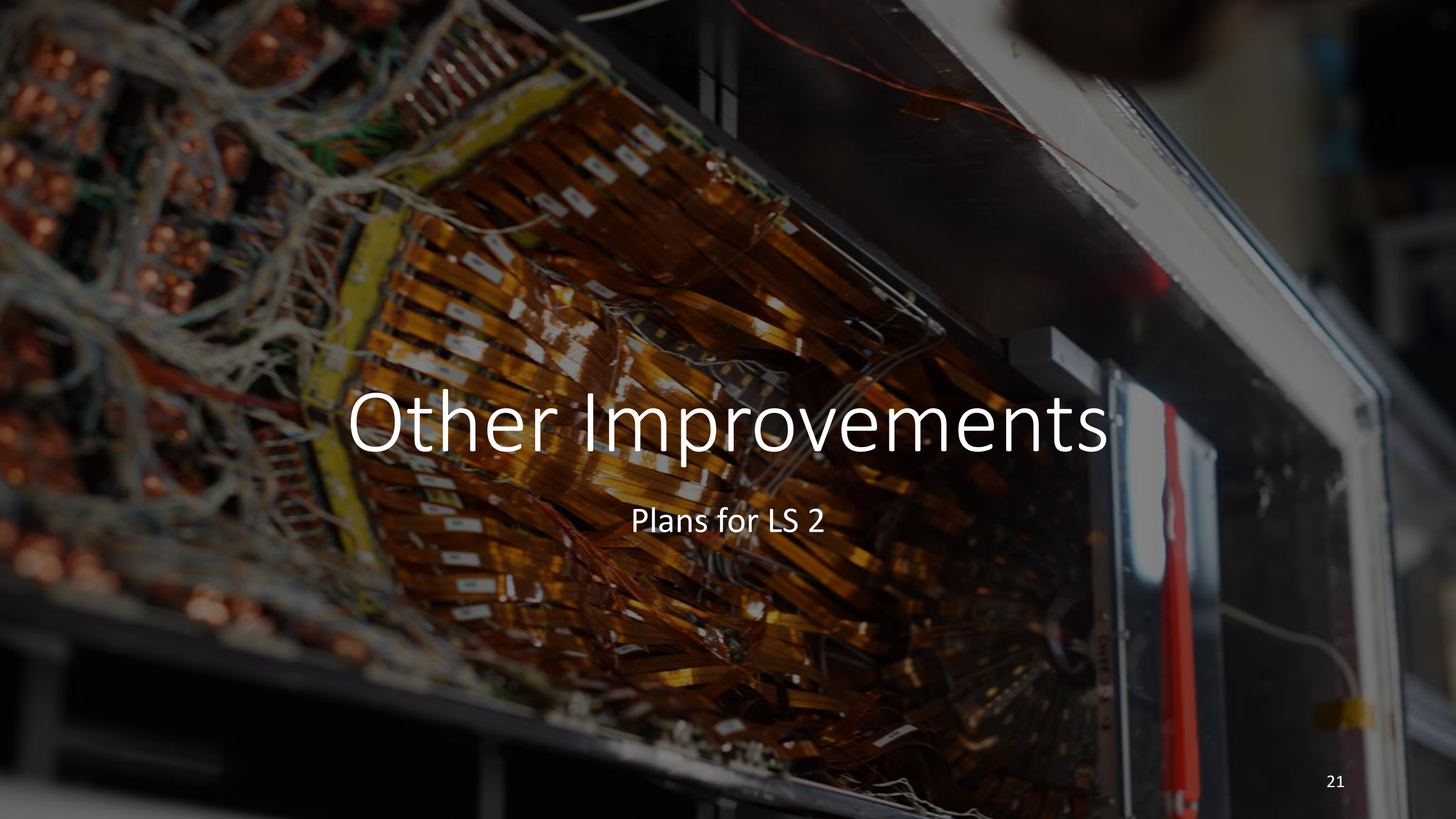
- New module cables showed HV problems:
  - Insulator was stripped to far back
  - PEEK insulation was too susceptible for mechanical damage
- New thicker PEEK insulation solved both issues





New Cable



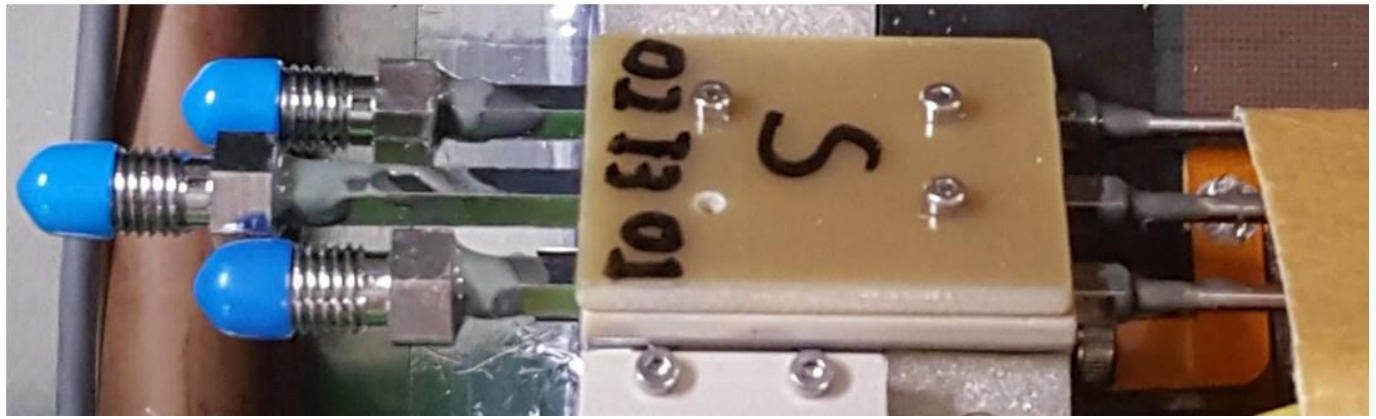


Other Improvements

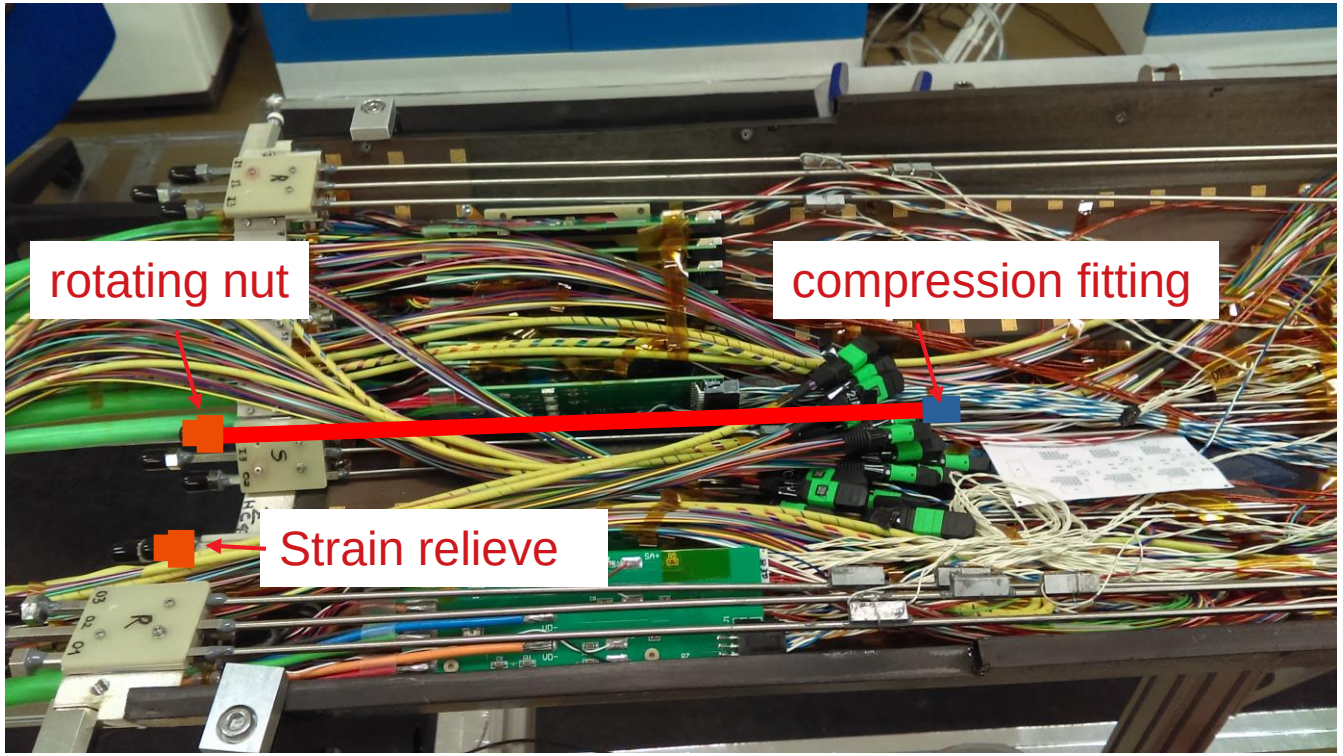
Plans for LS 2

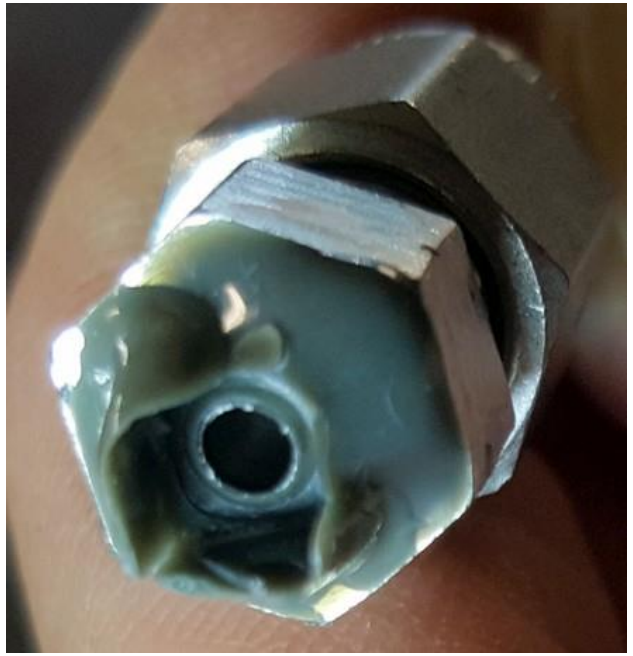
FPix cooling

- Fixed nut directly welded to 120 µm thick pipe
- Minimal mechanical torque needed to break off the nut
- Glue was meant to reduce the mechanical stress.

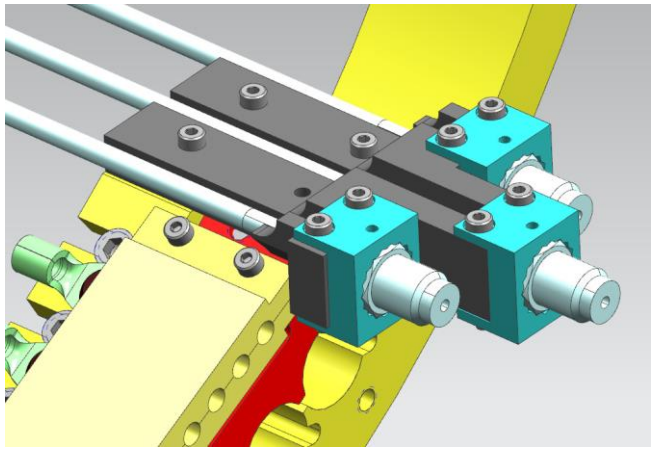


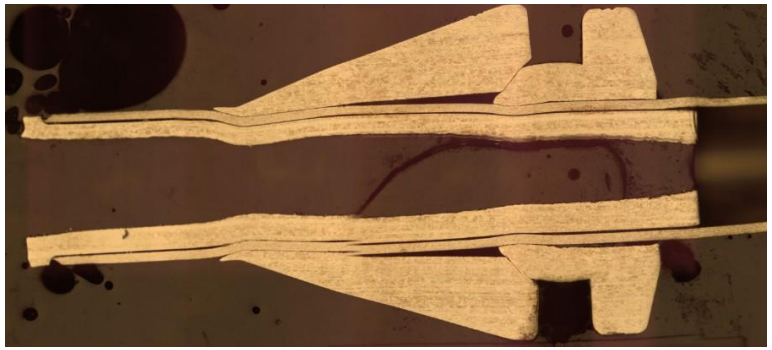
Solution:





FPix Cooling



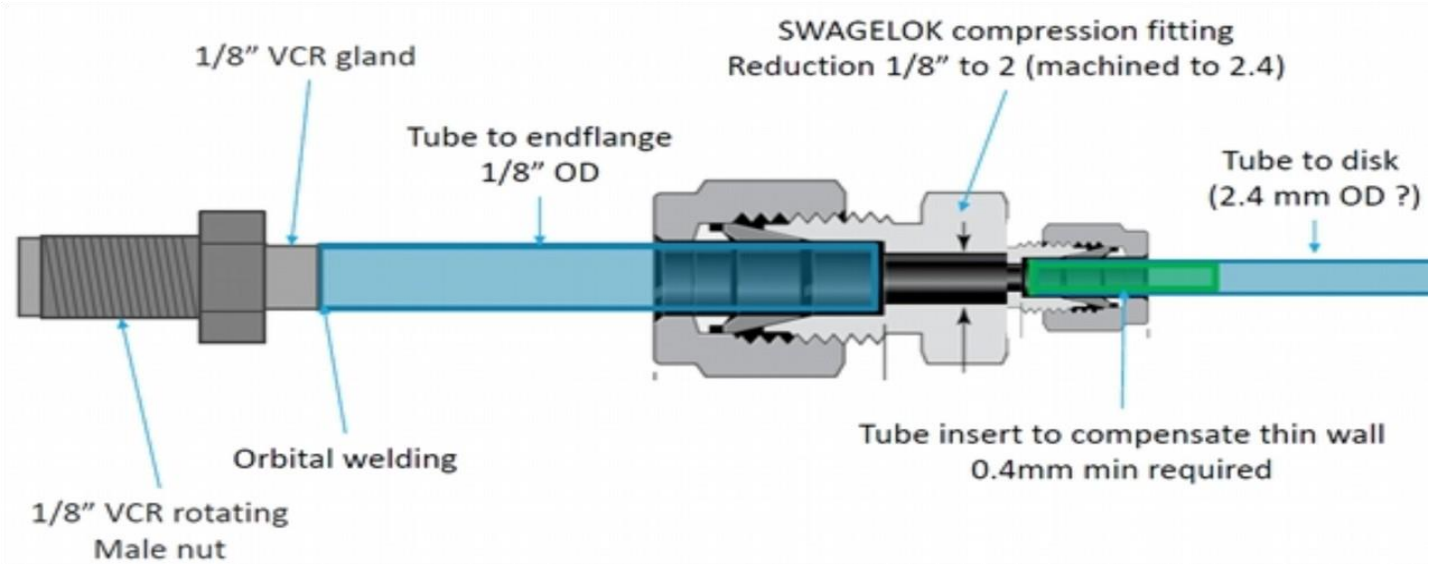


- Add a strain relieve to the end flange (for non broken pipes)

  OR

- Add a larger 1/8” (3.18mm) tube to the 2.4mm tube
- Connection done with a (custom) VCR fitting

- Which solution will be used on how many pipes will be decided during the repair works



FPix HV granularity

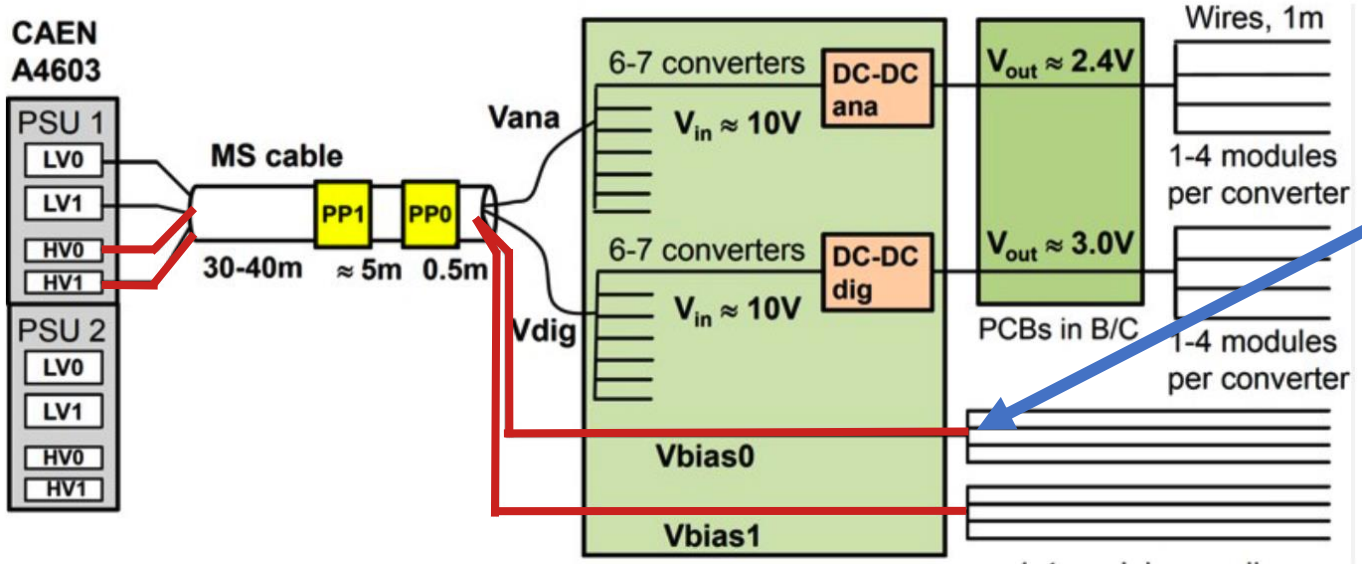
Problem:

- We know that HV without LV damages the ASIC preamplifier (leakage current)
- HV granularity is one powergroup at the moment

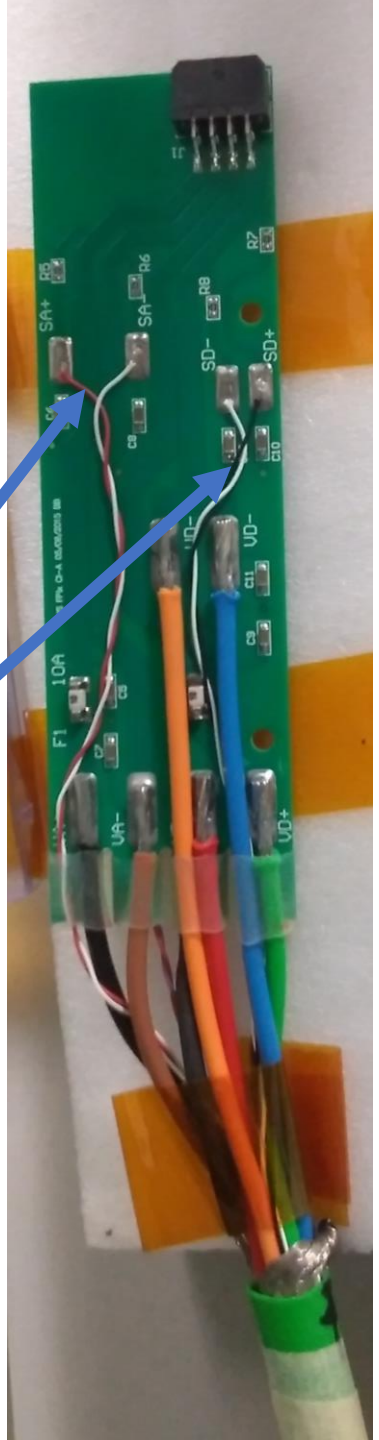
Solution:

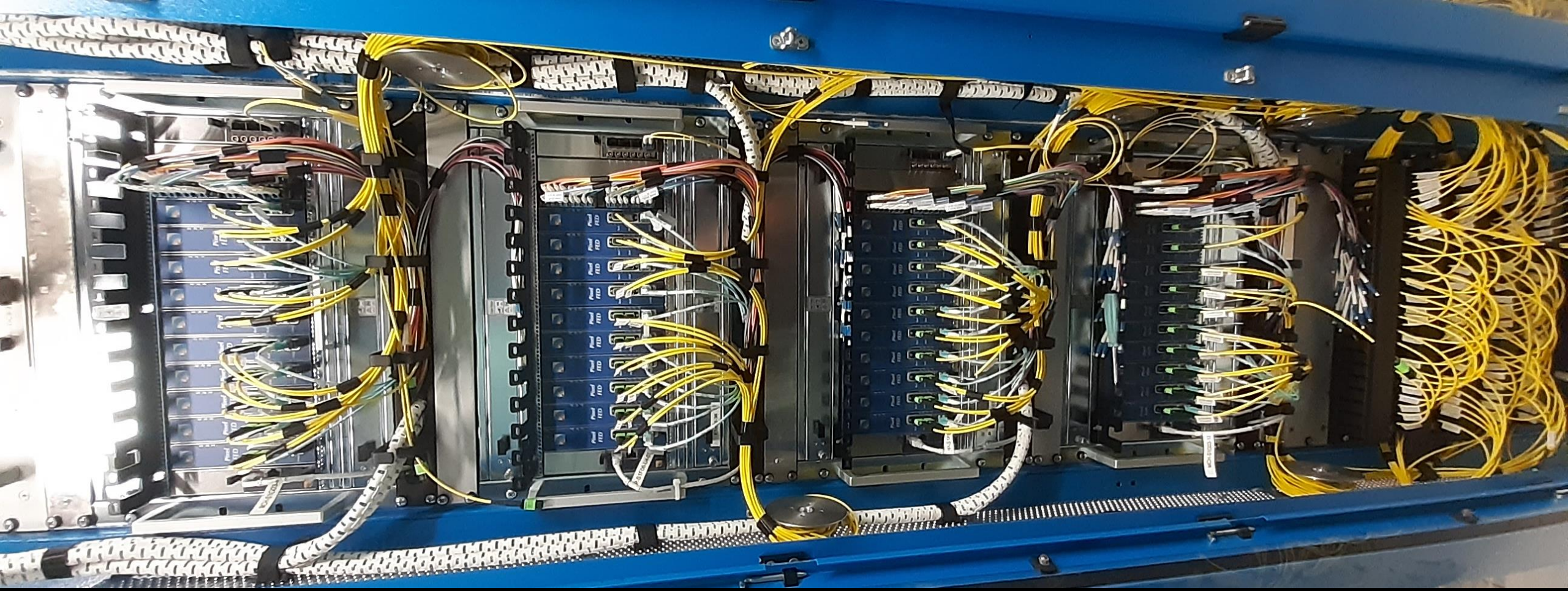
- We have 8 HV lines per cable, that can be switched with jumpers in the power supplies.

→ Need to connect the unused cables



Increase
Granularity



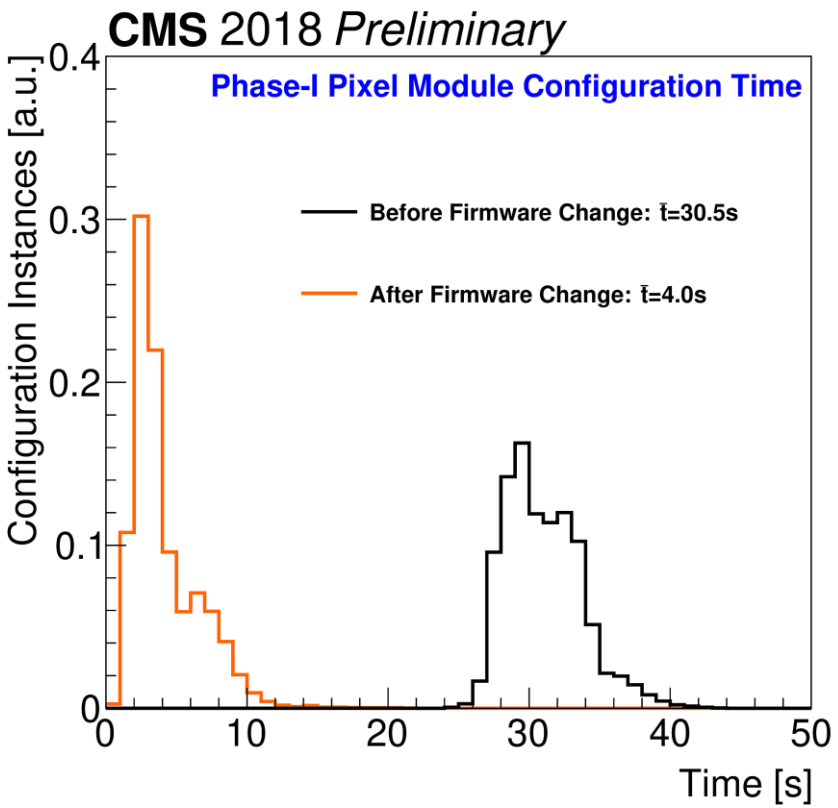


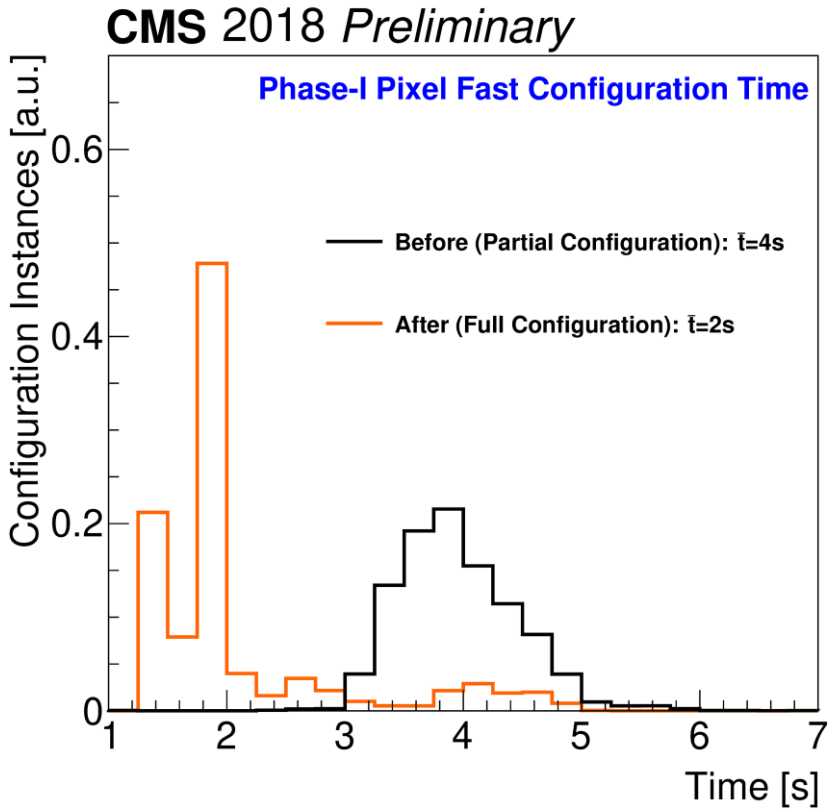
DAQ

Front end controller (FEC) improvements

In 2018 the Pixel configuration time could be reduced drastically.

The main change is that configurations are saved in the DDR of the backend





Front end controller (FEC) im

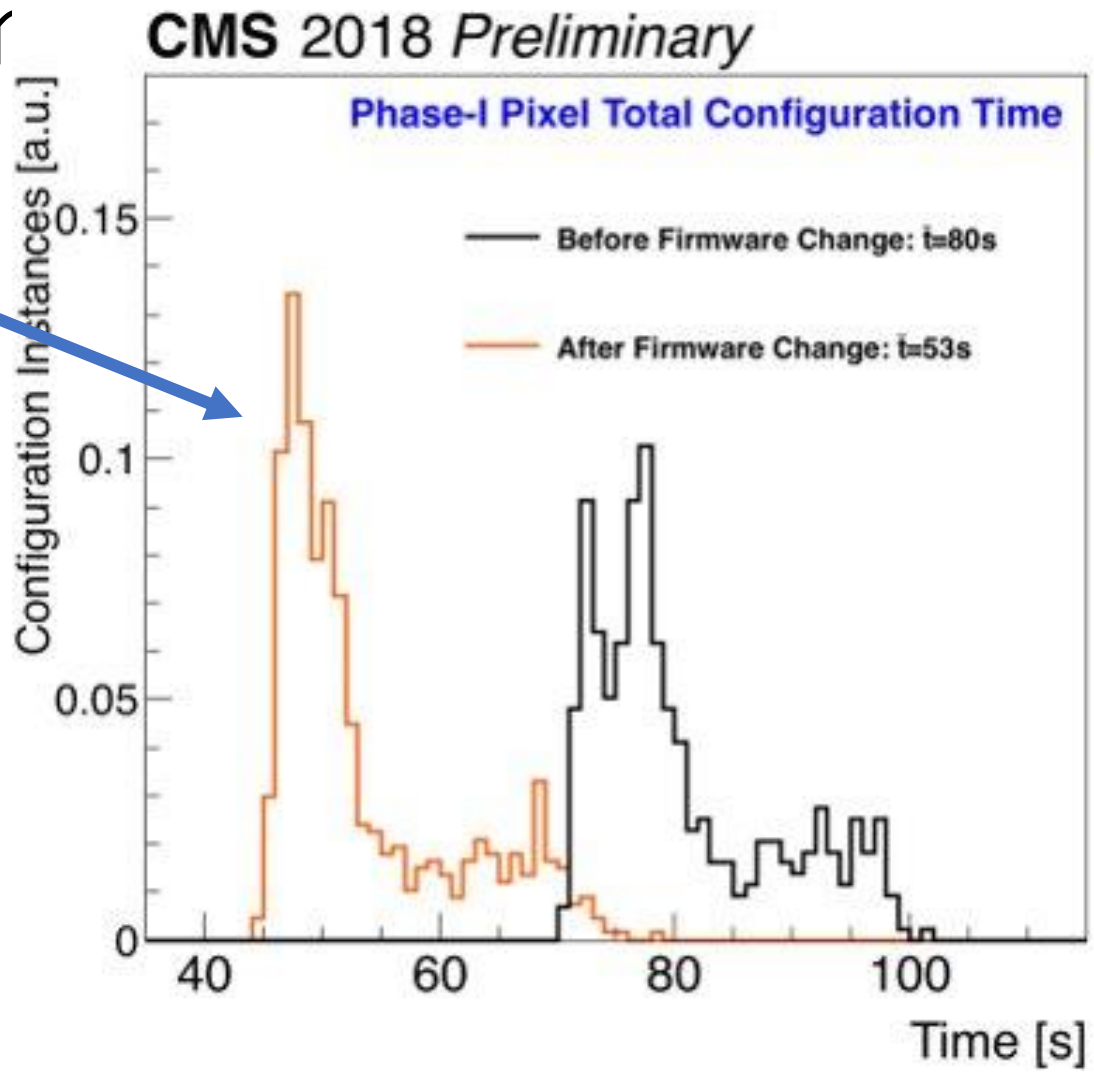
In 2018 the
could be re

The main c
configurations are sa
DDR of the backend

The configuration is now dominated by the TkFEC (non module configuration), instead of the pxFEC (module configuration)

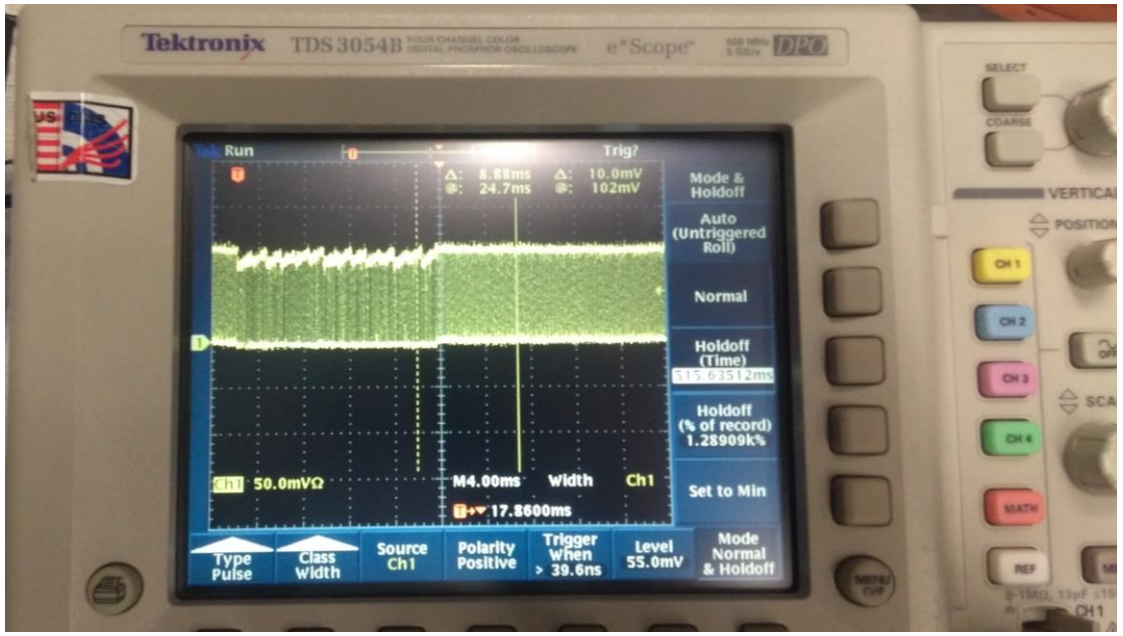
Plan to increase the number of TkFECs by x2

Subsystem	PIXEL
State	Configured
Time	00:43.9
Applied Run Key	N/A
New Run Key	
Commander	select



Reconfiguration During running

- So far the sending of the module configuration data was initiated via software
- For Run 3 the plan is to reconfigure the Pixel on a B-Go signal (Non readout trigger signal) with every TTC Resync (every 5-30 min)



In the TTC Resync sequence there are 23 µs time to reprogram the modules

No additional deadtime

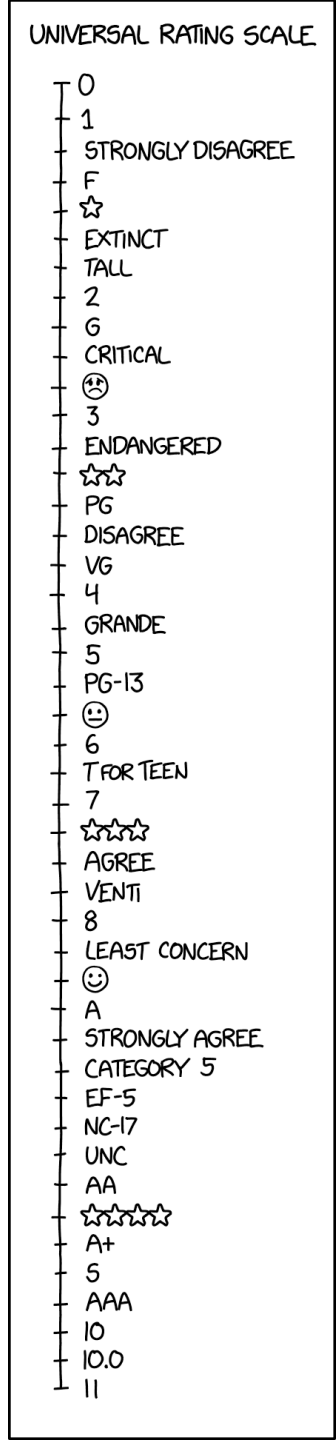
All vital registers will be refreshed

Pixel Offline

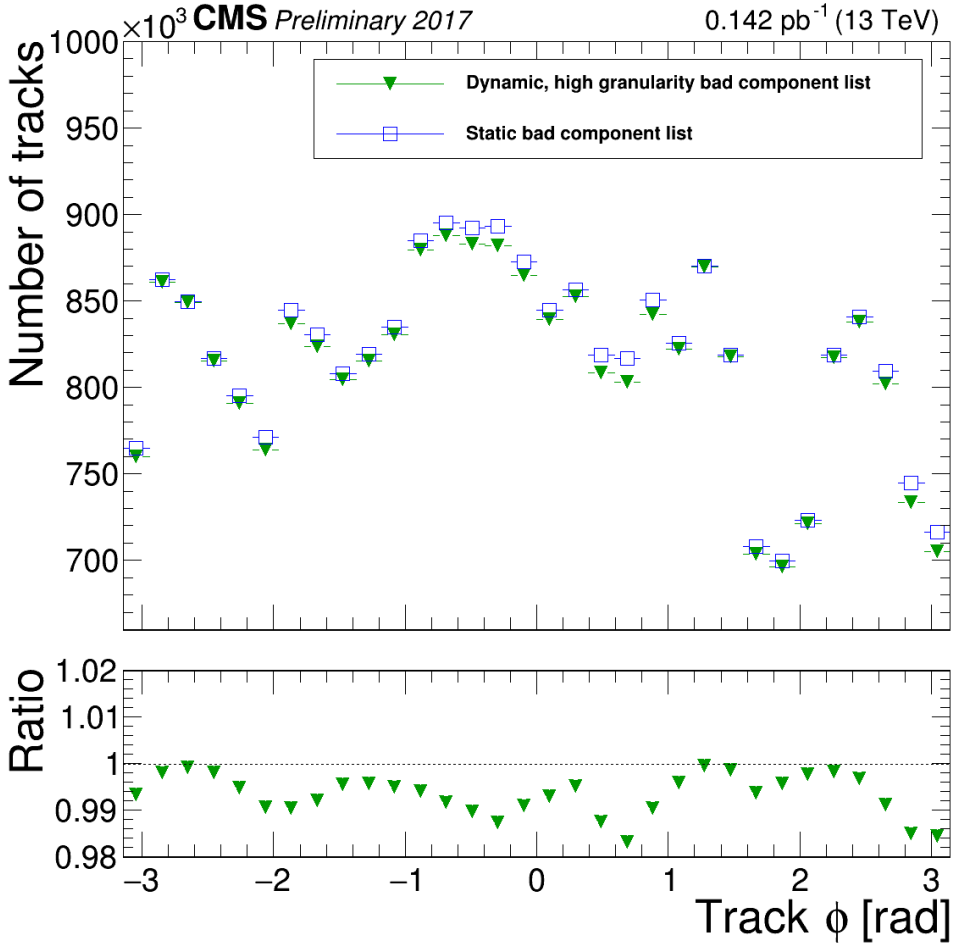
Reconstruction and Performance

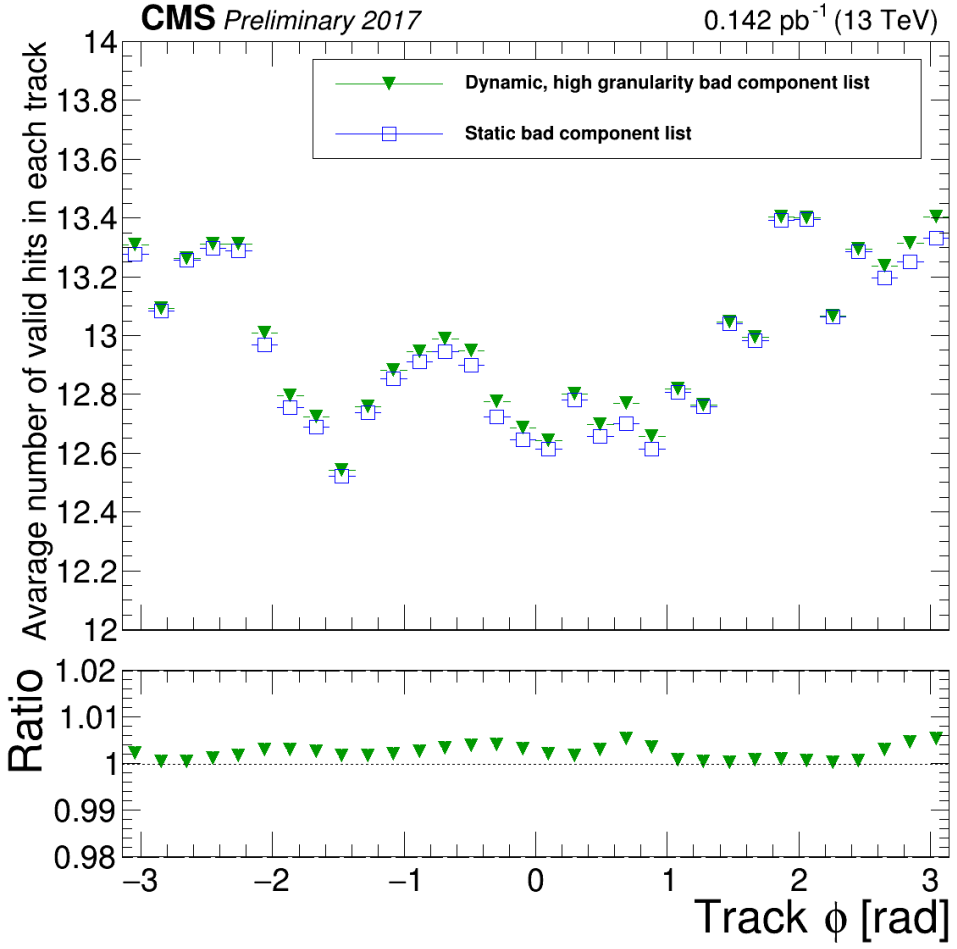
Run2 Legacy Reconstruction

- Reconstruction for Run 2 (including Phase 0 Pixel in 2016) with the best knowledge up to date.
- Many improvements in the track reconstruction
  - Higher granularity radiation correction
  - Higher granular alignment
  - Better cluster description
  - Better tracking of non responsive detector parts



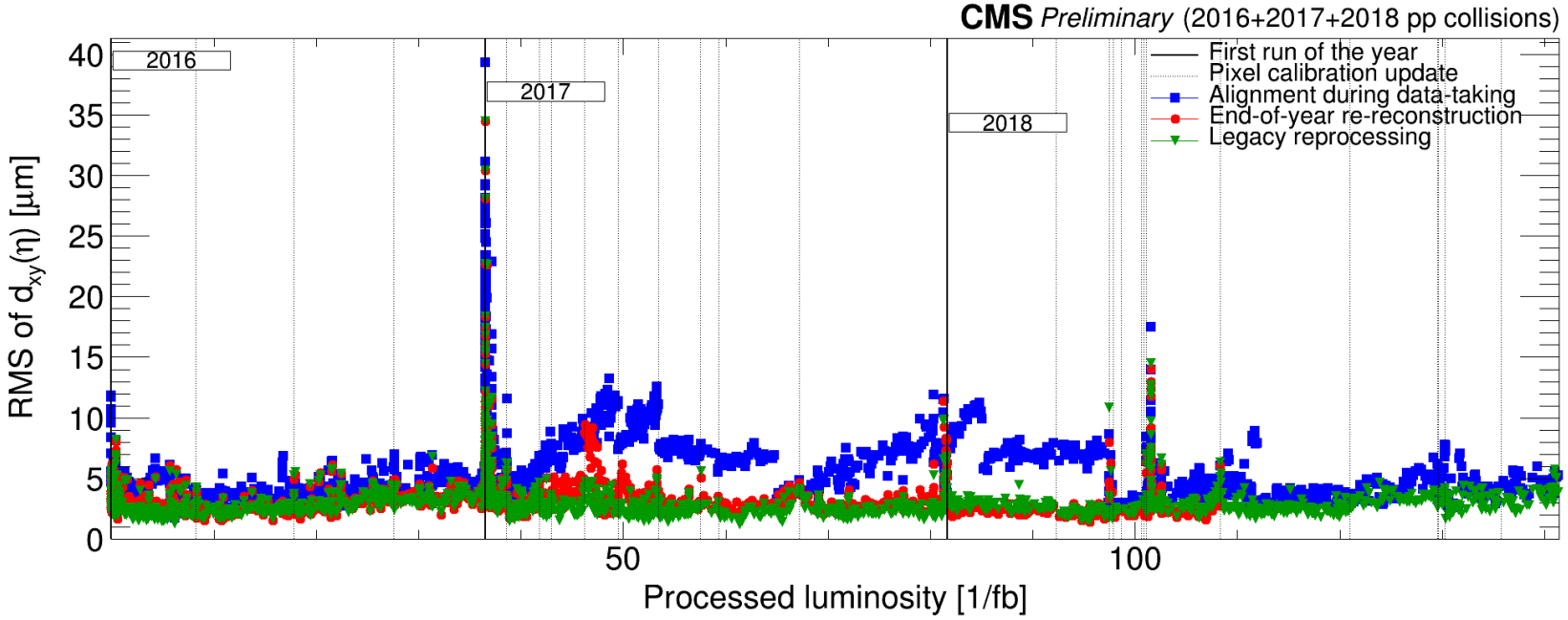
Dynamic bad components

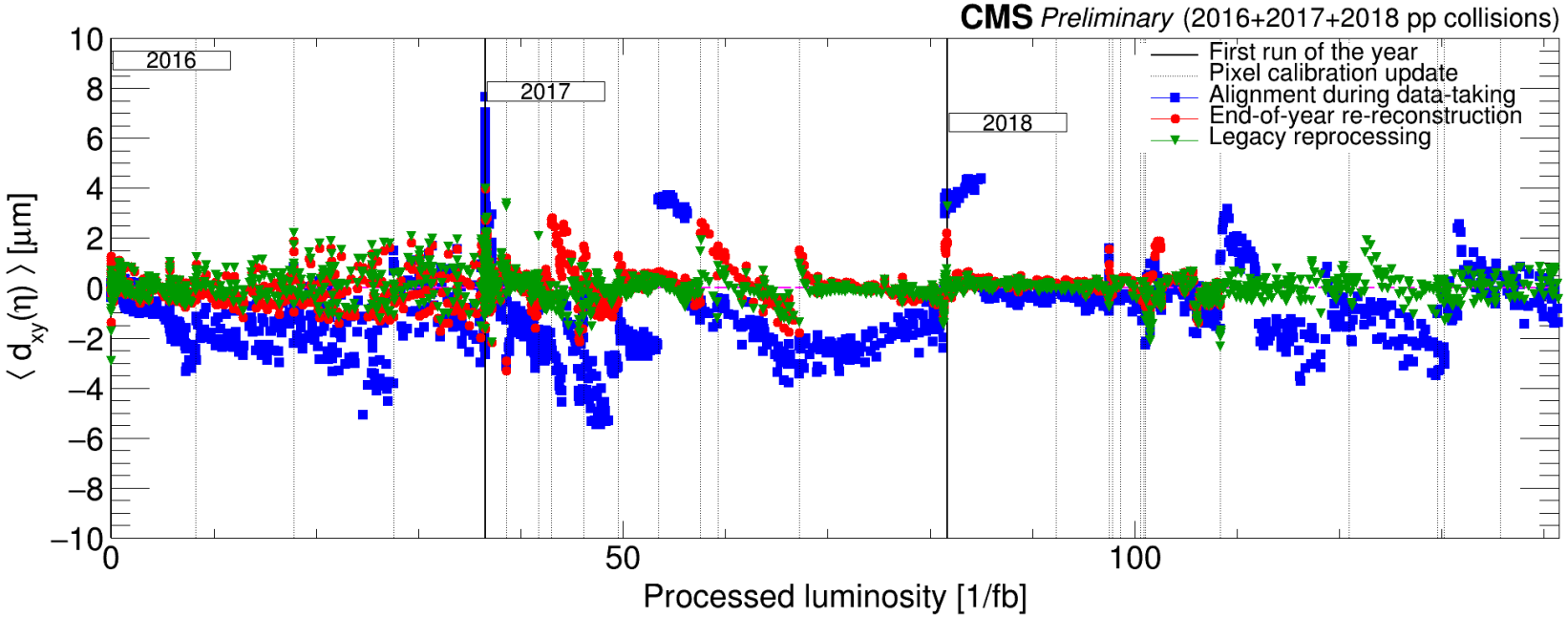




The rapidly changing detector in 2017 (DCDC) and 2018 (“stuck” TBM) created a need to automatically take the non working components into account.

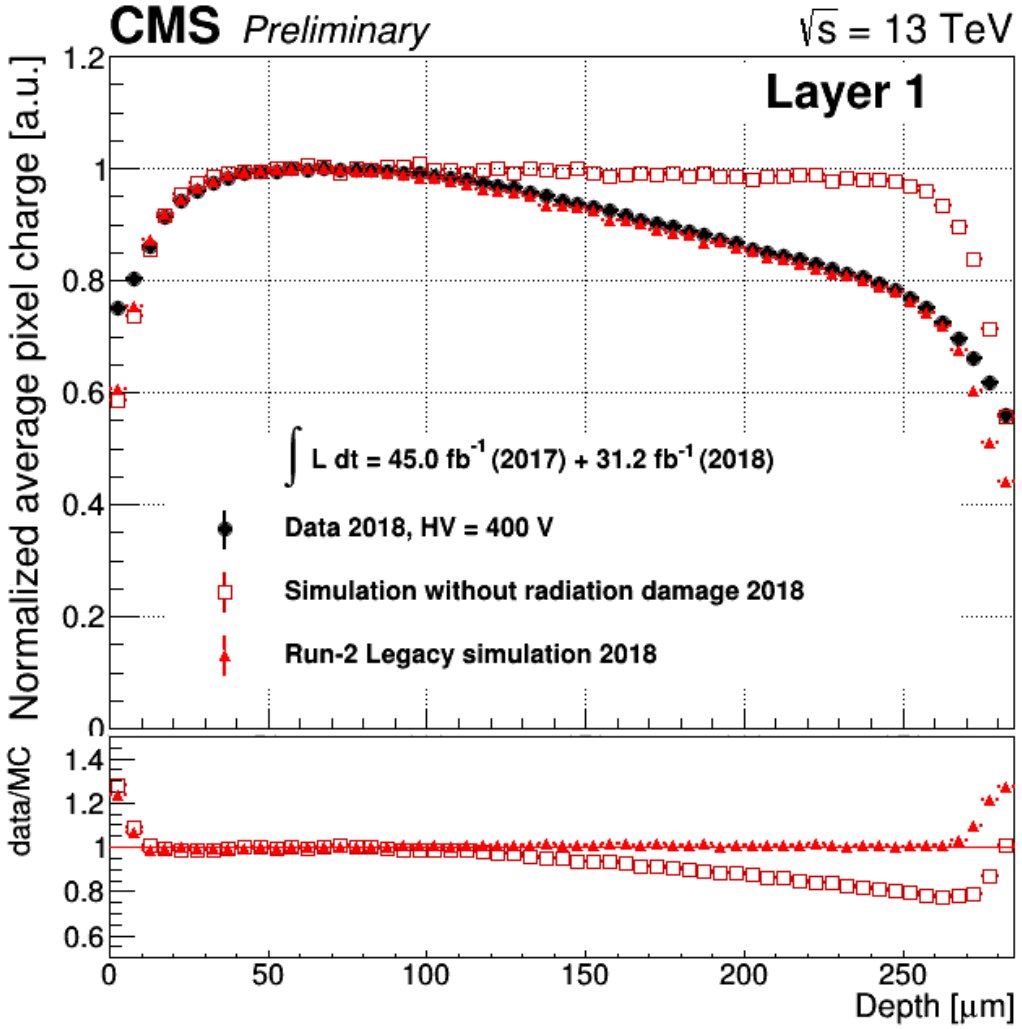
Alignment



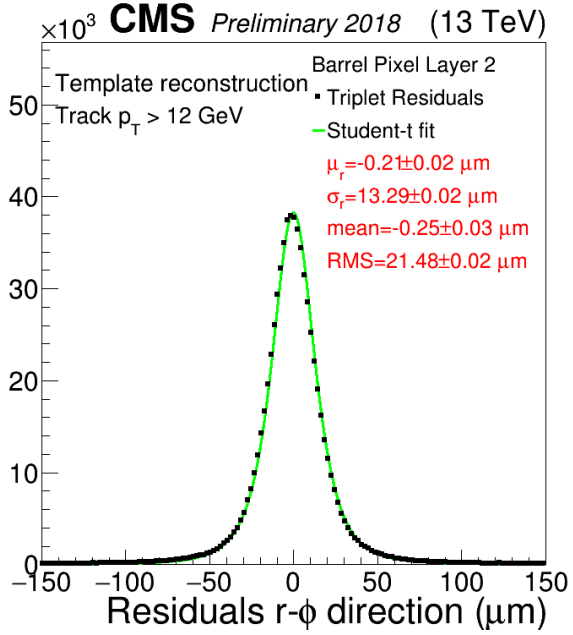


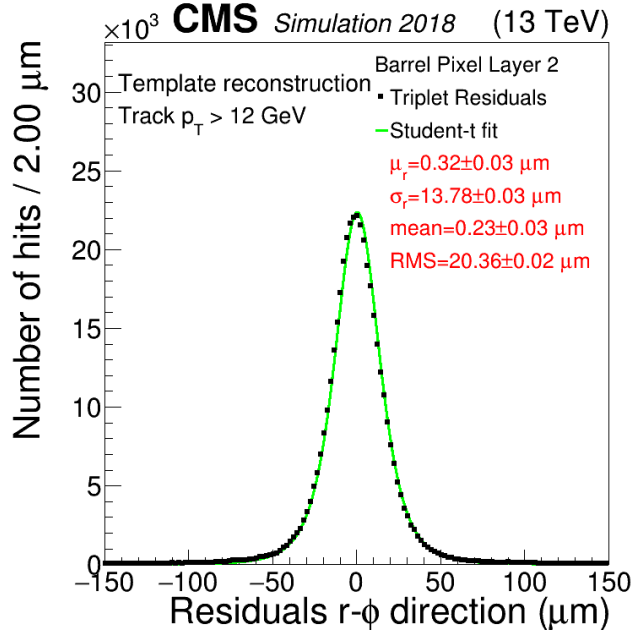
The Tracker alignment could be improved due to an increase of fitted components, shorter time intervals for the fitting and a much improved understanding off the detector.

Combined very good resolution

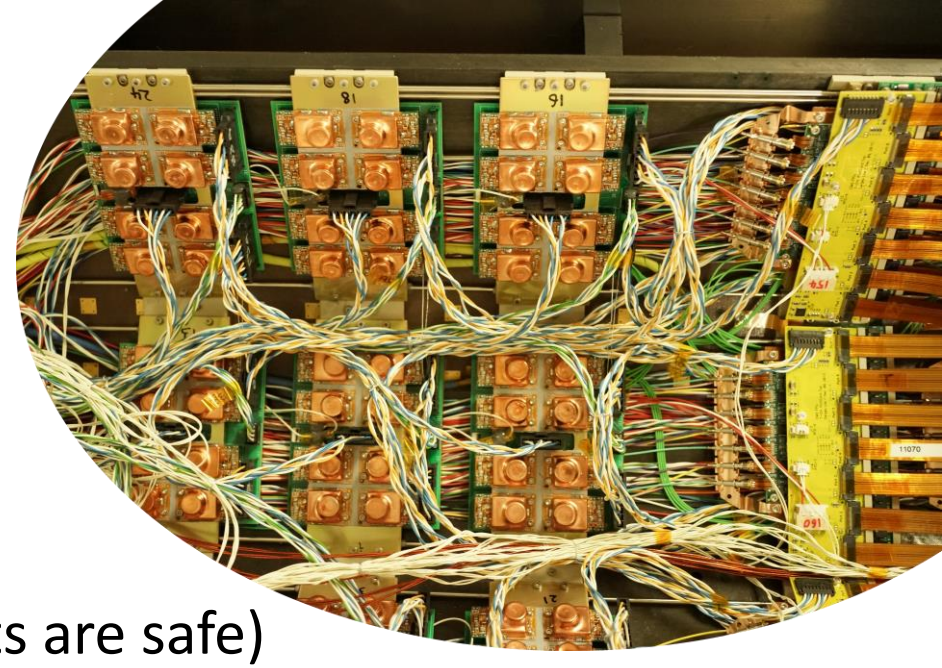


With the ultra legacy reconstruction the Run 2 can be described in great detail.





Lessons Learned



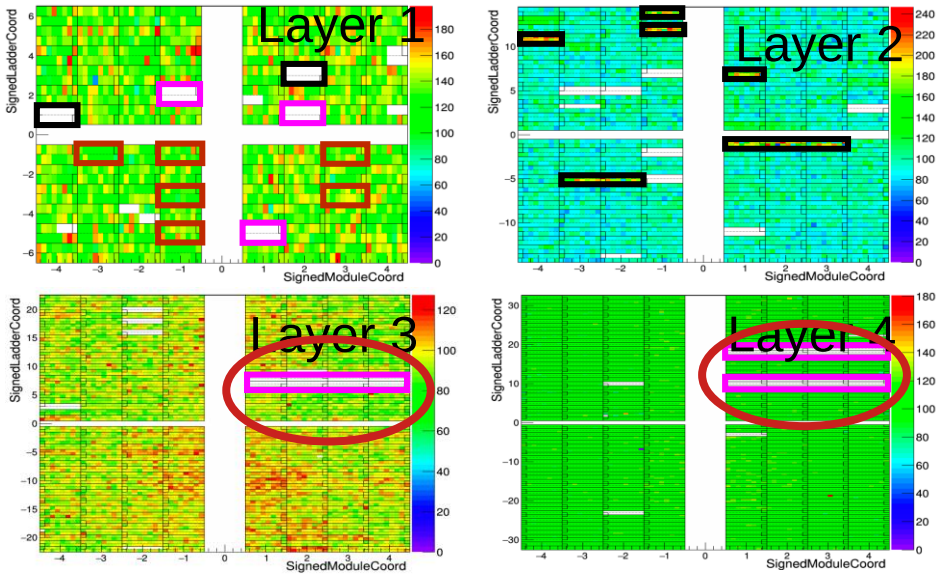
- The CMS Pixel performed very well given the issues
- DCDC converter breakdown is understood (Phase 2 projects are safe)
- Looking forward to new Layer 1
- Be sure that your power system works (biggest holes in the active detector faction)
  - Check for failure scenarios (how big would be the holes)
- If you break something, do it in a LS
- Never stop developing the offline reconstruction

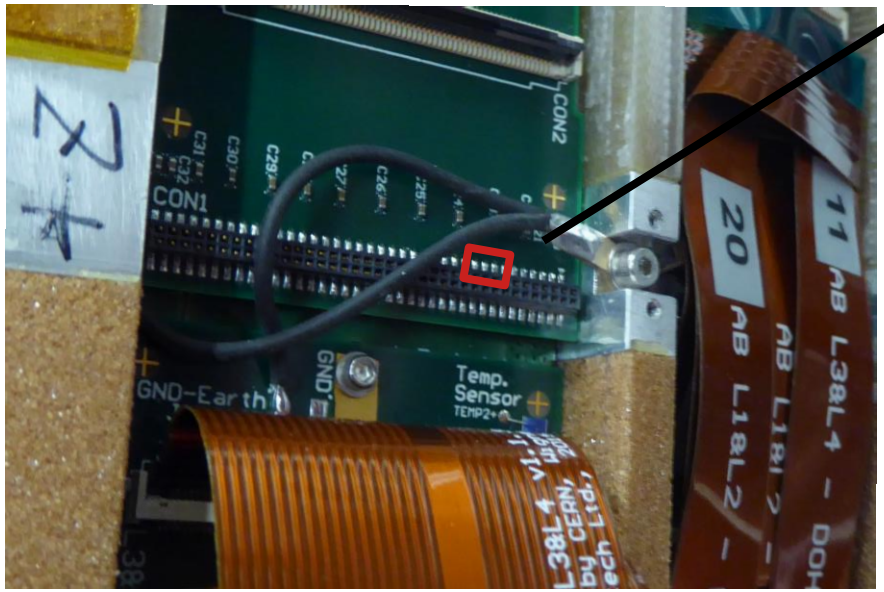
Backup Slides

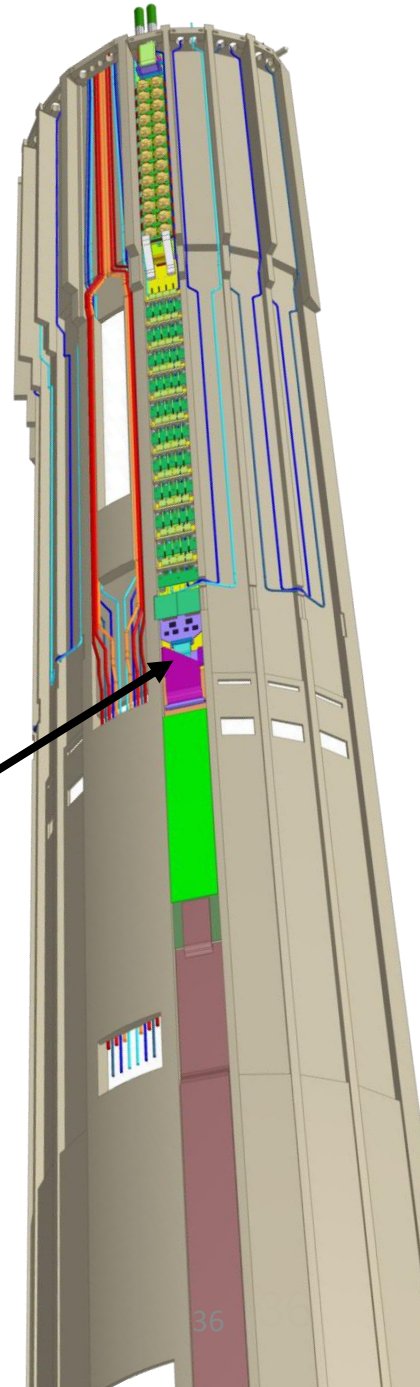
Connection problems

- Two LV lines were disconnected during operations in 2018
- To avoid damages, the HV was shut of (full sectors)
- The problem was in the connection between two boards
- A better mechanical support is planned

Work in Progress





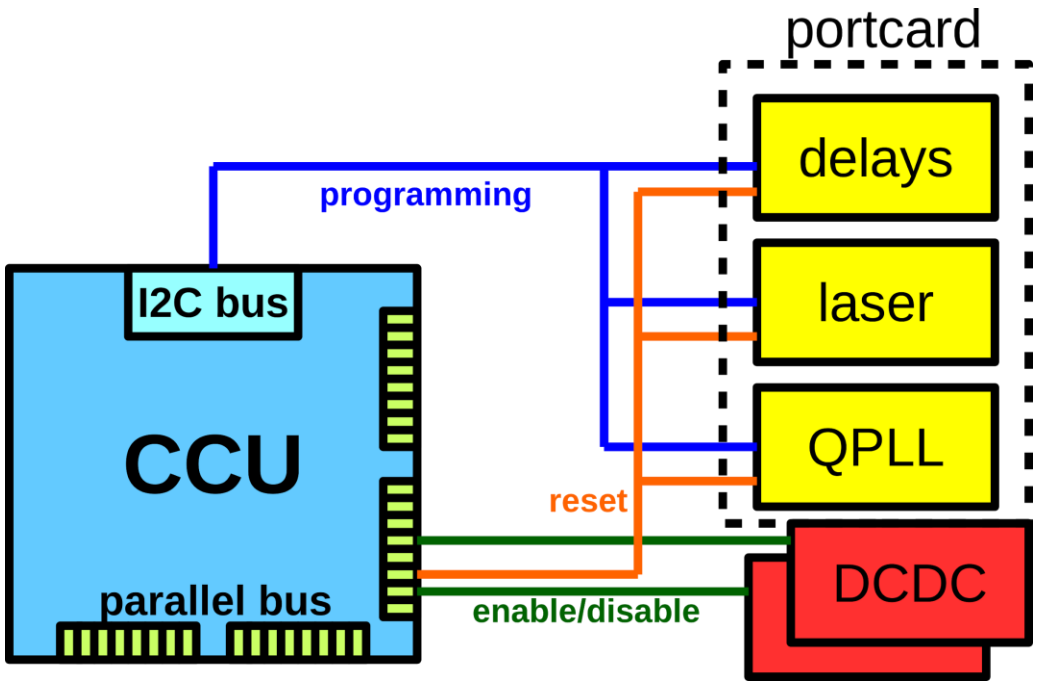


CCU losses during running in 2018

two classes of problems

control current drop

- Observed 2017 already
- No data from one portcard
- Portcard recovery catches these cases
  - Reprogramming of portcard fixes the problem portcard



module current drop

- Symptoms: modules in granularity of DCDC converters send no data
- Modules are really powered off and come up unconfigured again
- Module SER ~ catches this problem

parallel bus used for:

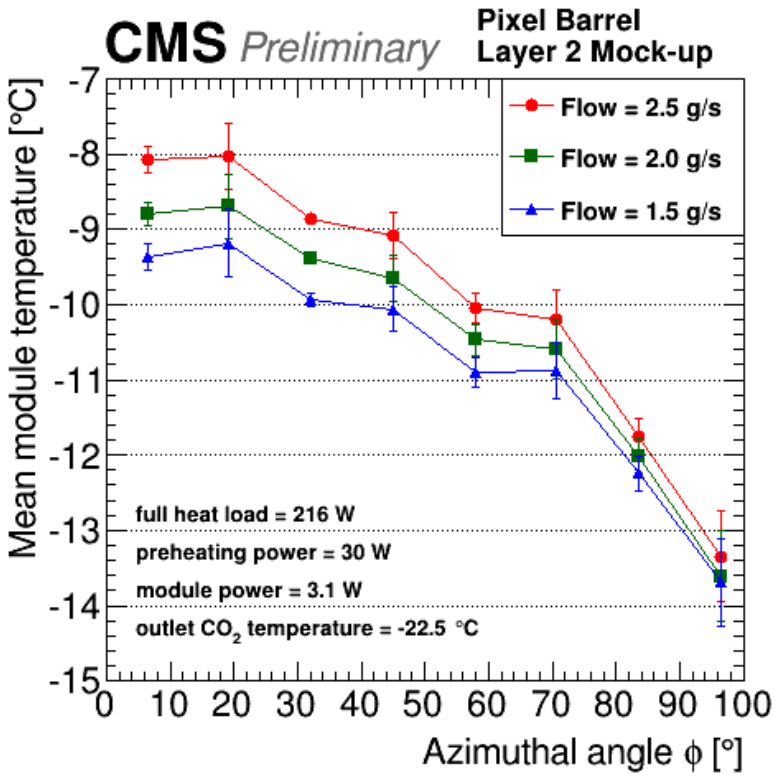
- Enabling/disabling DCDC
- Sense power state of DCDC
- Reset line
- QPLL status

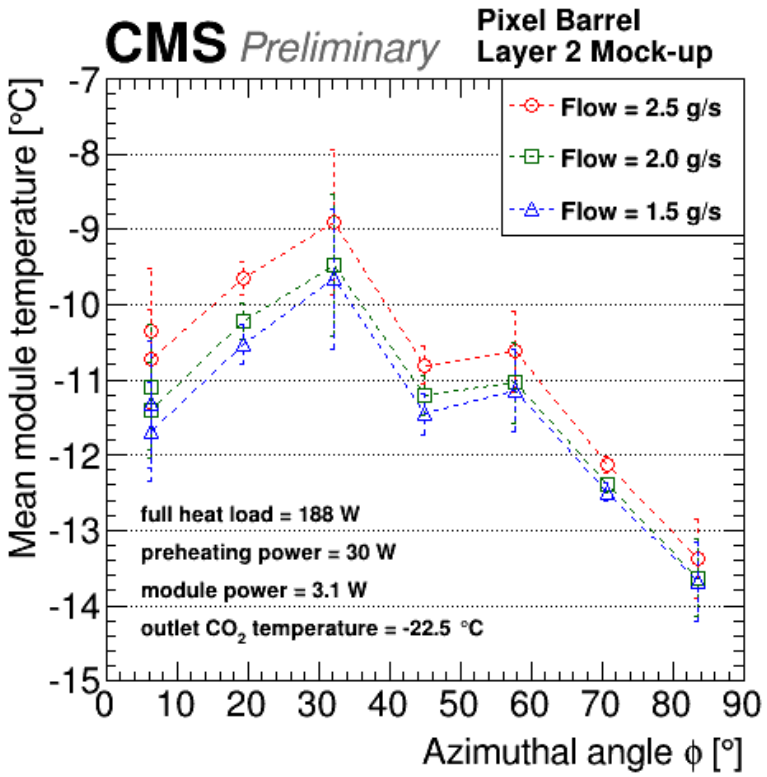
both classes of problems could be explained by problems in parallel bus

CO^2 cooling

Things that we learned from the CO2 cooling:

- It works
- You do want a (controllable) preheating system
- The temperature might be non homogeneous
- **Be careful how you do the connections**





LHC Schedule 3.1 2021