New silicon trackers for a triggerless LHCb: the Vertex Locator (VELO) and the Upstream Tracker (UT)

Manuel Franco Sevilla
on behalf of the LHCb collaboration
University of Maryland

5th October 2020
The 29th International Workshop on Vertex Detectors (Virtual)
The LHCb experiment

~ General purpose forward detector
~ Focus on **flavor physics**
  - 25% of $b\bar{b}$ production with 4% of solid angle
    - $2 \leq \eta \leq 5$
  - 100k $b$-hadrons produced every second

~ Excellent secondary vertex reconstruction
  - Large boost is major help

~ PID: $\pi$, K, p, $\mu$
Huge sucessful Runs 1 and 2

LHCb has demonstrated emphatically that the LHC is an ideal laboratory for particle physics

Forward top pair production cross section

Most precise measurement of $\phi_s$

R($D^*$) from $B \to D^*\tau\nu$

 Vertexing and tracking are the cornerstones of these results


LHCb simulation

Prompt ($D^*\pi\pi\pi\chi$)

Double-charm ($D^*DX$)

Signal ($D^*\tau\nu$)


New silicon trackers for a triggerless LHCb: VELO and UT
Limitations of LHCb

~ Have been luminosity leveling since 2011
- Data sample limited to 1-2 fb⁻¹/year

~ Limitations for higher luminosity of 2011-2018 detector
- Overall performance degrades quickly for high occupancy
- Low efficiency for hadronic decays at higher lumi due to hardware trigger
- Radiation hardness of trackers

~ Upgrade I being installed will remove these constraints
Upgrade I

Run 1 | LS1 | Run 2 | LS2 | Run 3 | LS3 | Run 4

Upgrade I (being installed)

All electronics upgraded to send every hit to flexible software trigger
Increase granularity and longevity of 3 new trackers
New RICH optics, lower PMT gain in CALO

Upgrade II to be covered by Martin Van Beuzekom on Thursday
~ Not only able to withstand 50 fb⁻¹ + 40 MHz readout, but improved performance

- Better 3D impact parameter resolution
  - Translates to improvements of 10-15% in the B decay time resolution
- Better $p_T$ resolution
- Dramatic reduction of ghost rate

~ Significant speed up in reconstruction time
- Make possible the software-only trigger

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**Tracking upgrade**

- VELO Silicon strips
- SciFi Scintillating fibers
- IT + OT Silicon strips + straw tubes

**LHCb Simulation**

- Relative population of $b$-hadron daughter tracks

**CERN/LHCC 2013-021**
Pixel Vertex Locator (VELO)
### Pixel VELO overview

In vacuum as close to IP as possible

- Crucial for vertexing and tracking

<table>
<thead>
<tr>
<th></th>
<th>VELO</th>
<th>Pixel VELO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Years of operation</td>
<td>2010 – 2018</td>
<td>2022 – 2030</td>
</tr>
<tr>
<td>Sensors</td>
<td>173k R-φ</td>
<td>41M pixels</td>
</tr>
<tr>
<td>Number of layers</td>
<td>23</td>
<td>26</td>
</tr>
<tr>
<td>Distance from IP</td>
<td>8.2 mm</td>
<td>5.1 mm</td>
</tr>
<tr>
<td>Fluence$<em>{\text{max}}$ [1 MeV n$</em>{\text{eq}}$ cm$^{-2}$]</td>
<td>4.3×10$^{14}$</td>
<td>8×10$^{15}$</td>
</tr>
<tr>
<td>HV Tolerance</td>
<td>500 V</td>
<td>1000 V</td>
</tr>
<tr>
<td>ASIC Readout</td>
<td>1 MHz</td>
<td>Data driven</td>
</tr>
<tr>
<td>Data Rate</td>
<td>~150 Gb/s</td>
<td>2.8 Tb/s</td>
</tr>
<tr>
<td>Power</td>
<td>~0.8 kW</td>
<td>~1.6 kW</td>
</tr>
<tr>
<td>Operating temp.</td>
<td>-8°C</td>
<td>-25°C</td>
</tr>
</tbody>
</table>

VELO foil etching status

Paula Collins, summary of document produced by Krista de Roo, Willem Kuilman, Kazu Akiba, Victor Coco, Paula Collins, Wolfgang Funk, Wouter Hulsbergen, Tjeerd Ketel, Marcel Merk, Freek Sanders, and work of many others...

### VELO Status Report

LHCb acceptance

- Acceptance 103 cm
- Acceptance 55 cm

Sensors

- 173k R-φ
- 41M pixels

Number of layers

- 23
- 26

Distance from IP

- 8.2 mm
- 5.1 mm

Fluence$_{\text{max}}$ [1 MeV n$_{\text{eq}}$ cm$^{-2}$]

- 4.3×10$^{14}$
- 8×10$^{15}$

HV Tolerance

- 500 V
- 1000 V

ASIC Readout

- 1 MHz
- Data driven

Data Rate

- ~150 Gb/s
- 2.8 Tb/s

Power

- ~0.8 kW
- ~1.6 kW

Operating temp.

- -8°C
- -25°C

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VELO fully closed (stable beams)

VELO fully open

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New RF foil

~ RF foil separates beam/VELO vacua and shields electronics

~ Largest contributor to material budget

~ Initial proposal to reduce thickness from 300 to 250 μm

  - Decided last year to chemically etch it to 150 μm!

~ RF now milled and etched

  - Extensive metrology campaign

Milled from Aluminum block

Beautiful video

Chemical etching the innermost region with NaOH

Significant improvement on impact parameter resolution

Impact on Physics

- Foil has a corrugated shape: clearance from Modules
- Particles often traverse foil multiple times before first measuring point
- This impacts the physics performance
- Only free variable: foil thickness
- Simulation shows 10% improvement on key physics parameters when reducing thickness from 250 μm to 150 μm

Kristof De Bruyn (CERN)
The LHCb Vertex Locator Upgrade
Vertex 2019 – 14/10/2019

0 X

Total material: 25.01%$X_0$

Impact Parameter Resolution

Background rejection

Decay Time Resolution

Electron Energy Loss
~200 μm-thick silicon sensor
- n-in-p built by HPK
  - Lifetime fluence of $8 \times 10^{15}$ 1 MeV n$_{eq}$/cm$^2$, 400 Mrad
- 768×256 pixels, each 55×55 μm$^2$

~Three VeloPix ASICs per sensor (tile)
- Thinned to 200 μm, 130 nm CMOS technology
- Each bump-bonded to 256×256 pixels
- 400 Mrad and SEU tolerant
- Readout of every hit
  - 800 Mhits/s → 50 khits/s/pixel
- Up to four output lines at 5.12 Gbps each
- Power consumption < 2 W
Readout electronics

~ ASICs wirebonded to FE hybrids
- 20 data links at 5.12 Gbps
  ✦ Up to 4 links/ASIC on innermost ASICs

~ GBTx hybrids deserialize control signals
- Charge-pump current increase fixes GBTx relocking, used through LHCb

~ OPB outside vacuum and high radiation zone
- FEASTMP DC/DC converters, 10 VTTx and 3 VTRx

\[ T_{\text{sensor}} < -20^\circ \text{C for longevity} \]
Micro-channel cooling

~ 4 tiles (12 ASICs) on each module
~ Cooled by evaporative CO₂ in micro-channels
  - Etched in 500 μm-thick silicon
  - Excellent thermal efficiency
  - No thermal expansion mismatch with silicon ASICs/sensors

Increase in cross section between the restriction and the main channels triggers the boiling
Cooling integration and performance

**CO₂ pipes soldered to metallization on micro-channels**
- Leak tight, keep planarity, pressure up to 186 bar

**~ASICS glued to micro-channels**
- **Innermost sensors** have 5 mm overhang
- **Demonstrated power dissipation** up to 30 W with small ΔT on the sensor
  - Even by end of life (27 W), T\textsubscript{sensor} well below -20°C

**CO₂ at -32°C and 0.3 g/s flow**

Long R&D campaign proved great robustness, quality, and performance of the substrate, microchannel production finalized
During module QA in September 2019, a **strange** T-dependence observed

- Tile detached after removing wirebonds!

- Exhaustive testing campaign discovered **catalyst absorbed moisture** during deposition

  - Catalyst 9 rather hygroscopic

Moisture can be greatly reduced by re-heating the catalyst → Part of the solution
Glue crisis... and resolution!

Several options studied

- Aging simulated with thermal cycling
- Irradiation of Stycast + 23LV
- Peel tests with double-cantilever beam setup at CERN
- Shear tests at Manchester

Chosen solution

<table>
<thead>
<tr>
<th>Glue propriety</th>
<th>Stycast 2850FT CAT 9</th>
<th>Stycast 2850FT CAT 23LV</th>
<th>Araldite 2011</th>
<th>EPO-TEC T7109-19</th>
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<tbody>
<tr>
<td>Manufacturer</td>
<td>Henkel</td>
<td>Henkel</td>
<td>Huntsman</td>
<td>Epoxy Technology</td>
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<tr>
<td>Adhesion properties</td>
<td>Shear and peel tests in general high, but this and adhesion checked for our case (see next slides)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Filler</td>
<td>Alumina</td>
<td>Alumina</td>
<td>—</td>
<td>Boron</td>
</tr>
<tr>
<td>Glue thickness</td>
<td>60-80 µm</td>
<td>60-80 µm</td>
<td>70-100 µm</td>
<td>30-50 µm</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>1.25 W/mK</td>
<td>1.1 W/mK</td>
<td>0.22 W/mK</td>
<td>1.3 W/mK</td>
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<tr>
<td>CTE (°C⁻¹)</td>
<td>35 ppm</td>
<td>39.4 ppm</td>
<td>85 ppm</td>
<td>59 ppm</td>
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<tr>
<td>Mix ratio</td>
<td>100:3.5</td>
<td>100:7.5</td>
<td>100:80</td>
<td>100:15</td>
</tr>
<tr>
<td>Working time</td>
<td>45 min</td>
<td>60 min</td>
<td>Many hours</td>
<td>120 min</td>
</tr>
<tr>
<td>Viscosity</td>
<td>58000</td>
<td>5600</td>
<td>45000</td>
<td>50000-70000</td>
</tr>
<tr>
<td>Cost</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Medium</td>
</tr>
<tr>
<td>Shore number</td>
<td>D96</td>
<td>D92</td>
<td>D74</td>
<td>D41</td>
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<tr>
<td>Radiation tested</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Environment</td>
<td>Humidity</td>
<td>Humidity</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Other comment</td>
<td>Catalyst reheated</td>
<td>Catalyst reheated</td>
<td>Retracts on curing</td>
<td></td>
</tr>
</tbody>
</table>

Potential delay due to bleeding and new procedures

LHCb week February 2020
COVID-19 impact

〜 COVID-19 shut down most activities in March
- Work on documentation, database, procedure optimization

〜 RF foil installation one of CERN's pilot projects
- Zoom-supervised and completed in May!

〜 Pandemic slows down everything
- Bubble working, quarantines, difficulty of travel
- eg, significant effort designing micro-channel transport box since it is not easy to fly anymore
First post-COVID-19 modules

~ Module production resumed over the summer
  - Improved procedures

~ On track to meet updated LS2 schedule

No PPE shortage will stop the VELO production
Upstream Tracker (UT)

128 channels, 6-bit ADC (5 bit and polarity), 40 MHz readout

M. Artuso et al, First Beam Test of UT Sensors with the SALT 3.0 Readout ASIC, DOI:10.2172/1568842
UT overview

- Placed between VELO and dipole magnet
- Crucial for triggering and long-lived particle reconstruction
- 4 layers of silicon strips with same arrangement as TT
- Vertical/stereo layers provide x-y position
- Improved performance
  - 40 MHz readout
  - Finer granularity
  - Close to the beam 187.5 μm pitch → 93.5 μm
  - Larger coverage (closer to beampipe)
  - Reduced material budget

![Diagram of UT geometry looking downstream.](image)
Silicon sensors

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Type</th>
<th>Pitch</th>
<th>Length</th>
<th>Strips</th>
<th># sensors</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>p-in-n</td>
<td>187.5 μm</td>
<td>99.5 mm</td>
<td>512</td>
<td>888</td>
</tr>
<tr>
<td>B</td>
<td>n-in-p</td>
<td>93.5 μm</td>
<td>99.5 mm</td>
<td>1024</td>
<td>48</td>
</tr>
<tr>
<td>C</td>
<td>n-in-p</td>
<td>93.5 μm</td>
<td>50 mm</td>
<td>1024</td>
<td>16</td>
</tr>
<tr>
<td>D</td>
<td>n-in-p</td>
<td>93.5 μm</td>
<td>50 mm</td>
<td>1024</td>
<td>16</td>
</tr>
</tbody>
</table>

**Optimization with 4 designs**

- **Outer region** with p-in-n, 187.5 μm pitch
  - Cost effective

- **Inner region** with n-in-p, 93.5 μm pitch
  - Radiation-hard and good granularity

Circular cutout near the beamline

Embedded pitch adapters
SALT: Silicon ASIC for LHCb Tracking

~ 4192 ASICs with **128 channels** each
- 130 nm-TSMC with **30 MRad** radiation tolerance

~ **Wire-bonded** to sensors
- Input pitch 80μm

~ Allow for **40 MHz** readout of UT
- Up to 5 SLVS e-links @ **320 Mbps**

~ **Fast shaping** time/return to baseline
- $T_{peak} \leq 25$ ns, less than 5% after 2 $T_{peak}$

~ **6-bit ADC** (1 for polarity)

~ **DSP featuring**
  - Pedestal and **common mode subtraction**
  - **Zero-suppression**
  - Data formatting

~ **On-chip memory**

After a bumpy road and a few iterations, performance is now more than satisfactory!
Sensor+ASIC characterization

~ **Beam test** at Fermilab (March 2019)

~ **Type A unirradiated sensor**
  - 99.5% efficiency and SN ~ 12

~ **Type B sensor irradiated to 2x maximum dose**
  - 94% efficiency and SN ~ 11

  *Partly due to readout limitation, most efficiency will be recovered with LHCb readout*

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Final system expected to have single-hit **high efficiency** (> 99%) and **good signal-to-noise ratio** throughout experiment lifetime

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M. Artuso et al, "First Beam Test of UT Sensors with the SALT 3.0 Readout ASIC" (2019) [DOI:10.2172/1568842]
At PSI and MGH beam tests (Aug 2019), observed some SEU sensitivity in certain configuration registers

Issue tracked down to
- Increased combinatorial logic when moved from RTL Compiler/Encounter to Genus/Innovus
  - Eg, synthesized $A \& (A \mid B)$ instead of $A$
- Some registers grouped for SEU self-correction

Simulated vulnerability and found window as large as 3 ns
- Only 12% of clock cycle, so could be mitigated by adjusting phase
  - Beam background concentrated around bunch crossing

New SALT version with more synchronizers, reduced logic, no register grouping
- Negligible VW in simulation, to be confirmed in beam test
- To be used at least in innermost sensors
Hybrids and flex cables

~ ASICs mounted on **hybrid flex boards**
  - 4 (A sensor) and 8 (BCD sensors) ASIC variants

~ Hybrids then readout by **flex cables**
  - 100 Ω differential input **impedance** traces
  - Up to 1000V between **adjacent lines**
  - Less than 500 mV roundtrip voltage **drops**
Integration into stave

~ Modules (hybrids+sensors) and flex cables are mounted onto a stave
  ~ Low-mass support of 1.6 m x 10 cm

~ Overlap between sensors on the front and back

~ Integrated titanium pipe for CO₂ cooling

Stencil application of TIM, epoxy, silicone pedestal
Heat TIM, place module, overnight curing
Another module on the stave!
~ **Flexible pigtail cable** connects the stave to PEPI
~ **Backplane** distributes **balanced load** to DCBs
~ **DCBs optically** send data to LHCb DAQ

- **Bandwidth:** $248 \text{ DCBs} \times 3 \text{ VTTx/DCB} \times 2 \text{ links/VTTx} \times 4.8 \text{ Gb/s} = 7.1 \text{ Tb/s}$
- Also control system via VTRx

Each DCB (Data Control Board) has:
- 7 GBTx (rad-hard serdes ASIC),
- 3 VTTx (twin optical transmitter),
- and 1 VTRx (optical TX/RX)

Due to space constraints, backplane ended up being an **ultra-dense** board with **28 layers** at the limit of manufacturability
Staves cooled by CO₂, tested between -30° and 20°

PEPI cooled by water, boxes sit directly on top and below staves

LV and HV regulation at the service bays
Operations severely impacted by lockdowns set up to stop the spread of COVID-19
- Some activities such as design or fw/sw development continued

Most components delivered

Ongoing activities
- Hybrid and readout electronics qualification
- Module production and stave assembly
- Cabling, soldering, and mechanics assembly/procurement

Key challenges
- Inner ASIC and 8-ASIC hybrid designs to be validated
- Manpower at CERN for installation and commissioning

On track to meet updated LS2 schedule, but no contingency!
~ LHCb undergoing a **significant upgrade** to increase **data taking rate** 5\(\times\)
- Remove hardware trigger → All hits are read out
- Increase detector longevity
- Improve performance

~ **Pixel VELO and UT** have **overcome all major challenges**
- Final stages of **production and installation**

~ **Significant impact** from **COVID-19**
- Challenging schedule but still broadly on track